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7.1 Front Panel Unit (FPU)

7.1.1 Display

The display is of 6 digits (ICs 4 to 9). Each digit (HDSP7801, green) is an individual 7 segment display unit with decimal point. The display units are driven by ICs 2 & 3 (SAA1064), I²C compatible LED drivers operating in dynamic mode (C13 & C14) control the multiplex frequency. TRs 1 to 3 are included to allow extra drive current and therefore increased segment brightness, which is ultimately controlled by software. This is not adjustable by the user.

7.1.2 Indicator LEDs

Three LEDs are fitted onto the FPU PCB. These are 'PWR' (green), 'BUSY' (yellow) and 'TX' (red). Each LED has two states i.e., on / off, to indicate the status of their respective function. LED brightness is controlled by software. This is not adjustable by the user.

7.1.3 Buttons and Switches

Control button and switch presentation is via an illuminated keymat. Keymat illumination and brightness is achieved by red and yellow LEDs with current limiting series resistors.

The Buttons are used to select dedicated functions i.e., 'PWR'; 'SCAN'; 'SQUELCH' and 'PRIORITY'. Switches (double-ended 'rocker' type) are used to select user variables i.e., 'VOLUME' up/down, 'CHANNEL' up/down and 'CHANNEL SELECT' up/down.

IC1 (PCF8574) provides remote expansion for the two-line serial I²C bus, allowing FPU control/status information to be transmitted to the EXP board/SPU via SK1.

7.1.4 Microphone connection

The microphone signals are received via a 6 way FCC 68 series connector (CON 1) accessed through a hole on the underside of the FPU. Each signal is individually filtered before subsequent routing to the SPU via SK3. This connection also allows mobile radio programming by inserting a programming interface lead in place of the microphone.

7.2 Signal Processing Unit (SPU)

7.2.1 General

The SPU implements the base-band digital signal processing functions required for Reference vector equalisation (RVE) and Feed Forward Signal Regeneration (FFSR) channel equalisation. It also performs all control functions for the mobile radio including the user interface functions, (channel selection, on/off switching etc.).

The SPU contains the power supply for the mobile radio, receiving the vehicle's nominal 13.2 volt dc supply, and generating +5 V, +9 V, +18 V and -9 V rails from it.

The loudspeaker output volume is controlled by the SPU, the audio gain being set by the FPU volume control up and down keys.

The LMM4312 Series SPU is built around a single DSP processor, the TMS320C51 (U102). The main input/output analogue signals (Receive and Transmit) are interfaced to the processor by A-to-Ds and D-to-As within the CODEC, CS4225-B (U17). The processor has access to ROM and RAM and reads the mobile radio personality information from EEPROM, U27. Digital interfacing and glue logic functions are performed by an ASIC, U18.

7.2.2 Detailed Circuit Description

Block diagrams showing the function of the various circuits of the mobile radio are at the end of this section. Circuit diagrams are in section 9 of this manual.

7.2.3 Digital Signal Processor (DSP)

The application and personality are stored in flash memory.

The DSP processor TMS320C51 (U102) accesses paged flash memory (U16), 128K by 8, and SRAM (U13 & U14), total 32K by 16, using its address and data buses.

The U102 clock (39.32160 MHz) is supplied by clock chip U10.

7.2.4 ASIC

The ASIC provides memory mapped I/O and glue logic functions.

7.2.5 CODEC and Analogue Signals

The processor (U102) communicates with the CODEC (U17) by means of a high-speed serial bus, running at 2.4576 Mbits/second (on lines CDCSDO, CDCSDI, SCLK and FSYNC, FSYNC, produced by the ASIC).

The main received signal, RXSIGNAL+ and RXSIGNAL- from the RFU, is first converted to a single ended signal, AIN1L by U2D, then A to D converted by U17.

The 16 bit A to D converter in the CODEC (U17) is internally multiplexed, and is used, under control from U102, to convert AIN1L, AIN1R and AIN3L to digital form. Thus the received and the microphone signal are read at different times by the processor (U102).

The signal for transmission, TXI (transmit in phase) and TXQ (transmit quadrature) is produced by the CODEC (U17) D-to-As (under control from the processor U102), and then level shifted by U2. After filtering, the signal is fed to the RFU for transmission. The transmitter AFC and AGC signals are produced in the same way.

The ADC source inputs to the SPU are converted to a low impedance signal, referenced to ground by U30D, and then fed to the AIN1R input of the CODEC to be converted to digital form and fed to the processor (U102). The ADC input is produced on the RFU by multiplexing various analogue signals including reverse power and PA temperature signals. The appropriate signal is selected by the processor (U102) through the SS0 to SS2 lines, which drive the RFU from the ASIC.

7.2.6 Configuration Information

The mobile radio configuration information is read out of EEPROM (U27, 16 kbits) by ASIC (U18) to the processor (U102).

7.2.7 Serial UART

A serial UART is implemented in software in the processor (U102). This is connected to the SER RxD and SER TxD signals from the FPU. Serial communications, for mobile radio programming and other functions, are achieved by removing the microphone and plugging in a programming interface lead. When the microphone is used, the serial receive pin on the FPU microphone connector is used for the PTT function. The receive serial data line is multiplexed with the CODEC LRCLK signal within the ASIC and is only set for serial data receive when the mobile radio is in programming mode.

7.2.8 RFU Interface and PA Control

RFU control signals to or from the processor (U102) are interfaced by the ASIC (U18) and fed to or from the RFU. These include:

- *SS0, SS1 and SS2* which control the multiplexer selecting monitor signals on the RFU, to be fed to ADC Source and then to the DSP processor (U102).
- *Tx/nRx*, which is used to switch the mobile radio between, transmit and receive.
- *PA enable*, which switches the bias to the PA block (IC1, PA) and the supply to the PA drivers to allow transmission.

7.2.9 Power Supply

The power supply unit consists of a switched, charge pump circuit (U6, U7, Q10 and Q11) which produces the +18 V and -9 V rails, and linear regulators (U3 and U4) for the +9 V and +5 V rails. The charge pump switching signal, PSU_SYNC is produced by the ASIC (U18) and is a nominally 102.4 kHz square wave. The charge pump circuit takes the +9 V signal output from the linear regulator U4 and doubles it to +18 V and mirrors it to -9 V. The outputs from the charge pumps are filtered to reduce noise on the output supply.

The vehicle's nominal 12 VDC supply is first filtered by L20, C158 and C159 to remove noise, then fused by F1 and fed to transient protector D3 which prevents the voltage exceeding 24V during load dump conditions. D2 protects MOS switch Q3 by preventing the drain to gate voltage exceeding 10V. The RFU 12 V supply (for the PA) is further filtered by L17, C160 and C161 before leaving the board via a feed-through.

7.2.10 Mobile Radio On / Off Switching

MOS switch Q3 acts as the on / off switch. It is driven by the ON/OFF signal, which in turn is fed via diode D4 from the FPU ON/OFF line which connects to the FPU on /

off key switch. When the front panel on / off switch is operated, FPU ON/OFF is shorted to ground and Q3 switches on which enables the mobile radio supply rails. As VCC comes up, Q8 switches on which latches the supply on. When the on/off key is pressed again, the base of Q8 is pulled down, switching off Q3 and the mobile radio supply. Q14 is switched on during the power down sequence to ensure that Q8 is held off as the supply rails collapse.

7.2.11 Ignition Sense

The ignition sense input, wired via connector JP6, allows the processor to sense when the vehicle ignition is switched on. The ignition sense is also AC coupled to Q9, which is connected to the FPU ON/OFF line in order to switch the mobile radio on when the vehicle ignition is switched on.

7.2.12 Reset Generator

Reset generator U201 generates reset signals for the processor if the VCC supply rail falls below 4.5 Volts, and provides reset management.

7.2.13 Octal Buffer U105

I/O address mapped octal buffer U105 takes the microphone control signals (CALL/END, PTT, ON HOOK) and multiplexes them onto the bus under the control of the processor U102.

7.2.14 PTT Inputs.

U103 is a hex Schmidt input gate used to clean up the PTT inputs.

7.2.15 Confidence Tones

Confidence tones are fed to the loudspeaker to inform the operator of the status of the mobile radio. These are generated by pulse width modulated signals from the ASIC (U18) that are fed into an integrating filter (R120, C136 and C139) to produce the tone output. The confidence tone signal (CONF TONE) is multiplexed with the received audio output (AOUT1) by switches U28A and U28B, then buffered by follower U2C that feeds the audio PA.

7.2.16 Audio PA

The audio drive to the PA is derived from the CODEC AOUT1 signal. AOUT1 is used to produce the TXQ signal when the mobile radio is in transmit mode and the CHAN RX signal when it is in receive mode.

The RESET signal for the audio PA is used to prevent excessive current draw by the PA as it switches on. The PA MUTE signal is used to mute the PA when the mobile radio is in transmit mode.

7.2.17 Microphone DC Bias

Microphone DC bias current is controlled by Q2.

7.2.18 Filtering of I / O Connections

All inputs and outputs from the SPU are filtered to remove conducted noise and prevent interference to the RFU. The filtering also prevents noise from entering the mobile radio via the external connections e.g. the loudspeaker leads.

7.2.19 Watchdog Circuit

A 600 ms watchdog circuit is built into the ASIC (U18). If the keep alive signal fails for 600 ms then the processor (U102) is reset. If the signal is still absent then the whole mobile radio is powered down.

7.3 *Radio Frequency Unit (RFU)*

7.3.1 General

The RFU implements signal conversion to and from radio frequency, including all receiving, transmitting and frequency synthesis functions.

The internal frequency reference provides a local reference for the synthesisers in the mobile radio.

Programmable synthesisers provide local oscillators for receive and transmit mixing. The synthesisers can be programmed in 4.17kHz (approx.) steps.

The receiver down-converts the received signal to a final IF of 12.5 kHz for processing by the SPU. Automatic Gain Control (AGC) is incorporated to accommodate strong signals, and this is controlled by the SPU.

The transmitter mixes base-band In-phase and Quadrature signals up to channel frequency and provides pre-amplification of the signal to the power amplifier. A Cartesian loop circuit is used to linearise the separate power amplifier module. The output power is controlled by the SPU.

7.3.2 Receiver RF Amplifier

RF signals from the antenna pass through the BNC connector on the rear of the mobile radio, through the transmit/receive relay and filter on the PA, and via a coax link to PL4 on the RFU. The signal is then fed to RF amplifier TR1. The input filter is tuned to the RF band centre frequency, providing matching and image rejection. A switchable filter is at the output to provide additional spurious rejection.

7.3.3 First Mixer

MX6 is a double balanced mixer, with approximately 6dB loss. Signals from the receive LO 1 (which is at a frequency 45 MHz above the received signal) are fed into the LO port. The wanted output from the first mixer is at 45 MHz.

The 9V supply to the RF amplifier is disabled during transmit. This prevents amplification of unwanted signals.

7.3.4 First IF and Second Mixer

The output of the first mixer (MX6) is fed to a low-gain IF amplifier stage, TR2. The output of this amplifier feeds the first IF filter, formed by F1-A and F1-B. This is a four-pole filter with a 3 dB bandwidth of 15 kHz. It should be noted that the crystal units forming the filter come in matched pairs and should not be changed individually. Replacement devices should also be fitted maintaining the correct orientation (spot towards top of board etc.) Failure to comply with this method will lead to filters, which are out of specification. The same consideration applies to filters F2-A and F2-B.

The output of F1-B is fed into gate 1 of the dual gate mosfet amplifier TR3. AGC operation is obtained by feeding a dc voltage onto gate 2.

The AGC voltage originates from the SPU board, and is set by the SPU processor to provide the required level of RF gain. As the AGC voltage rises so the level of gain increases.

The output of the second IF filter, formed by F2-A and F2-B, is fed to the second mixer, IC1 which is an active Gilbert Cell design. The local oscillator (45.0125 MHz) for the second mixer is generated by the receive LO 2. The resulting 12.5 kHz second IF signal is buffered by IC2 and routed to the SPU A to D for digitisation.

7.3.5 Reference Oscillator

10 MHz TCXO reference oscillator a miniature can type unit TCX1 The output (2 V peak to peak) feeds buffer/amplifier IC4 which is used to drive the RFU synthesisers (BREF).

The frequency of the TCXO is adjusted by the AFC signal from the SPU board.

7.3.6 TX and RX Local Oscillators, Synth and Offset Loop

The receiver first LO covers the frequency range 163 to 182 MHz in 4.17kHz steps. The signal is synthesised at 652 to 728MHz in 16.17kHz steps and divided by 4. By operating the loop at a high frequency and dividing down to the output a clean, low phase noise signal is produced, with the required frequency step size.

The synthesizer reference is a 10.0 MHz voltage controlled, temperature compensated crystal oscillator (TCX1). The 10 MHz signal is divided internally within synthesizer device IC3 to the reference 16.17kHz frequency. VCO1 output at 652 to 728 MHz is divided within IC3 and the output is compared against the reference frequency. Phase and frequency error outputs are then summed at the DoRF pin and fed back through a loop RC filter to VCO 1. The VCO 1 frequency is then $N \times 16.17\text{kHz}$, where N is the internal division ratio for FINRF within IC8. The output LORX1 is then routed to the receiver circuit where it is divided by 4 to give the receiver first local oscillator.

A second phase / frequency locked loop is used to provide the second receiver local oscillator. The 180.0MHz VCO is based on TR5. The VCO frequency is locked by the DoIF comparator output from IC3, suitable loop filtering having been applied. The output of the VCO is fed back to IC8 on the FINIF input. The output LORX2 is

then routed to the receiver circuit where it is divided by 4 to give the receiver second local oscillator.

The transmitter local oscillator is synthesised by mixing (MX1) the LOTX input on 652 - 728MHz with the OFFSET LO at 180MHz. The resulting difference frequency is filtered to give the TX LO output on 472 to 548MHz. Losses in the filters are overcome using an amplifier (IC16) to set the correct drive level for IC32 (divider IC).

To prevent cross talk and noise, a single regulator is used for VCO 1, TCX1 and the offset VCO, and a separate regulator for the synthesizer device (IC3). These are IC17+TR8, and IC12 respectively.

7.3.7 Cartesian Loop

To achieve linearity, a Cartesian loop transmitter is used. The loop allows a large degree of negative feedback linearisation to be applied to the transmit system. This ensures that unwanted spectral products generated by the transmitter are within approved specification.

The RF output signal is sensed on the PA PCB by a directional coupler and fed back onto the RFU. . The signal is then split into two paths, one of which is attenuated by a fixed pad, and then mixed down to baseband using the TX LO synthesizer output divided by 4. The mixer outputs are then compared with the TXI and TXQ inputs derived from the TXI+, TXI-, TXQ+ and TXQ- signals from the SPU in error amplifiers. The error amplifiers are DC-compensated to reduce drift. 38 kHz low pass image filters are used on the TXI and TXQ inputs to prevent aliasing effects.

The resulting outputs are up-converted to the output RF frequency and RF combined. The local oscillator used for up-conversion is phase shifted by a programmable phase shift circuit, which is set by the DSP on the SPU.

The upconverted signal is then amplified by the RF Buffer TR11 and TR17, which raises it to the level required by the PA board.

The second signal from the splitter is used for forward power detection, by rectification of the forward signal using a temperature compensated differential detector consisting of D15, D16 and IC29.

The circuit formed by IC30-A and IC30-B detects loop instability. The output is read by the SPU via the Analog MUX IC18. If instability is detected the RF output is switched off to prevent out of channel emissions.

7.3.8 Digital Inputs from SPU

Digital interfaces are used to control the RFU: a 3-wire serial link for the synthesizer, a 3 wire parallel bus for the 1-of-8 analogue multiplexer, a 6-wire parallel bus to control the phase shifter, and four individual control lines, SAMPLE, PAENABLE, OPEN LOOP and TX, to control the transmitter.

Serial digital programming data from the SPU is input to the RFU on lines LP0, LP1 and LP2 and then routed to the synthesizer device LMX 2332 (IC3) for programming of the registers to control the output frequency.

Analogue inputs to the multiplexer are selected for output by control lines MS0, MS1 and MS2, from the SPU board. Analogue signals that can be selected in this way are: the transmit feedback in phase (I) and quadrature (Q) outputs, the reverse transmitter power, the TCXO temperature, the PA temperature and the loop instability.

7.4 Power Amplifier (PA)

7.4.1 General

The power amplifier accepts the radio frequency drive signal from the RFU and amplifies it to a level suitable for transmission. The circuit also contains a relay for transmit/receive switching and a reverse power level detector. A thermistor is used as a temperature sensor to prevent the PA from overheating.

7.4.2 Detailed Circuit Description

The RF drive signal from the RFU is input on PL5 and amplified by driver TR2. TR2 is constant current biased by the TR3 circuit. The output from TR2 is matched and feeds the PA block (IC1) input.

The 12 Volts supply reaches the PA on PAD1 after filtering and fusing on the SPU board. The supply is further filtered by L3, C21 and C22 and then switched by the P-channel FET TR8. The switched supply feeds the PA driver stages of the PA-module (IC1, pin 2). When the PA is not enabled, the supply rail to the PA module (IC1) driver is thus switched off, preventing noise generation or oscillation. The gate of TR8 is switched by TR6, which is, in turn, driven by the PA ENABLE board input. The PA ENABLE input is also used to switch off the bias to IC1, via TR5, so that the loop can be broken for calibration purposes.

The PA module (IC1) output is switched by transmit/receive relay RL1. When the PA relay is in transmit mode, set by the TX line, then IC1's output is connected to the 7-element output filter formed by L5, L6, C29 etc. The output filter attenuates signal harmonics. When the mobile radio is in transmit, the RFU receiver input is grounded via a 51 Ohm resistor by RL1. When the mobile radio is switched to receive mode, driver (TR2) is switched off by TR1, which is controlled by the TX line. The mobile radio input signal is fed, from the rear panel BNC connector, through the output filter, back to PL4 and on to the RFU.

CPLR1 is a printed directional coupler that provides feedback to the RFU at -24dB. The tap is also used to sense the reverse power, D4 providing a DC level for this purpose. The PA is protected against excessive mismatch by the SPU monitoring this level and controlling the output power accordingly.

TH1 is a positive temperature coefficient thermistor that is used to sense the PA-block temperature, allowing the SPU to shut down the PA if an over-temperature condition is detected.

7.5 I²C Expander Board

The Expander I²C board provides an interface between the microprocessor/parallel data bus from the SPU and the two line serial I²C bus to the FPU.

Data and control lines are routed from the SPU via SK1 and are filtered to improve EMC. The expander card is the I²C bus master.

ICs 10 to 12 are used to satisfy timing requirements for the /WE instruction with respect to /CS.

+5V and 0V are provided by the SPU via SK1. The I²C clock and data lines are routed to the FPU via SK2.

7.6 Overview and Interconnection Block Diagrams

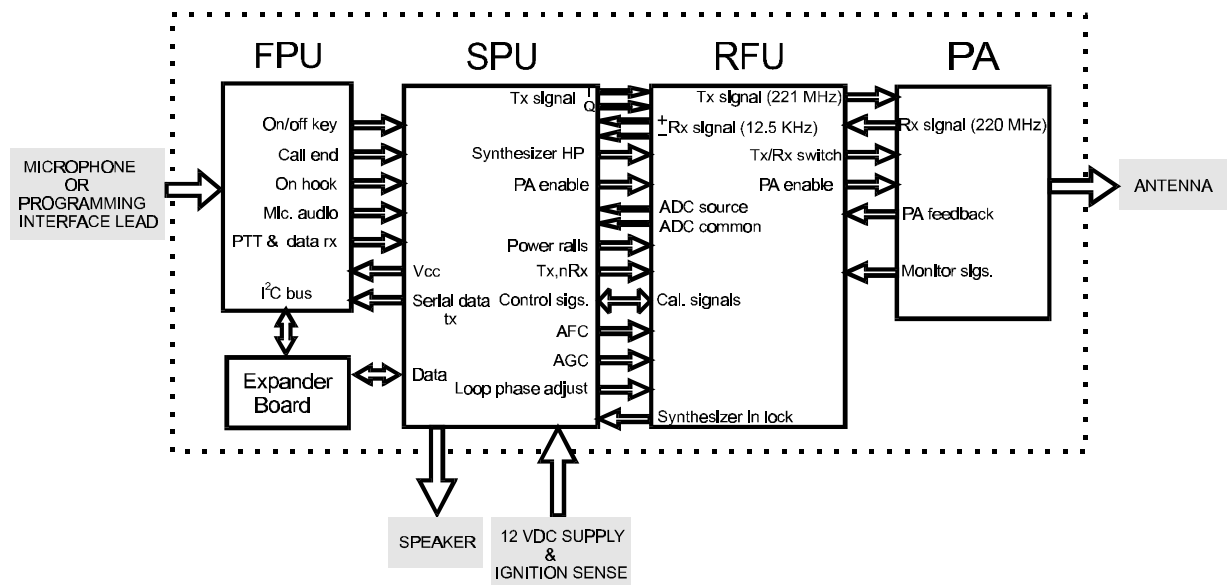


Figure 7-1 Overview connection diagram

7.7 Functional Block Diagrams

The block diagrams shown on the following pages illustrate the function of the mobile radio's modules in more detail.

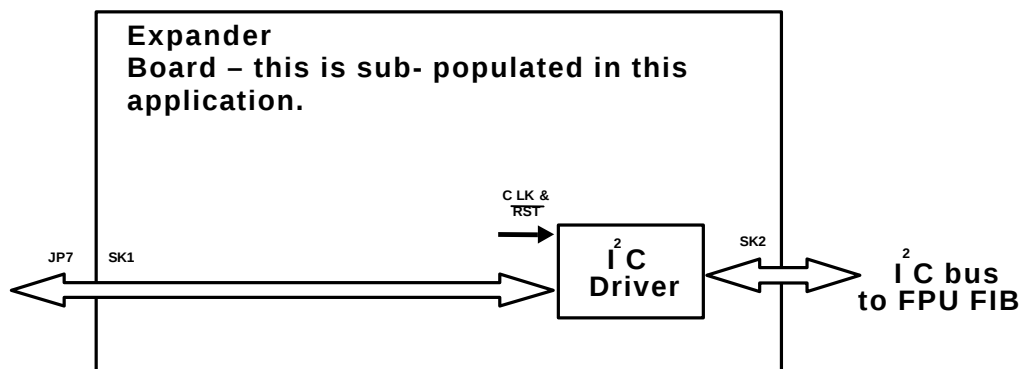


Figure 7-2 Expander Card