Theory of operation : SN921

The SN921-Repeater is designed to repeat messages, sent by specific transmitters, for reception by another SpreadNet repeater or receiver.

The repeat process is described as following:

-The SN921's re-receiver receives messages sent by many transmitters. These messages may or may not belong to the security system or the repeater.

-The SN921's re-receiver filters out all messages which have a property code that is greater than it's programmed property code.

-The SN921's re-receiver retains valid messages (those with proper property code) in the buffer.

-The SN921's re-receiver then converts valid messages into data mode commands, and sends the commands to its re-transmitter through a serial interface.

-Upon receiving the valid messages from re-receiver, the re-transmitter re-formats the message and re-transmits the message using the re-transmitter's property code.

POWER SUPPLY:

The power supply used is an off-the-shelf item.
A class 2, 16.5 VAC, 50/60 Hz, 40 VA transformer provides power to the power supply. The power supply provides a 12VDC 1 Amp regulated output. The power supply also has a charger used to charge a 12VDC, 6.5 AH back-up battery. If AC power is off, this back up battery supplies power to the repeater for 18 hours. The 12VDC output is connected to SN921 re-receiver TB-1 pins 7 and 8.

RECEIVER OPERATION:

The SN921 Repeater is a dual down conversion super-heterodyne spread spectrum receiver operating in the 900Mhz ISM band.

RF Section:
The Repeater is tuned for a carrier frequency of 923.58Mhz entering in at either Ant A or Ant B. The antennas are positioned orthogonally to each other to achieve polar diversity and are enabled on and off until final synchronization is achieved and then the higher power antenna is selected. The 923.58Mhz signal passes through a series of wide-band filters after being amplified by the LNA (Low Noise Amplifier) stage. The first down-conversion is accomplished by mixing the first LO1 signal of 684.66Mhz with the incoming 923.58Mhz received signal to achieve a 238.92Mhz IF signal after filtering out the positive image frequency. After filtering, the 238.92Mhz signal is mixed with the second LO2 of 228.22Mhz to achieve the final IF of 10.7Mhz.

The 10.7Mhz spread spectrum IF signal is fed into the 1496 decorrelator IC where the spread spectrum code sequence is mixed with the received 10.7Mhz signal to de-spread the signal. The de-spread signal is passed through a series of 10.7Mhz band-pass ceramic filters and fed into the

NE604 IF amplifier. Signal is then taken from the NE604 RSSI (received signal strength indicator) output.

Digital Section:
Three micro-controllers are used to provide parallel operation between processing incoming RF signals and outgoing serial data. All CPU's are interfaced using a parallel bus configuration. The Master CPU controls all functions of the data acquisition and synchronization. The Slave CPU is responsible for the spread spectrum code generation, antenna switching, and sample and hold control. The Communications CPU is the interface buffer between the Master CPU and the external interface which is a Host or its Transmitter. It manages the FIFO buffering and CRC detection/correction and formats data specific to do proper tasks.

The RSSI signal feeds a sample and hold circuit controlled by the Master and Slave CPU's. The sampled RSSI signal feeds into the Master CPU A/D where the data is processed. During synchronization, the Master CPU slides the code sequence chip by chip until it receives a hit from a transmitter. The Master CPU then locks on to the signal and achieves a fine search by controlling the clock of the Slave CPU to purposely shift the code sequence in increments of 1/8 of a chip. After the complete message is received, the Master CPU transfers the message to the COM CPU where it is checked for validity, compressed, and stored in the COM CPU's internal FIFO buffer. When a poll request arrives from an external device, the message is transferred if it is operates 911 mode.

In the repeater mode, the COM CPU manages and analyzes all incoming messages and depending on the programmed parameters, it sends the messages to its transmitter to be repeated.

Transmitter Operation:

The SN-921 transmitter section has two primary sections, one digital and one RF.

The digital section, in summary, provides all transmitter timing, RF control, and data message organization. Most of these functions are performed by the microprocessor. Several functions external to the microprocessor provide power supply regulation, battery low detection, alarm signal input conditioning, and non-volatile transmitter setup information that the microprocessor accesses during the transmit interval to construct its transmitted data message. A low power wake up timer also connects to the microproccessor and will reset the microprocessor if a lock up condition exists.

The transmit sequence is initiated when data mode commands are sent by the receiver to the transmitter via a serial interface. The tranmitter microprocessor then re-formats the message and begins the tranmit sequence.