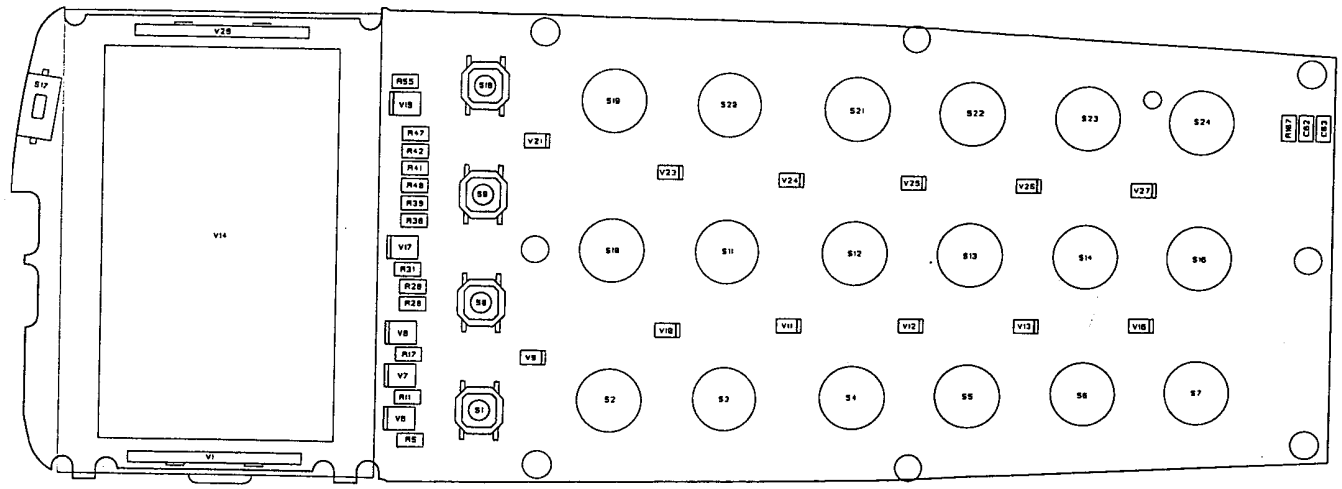
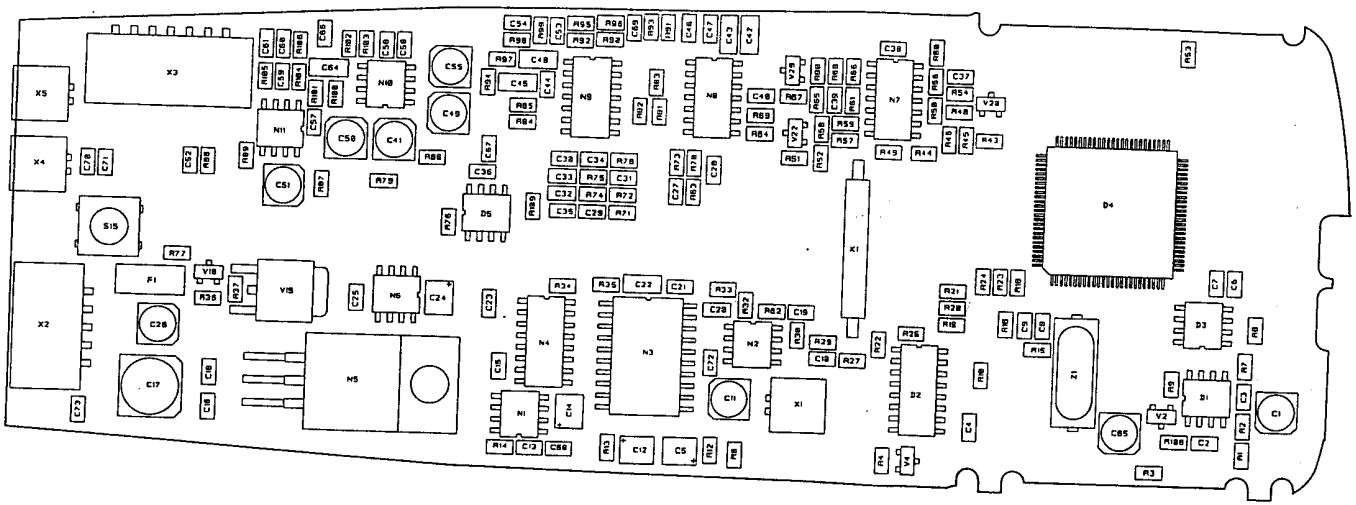
5.1 HxC AF & MMI Unit 632261

Component location HxC AF & MMI Unit 632261



Seen from primary side with primary side tracks.

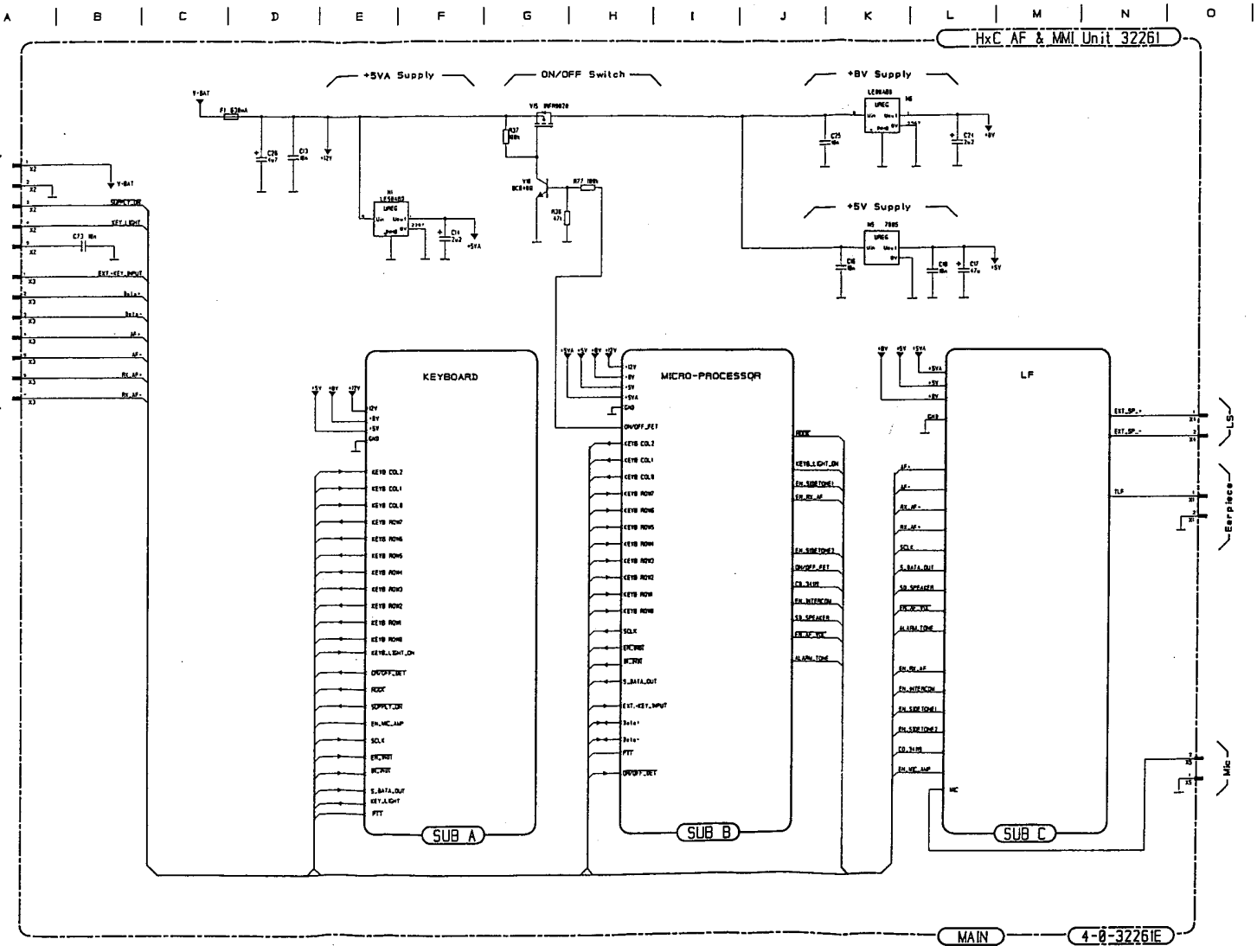
PCB rev. 32261E



Seen from secondary side with secondary side tracks.

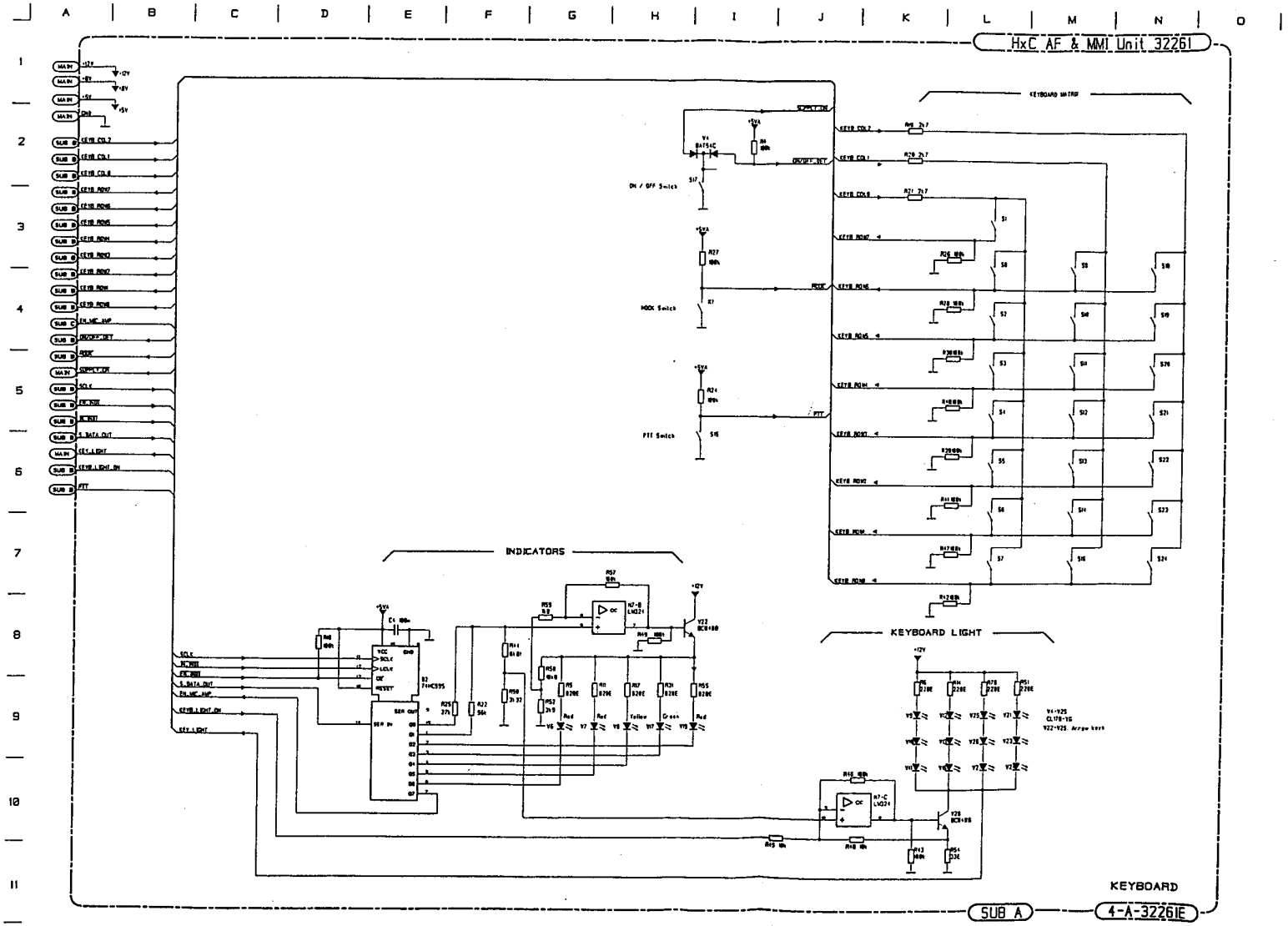
PCB rev. 32261E

HxC AF & MMI UNIT 632261



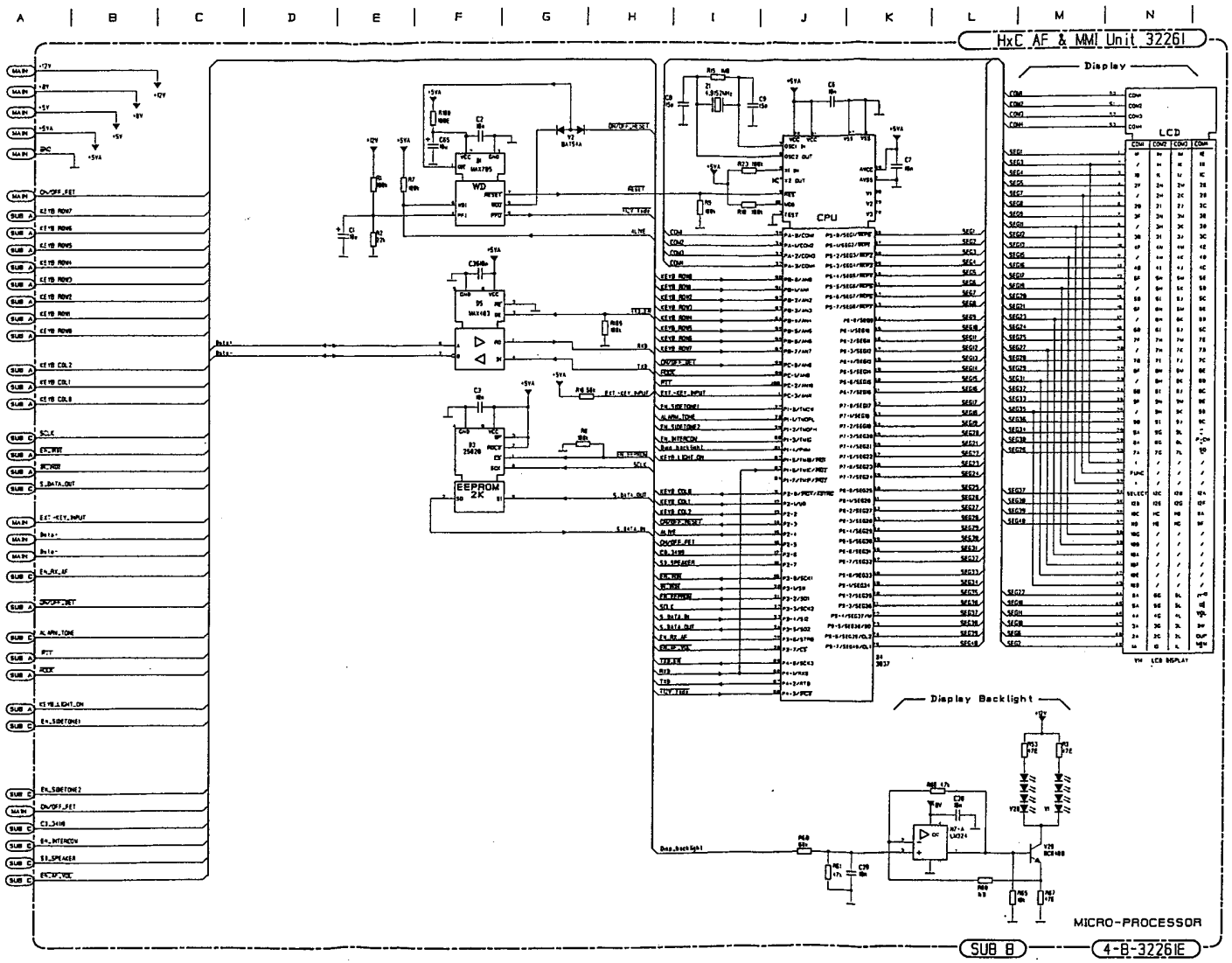
This diagram is valid for PCB rev. 32261E

HxC AF & MMI UNIT 632261

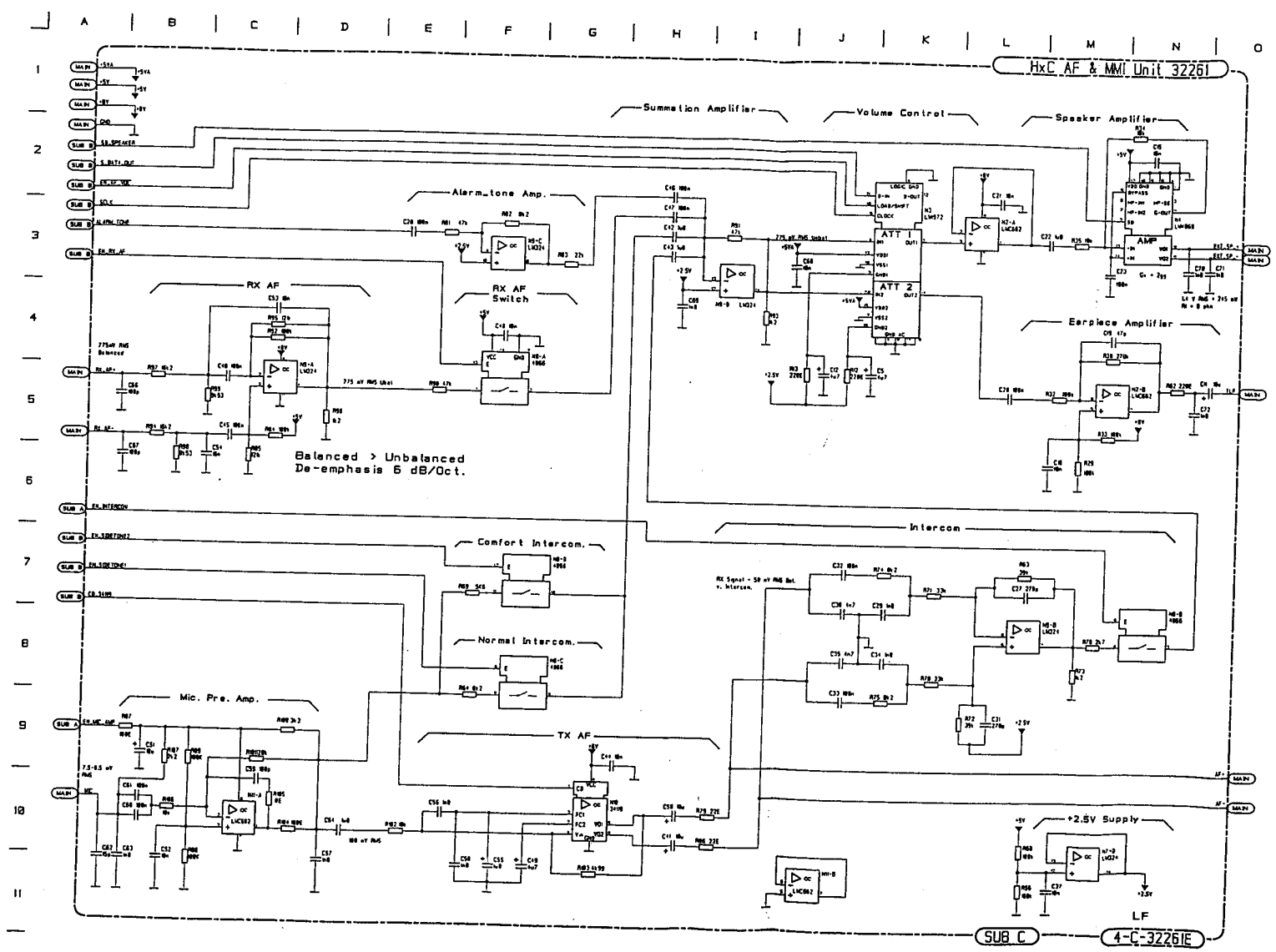


This diagram is valid for PCB rev. 32261E

HxC AF & MMI UNIT 632261



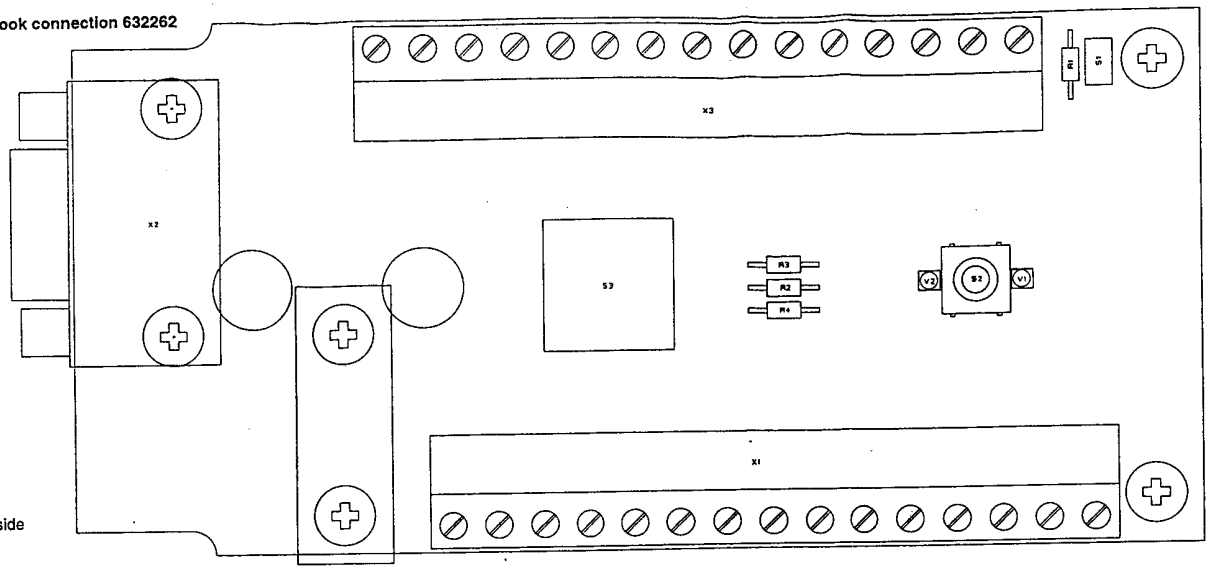
This diagram is valid for PCB rev. 32261E



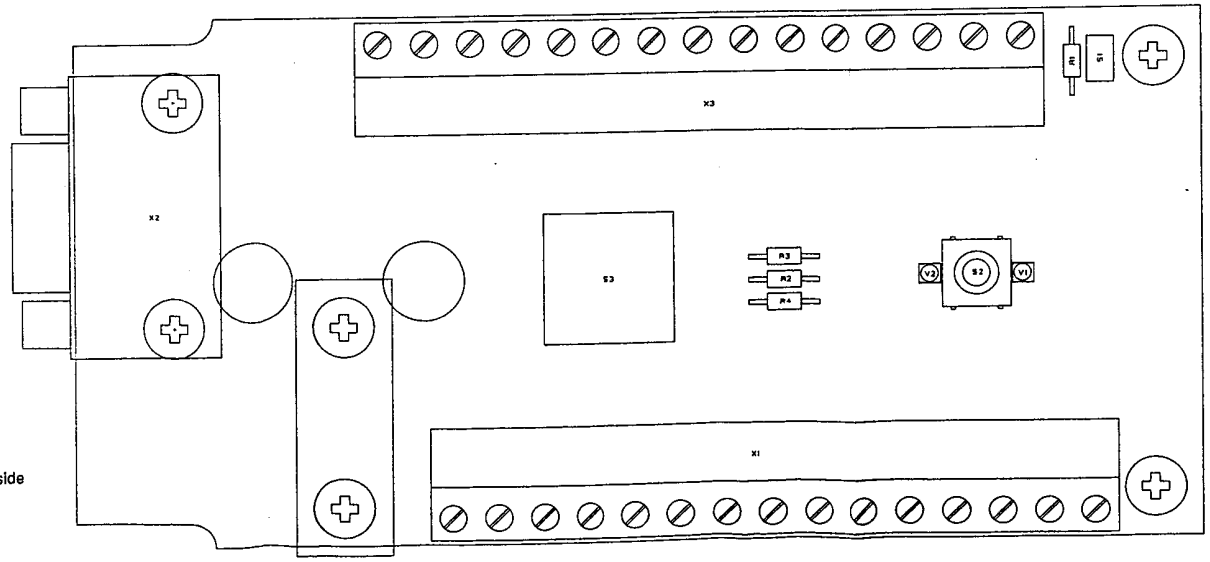
This diagram is valid for PCB rev. 32261E

5.2 Hook Connection 632262

Component location Hook connection 632262



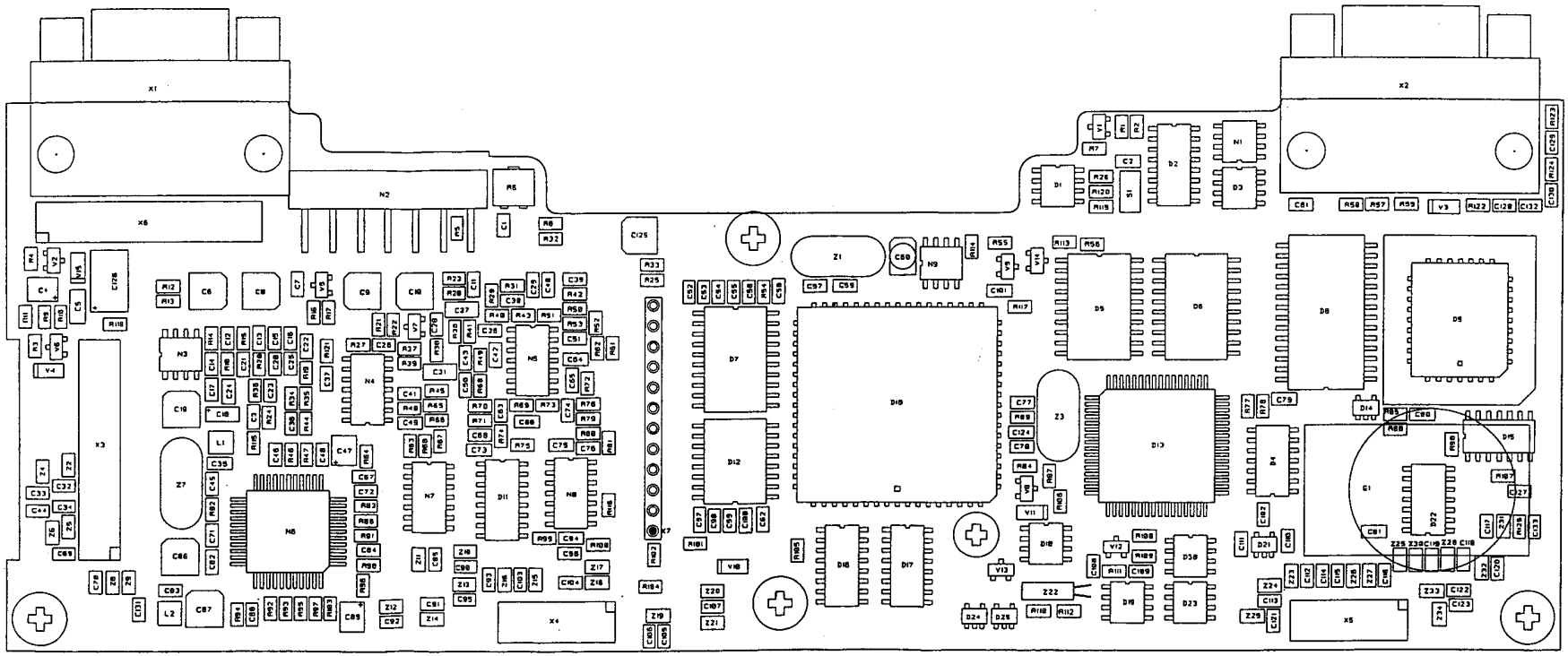
Seen from component side with upper side tracks.



Seen from component side with lower side tracks.

PCB rev. 32262C

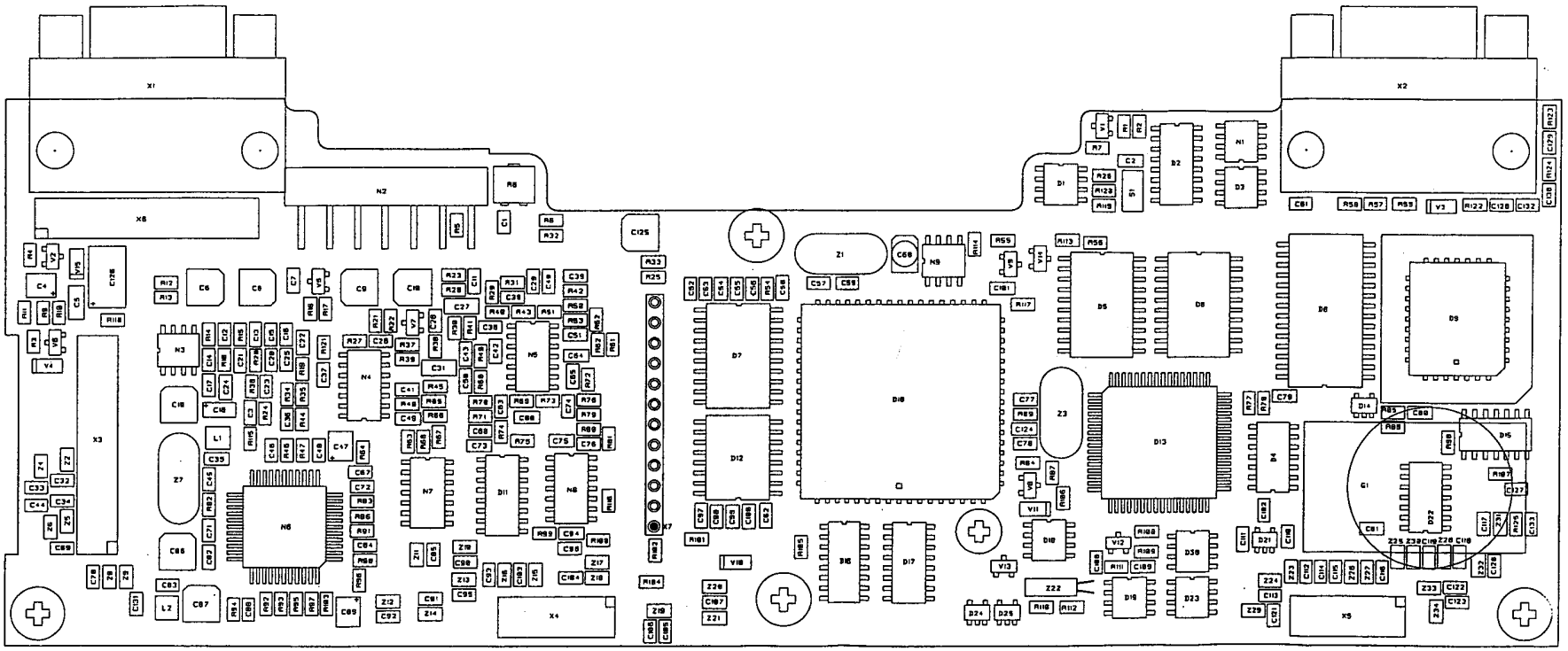
Component location AF and processor unit 63225001/02



Seen from component side with upper side tracks.

PCB rev. 32250G

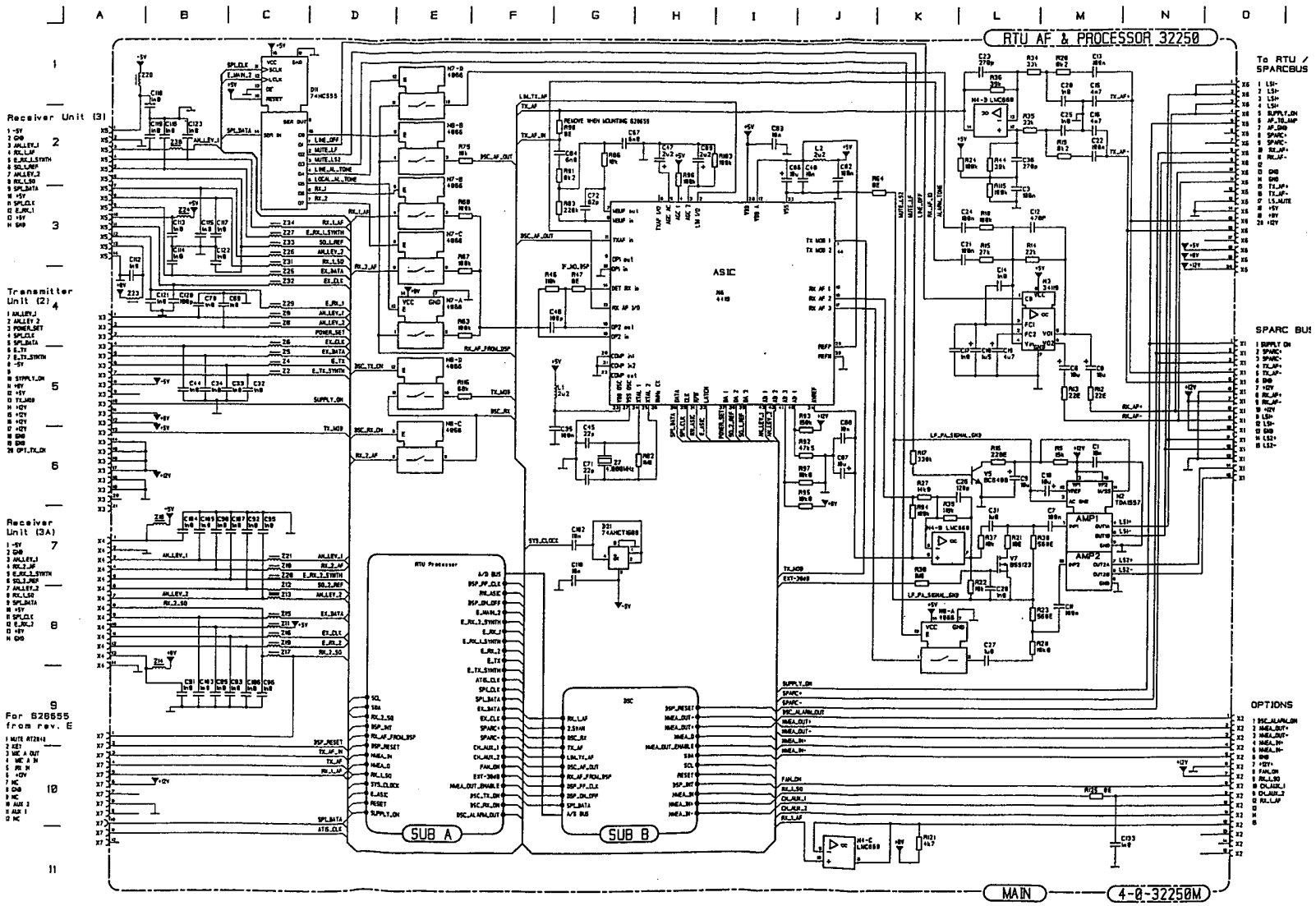
Component location AF and processor unit 63225001/02



Seen from component side with lower side tracks.

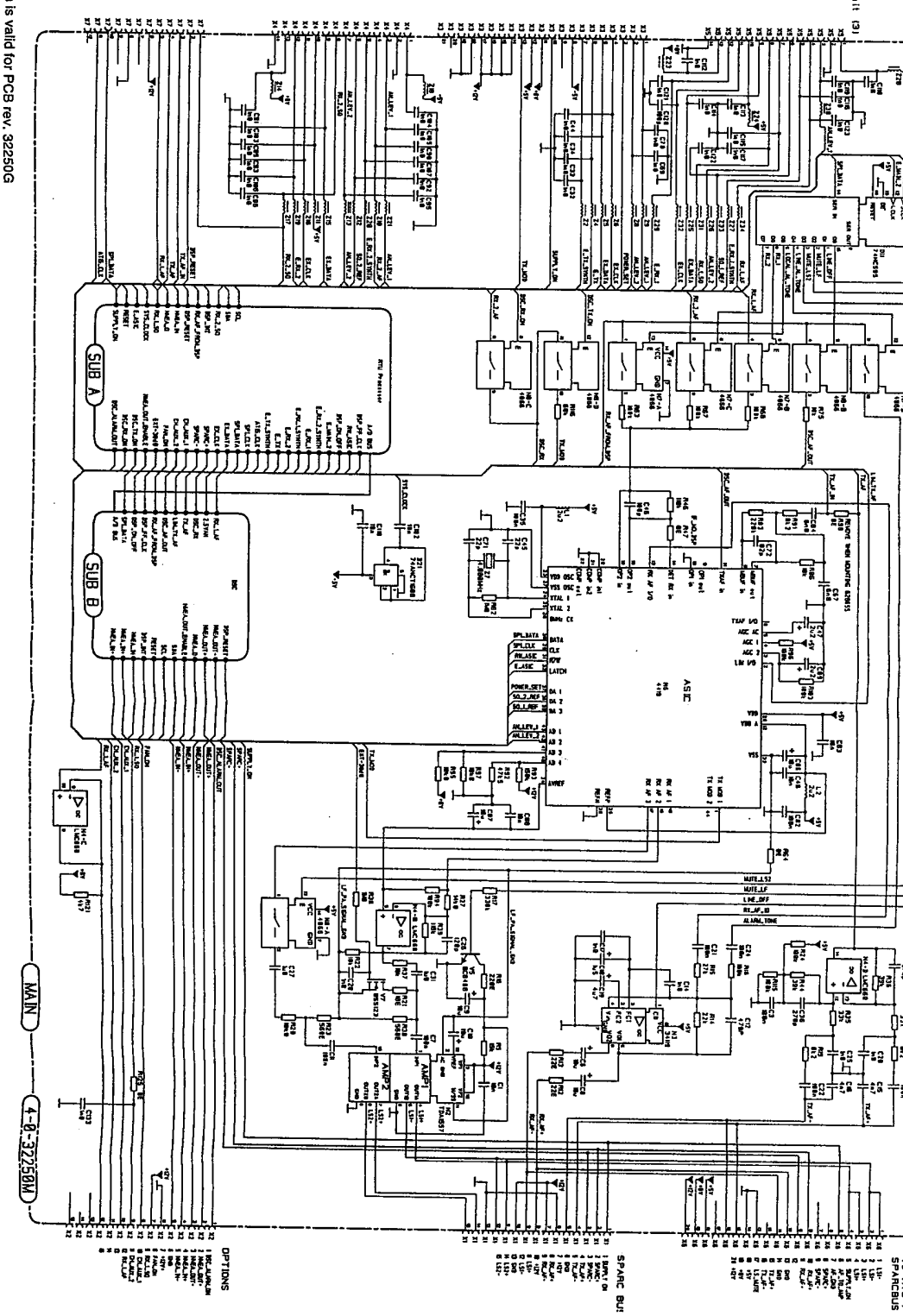
PCB rev. 32250G

AF and processor unit 63225001/02



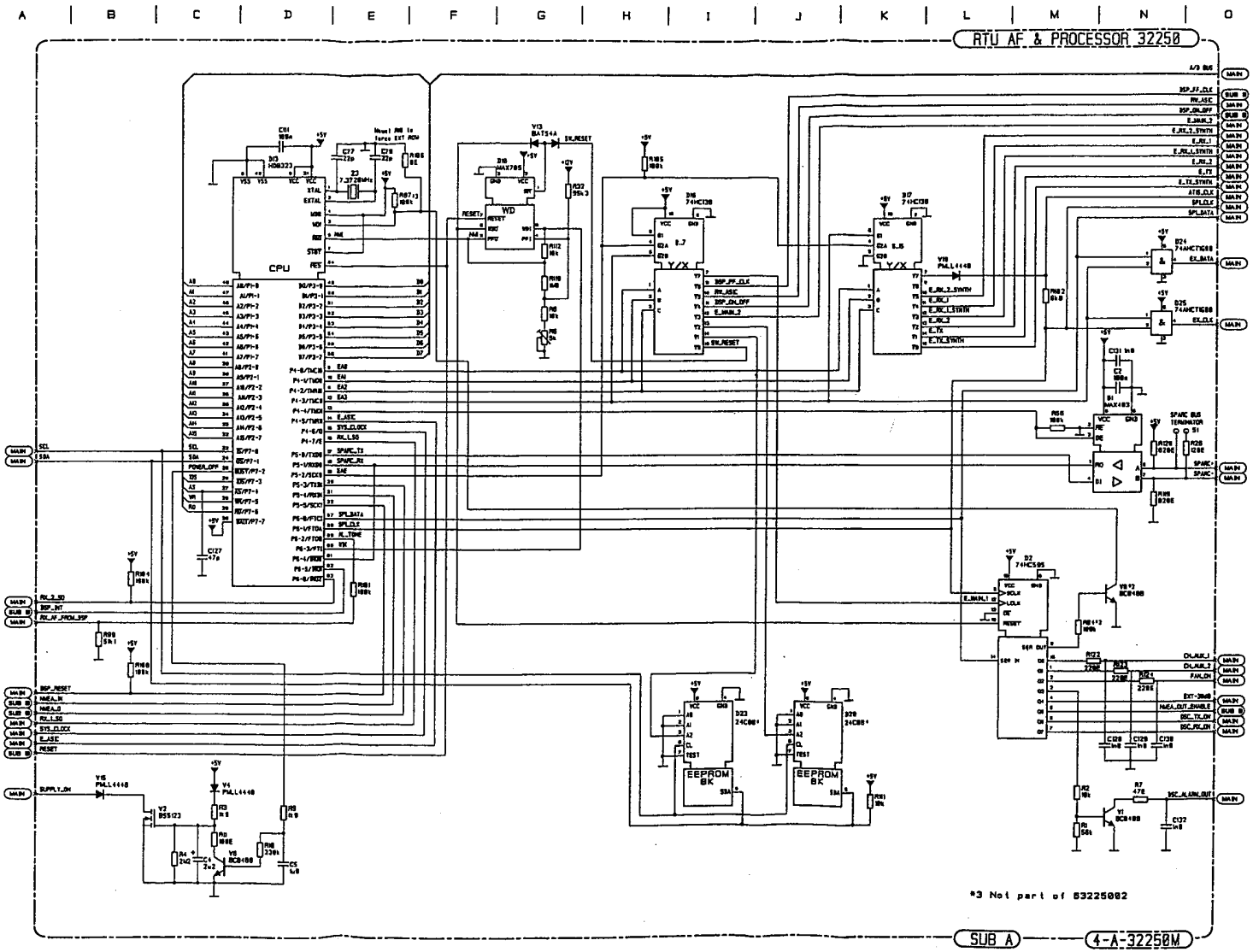
This diagram is valid for PCB rev. 32250G

AF and processor unit 6322500 1/02



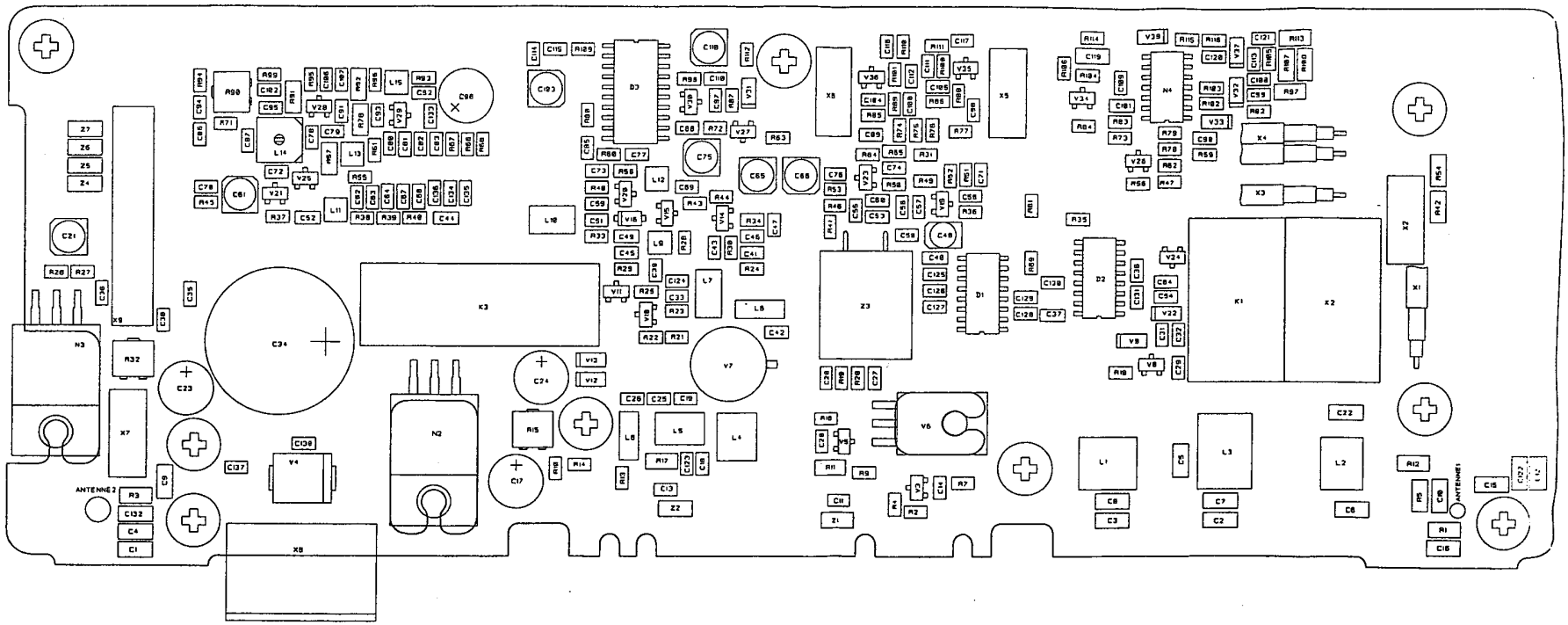
This diagram is valid for PCB rev. 32250G

AF and processor unit 63225001/02



This diagram is valid for PCB rev. 32250G

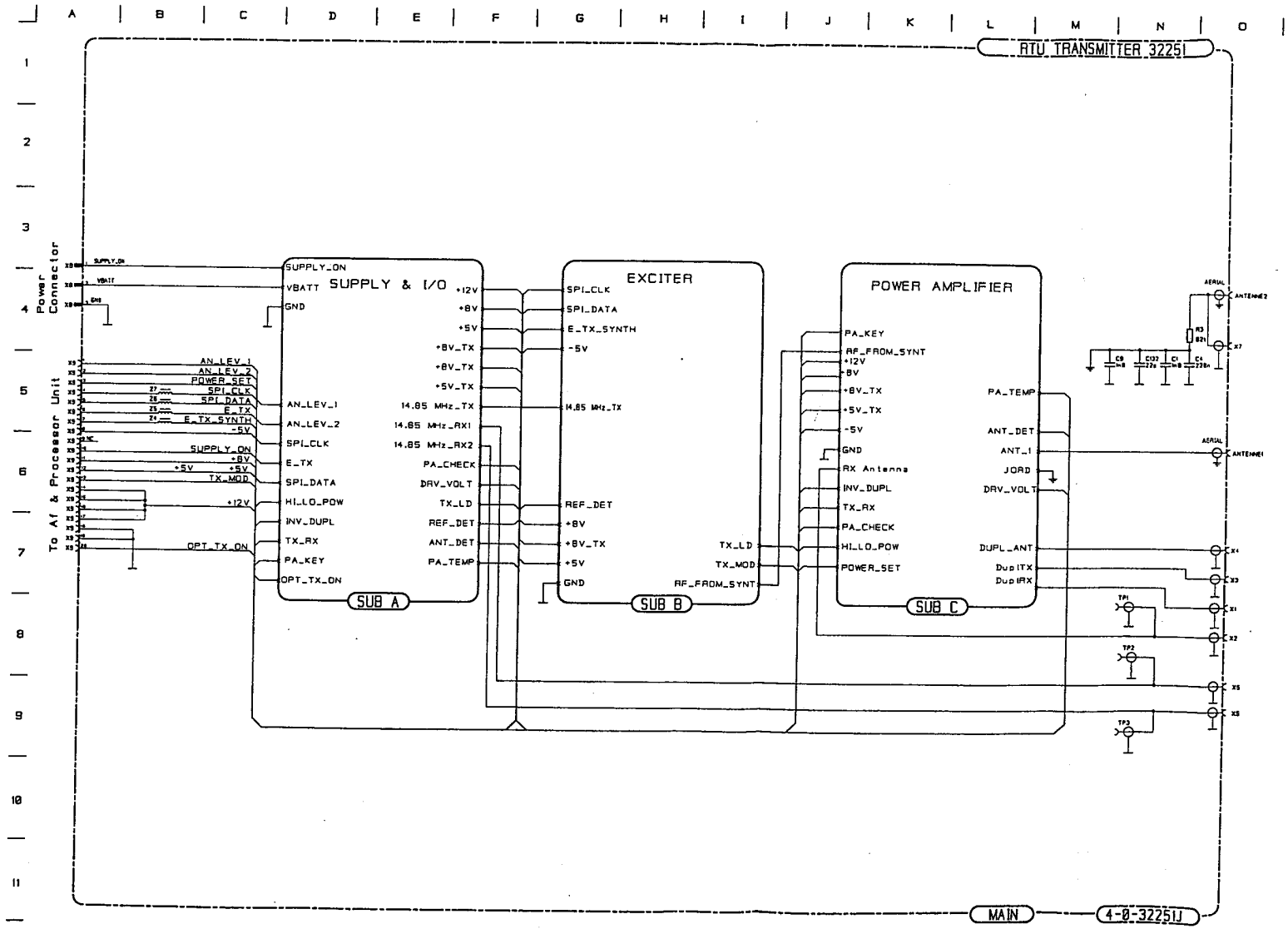
Component location Transmitter unit 632251



Seen from primary side with primary side tracks.

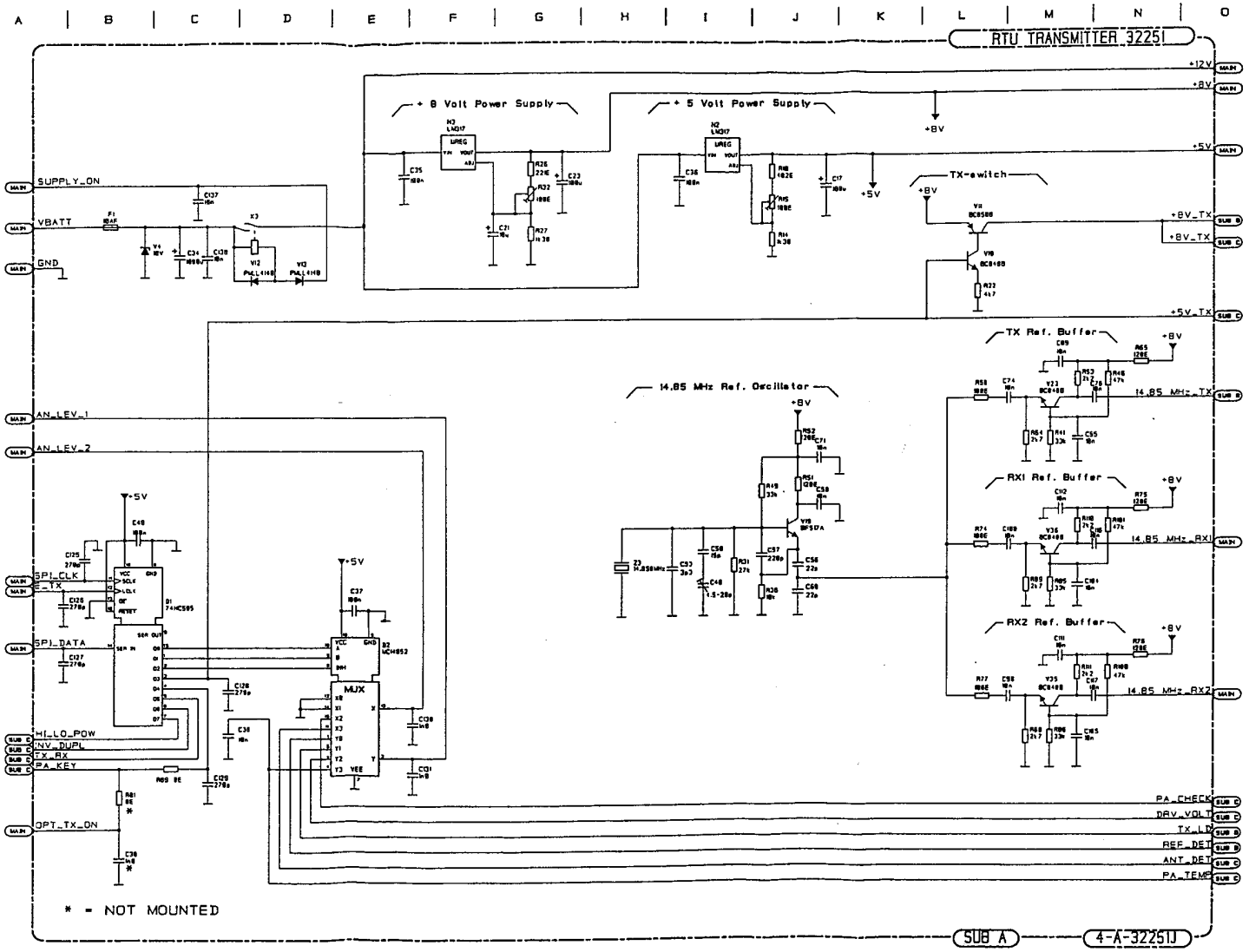
PCB rev. 32251H

Transmitter unit 632251



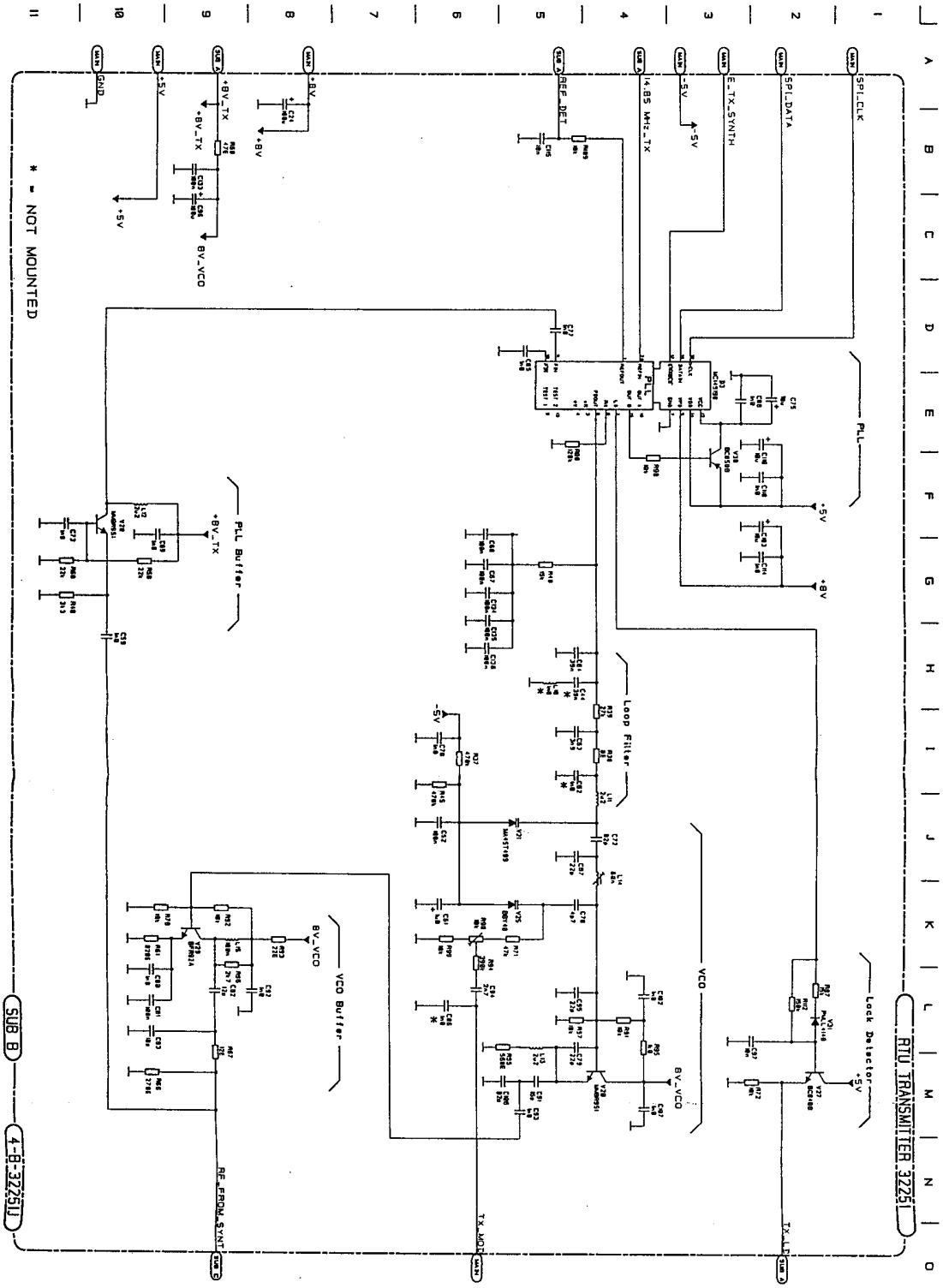
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251



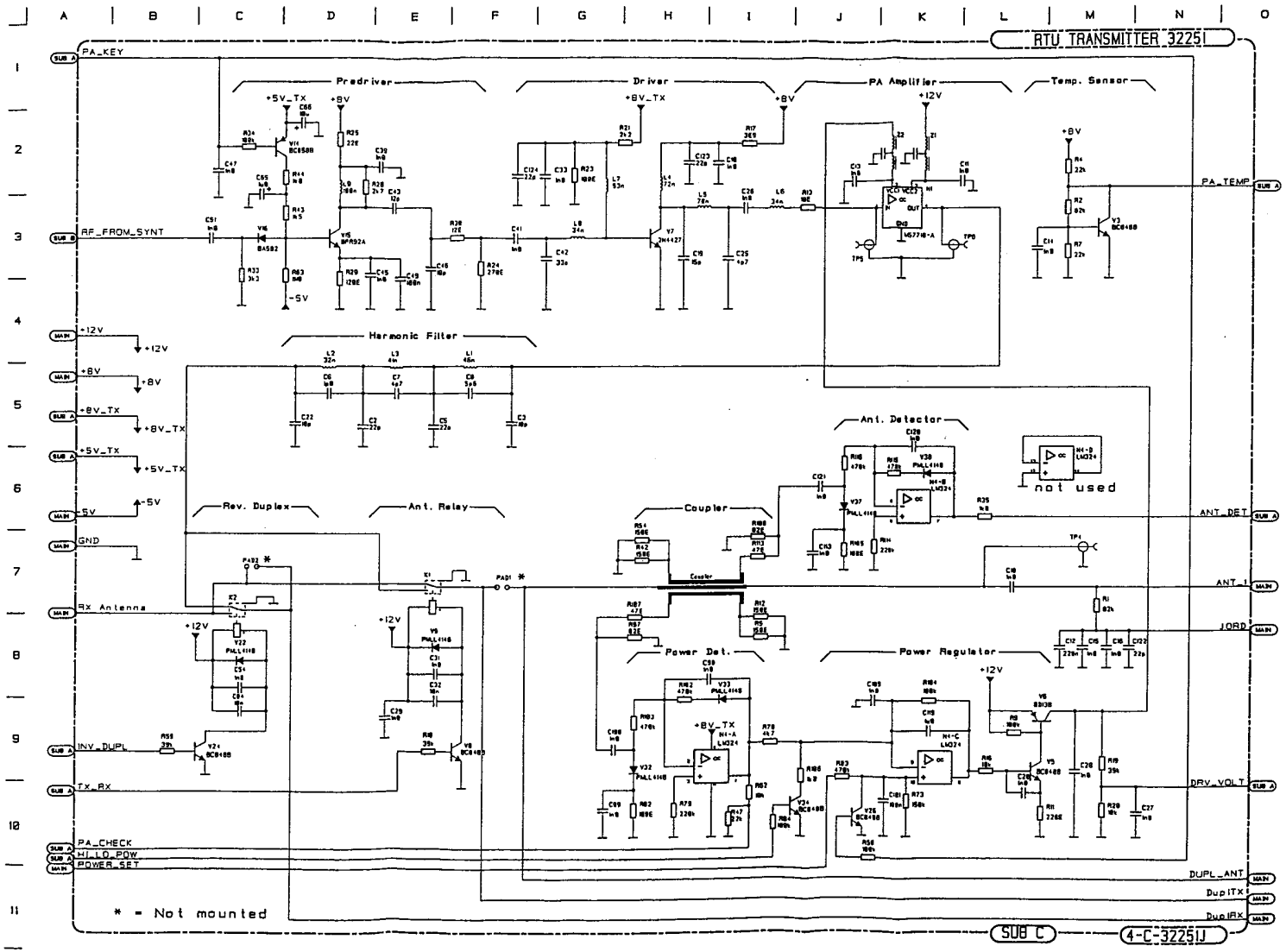
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251



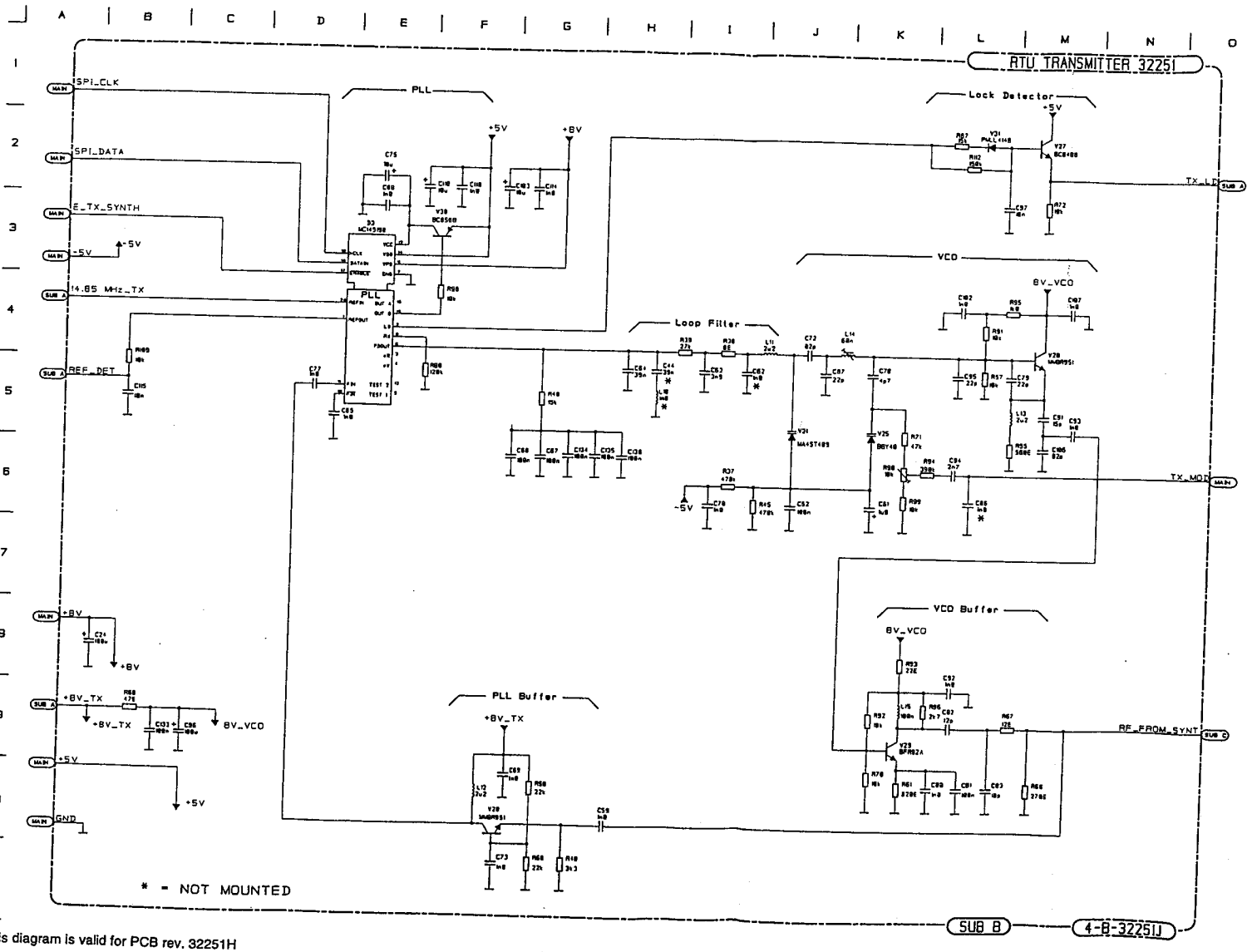
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251



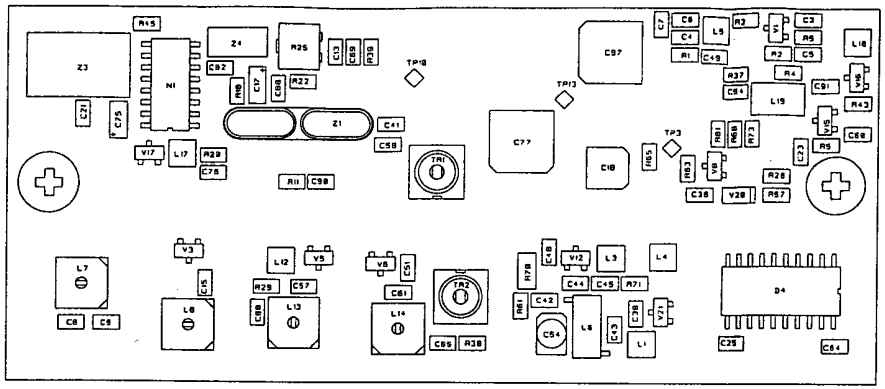
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251

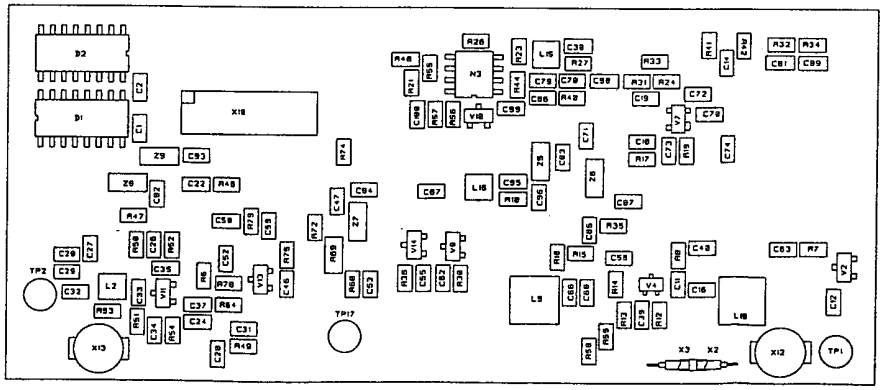


This diagram is valid for PCB rev. 32251H

Component location Receiver unit 632252



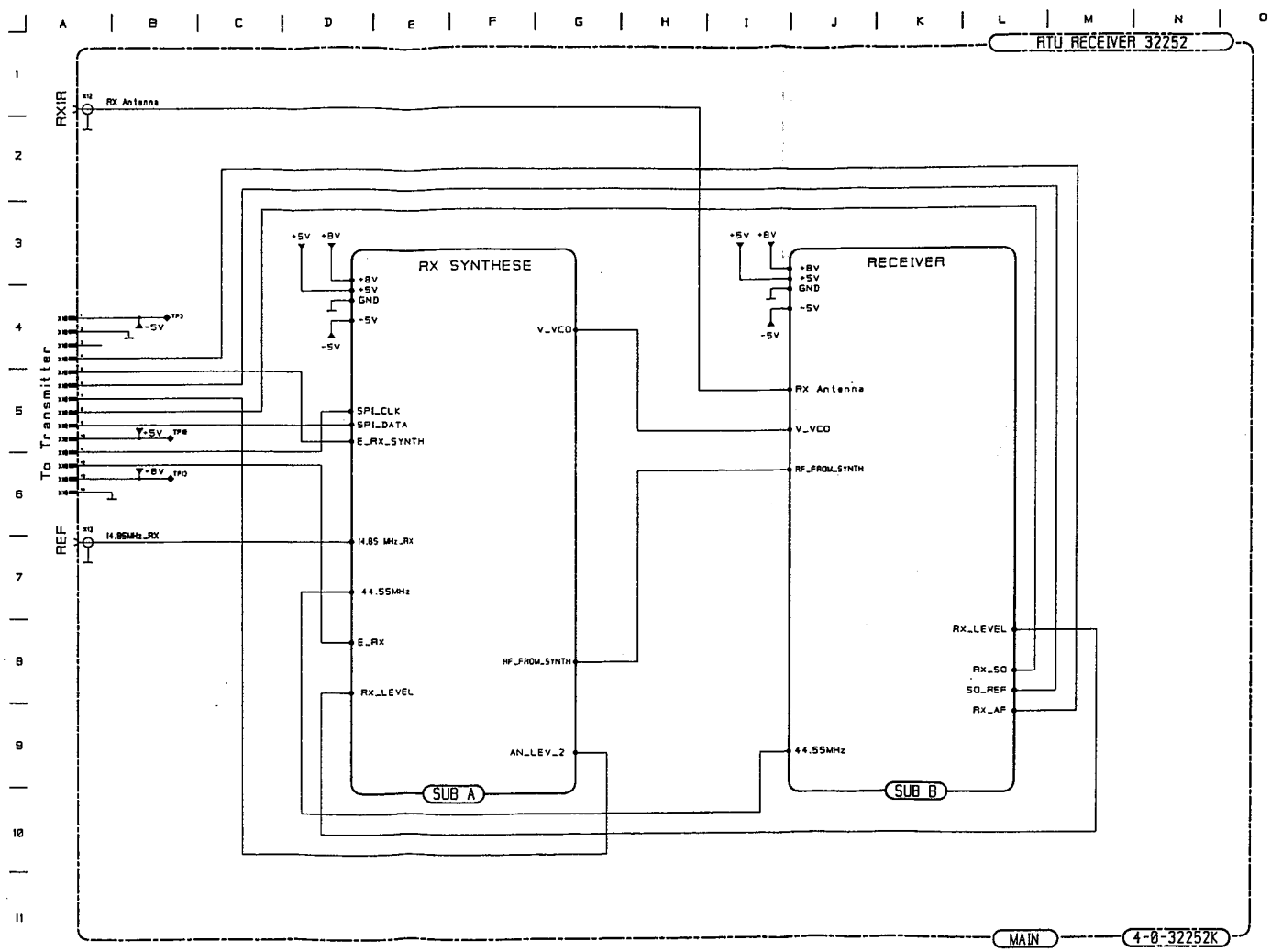
Seen from primary side with primary side tracks.



Seen from secondary side with secondary side tracks.

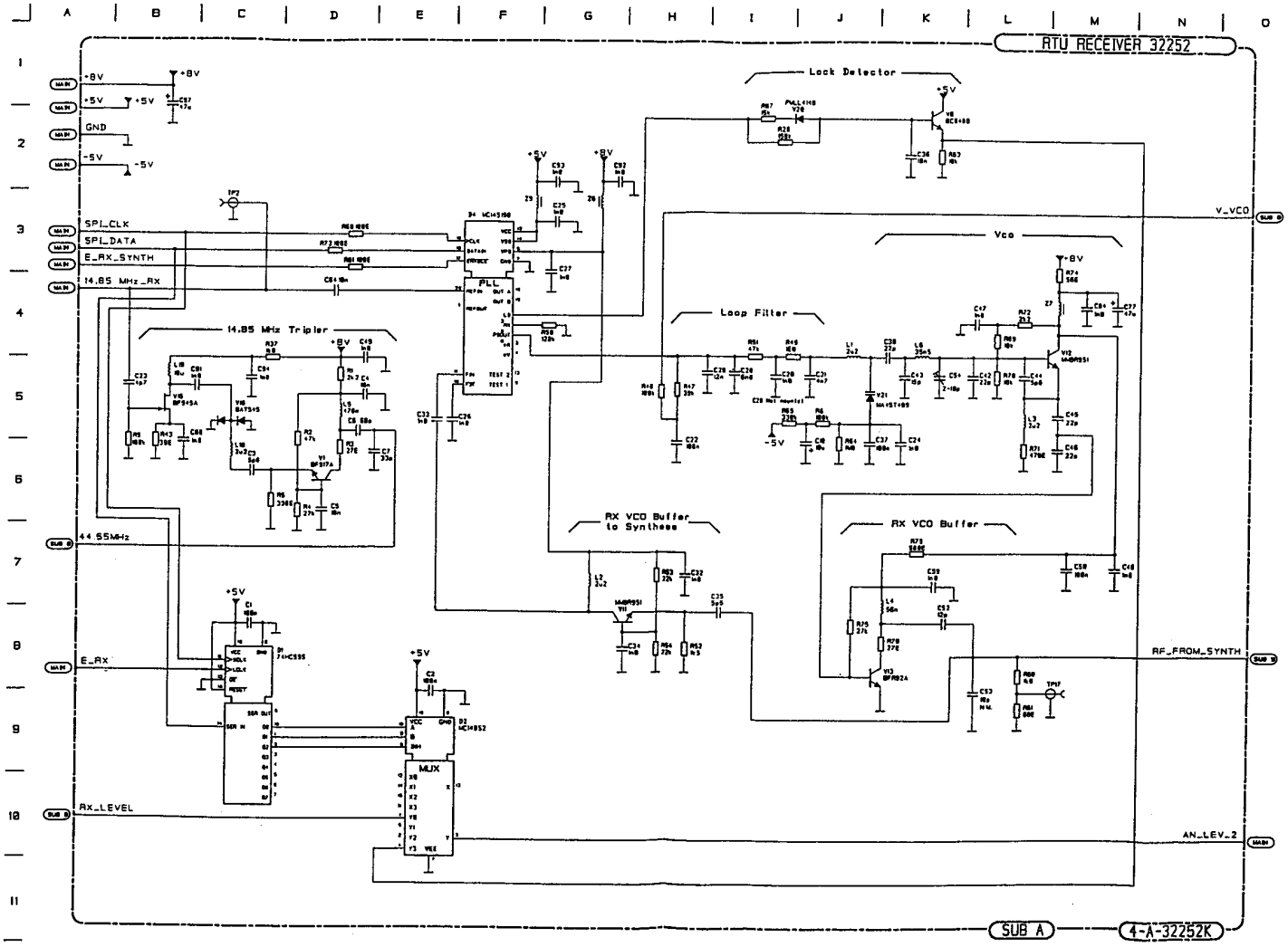
PCB rev. 32252F

Receiver unit 632252



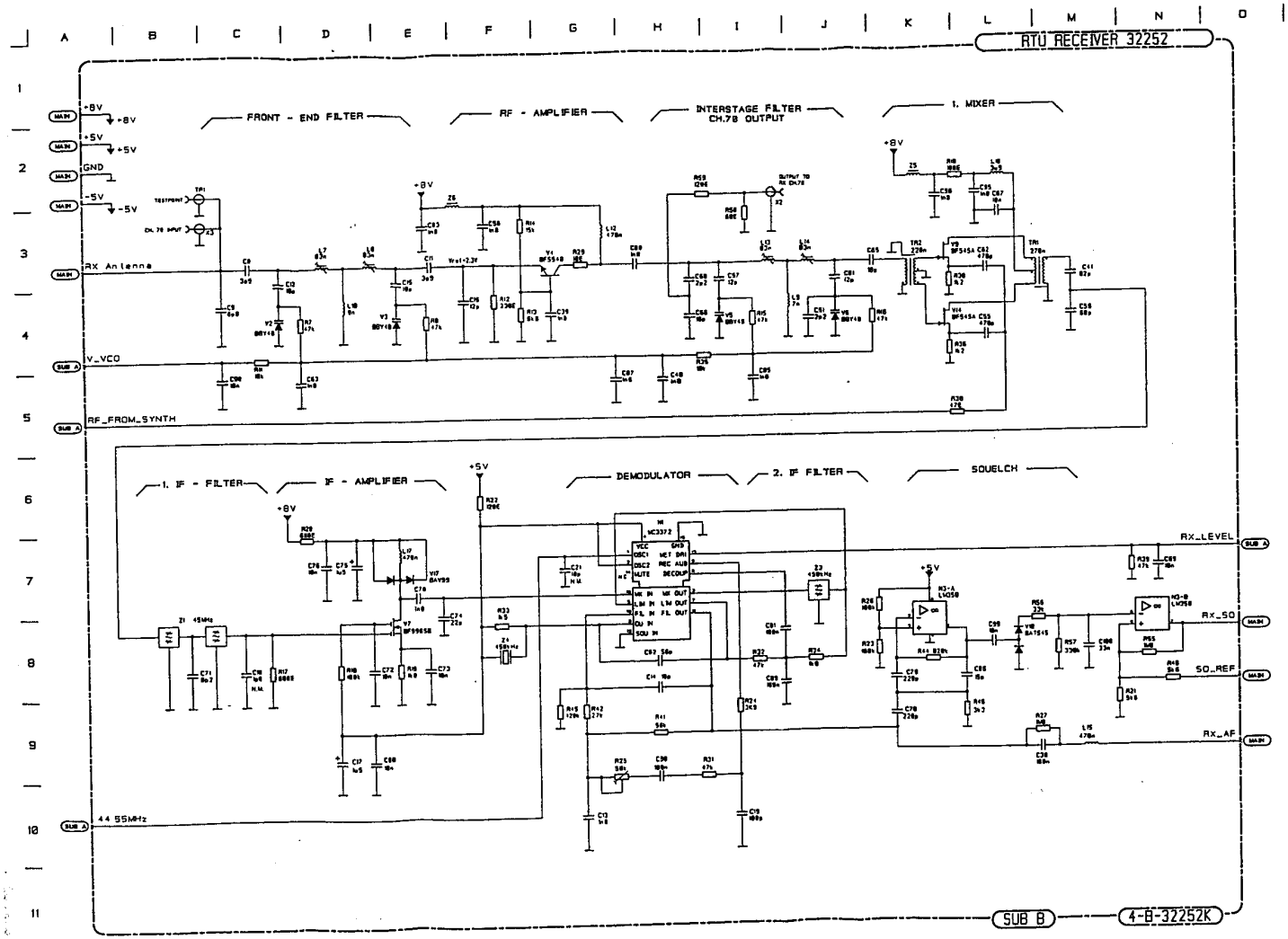
This diagram is valid for PCB rev. 32252F

Receiver unit 632252



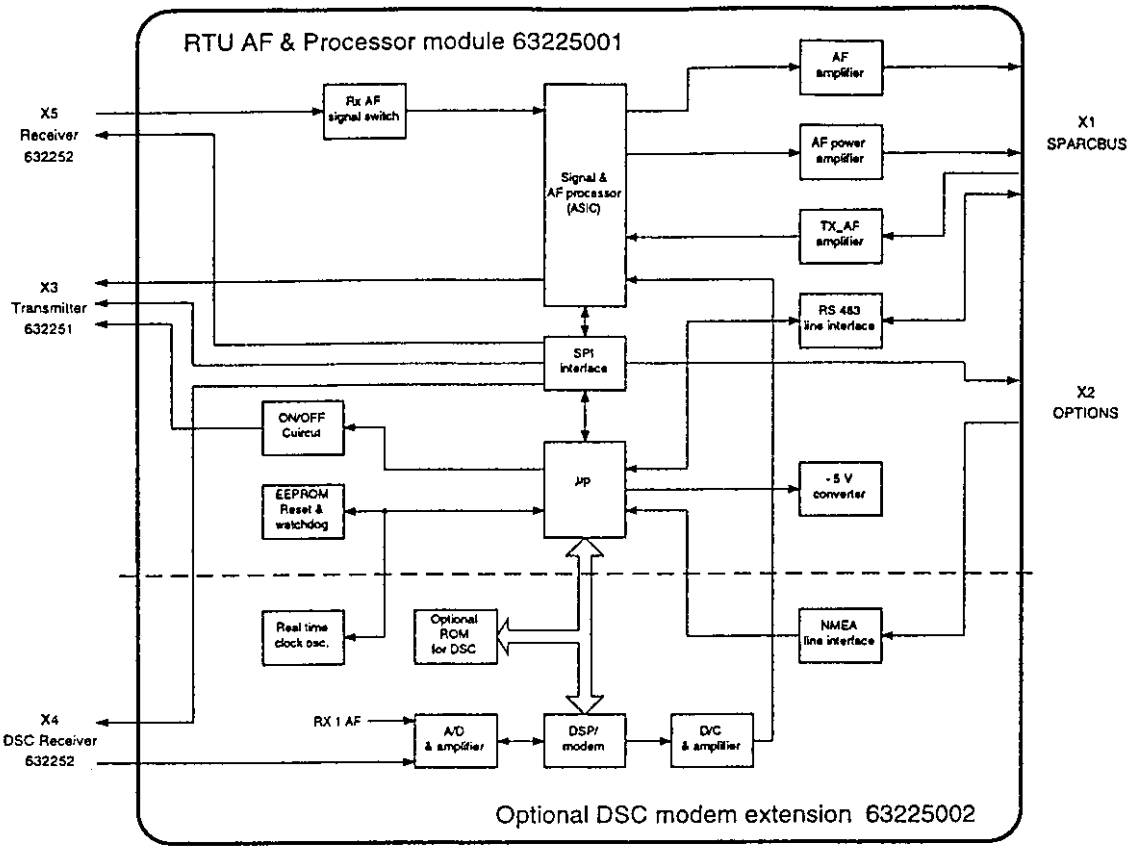
This diagram is valid for PCB rev. 32252F

Receiver unit 632252



This diagram is valid for PCB rev. 32252F

4.1 AF and processor unit 63225001/02



35241

Input selector
N7-A -> N7-C is used as input selector. Selection is made by the microcontroller via latch D11.

Summation amplifier
The inputs are added together in ASIC OP2. To compensate for the lost signal in the input selector the gain is set to 1.1. Output from the summation is fed into ASIC "DET RX in".

ASIC N6
The received signal is de-emphasized for LS1 and LS2 amplifier. The buffered signal is passed on to LF amplifier N2.

Balanced amplifier N3
This amplifier converts the signal from single end to balanced. Alarm tone can be added to the signal.

dB attenuator
V7, R21 is used to attenuate LS1 by 30dB.

LF switch
N8-A is used to mute LS2.

LF amplifier
N2 is a double amplifier with two inputs and outputs; one for LS1 and the other for LS2.
LS1 is for an internal speaker and goes up to 4W in 4W.
LS2 is for an external speaker and goes up to 6W in 4W.

Pre-emphasis
Pre-emphasis is made by C84, R91 and limited by R83, C72, R86 and C67 together with the input amplifier in the ASIC N6.

IF amplifier
The transistor V7 amplifies the 45MHz output signal from the crystal filter to the second mixer, which has a tuned drain circuit consisting of L17, C70 and C74.

Second mixer, demodulator, second IF filter and multiplexer
The 45 MHz signal is down converted to 450 kHz by the second LO of 44.55 MHz. The mixer output is fed through the ceramic filter Z3 to the limiter amplifier and demodulator in the N1. The AF signal is amplified by an internal operation amplifier. The output signal can be adjusted by R25. The RX_level, which is an output from N1 to indicate the strength of the received signal, is multiplexed with the lock detector signal, from the pLL (D4), by D2 and the output is routed to AN_LEV_2.

VCO and VCO buffer
The VCO, which is built around V12, is oscillating at +45 MHz above the selected channel frequency. The oscillator can shift the band by means of the trimmer capacitor C54. The output voltage of the VCO is fed to the VCO buffer, which is implemented with V13.

Loop buffer, PLL and loop filter
The output of the VCO buffer is fed to the prescaler of the PLL, which is implemented by IC MC145190, via the loop buffer. This is realized by V11. The output from the phase detector of the PLL is fed to the VCO through the loop filter providing optimum settling and filtering of the VCO.

Tripler and 44.55 MHz amplifier
The second LO is generated from the 14.85 MHz, which is amplified and clipped by a dual schottky diode V16 generating 3rd harmonic signal. This signal is selectively amplified at 44.55 MHz by V1.

4.5 Interface unit 632253

Power supply
+5V, +8V, and +12V are applied from the transceiver unit 632250.
Negative supply for the contrast voltage to the display is generated by the circuit around N1-D including temperature compensation.

On/off circuit
The on/off circuit is used for the detection of the on/off condition. Hardware turn on and software turn off.
The on/off key is separately read by the microprocessor input pin_25.
The circuit around V6-V7 enables the microprocessor to watch the state of the on/off key, together with the hardware turn-on function by pulling the line signal ON_OFF logic low.

Reset
A reset circuit (D2) keeps the microprocessor reset for at least 100 milliseconds after power on, waiting for voltage settling before program execution starts up.

Microprocesser, memories and chip selection
The microprocessor used is an H83003 (D4), and with a 512 kbyte PROM, a 128 kbyte RAM, and a 128 kbyte Flash PROM, it makes the microcomputer part of the control unit. The processor has a built-in watchdog, which will reset the system if program failure occurs.
The EEPROM (256 bytes) D3 is used to read/store setup parameters used in the control unit.

Backlight
There are three different circuits for regulating indicators (N1-A), display (N1-C) and keyboard (N1-B). The microprocessor makes a voltage by means of a PWM output. This voltage is used as a reference input for the regulation.

Contrast control
The microprocessor makes a voltage by means of a PWM output. This voltage is amplified (N1-D) and used as the contrast voltage for the display.

SPARC-bus interface
The RS483 driver (D11) is used as a SPARC-bus interface to communicate with the transceiver and other control units.

Centronics interface
The Centronics interface is used to print out received DSC calls. The latches (D8,D9) are the hardware interface.

MIC amplifier
The microphone amplifier signal (MIC) is converted from unbalanced to balanced in the circuit around N7. The AF signal is the input to the transmitter.

RX AF
The RX AF is converted from balanced to unbalanced in the circuit around N6-D.

Intercom
When an intercom between control units is performed, the SPARC-bus AF signal is switched by N5-A and converted (balanced/unbalanced) by the circuit around N6-C.

Summation amplifier and attenuator
The summation point of the AF is made in N3-D. The audio attenuator (N2) is used to control the output level to the earpiece.

Earpiece amplifier
The earpiece amplifier N4-A amplifies the signal from the volume control to the earpiece in the handset. (TLF).

Power driver
This part of the transmitter chain consists of two amplifier stages. The first stage of amplification is accomplished by a common emitter buffer, V15. A switching transistor, V14, shuts this stage down during reception. This stage delivers 13 dBm and the output power rise and decay times are shaped in such a way that frequency pulling of the VCO is avoided.
The final discrete stage of amplification contains a medium power VHF transistor, V7, running in class C. This amplifier puts 25 dBm out during transmission and is turned off during reception in order to save current.

PA stage
The final boost of amplification consists of an integrated power module, N1, capable of delivering 30W and withstanding a large amount of load mismatch. This stage provides a minimum gain of 20 dB, which can be reduced by varying the supply voltage to the first amplifier in the power module. This feature is used in order to obtain two output powers: 1W and 25W.

Harmonic filter
All of the harmonic signals of the carrier frequency are suppressed by a 7th order elliptic filter.

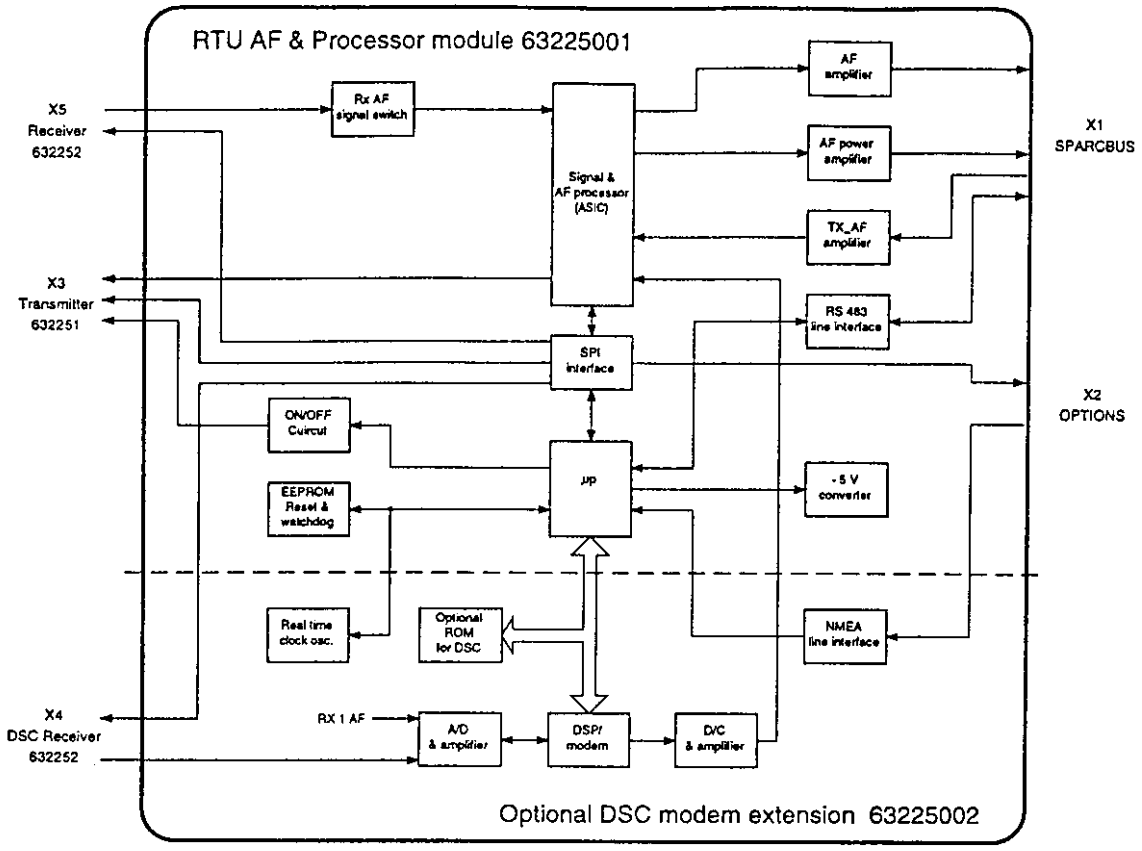
Aerial switch
The aerial is switched between the transmitter and the receiver by relay K1. As an option the transceiver can be operated as a coast station in reverse duplex by means of a second aerial relay, K2.

SWR Detector
The SWR detector consists of three elements: a directional coupler and two power detectors. The coupler samples forward and reverse going power in the transceiver.
A temperature compensated power detector consisting of an operational amplifier, N4-A, and two fast switching diodes, V32 and V33, provides the regulating circuitry with a voltage proportional to the output power.
The same circuitry used in the power detector is used in the reverse power detector around N4-B, V37 and V38. This is done to avoid transmitting at a high power level in case of aerial failure or high SWR.

Power regulator
The heart of the power regulator is the operational amplifier N4-C, which compares the detected output power with a power setting voltage. In this way the output power from the transmitter can be regulated by adjusting the voltage at pin 10 of N4-C. The transistor V26 is one of the shutdown mechanisms incorporated in the transmitter. This transistor and the surrounding RC network also contribute to the power envelope shaping done at the first stage of the power driver.
The HIGH-LOW power selection is done by shunting the output voltage from the forward power detector with V34.
Finally, the output from N4-C is buffered by the amplifier around V5 and V6, which is capable of driving the PA stage.

Temperature sensor
A forward biased transistor, V3, placed near the PA stage is used as a temperature sensor to alert the controlling circuitry and thereby prevent damage at the PA stage due to high temperatures.

4.1 AF and processor unit 63225001/02



35241

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The final discrete stage of amplification contains a medium power VHF transistor, V7, running in class C. This amplifier puts 25 dBm out during transmission and is turned off during reception in order to save current.

PA stage
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Harmonic filter
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Power regulator
The heart of the power regulator is the operational amplifier N4-C, which compares the detected output power with a power setting voltage. In this way the output power from the transmitter can be regulated by adjusting the voltage at pin 10 of N4-C. The transistor V26 is one of the shutdown mechanisms incorporated in the transmitter. This transistor and the surrounding RC network also contribute to the power envelope shaping done at the first stage of the power driver.
The HIGH-LOW power selection is done by shunting the output voltage from the forward power detector with V34.
Finally, the output from N4-C is buffered by the amplifier around V5 and V6, which is capable of driving the PA stage.

Temperature sensor
A forward biased transistor, V3, placed near the PA stage is used as a temperature sensor to alert the controlling circuitry and thereby prevent damage at the PA stage due to high temperatures.