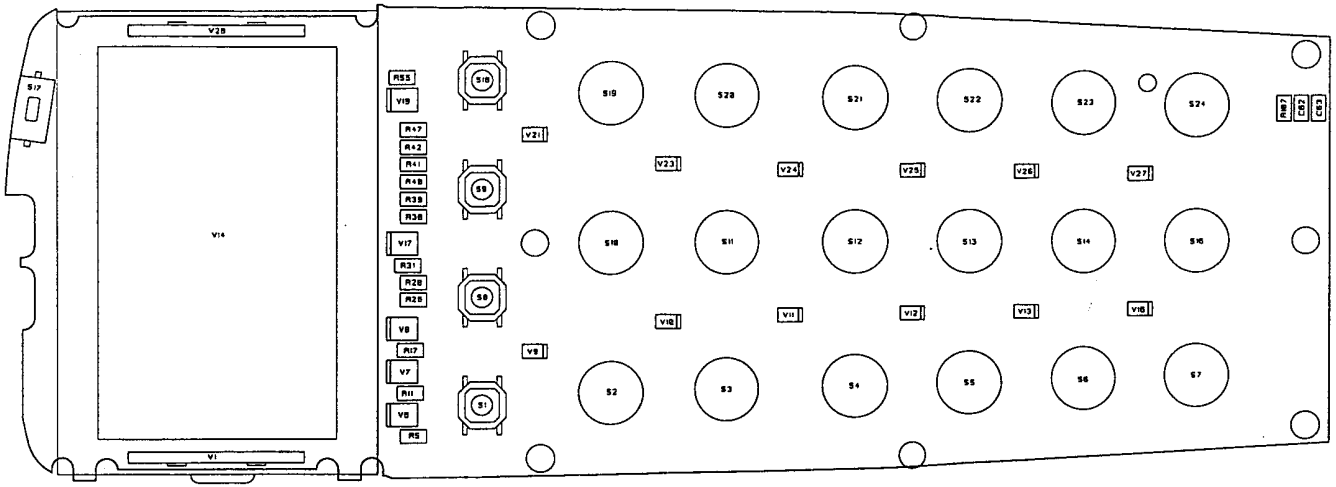
5.1 HxC AF & MMI Unit 632261

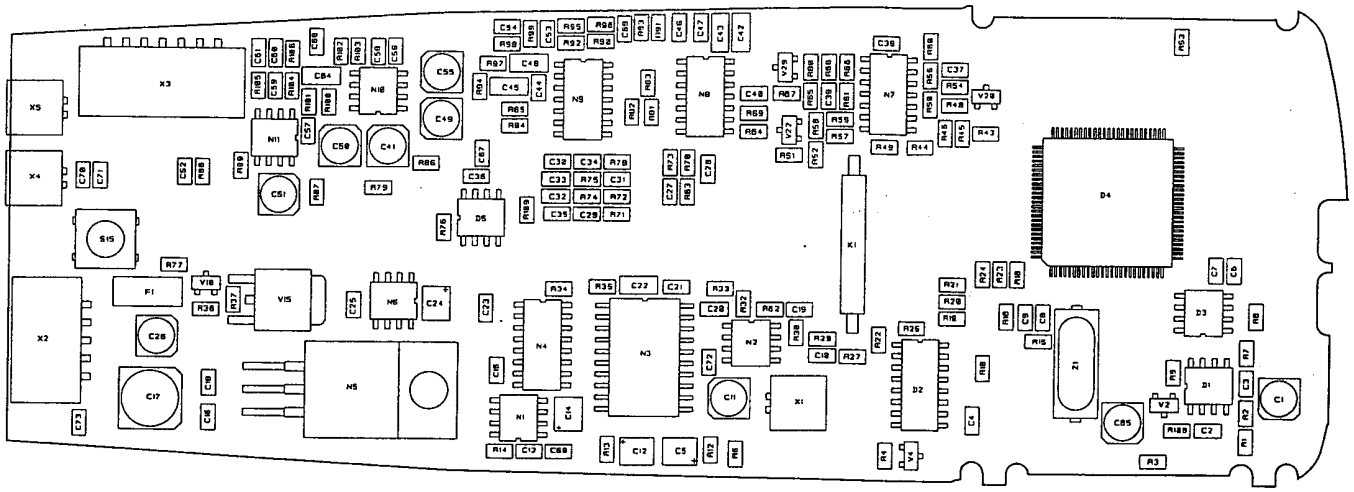
Component location HxC AF & MMI Unit 632261



Seen from primary side with primary side tracks.

PCB rev. 32261E

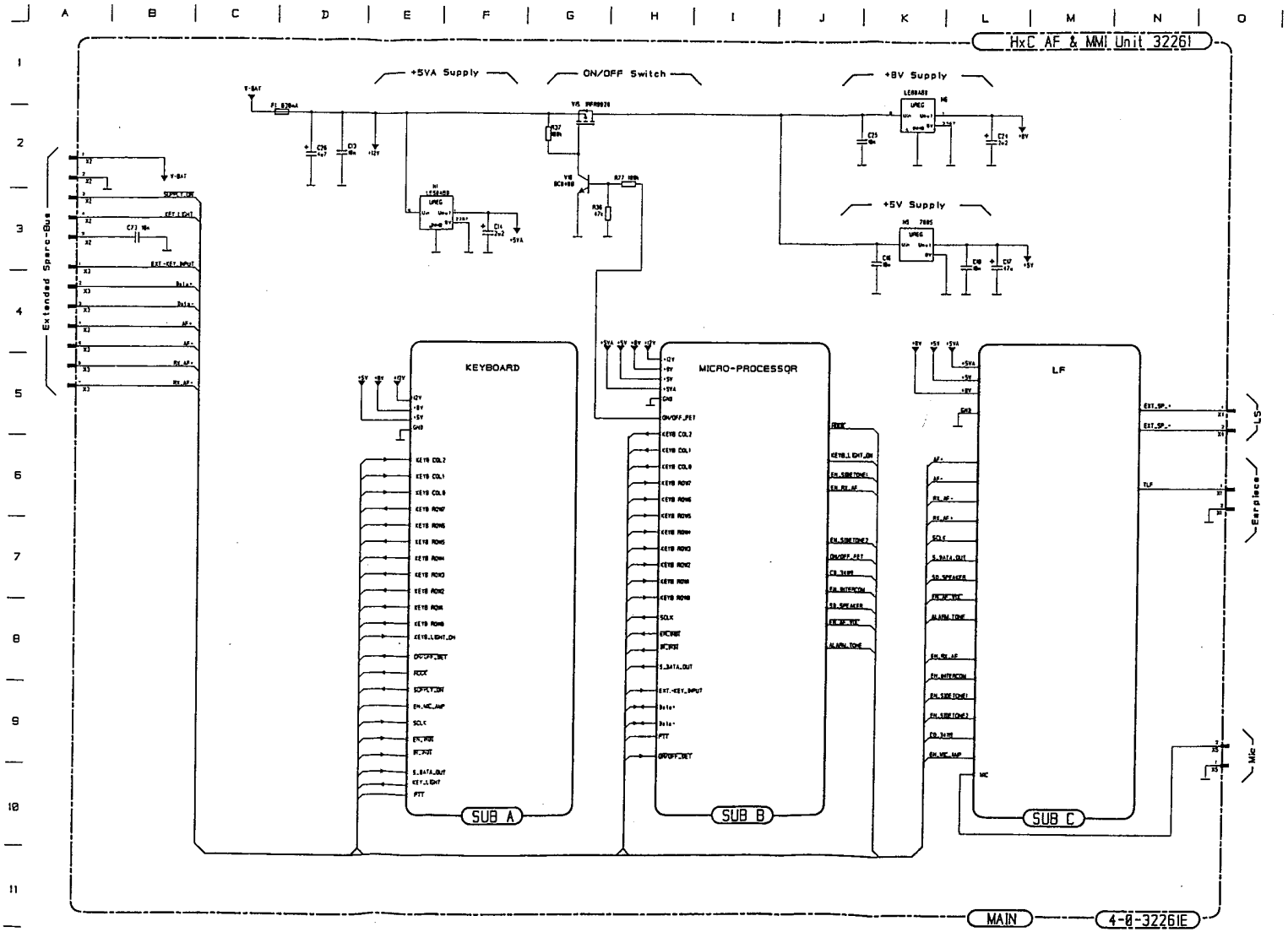
Component location HxC AF & MMI Unit 632261



Seen from secondary side with secondary side tracks.

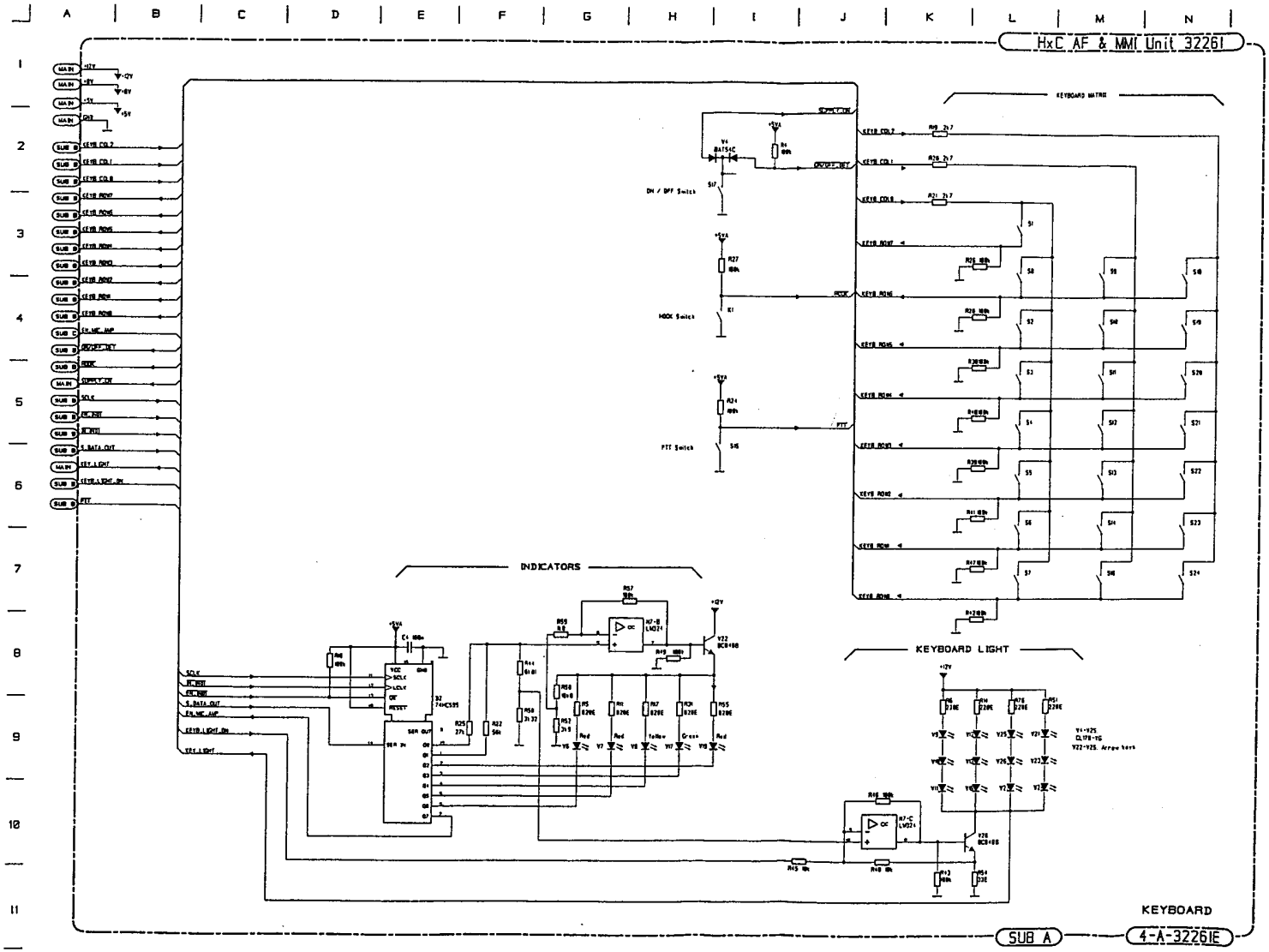
PCB rev. 32261E

HxC AF & MMI UNIT 632261



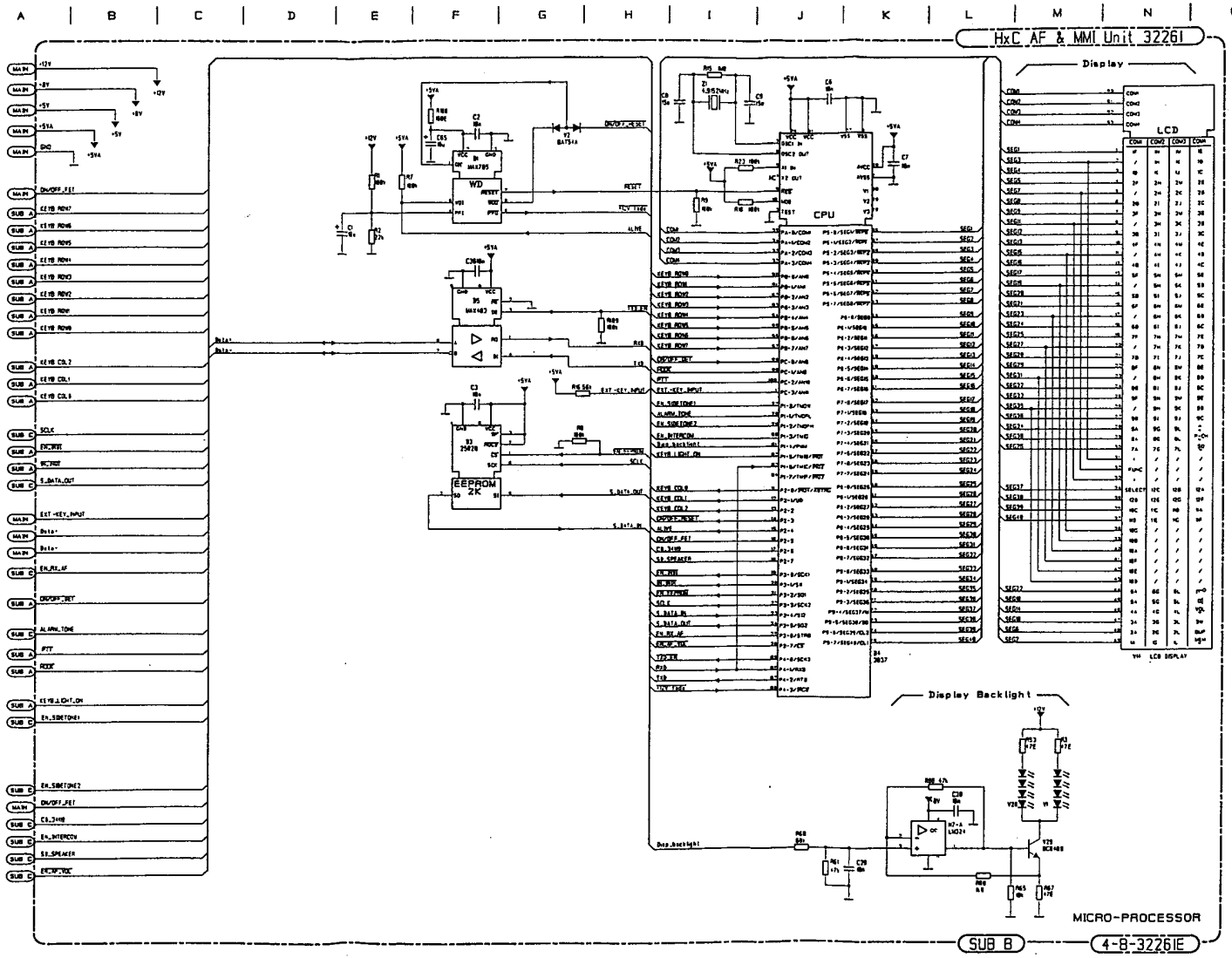
This diagram is valid for PCB rev. 32261E

HxC AF & MMI UNIT 632261



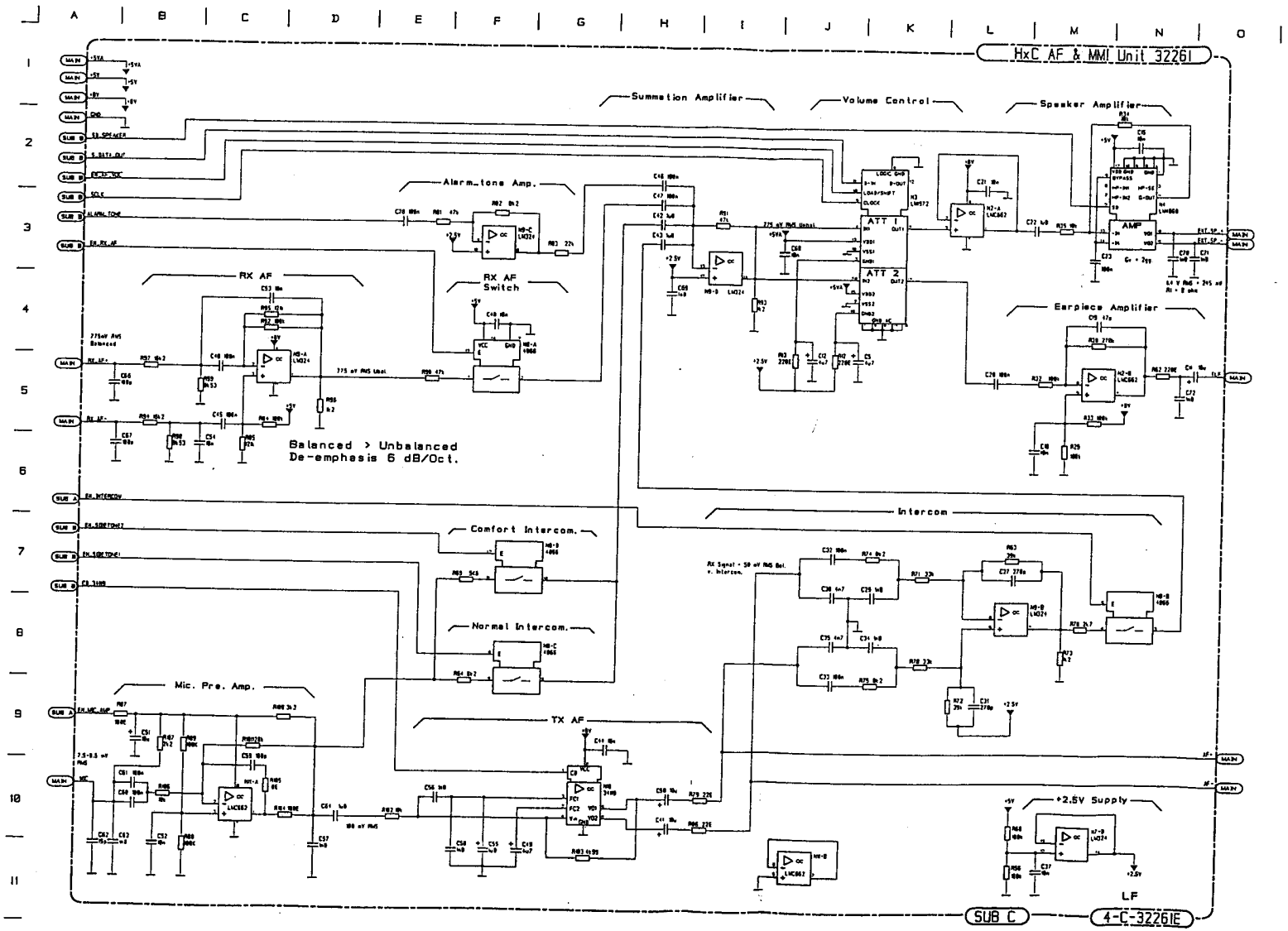
This diagram is valid for PCB rev. 32261E

HxC AF & MMI UNIT 632261



This diagram is valid for PCB rev. 32261E

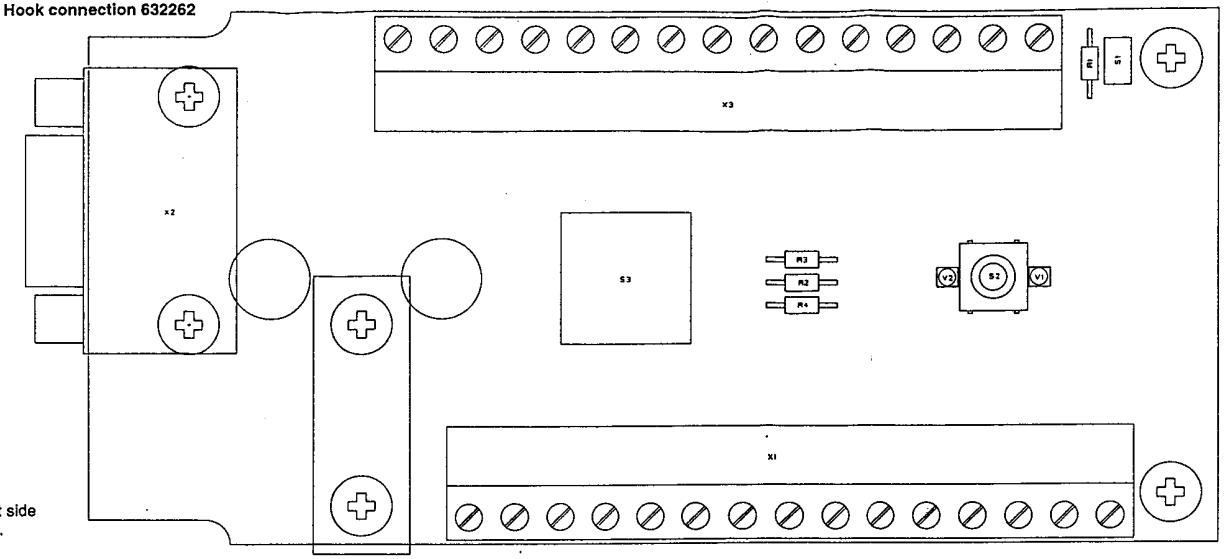
HxC AF & MMI UNIT 632261



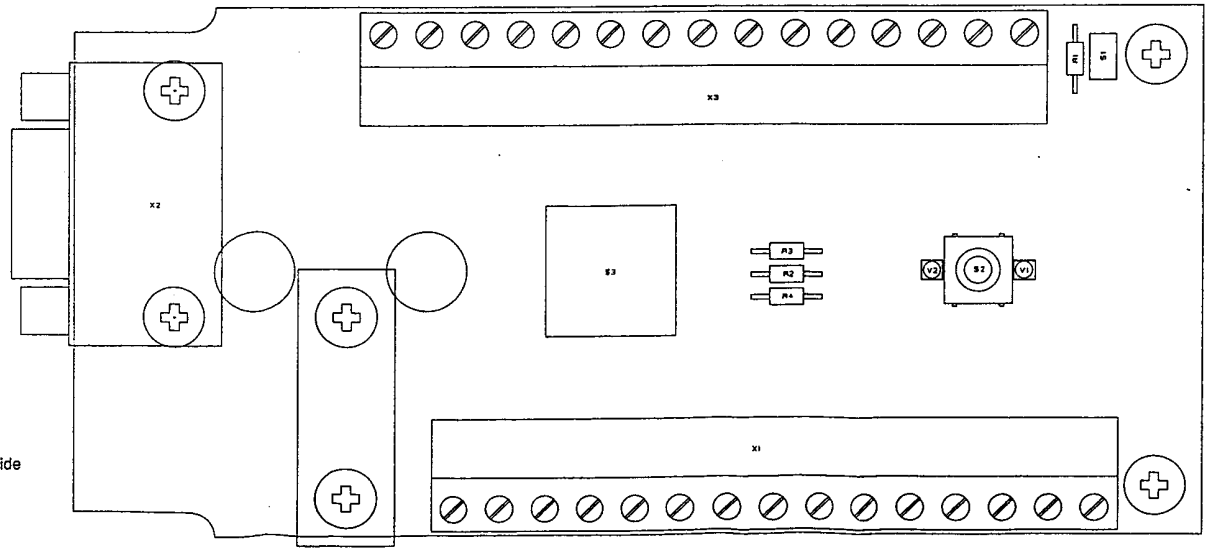
This diagram is valid for PCB rev. 32261E

5.2 Hook Connection 632262

Component location Hook connection 632262



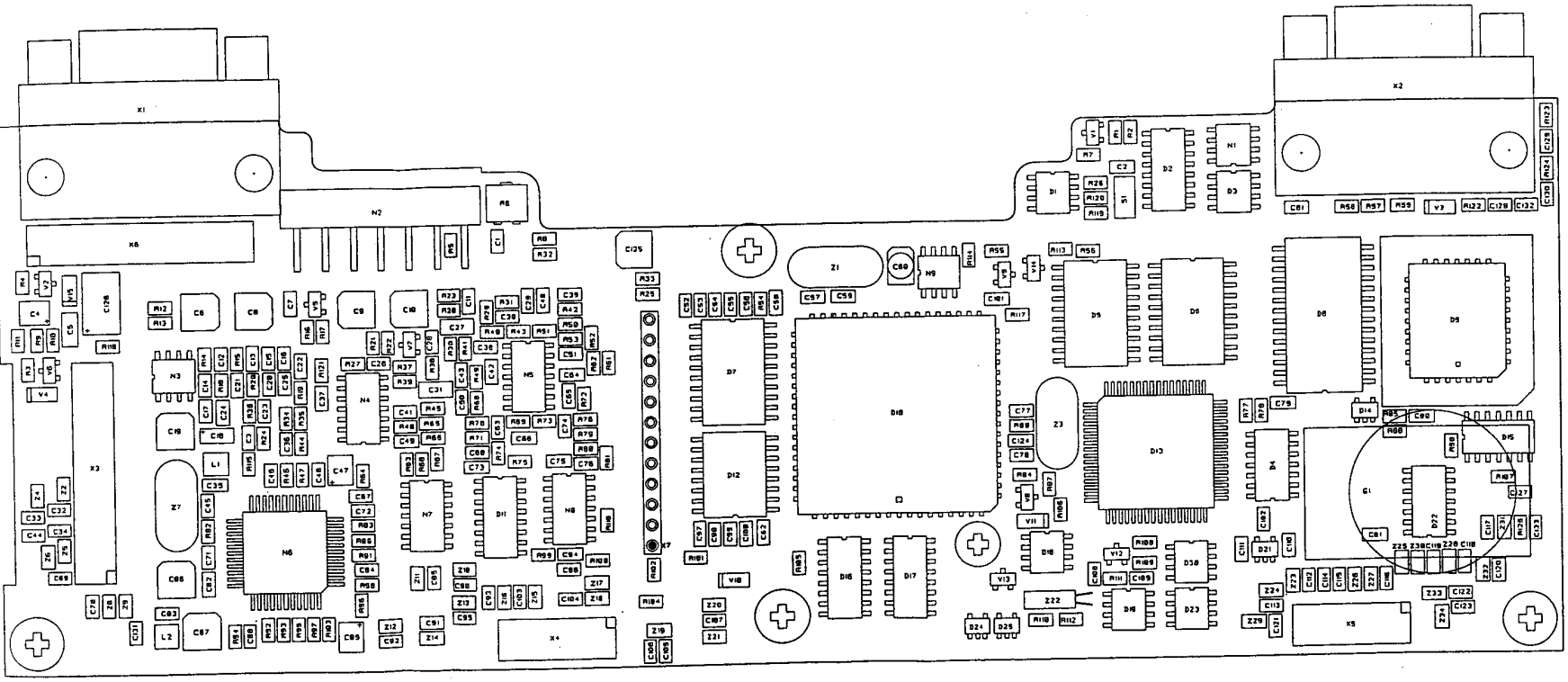
Seen from component side with upper side tracks.



Seen from component side with lower side tracks.

PCB rev. 32262C

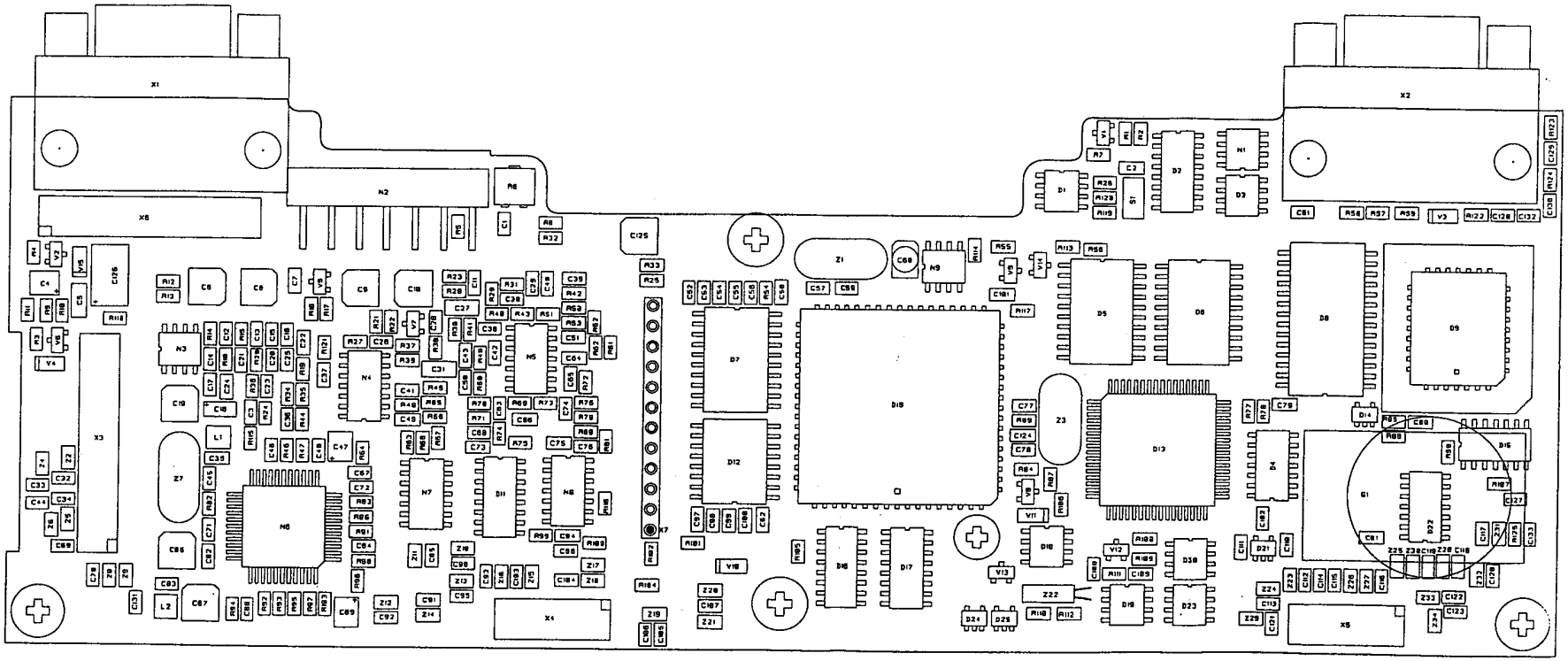
component location AF and processor unit 63225001/02



Seen from component side with upper side tracks.

PCB rev. 32250G

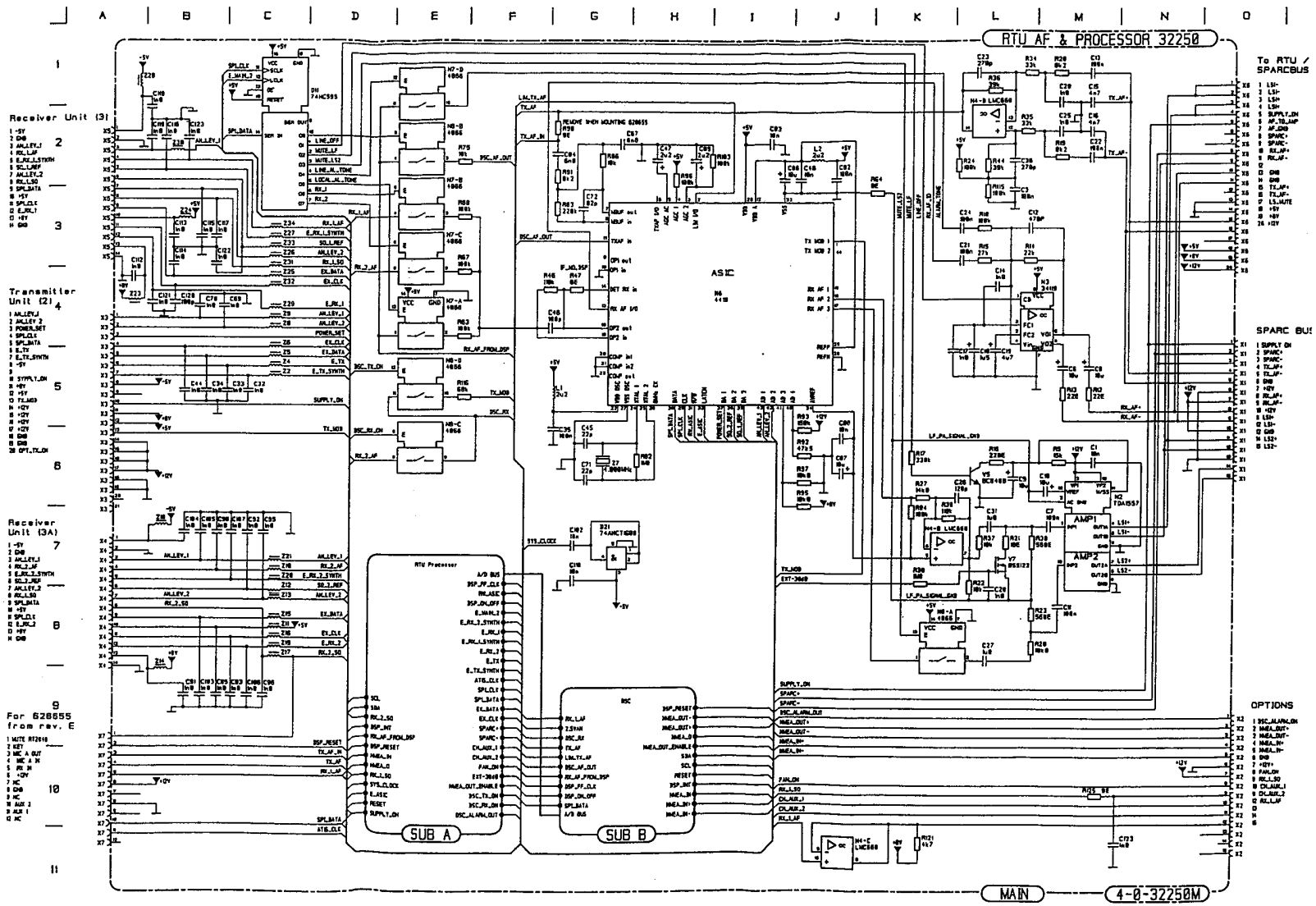
Component location AF and processor unit 63225001/02



Seen from component side with lower side tracks.

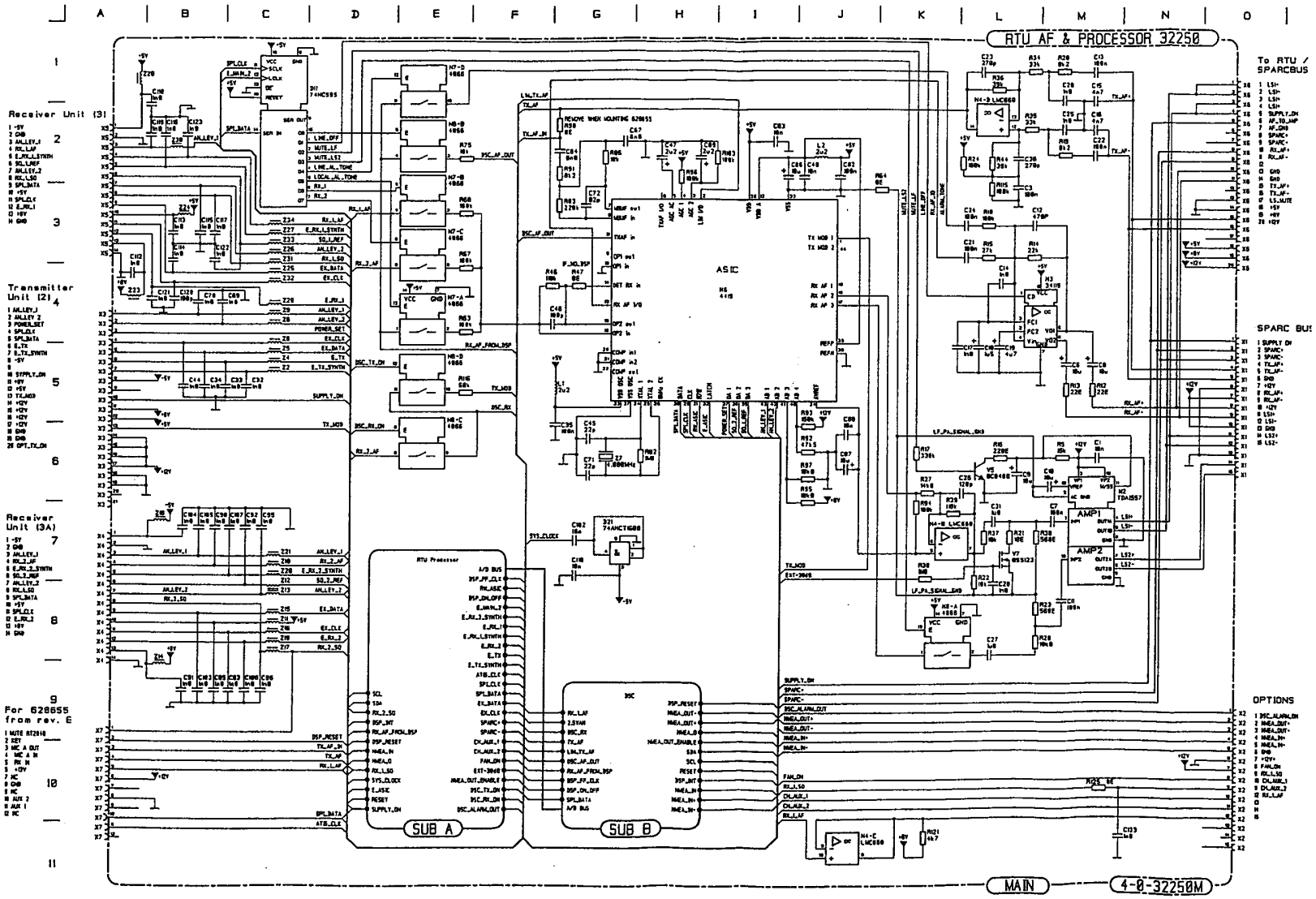
PCB rev. 32250G

AF and processor unit 63225001/02



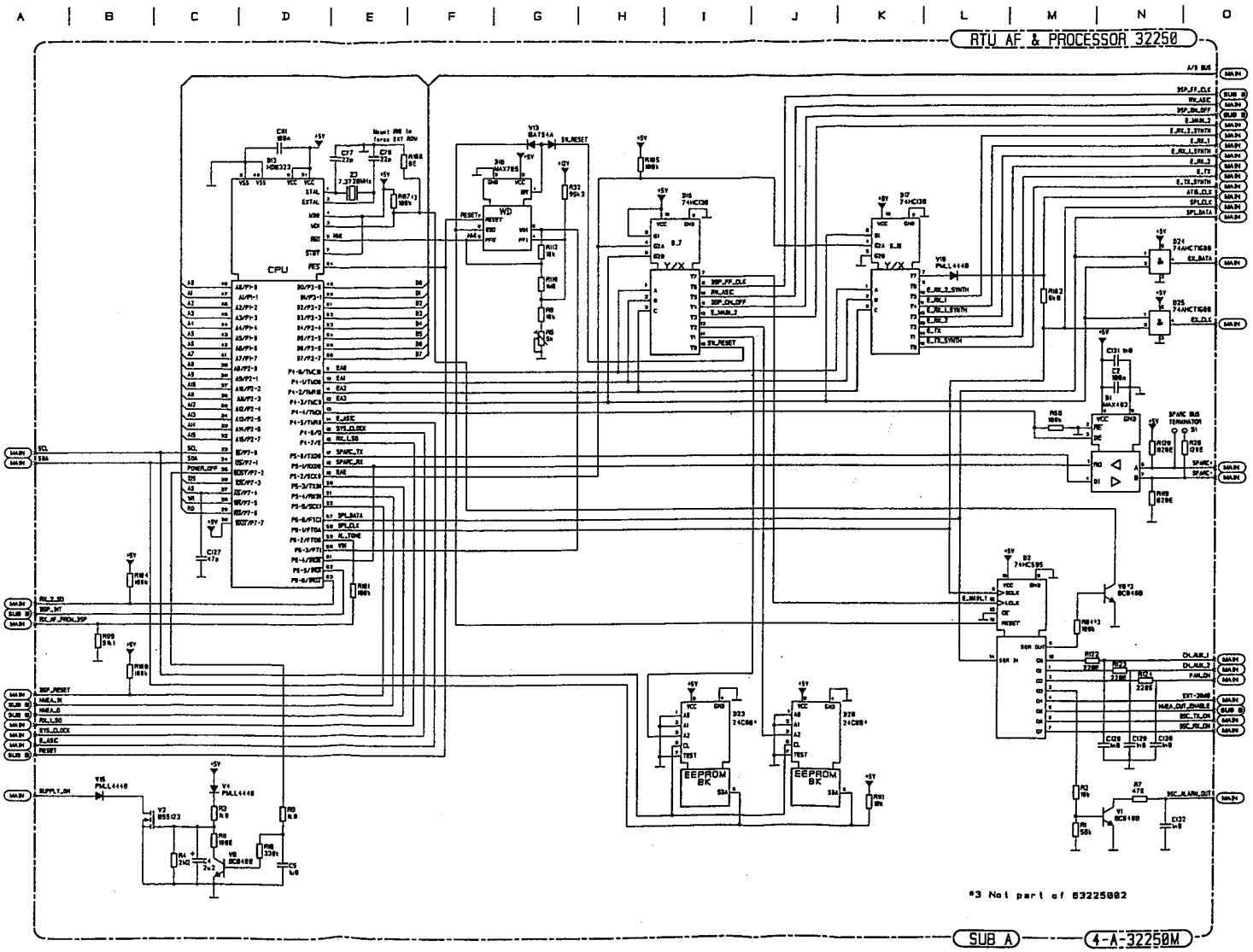
This diagram is valid for PCB rev. 32250G

AF and processor unit 63225001/02



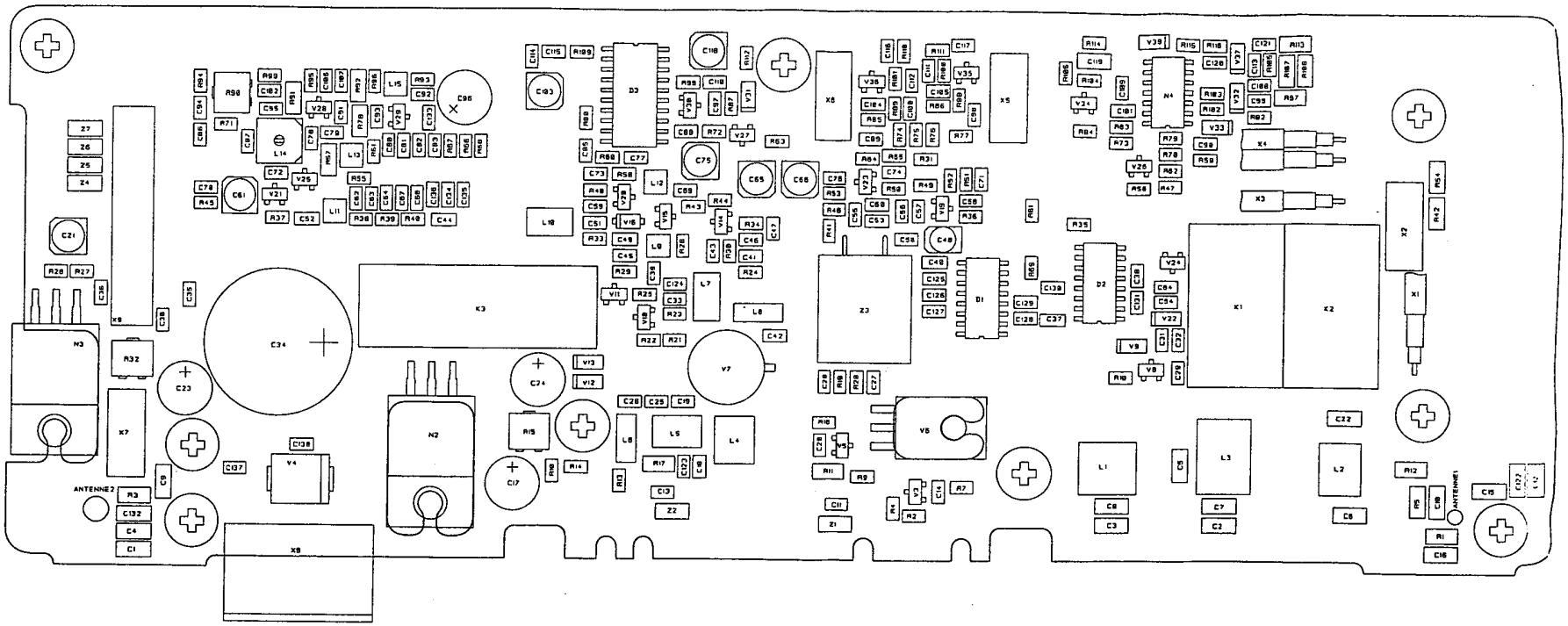
This diagram is valid for PCB rev. 32250G

AF and processor unit 63225001/02



This diagram is valid for PCB rev. 32250G

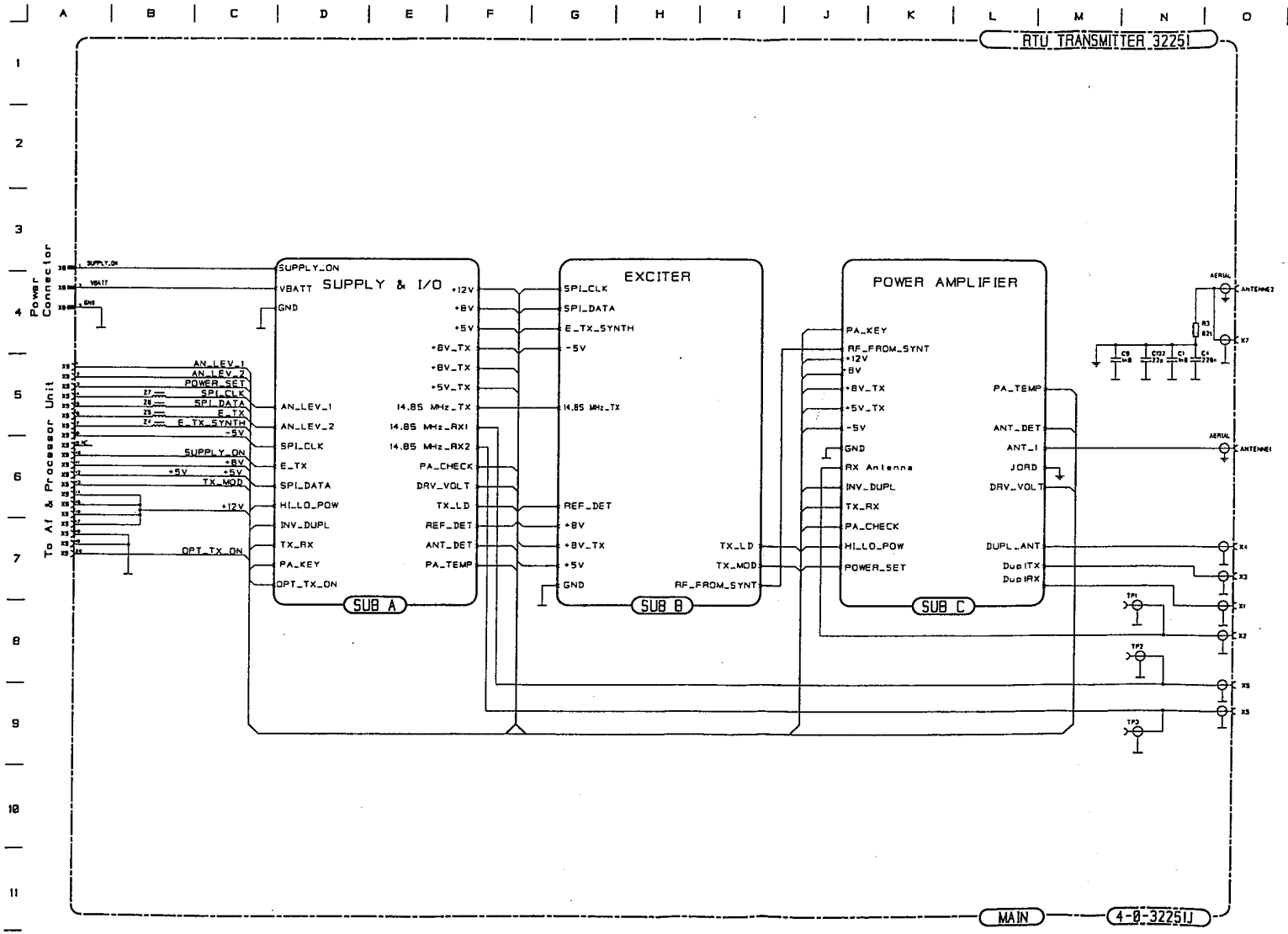
Component location Transmitter unit 632251



Seen from primary side with primary side tracks.

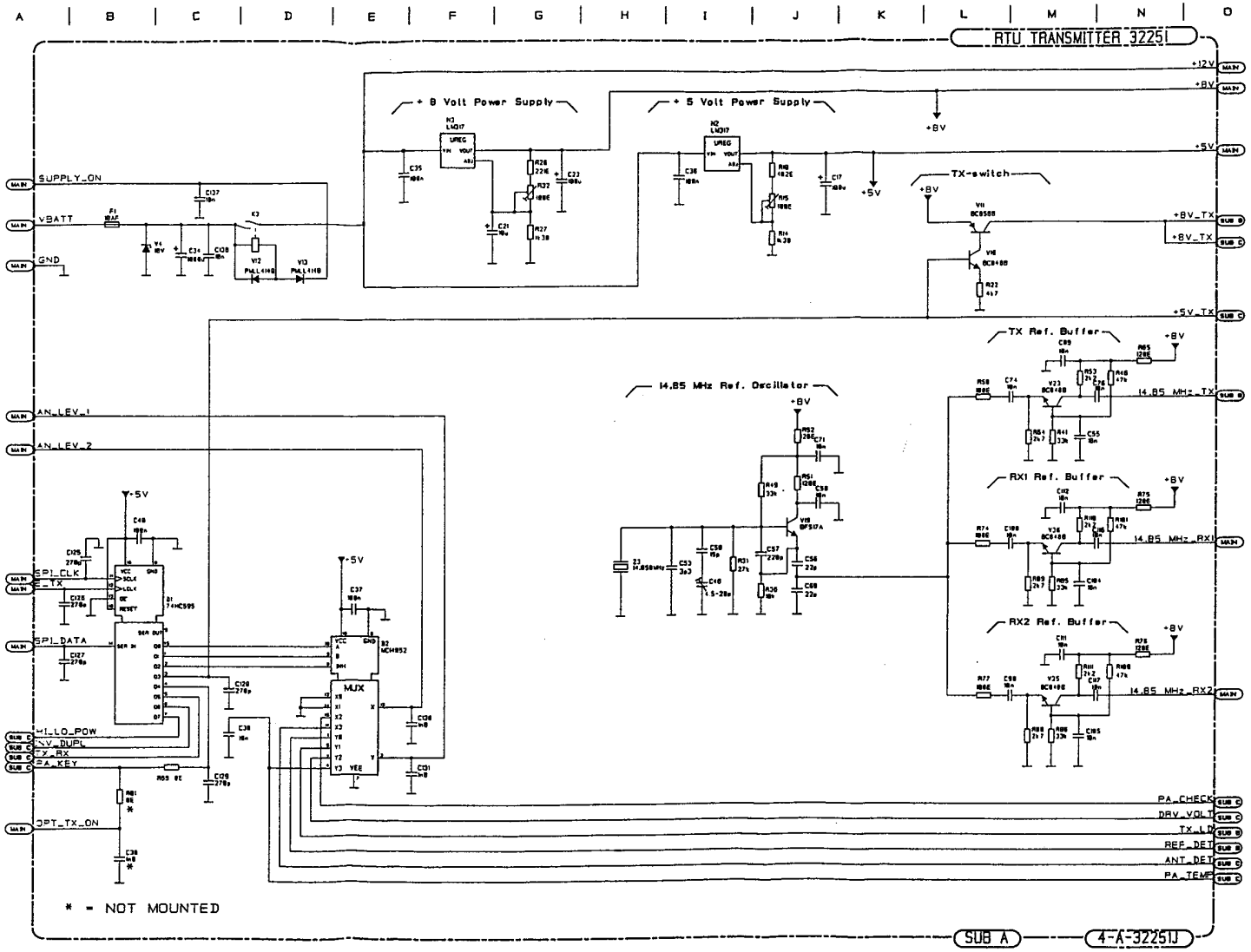
PCB rev. 32251H

Transmitter unit 632251



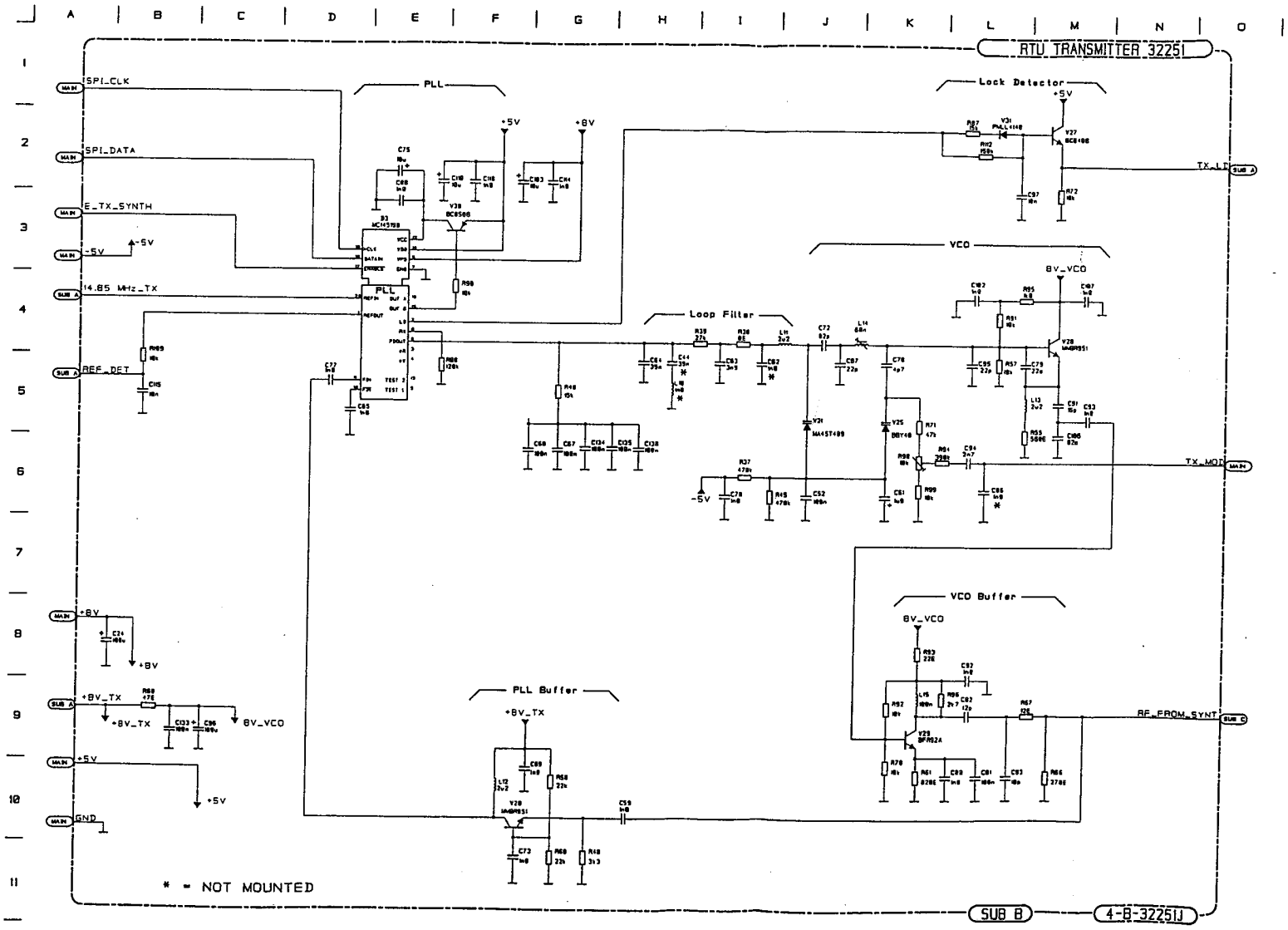
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251



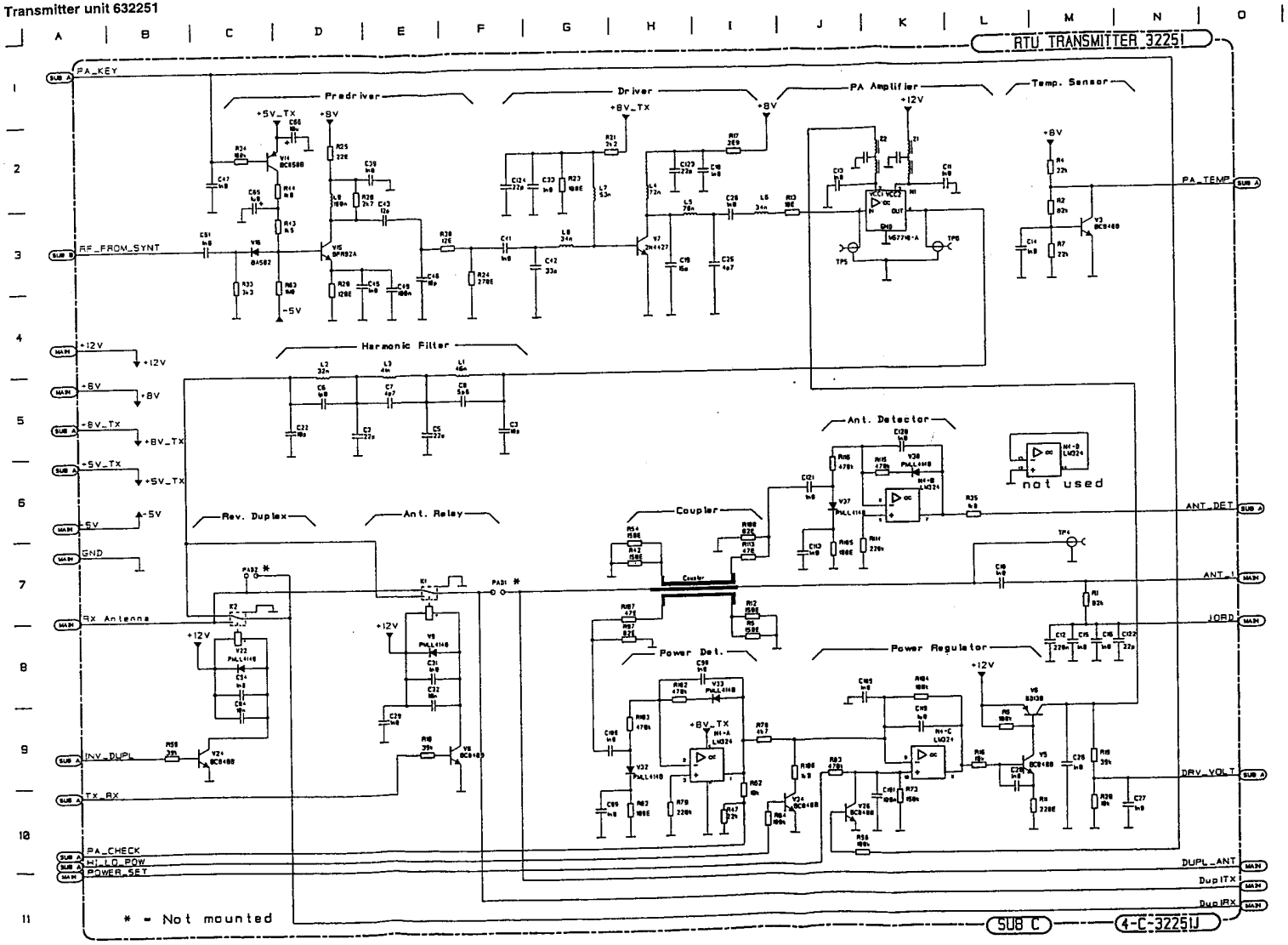
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251



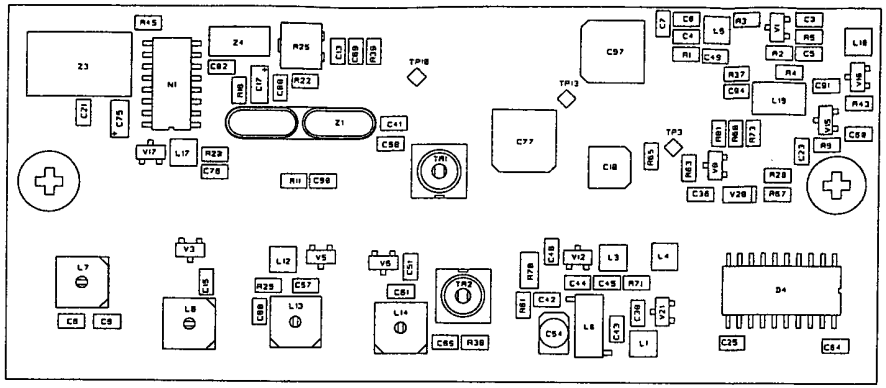
This diagram is valid for PCB rev. 32251H

Transmitter unit 632251

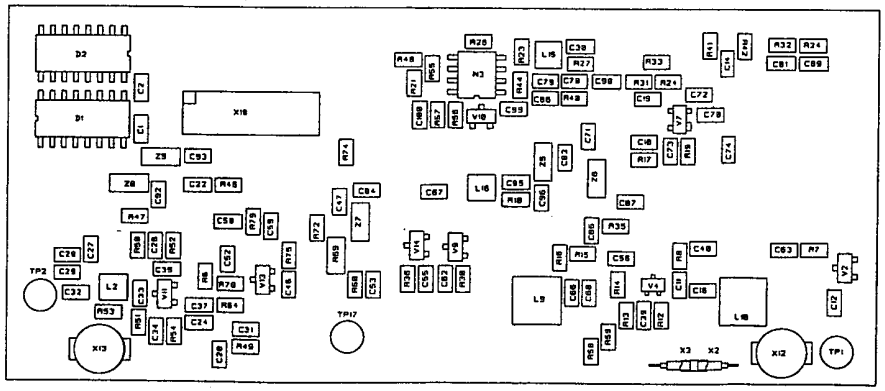


This diagram is valid for PCB rev. 32251H

Component location Receiver unit 632252



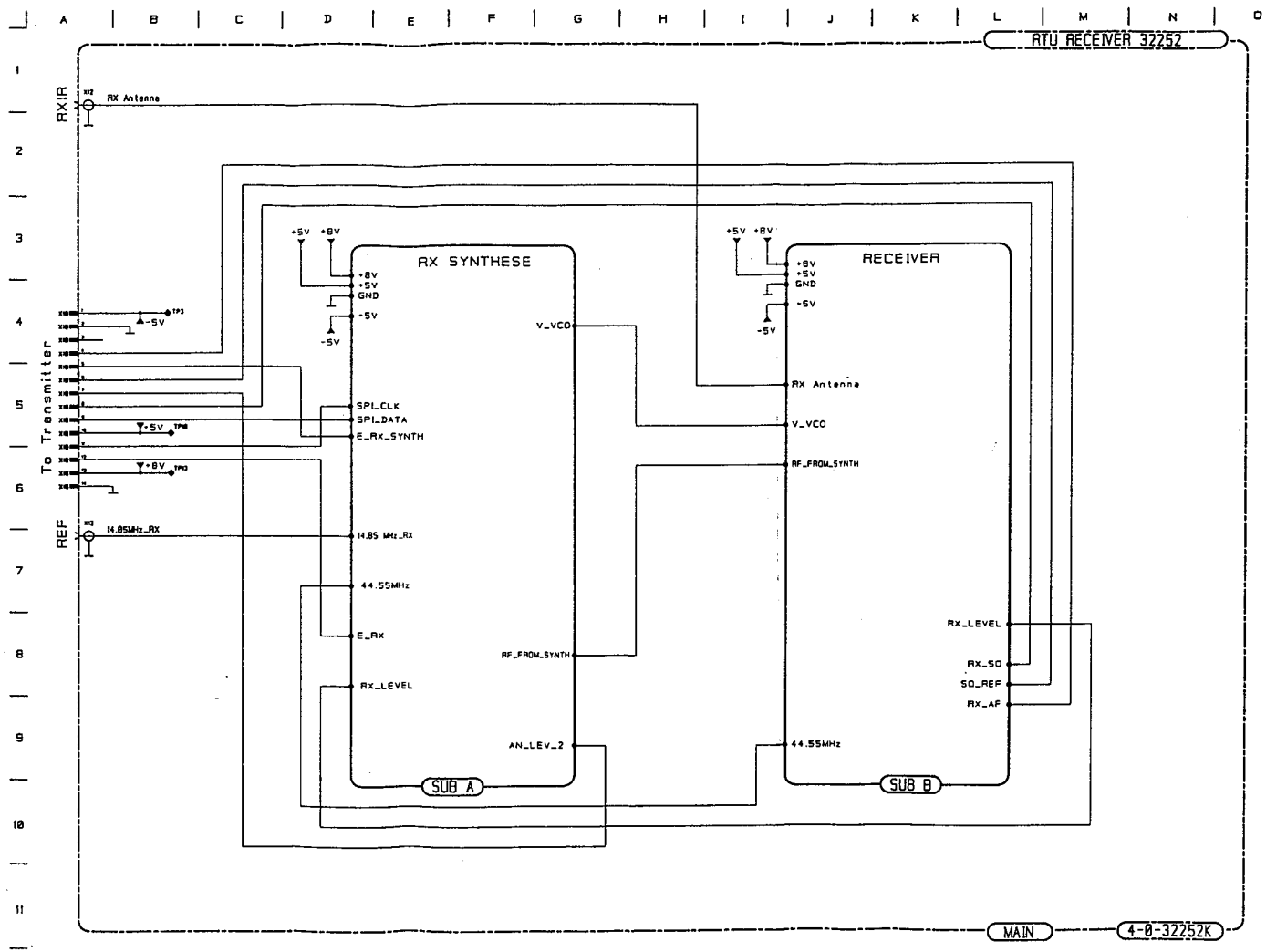
Seen from primary side with primary side tracks.



Seen from secondary side with secondary side tracks.

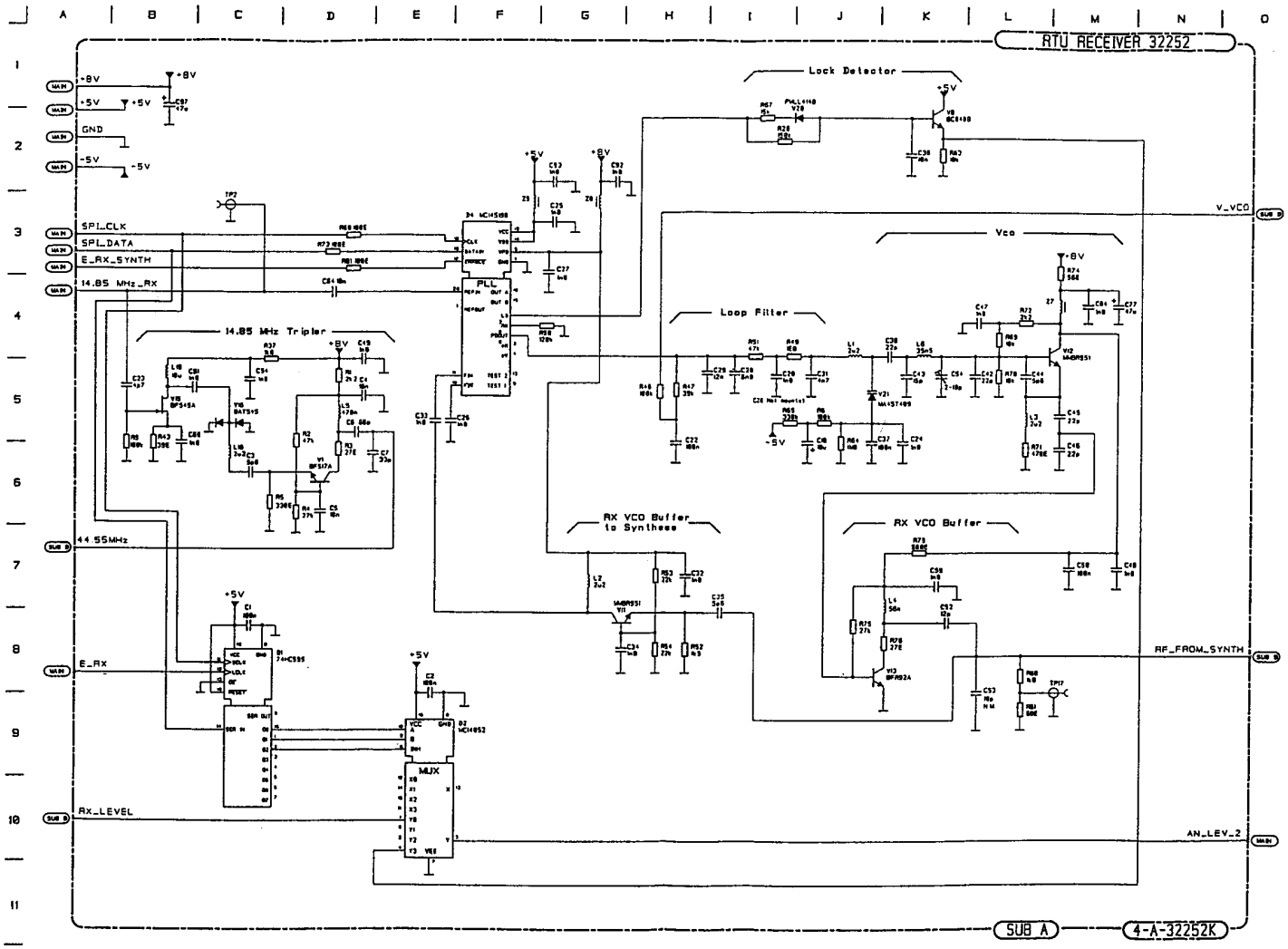
PCB rev. 32252F

Receiver unit 632252



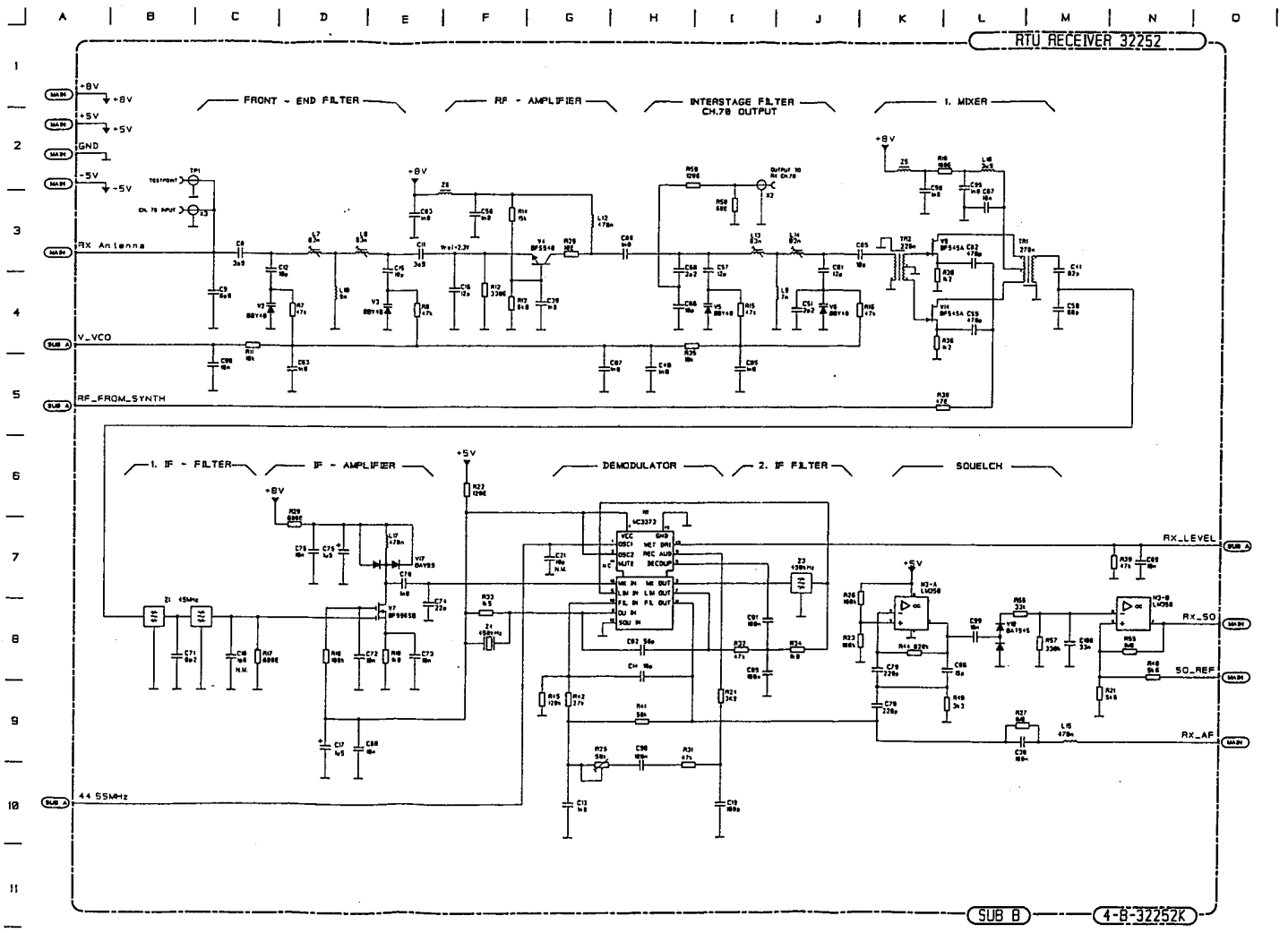
This diagram is valid for PCB rev. 32252F

Receiver unit 632252

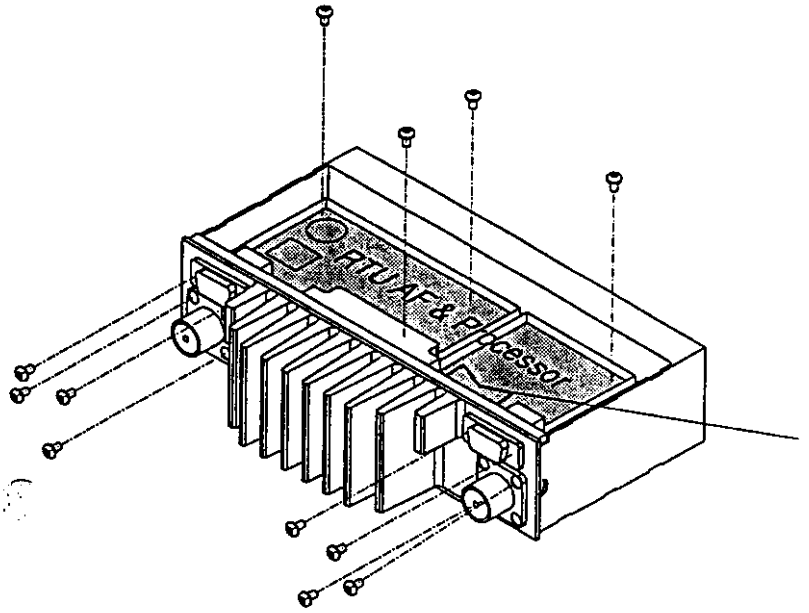


This diagram is valid for PCB rev. 32252F

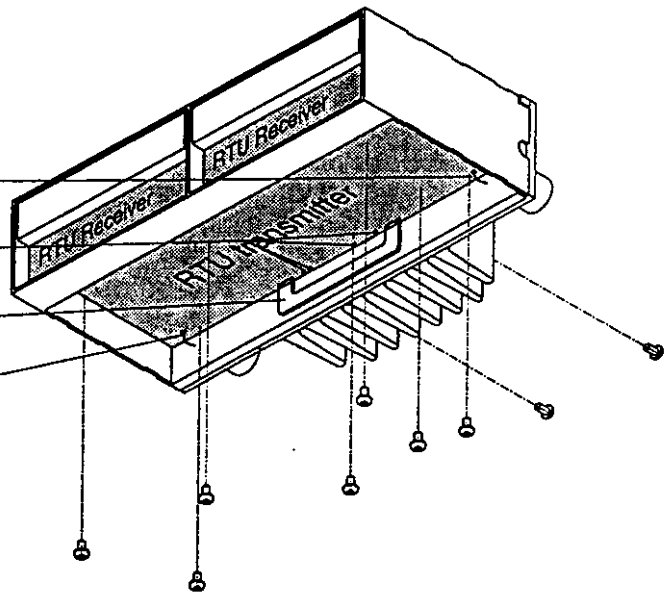
Receiver unit 632252



This diagram is valid for PCB rev. 32252F



Spring to sot-141 (58.514)



Antenna 1 terminal

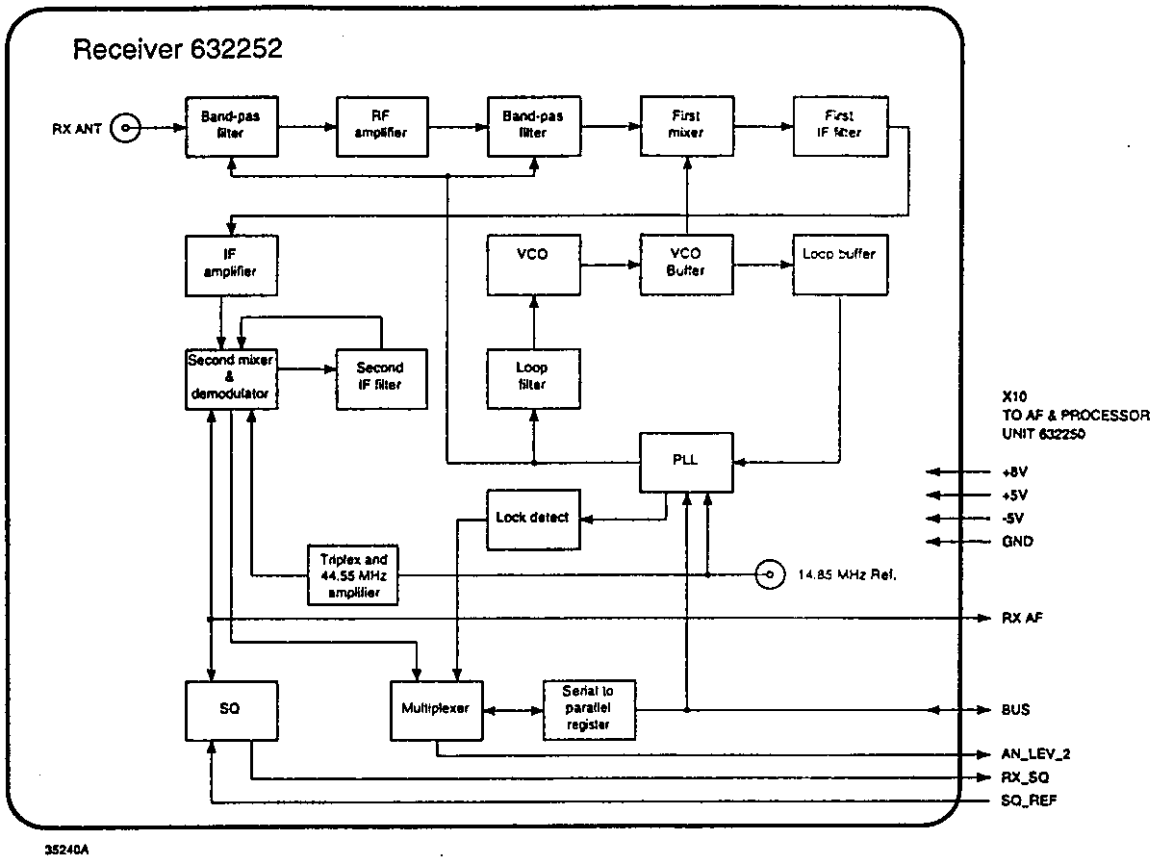
Solded PA. pins

Thread plate (233561)

Antenna 2 terminal

4-0-36036

4.3 Receiver unit 632252



The receiver is of the type FM double superheterodyne with a first intermediate frequency of 45 MHz and upper-injection first LO. Second intermediate frequency is 450 kHz with lower-injection secondLO.

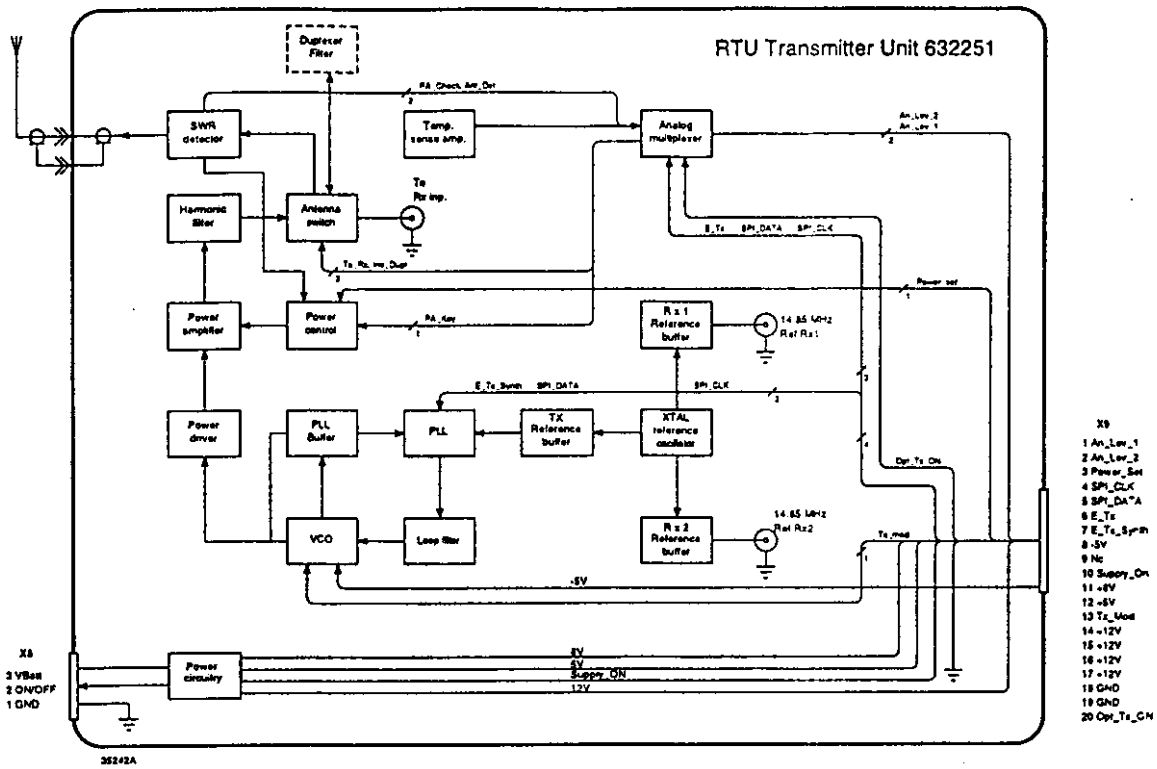
Band-pass filters
The received signal is led through an aerial relay to the input band-pass filter. This filter and the intermediate band-pass filter are controlled by a DC voltage on the diodes capacitors V2, V3, V5 and V6. This DC voltage is driven from the RX-VCO control voltage, and it secures an optimum filter response in the whole frequency range of the receiver. These two filters can be adjusted by L7, L8, L13 and L14 to create the necessary attenuation of unwanted signals and obtain maximum sensitivity.

RF amplifier
The RF amplifier covers the frequency range from 150.8MHz to 163.6MHz, and has high gain and low noise figure. The amplifier is implemented with V4.

First mixer
The first mixer is a balanced mixer implemented with V9 and V14, which are of the J-FET type. The RF signal is led to the balanced input transformer TR2 and then to the gates of the J-FET's, which are switched by injecting the first LO signal in to the sources of the V9 and V14. The mixed signals are fed to the balanced output transformer TR1 where the wanted signal on 45MHz is selected by the tune circuit consisting of TR1, C41 and C58.

First IF filter
The receiver adjacent channel selectivity is maintained by means of a 4-pole crystal filter Z1 in co-operation with the ceramic filter Z3. R17 gives the impedance matching of output of the crystal filter.

4.2 Transmitter unit 632251



Power circuitry

A power relay, K3, switches the transceiver on and off. Polarity inversion is avoided by means of a fuse, F1, and a high current zener diode, V4. The power supply also includes two voltage regulators, N2 and N3, providing +5V and +8V, respectively. These supplies are adjustable since they provide a voltage which is used as a reference.

Reference oscillator

In order to accomplish a constant and stable transmitting and receiving frequency, the transceiver includes a 14.850 MHz crystal oscillator with a precision of 10 ppm (5 ppm. is optional). The oscillator, which is of the Colpitts type, is built around V19 and Z3, and its frequency can be adjusted with trimmer capacitor C48. In order to avoid frequency pulling, three identical common base amplifiers are used. These three amplifiers have their inputs connected to the reference oscillator, while their outputs provide separate reference signals to the transmitter and the receiver(s).

Analogue multiplexer

An analogue multiplexer, D2, provides the capability of monitoring 6 analogue voltages carrying information about the functionality of the transmitter. This multiplexer is controlled by an 8 bit serial to parallel register, D1. This register also controls the transmitter state (ON/OFF) and output power.

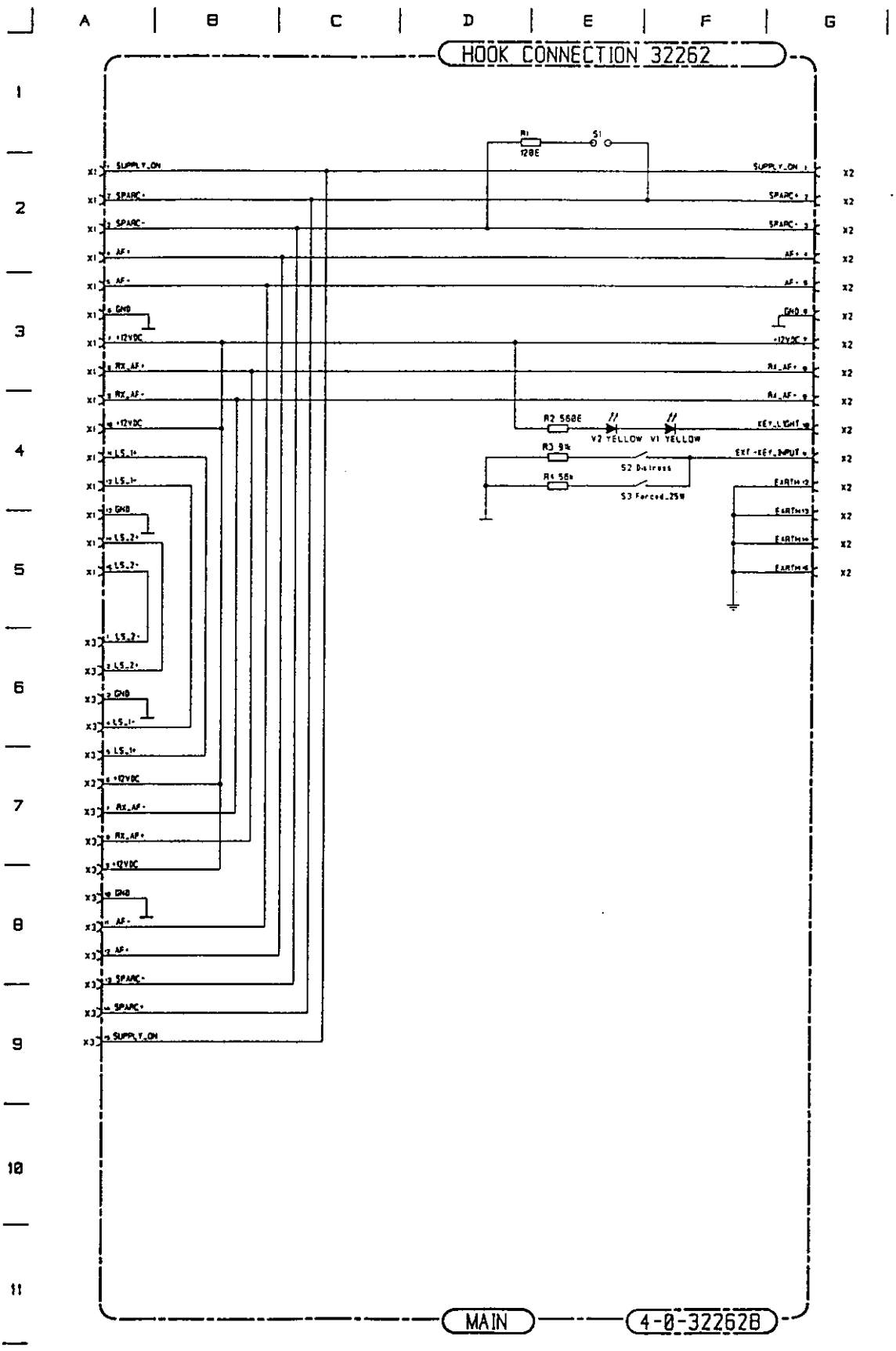
Voltage controlled oscillator

The oscillator of the transmitter is a series tuned colpitts around V28, containing two varicaps in order to accomplish frequency tuning by V21 and modulation by V25, independently. This oscillator with its buffer, V29, is capable of delivering 4 dBm over the frequency range 150.8 MHz to 163.6 MHz.

Phase locked loop, PLL buffer and loop filter

The transmitting frequency is maintained constant and stable by a serial controlled PLL, D3, with on-chip prescaler. An isolating amplifier containing V20 is used between the VCO and the PLL to ensure good spectral purity of the transmitted signal. A passive loop filter interfaces the PLL unit with the VCO.
A lock detector around V27 is included to ensure that the transmitter frequency is correct during transmissions.

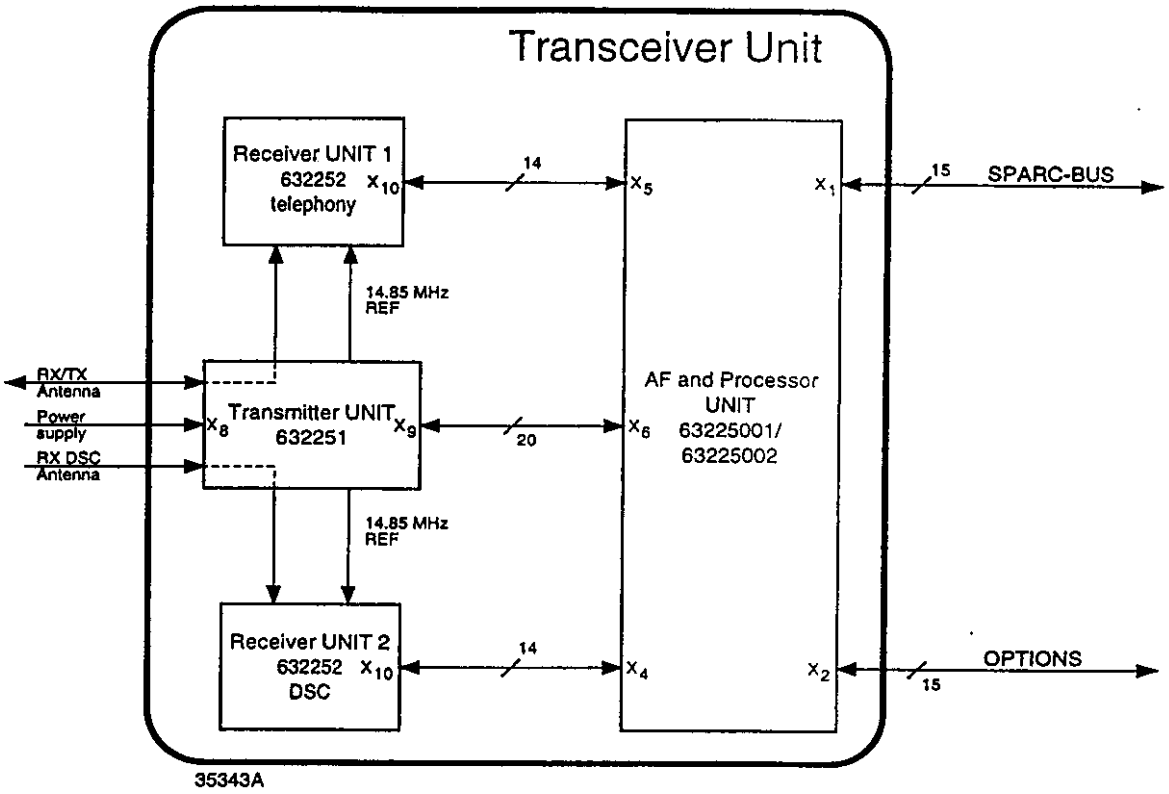
HOOK CONNECTION 632262



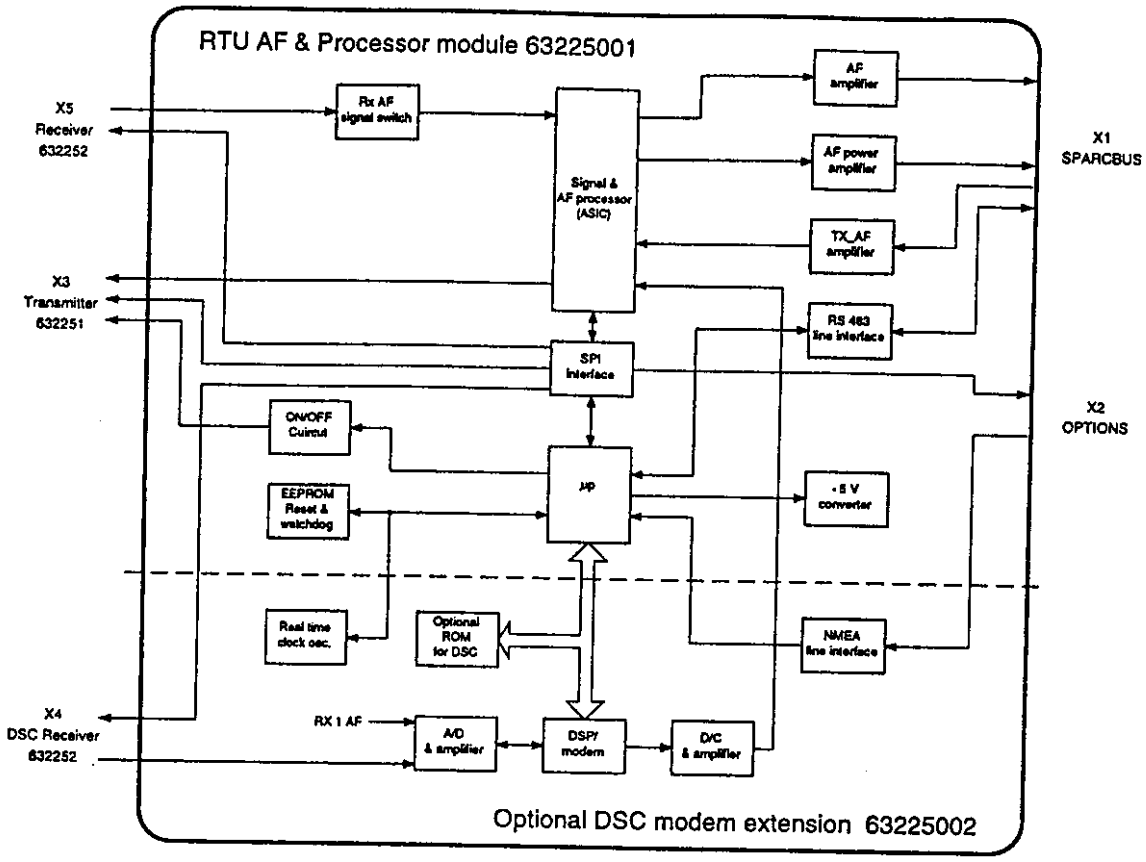
This diagram is valid for PCB rev. 32262C

4 Circuit description and schematic diagrams

Block diagram and circuit description of transceiver unit



4.1 AF and processor unit 63225001/02



35241

Input selector
N7-A -> N7-C is used as input selector. Selection is made by the microcontroller via latch D11.

Summation amplifier
The inputs are added together in ASIC OP2. To compensate for the lost signal in the input selector the gain is set to 1.1. Output from the summation is fed into ASIC "DET RX in".

ASIC N6
The received signal is de-emphasized for LS1 and LS2 amplifier. The buffered signal is passed on to LF amplifier N2.

Balanced amplifier N3
This amplifier converts the signal from single end to balanced. Alarm tone can be added to the signal.

dB attenuator
V7, R21 is used to attenuate LS1 by 30dB.

LF switch
N8-A is used to mute LS2.

LF amplifier
N2 is a double amplifier with two inputs and outputs; one for LS1 and the other for LS2.
LS1 is for an internal speaker and goes up to 4W in 4W.
LS2 is for an external speaker and goes up to 6W in 4W.

Pre-emphasis
Pre-emphasis is made by C84, R91 and limited by R83, C72, R86 and C67 together with the input amplifier in the ASIC N6.

Power driver
This part of the transmitter chain consists of two amplifier stages. The first stage of amplification is accomplished by a common emitter buffer, V15. A switching transistor, V14, shuts this stage down during reception. This stage delivers 13 dBm and the output power rise and decay times are shaped in such a way that frequency pulling of the VCO is avoided.
The final discrete stage of amplification contains a medium power VHF transistor, V7, running in class C. This amplifier puts 25 dBm out during transmission and is turned off during reception in order to save current.

PA stage
The final boost of amplification consists of an integrated power module, N1, capable of delivering 30W and withstanding a large amount of load mismatch. This stage provides a minimum gain of 20 dB, which can be reduced by varying the supply voltage to the first amplifier in the power module. This feature is used in order to obtain two output powers: 1W and 25W.

Harmonic filter
All of the harmonic signals of the carrier frequency are suppressed by a 7th order elliptic filter.

Aerial switch
The aerial is switched between the transmitter and the receiver by relay K1. As an option the transceiver can be operated as a coast station in reverse duplex by means of a second aerial relay, K2.

SWR Detector
The SWR detector consists of three elements: a directional coupler and two power detectors. The coupler samples forward and reverse going power in the transceiver.
A temperature compensated power detector consisting of an operational amplifier, N4-A, and two fast switching diodes, V32 and V33, provides the regulating circuitry with a voltage proportional to the output power.
The same circuitry used in the power detector is used in the reverse power detector around N4-B, V37 and V38. This is done to avoid transmitting at a high power level in case of aerial failure or high SWR.

Power regulator
The heart of the power regulator is the operational amplifier N4-C, which compares the detected output power with a power setting voltage. In this way the output power from the transmitter can be regulated by adjusting the voltage at pin 10 of N4-C. The transistor V26 is one of the shutdown mechanisms incorporated in the transmitter. This transistor and the surrounding RC network also contribute to the power envelope shaping done at the first stage of the power driver.
The HIGH-LOW power selection is done by shunting the output voltage from the forward power detector with V34.
Finally, the output from N4-C is buffered by the amplifier around V5 and V6, which is capable of driving the PA stage.

Temperature sensor
A forward biased transistor, V3, placed near the PA stage is used as a temperature sensor to alert the controlling circuitry and thereby prevent damage at the PA stage due to high temperatures.

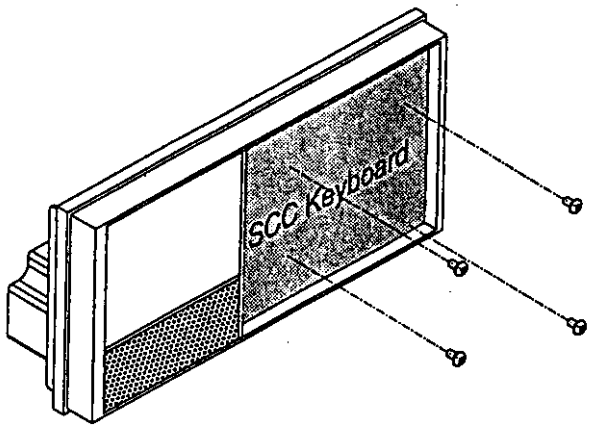
IF amplifier
The transistor V7 amplifies the 45MHz output signal from the crystal filter to the second mixer, which has a tuned drain circuit consisting of L17, C70 and C74.

Second mixer, demodulator, second IF filter and multiplexer
The 45 MHz signal is down converted to 450 kHz by the second LO of 44.55 MHz. The mixer output is fed through the ceramic filter Z3 to the limiter amplifier and demodulator in the N1. The AF signal is amplified by an internal operation amplifier. The output signal can be adjusted by R25. The RX_level, which is an output from N1 to indicate the strength of the received signal, is multiplexed with the lock detector signal, from the pLL (D4), by D2 and the output is routed to AN_LEV_2.

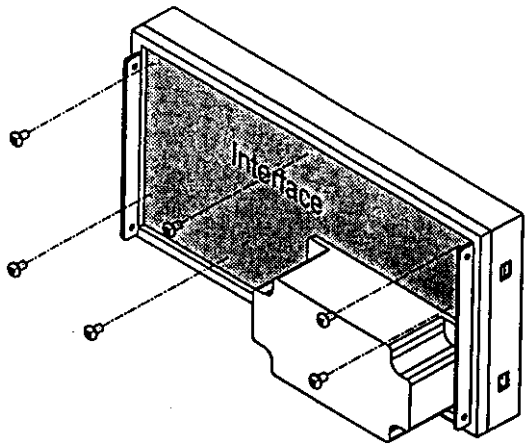
VCO and VCO buffer
The VCO, which is built around V12, is oscillating at +45 MHz above the selected channel frequency. The oscillator can shift the band by means of the trimmer capacitor C54. The output voltage of the VCO is fed to the VCO buffer, which is implemented with V13.

Loop buffer, PLL and loop filter
The output of the VCO buffer is fed to the prescaler of the PLL, which is implemented by IC MC145190, via the loop buffer. This is realized by V11. The output from the phase detector of the PLL is fed to the VCO through the loop filter providing optimum settling and filtering of the VCO.

Tripler and 44.55 MHz amplifier
The second LO is generated from the 14.85 MHz, which is amplified and clipped by a dual schottky diode V16 generating 3rd harmonic signal. This signal is selectively amplified at 44.55 MHz by V1.



4-0-36038



4-0-36039

7.1 Removal / installation of AF & Processor unit (632250)

To remove the AF & processor unit, it is necessary to remove both receiver units first (see section 2.7.3).
The removal of the AF & processor unit can be done as follows:

- Remove the spring of sot-141 (see the above figure).
- Unscrew the two 25-pole sub-D connectors.
- Disconnect the 20-pole flat cable.
- Unscrew the unit from the chassis, and remove the unit.

Install the new AF & processor unit by doing the opposite of the above steps in reverse order.

7.2 Removal / installation of Transmitter unit (632251)

To remove the transmitter unit, it is necessary to remove both receiver units first (see section 2.7.3).
The removal of the transmitter unit can be done as follows:

- Unsolder the power module and both aerial terminals.
- Unscrew and remove the thread plate and both aerial connectors.
- Disconnect the 20-pole flat cable.
- Unscrew and remove the unit from the chassis.

Install the new transmitter unit by doing the opposite of the above steps in reverse order.