Product Compliance
SAR Test Report

Product : Cellular Phone
Model : MVX 605
FCC ID : BFYM 3047
Reference no.: 10025

3D-EMC Laboratory,Inc.
for NEAR FIELD MEASUREMENTS

TABLE OF CONTENT

SAR Test Report

To: Audiovox

Date: 01/27/99

Re: 10025

Radio Information

Radio Type	:	Cellular Phone
Model Number	:	CDM4000
Serial Number	:	17400000736
Frequency Band(MHz)		800
Frequency Tested(MHz)		824
Nominal Output Power:(W)		0.600 pk / av
Antenna Type	:	Monopole
Antenna Position	:	IN
Signal Type	:	CW
Duty Cycle	:	-

Simulated Tissue

Type of Tissue	:	brain
Measured Dielectric Constant:		45.8
Measured Conductivity	:	0.88

Conditions

Robot	:	6 Axis
Scan Type	:	SAR
Measured Field	:	E
Measured Power(W):		0.526
Phantom Type	:	head
Phantom Position:		left ear
Room Temperature °C:		25
Distance Antenna-Shell:		24 mm

Probe

Probe Name	:	E
Probe Orientation:		-
Probe Offset(mm):		3.0
Sensor Factor	:	10.8
Conversion Factor:		0.63
Calibration Date	:	8/13/98

Results

Maximum Fields Location:	X : -5	Y : -40
Peak Voltage (mv):	26.64	
1cm Voltage (mv):	16.15	
SAR (averaged over 1 gram of tissue) W/kg:	1.24	

Comments @ 837 MHz, Power 0.565 W = SAR 1.16

@ 849 MHz, Power 0.467 W = SAR 0.80

Insertion loss of adapter cable = 0.81 dB (Measured by manufacturer)

Product Compliance Test Report

Re: 1025

Manufacturer : SHINTOM CO. Ltd.
Address : SHIN-YOKOHAMA, JAPAN
Product Description: Cellular Phone
Product Classification: UNCONTROL

Based on the above information and the test results shown in attached test report, of the aforementioned product, the undersigned states that ;

*Tests were performed to establish the maximum value of the **SAR** (Specific Absorption Rate) in a person holding the product as specified in the user's manual. The **D.U.T.** was found to be in compliance with the limits established in the **FCC 96-326** document.*

Name : OSCAR GARAY
Signed :
Date : 1-28-99

2 Applicable Documents

2.1 Guidelines

The Guidelines of the following documents were considered in the performance of this test :

1) NCRP report 1986,
2) ANSI C95.1 - 1982,
3) IEEE C95.1 - 1991,
4) FCC rules 96 - 326
5) OET Bulletin 65

Location of test

All tests were performed at the **3 D-EMC Laboratory, Inc.** for Near Field Measurements located on 5440 NW, 33rd Avenue, Suite 109, Fort-Lauderdale, Florida, 33309.

2.2 Measurement System Specifications

Positioner	Probe
Type : 3D Near Field Scanner Location Repeatability : 0.1mm Speed 180°/sec AC motors	Sensor : E-Field Spatial Resolution : 0.1 cm^3 Isotropic Response : ± 0.25 dB Dynamic Range : 2 μW/g to 100 mW/g
Computer	**Phantom**
Type : 166 MHz Pentium Memory : 32 Meg. RAM Operating System : Windows NT Monitor : 17" SVGA	Tissue : Simulated Tissue with electrical characteristics similar to those of the human at normal body temperature. Shell : Fiberglass human shell shaped (1.5 mm thick)

2.3 Test Description

In the SAR measurement, the positioning of the probes must be performed with sufficient accuracy to obtain repeatable measurements in the presence of rapid spatial attenuation phenomena. The accurate positioning of the E-field probe is accomplished by using a high precision robot. The robot can be taught to position the probe sensor following a specific pattern of points. In a first sweep, the sensor is positioned as close as possible to the interface, with the sensor enclosure touching the inside of the fiberglass shell . The SAR is measured on a grid of points which covers the curved surface of the phantom in an area larger than the size of the DUT. After the initial scan, a high resolution grid is used to locate the absolute maximum measured energy point. At this location, an attenuation versus depth scan will be accomplished by the measurement system to calculate the SAR value.

2.4 Phantom

The phantom used in the evaluation of the RF exposure of the user of the wireless device is a clear fiberglass enclosure 1.5 mm thick, shaped like a human head or body and filled with a mixture simulating the dielectric characteristics of the brain, muscle or other types of human tissue. The maximum width of the cranial model is 17 cm, the cephalic index is 0.7 and the crown circumference of the cranial model is 61 cm. The ear is 6 mm above the outer surface of the shell.

2.5 Simulated Tissue

1) Simulated Tissue : Suggested in a paper by George Hartsgrove and colleagues in University of Ottawa Ref.: Bioelectromagnetics 8:29-36 (1987)

Ingredient	Quantity
Water	40.4 %
Sugar	56.0 %
Salt	2.5 %
HEC	1.0 %
Bactericide	0.1 %

• Table. Example of composition of simulated tissue.

This simulated tissue is mainly composed of water, sugar and salt. At higher frequencies, in order to achieve the proper conductivity, the solution does not contains salt. Also, at these frequencies, D.I. water and alcohol is preferred.

2) Tissue Density : Approximately 1.25 g/cm^3

Preparation

We determine the volume needs and carefully measure all components. A clean container is used were the ingredients will be mixed. A stirring paddle and a hand drill is used to stir the mixture. First we heat the DI water to about 40 °C to help the ingredients to dissolve and then we pour the salt and the bactericide. We stir until all the ingredients are completely dissolved. We continue stirring slowly while adding the sugar. We avoid high RPM from the mixing device to prevent air bubbles in the mixture. Later on, we add the HEC to maintain the solution homogeneous. Mixing time is approximately 30 to 40 min.

2.6 Measurement of Electrical Characteristics of Simulated Tissue

1) Network Analyzer HP8753C or others

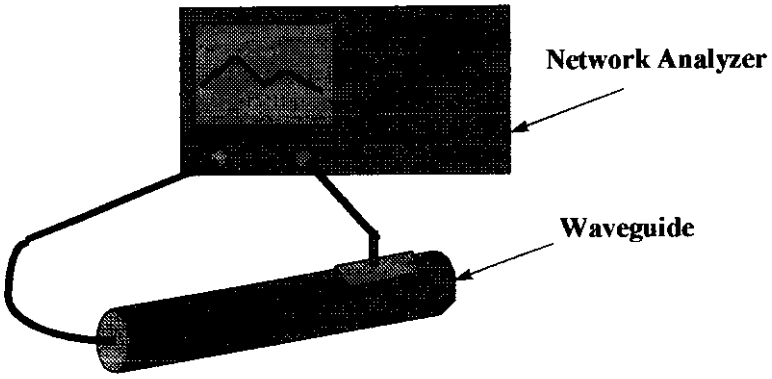
2) Slotted Coaxial Waveguide

Description of the slotted coaxial waveguide

The cylindrical waveguide is constructed with copper tube of about 30 to 40 cm of length, generally 12.5 mm diameter, with connectors at both ends. Inside of this tube, a conductive rod about 6.3 mm is coaxial supported by the two ends connectors (radiator). A slot 3 mm wide start at the beginning of the tube to almost the two third of the tube length. The outer edge of the slotted tube is marked in centimeters (10 to 12) every 1 centimeter, 0.5 if higher frequencies. A saddle piece containing the sampling probe is inserted in the slot so the tip of the probe is close but not in contact with the inner conductor (radiator).

To measure the electrical characteristics of the liquid simulated tissue, we fill the coaxial waveguide, select CW frequency and measure amplitude and phase with the Network Analyzer for every point in the slot (typically 11). An effort is made to keep the results dielectric constant and conductivity within 5 % of published data.

Electrical Characteristics Measurement Setup



$$c = 3 \cdot 10^8 \text{ m/s}$$

$$A = \frac{\Delta A}{20} \ln_{10} \frac{1}{m}$$

$$\theta = \frac{\Delta\theta \cdot 2\pi}{360}$$

$$\lambda = \frac{c}{f} \cdot \frac{100}{2.54} \text{inches}$$

$$\varepsilon_{re} = \frac{(A^2 + \theta^2) \cdot \lambda^2}{4\pi^2}$$

$$\theta' = \left| \frac{|A| \cdot \lambda}{4\pi\sqrt{\varepsilon_{re}}} \right|$$

$$S = \tan(2\theta')$$

$$\varepsilon_r = \frac{\varepsilon_{re}}{\sqrt{(1+S^2)}}$$

$$\sigma = S \cdot 2\pi \cdot f \cdot 8.854 \cdot 10^{12} \cdot \varepsilon_r \text{ (S/m)}$$

where;

ΔA is the amplitude attenuation in dB

$\Delta\theta$ is the phase change in degrees for 5 cm of wave propagation in the slotted line

f is the frequency of interest in Hz

2.7 System Description

The measurement system consists of an E-field probe, instrumentation amplifiers, RF transparent cable connecting the amplifiers to the computer, the robotics arm with its extension and proximity sensors, a phantom with simulated tissue and a radio holder to support the device under test. The E-field probe is a three channel device used to measure RF electric fields in the near vicinity of the source. The three sensors are mutually orthogonal positioned dipoles, and are constructed over a quartz substrate. Located in the center of the dipole is a Schottky diode. High impedance lines are connecting the sensor to the amplifier and then optically linked to the computer. The probe has an isotropic response and is transparent to the RF fields.

Calibration is performed by two steps :

1) Determination of free space E-field from amplified probe outputs in a test RF field. This calibration is performed in a TEM cell when the frequency is below 1 GHz and in a waveguide or some other methodologies above 1 GHz. For the free space calibration, we place the probe in the volumetric center of the cavity and at the proper orientation with the field. The probe is then rotated 360 degrees until the three channels show the maximum reading. This reading equate to $1 mW/cm^2$ if that power density is available in the correspondent cavity.

2) Correlation of the measured free space E-field, to temperature rise in a dielectric medium. E-field temperature correlation calibration is performed in a planar phantom filled with the appropriate simulated tissue.

For temperature correlation calibration, a RF transparent thermistor-based temperature probe is used in conjunction with the E-field probe. First, the location of the maximum E-field close to the phantom's inner surface is determined as a function of power into the RF source; in this case, a dipole. Then, the E-field probe is moved sideways so that the temperature probe, while affixed to the E-field probe is placed at the previous location of the E-field probe. Finally, temperature changes for 30 seconds exposure at the same RF power levels used for the E-field measurement are recorded. The following equation relates SAR to initial temperature slope :

$$SAR = C\frac{\Delta T}{\Delta t}$$ where :

Δt = exposure time (30 seconds),

C = heat capacity of tissue (brain or muscle),

ΔT = temperature increase due to RF exposure.

The heat capacity used for brain simulated tissue is 2.7 joules/^{0}C/g and 3.0 joules/^{0}C/g for muscle.

SAR is proportional to $\Delta T / \Delta t$, the initial rate of tissue heating, before thermal diffusion takes place. Now, it's possible to quantify the electric field in the simulated tissue by equating the thermally derived SAR to the E-field;

$$SAR = \frac{|E|^2 \cdot \sigma}{\rho} \qquad \text{where;}$$

σ = simulated tissue conductivity,

ρ = Tissue density (1.25 g/cm^3 for simulated tissue)

2.8 Data Extrapolation

There is a distance from the center of the sensor (diode) to the end of the protective tube called 'probe offset'. To compensate we use an extrapolation method to obtain the peak surface SAR from the SAR measured at the distance from the inner surface of the phantom. At the point where the highest voltage was recorded, the field is measured as close as possible to the phantom's surface and every 5 mm. along the ` Z ` axis for a distance of 50 mm. An average slope is obtained from the three data points nearest the surface and used to define an exponential decay of the energy density with depth using the following relations

$$Slope = \frac{\frac{E_{tot\_Z1}}{E_{tot\_Z2}} + \frac{E_{tot\_Z2}}{E_{tot\_Z3}}}{2}$$

$$\exp = \ln(slope) \cdot \frac{offset}{spacing}$$

$$E_{tot\_Z0} = E_{tot\_Z1} \cdot e^{\exp}$$

2.9 Interpolation and Gram Averaging

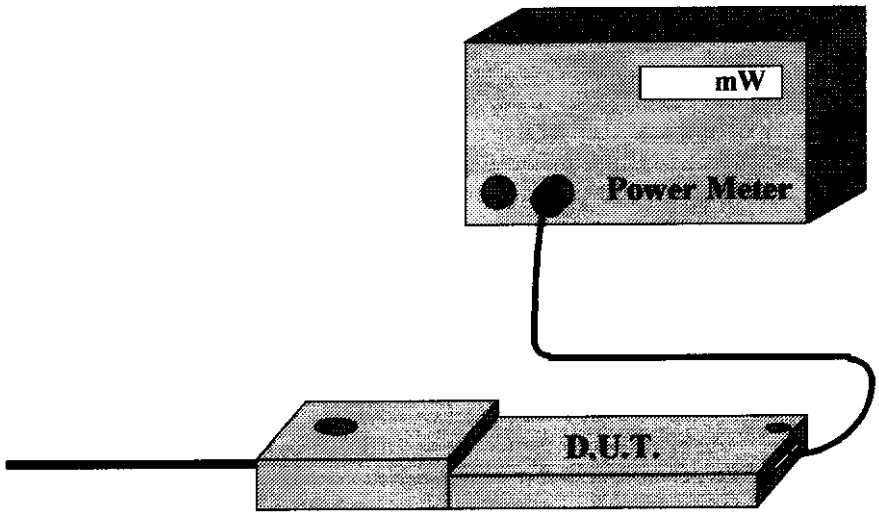
The voltage, 1 cm above the phantoms surface (E_{tot} 1 cm), is needed to calculate the exposure of one gram of tissue. The SAR value that estimates the average over 1 gram cubes is obtained from the extrapolated value. $E_{tot}Z_0$ and interpolated value, E_{tot} 1 cm, is obtained by interpolation;

$$SAR(mW \cdot g) = \frac{E_{tot\_Z0} + E_{tot\_1cm}}{2} \cdot \frac{CF}{SensorFactor}$$

2.10 Power Measurement

When ever possible, a conducted power measurement is performed. To accomplish this, we utilize a fully charged battery, a calibrated power meter and a cable adapter provided by the manufacturer. The data of the cable and related circuits losses are also provided by the manufacturer. The power measurement is then performed across the operational band and the channel with the highest output power is recorded.

Power measurement is performed before and after the SAR to verify if the battery was delivering full power for the time of test. A difference in output power would determinate a need for battery replacement and repetition the SAR test.



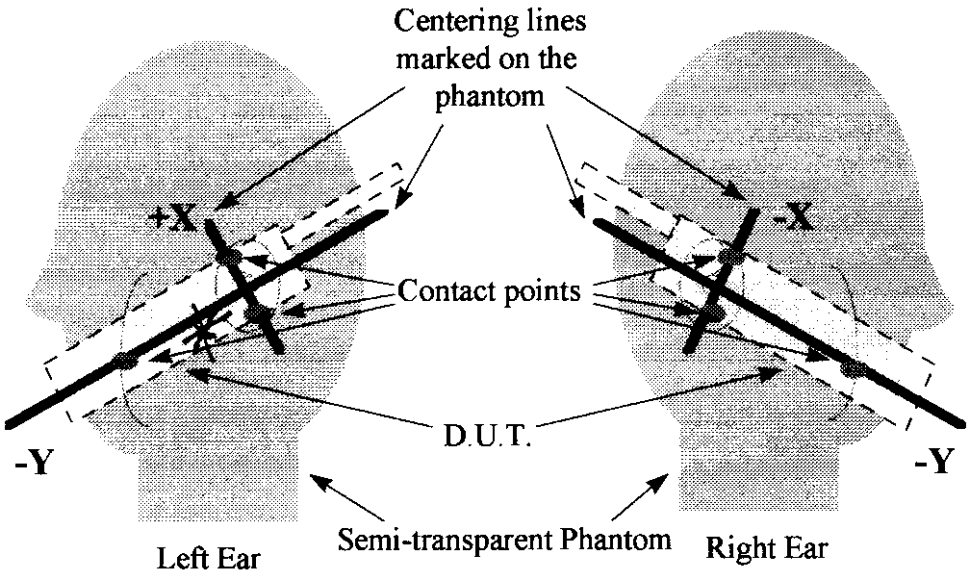
Measured Power ≈ Measured Power + Cable and Switching Mechanism Loss

2.11 Positioning of D.U.T.

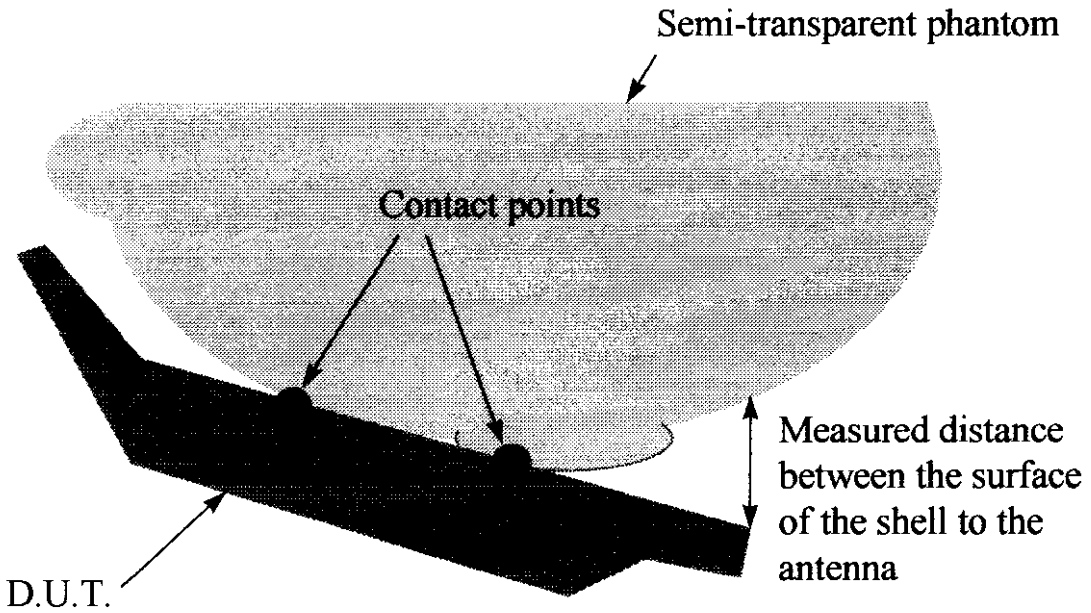
The clear fiberglass phantom shell have been previously marked with a highly visible line, so can easily be seen through the liquid simulated tissue. In the case of testing a cellular phone, this line is connecting the ear channel with the corner of the lips. The D.U.T. is then placed by centering the speaker with the ear channel and the center of the radio width with the corner of the mouth. At the same time the surface of the D.U.T. is always in contact with the phantoms shell. Three points contact; two in the ear region and one on the chin in addition to the previously describe alignment will assure repeatability of the test.

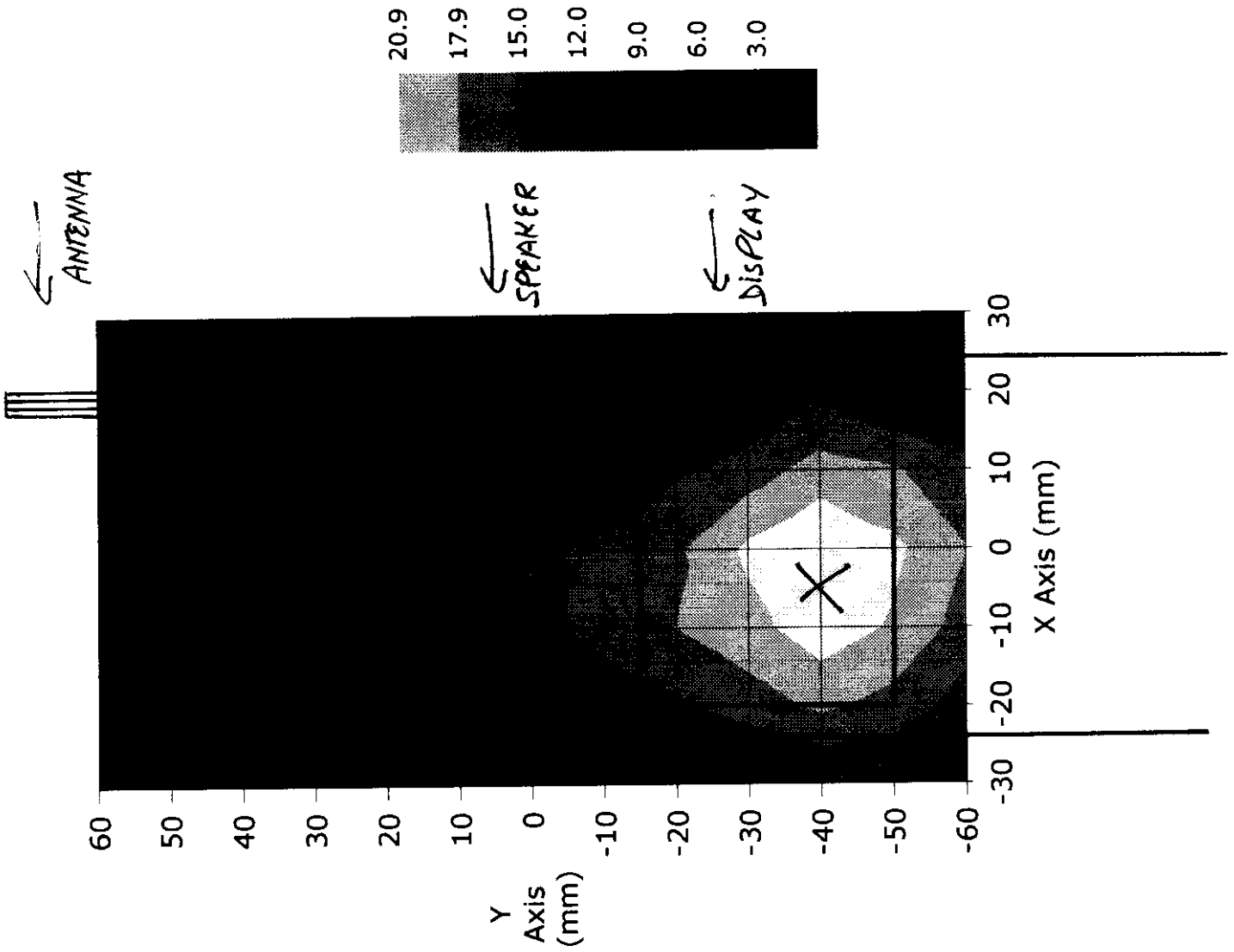
For HAND HELD devices (push-to-talk), or any other type of wireless transmitters, the D.U.T. will be positioned as suggested by manufacturer operational manuals.

Positioning of the D.U.T.



Side View




20.9
17.9
15.0
12.0
9.0
6.0
3.0
ANTENNA
SPEAKER
DISPLAY
60
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
Y Axis (mm)
30
20
10
0
-10
-20
-30
X Axis (mm)

3D-EMC Laboratory, Inc.
5440 NW 33rd Ave- Suite 109 Fort Lauderdale, FL. 33309

Applicant : Shintom Co., Ltd.
Transmitter Type: BFYM3047

Date: 1/28/99, 10:58

Frequency: 835 MHz

Comments: SHINTOM MVX605

Mixture: Brain ('Brain' or 'Muscle')

# of Points: 11

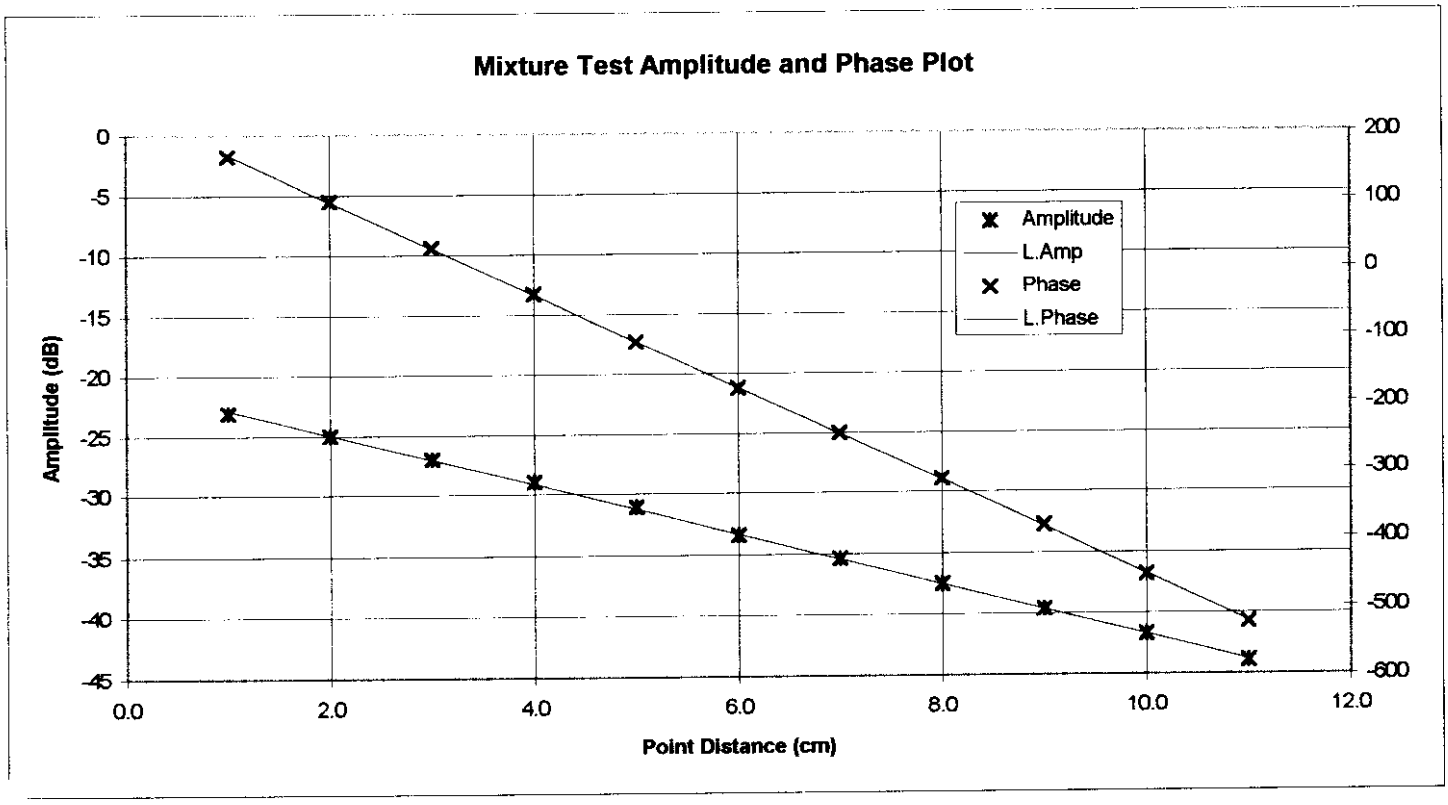
Point Dist: 1 cm.

Point	Amplitude	Phase
1	-23.10	167.90
2	-25.00	101.60
3	-27.00	32.30
4	-29.00	-37.10
5	-31.10	-107.10
6	-33.40	-177.20
7	-35.40	114.90
8	-37.50	45.80
9	-39.60	-21.80
10	-41.70	-94.10
11	-43.90	-163.80

Least Sqrs:	
ma=	-2.09
ba=	-20.79636364
mp=	-69.23454545
bp=	239.1709091

Omega:	5246459731	rad/sec
Epsilon 0:	8.85E-14	F/m
mu:	1.26E-08	H/m
alpha avg:	-0.240620142	Np/cm
beta avg:	-1.208370774	rad/cm

Results:		Target	Low Limit	High Limit	% Off Target
D. Const:	**45.8**	44.0	41.8	46.2	3.98
Cond:	**0.88**	0.90	0.855	0.945	-2.01



Test Information

Date : 1/27/99
Time : 11:17:27 AM

Ref. : /0025

Product	: Cellular Phone	**Test**	: SAR
Manufacturer	: SHINTOM	**Frequency (MHz)**	: 824
Model Number	: MVX605	**Nominal Output Power (W)**	: 0.600
Serial Number	: 17400000736	**Antenna Type**	: Monopole
FCC ID Number	: BFYM3047	**Signal**	: CW
Phantom	: Head - Left Ear	**Dielectric Constant**	: 45
Simulated Tissue	: Brain	**Conductivity**	: 0.88
Probe	: E	**Antenna Position**	: IN
Probe Offset (mm)	: 3.0	**Measured Power (W) (conducted)**	: 0.526
Sensor Factor (mV)	: 10.8		
Conversion Factor	: 0.63		
Calibrated Date	: 8/13/98		

Amplifier Setting :
Channel 1 : 0.0038 Channel 2 : 0.0041 Channel 3 : 0.0030

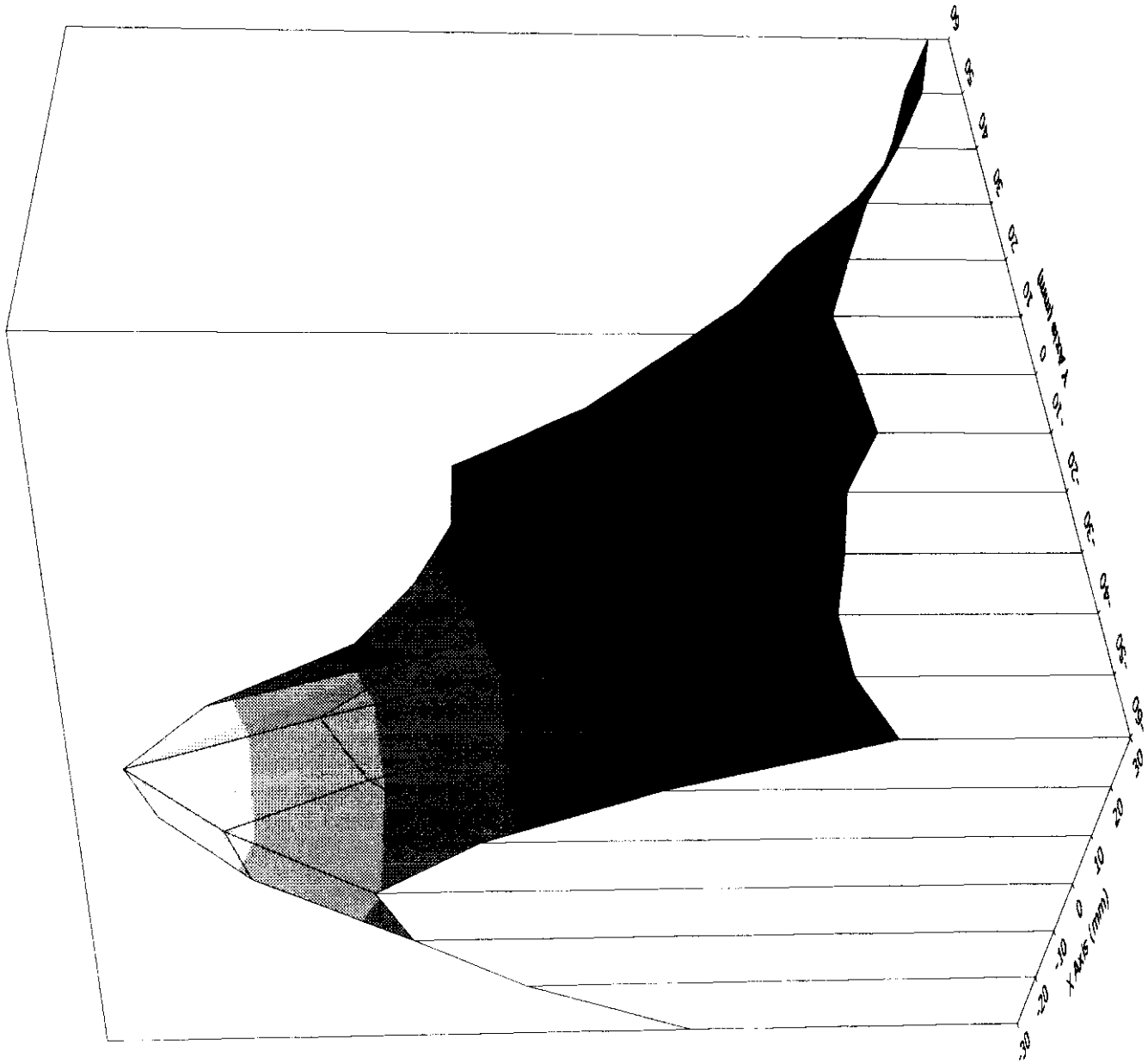
Location of Maximum Field :

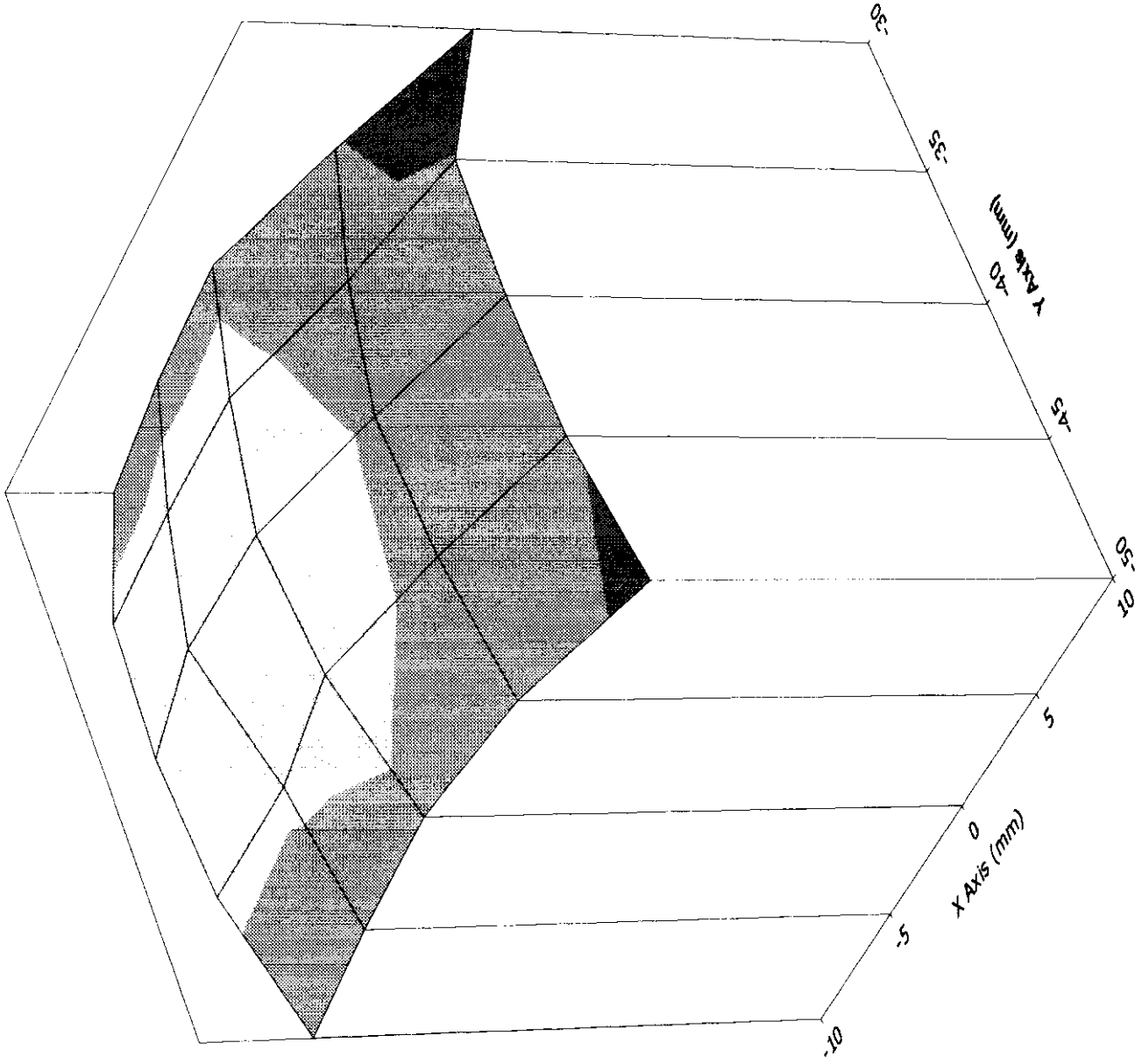
X = -5 Y = -40

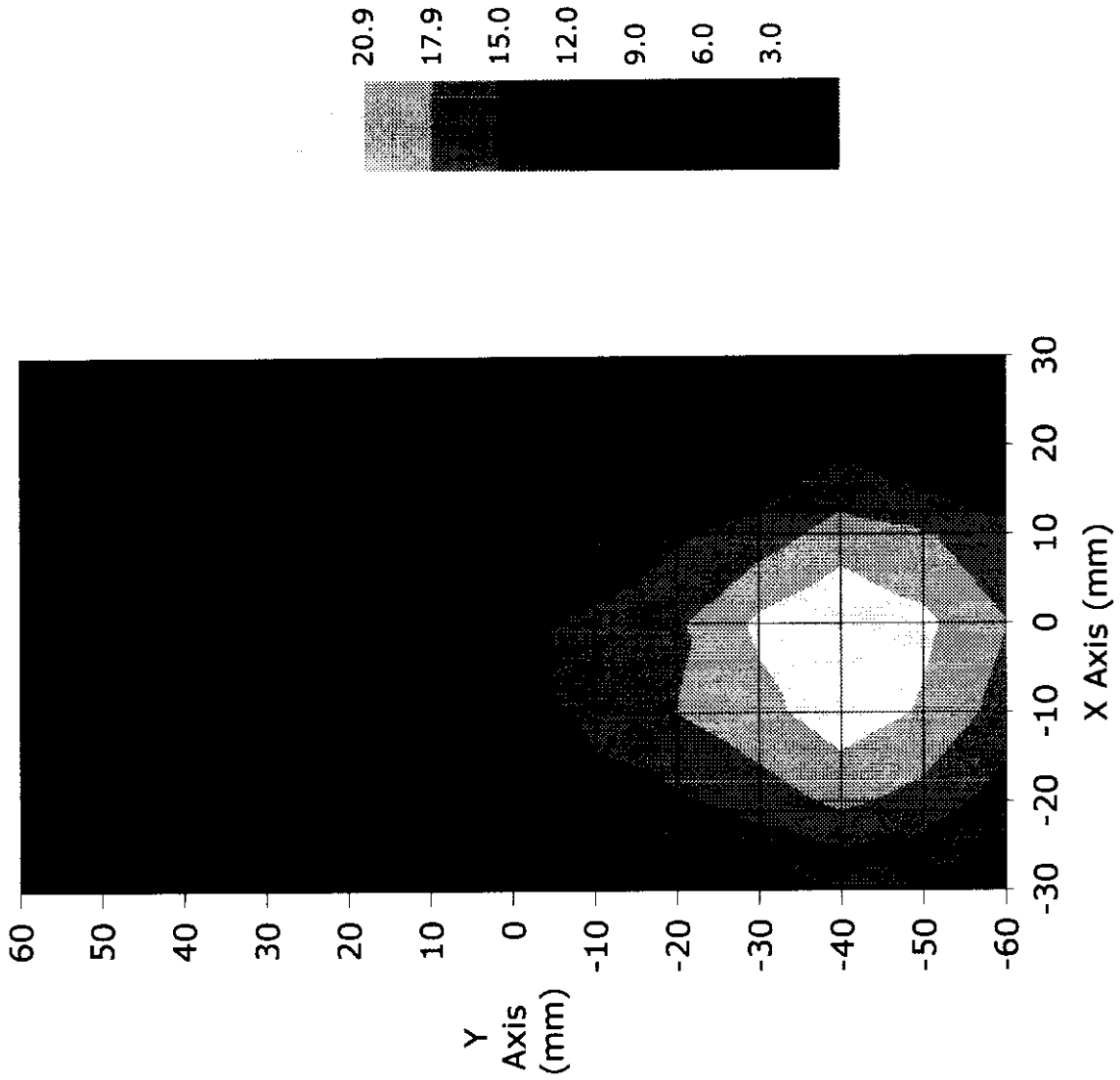
Measured Values (mV) :

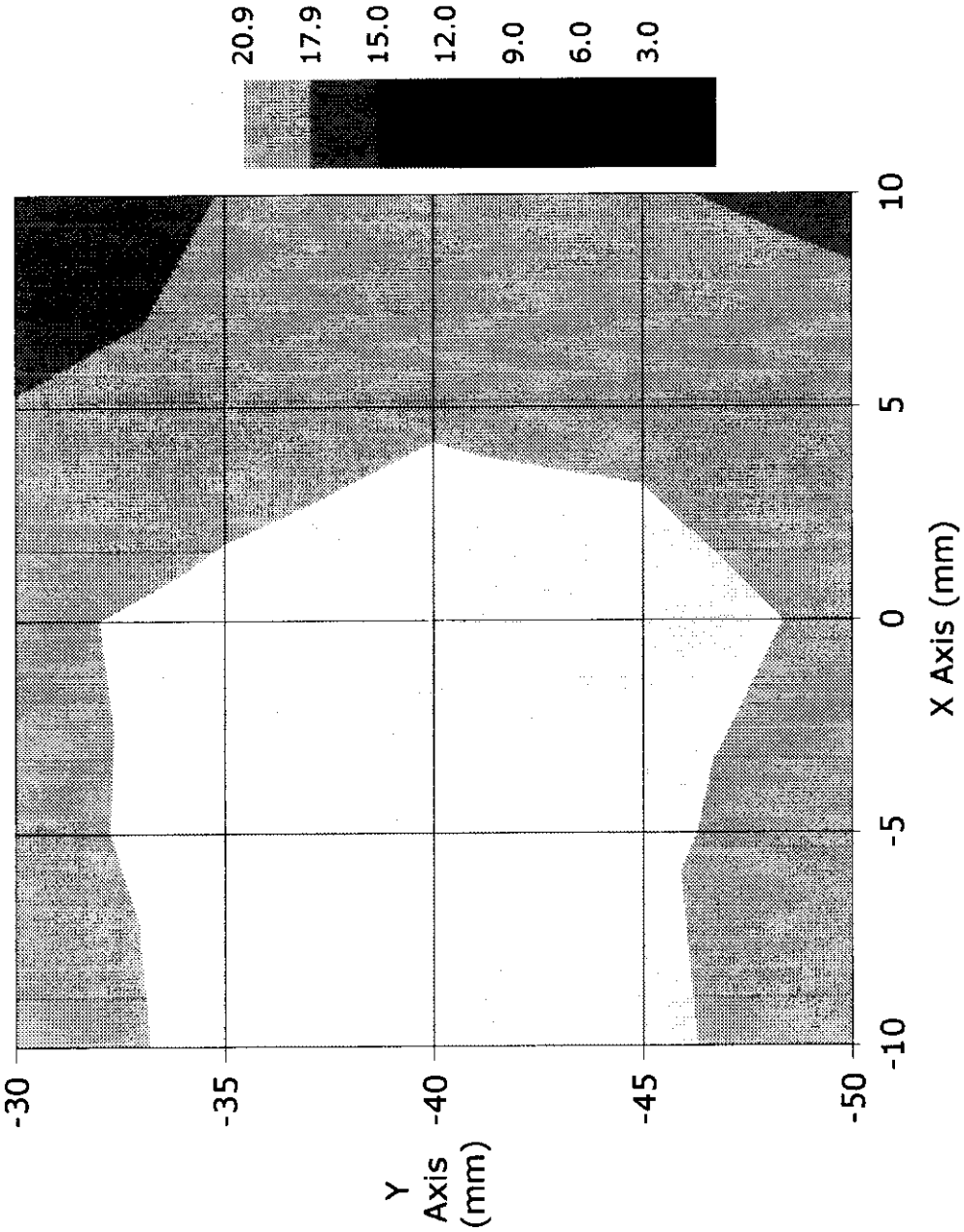
22.87	17.63	13.75	10.54	8.04	6.23
4.94	3.98	3.05	2.23	1.63	

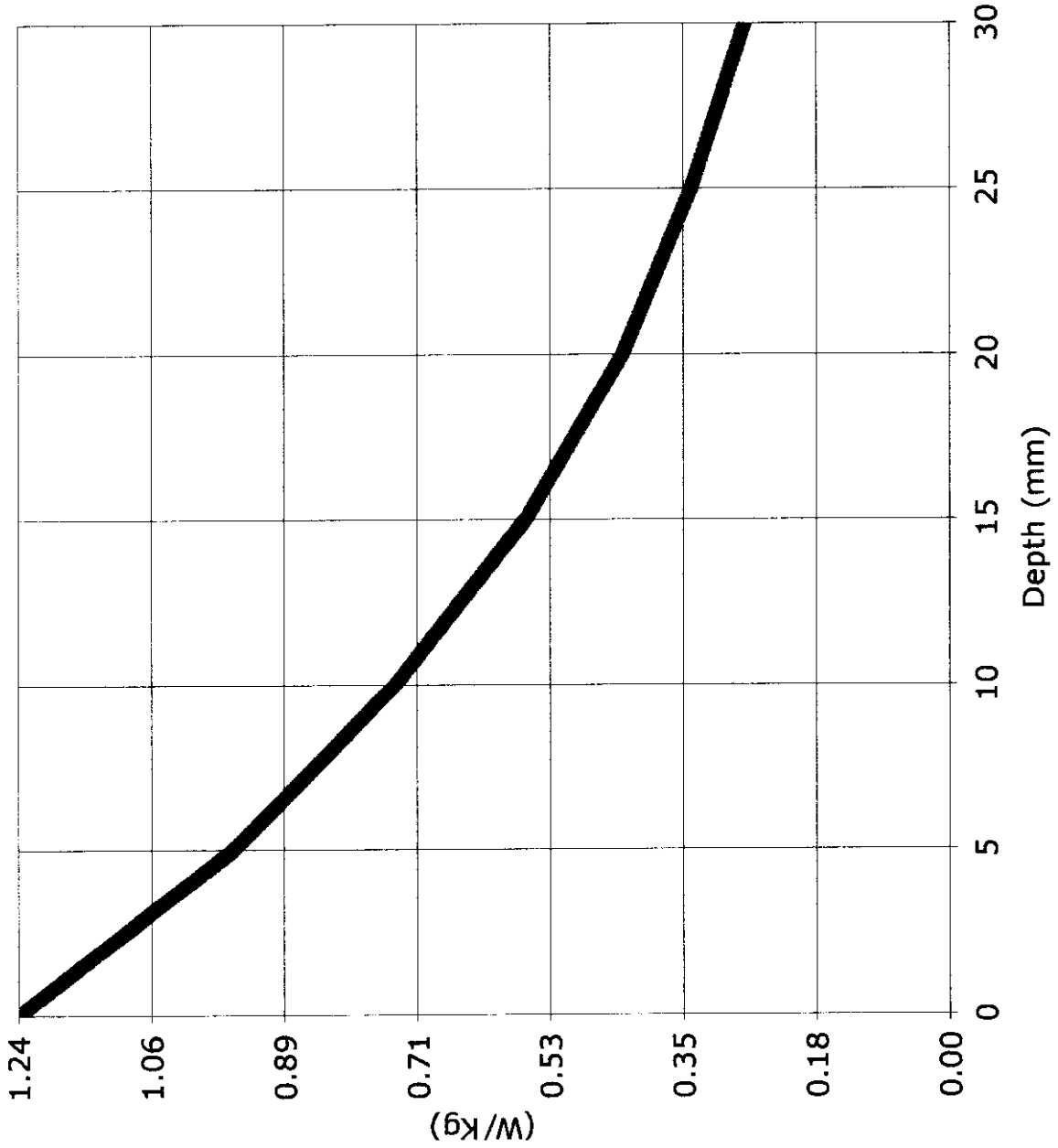
Peak Voltage (mV) : 26.64 **1 Cm Voltage (mV)** : 16.15 **SAR (W/Kg)** : 1.24


-30
-20
-10
0
10
20
30
X-Axis (mm)


-30
-35
-40
-45
-50
Y Axis (mm)
10
5
0
-5
-10
X Axis (mm)


20.9
17.9
15.0
12.0
9.0
6.0
3.0
60
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
Y Axis (mm)
30
20
10
0
-10
-20
-30
X Axis (mm)


20.9
17.9
15.0
12.0
9.0
6.0
3.0
10
5
0
-5
-10
X Axis (mm)
-30
-35
-40
-45
-50
Y Axis (mm)


1.24
1.06
0.89
0.71
0.53
0.35
0.18
0.00
(W/Kg)
0
5
10
15
20
25
30
Depth (mm)

Test Information

Date : 1/27/99
Time : 11:48:39 AM

Ref. : 10025

Product	: Cellular Phone	**Test**	: SAR
Manufacturer	: SHINTOM	**Frequency (MHz)**	: 824
Model Number	: MVX605	**Nominal Output Power (W)**	: 0.600
Serial Number	: 17400000736	**Antenna Type**	: Monopole
FCC ID Number	: BFYM3047	**Signal**	: CW
Phantom	: Head - Left Ear	**Dielectric Constant**	: 45
Simulated Tissue	: Brain	**Conductivity**	: 0.88
Probe	: E	**Antenna Position**	: OUT
Probe Offset (mm)	: 3.0	**Measured Power (W) (conducted)**	: 0.526
Sensor Factor (mV)	: 10.8		
Conversion Factor	: 0.63		
Calibrated Date	: 8/13/98		

Amplifier Setting :
Channel 1 : 0.0038 Channel 2 : 0.0041 Channel 3 : 0.0030

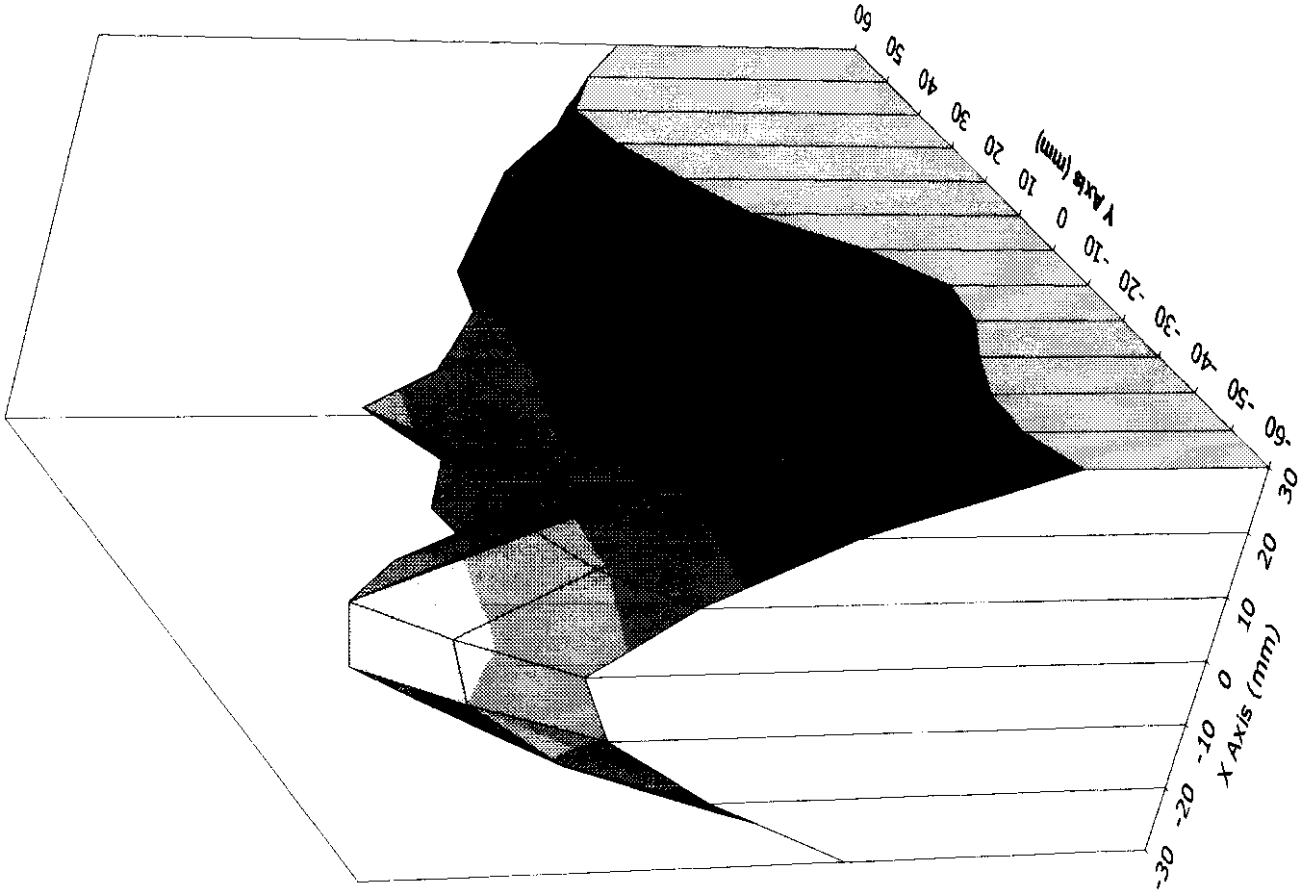
Location of Maximum Field :

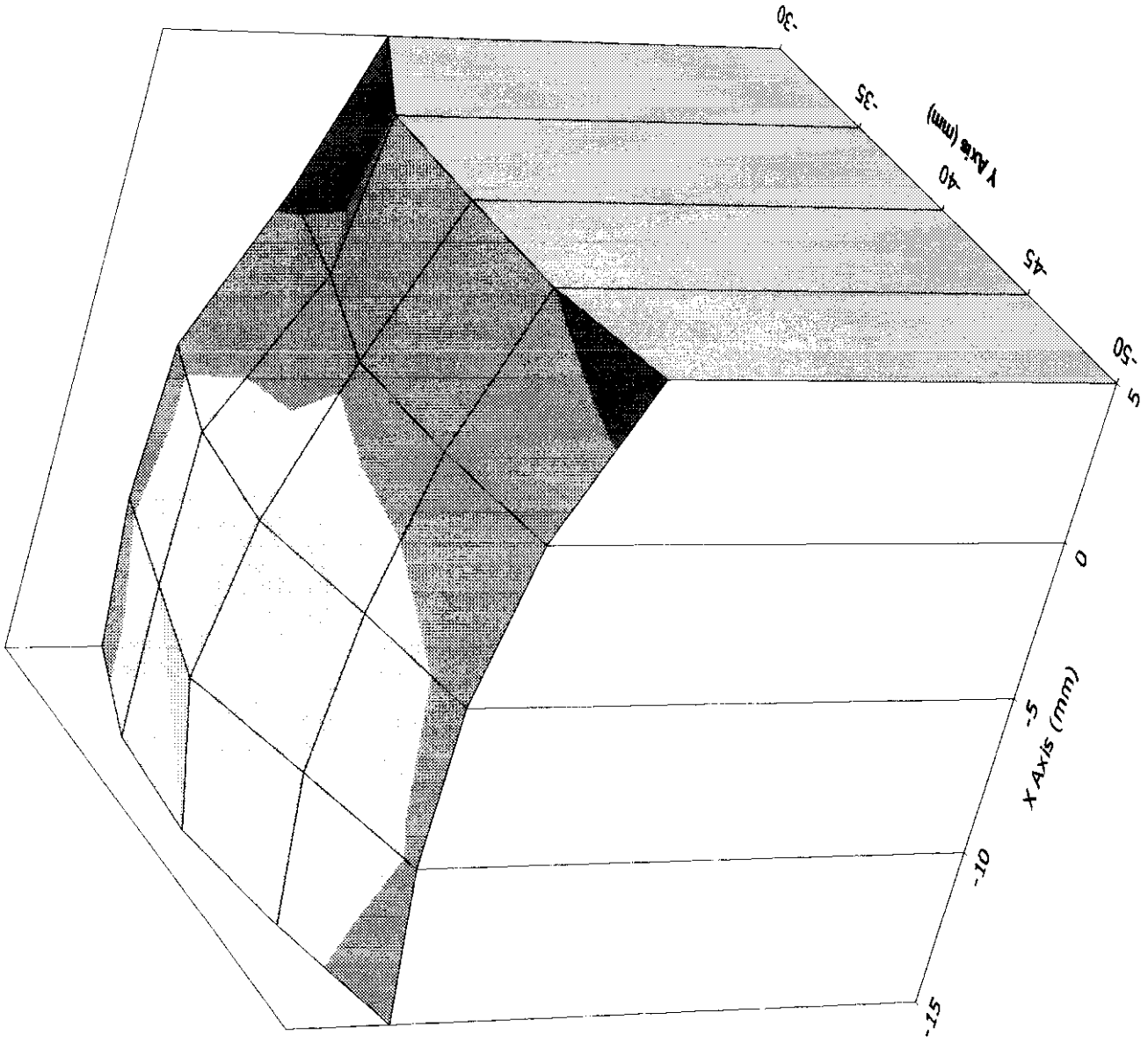
X = -10 Y = -40

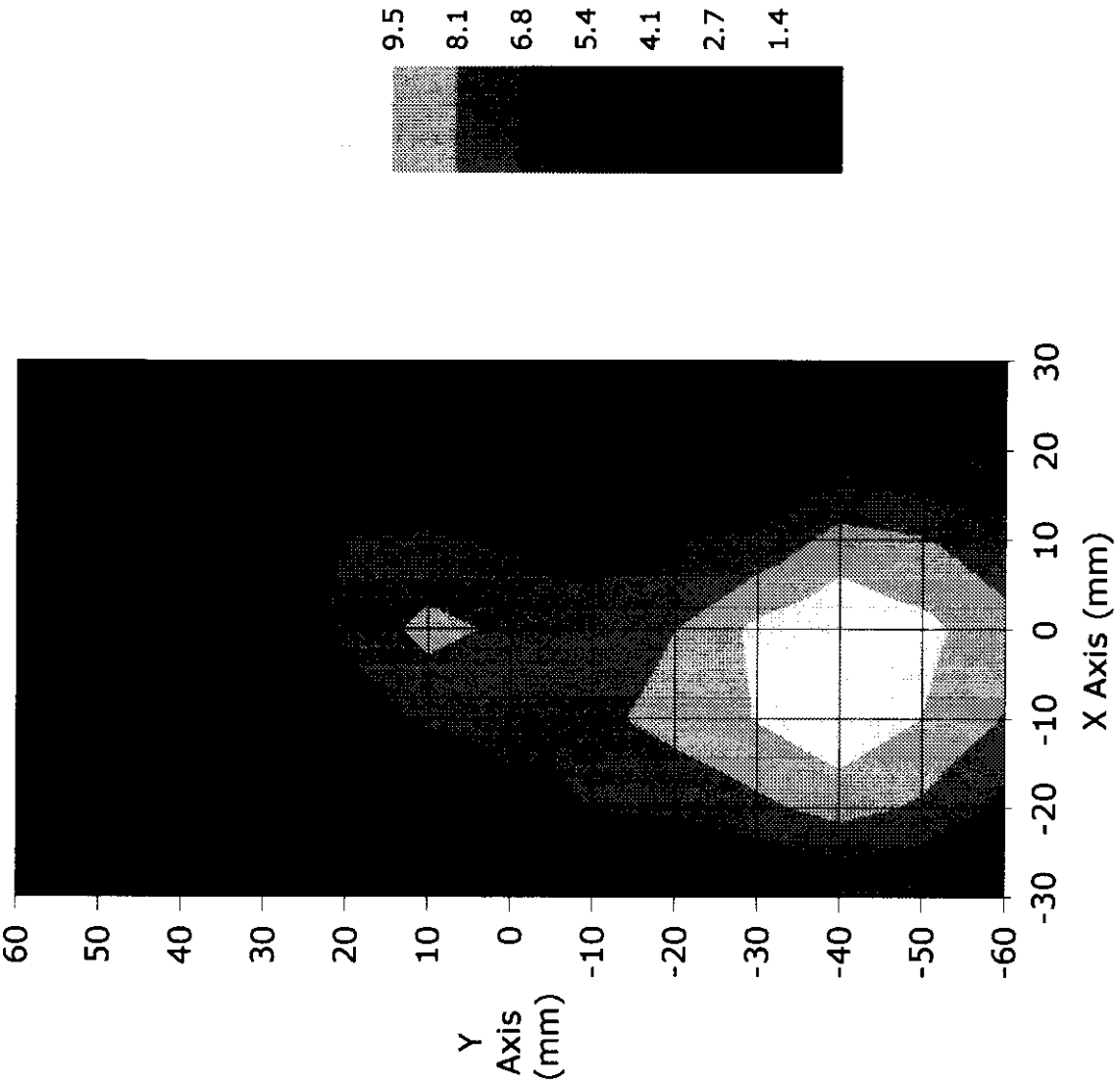
Measured Values (mV) :

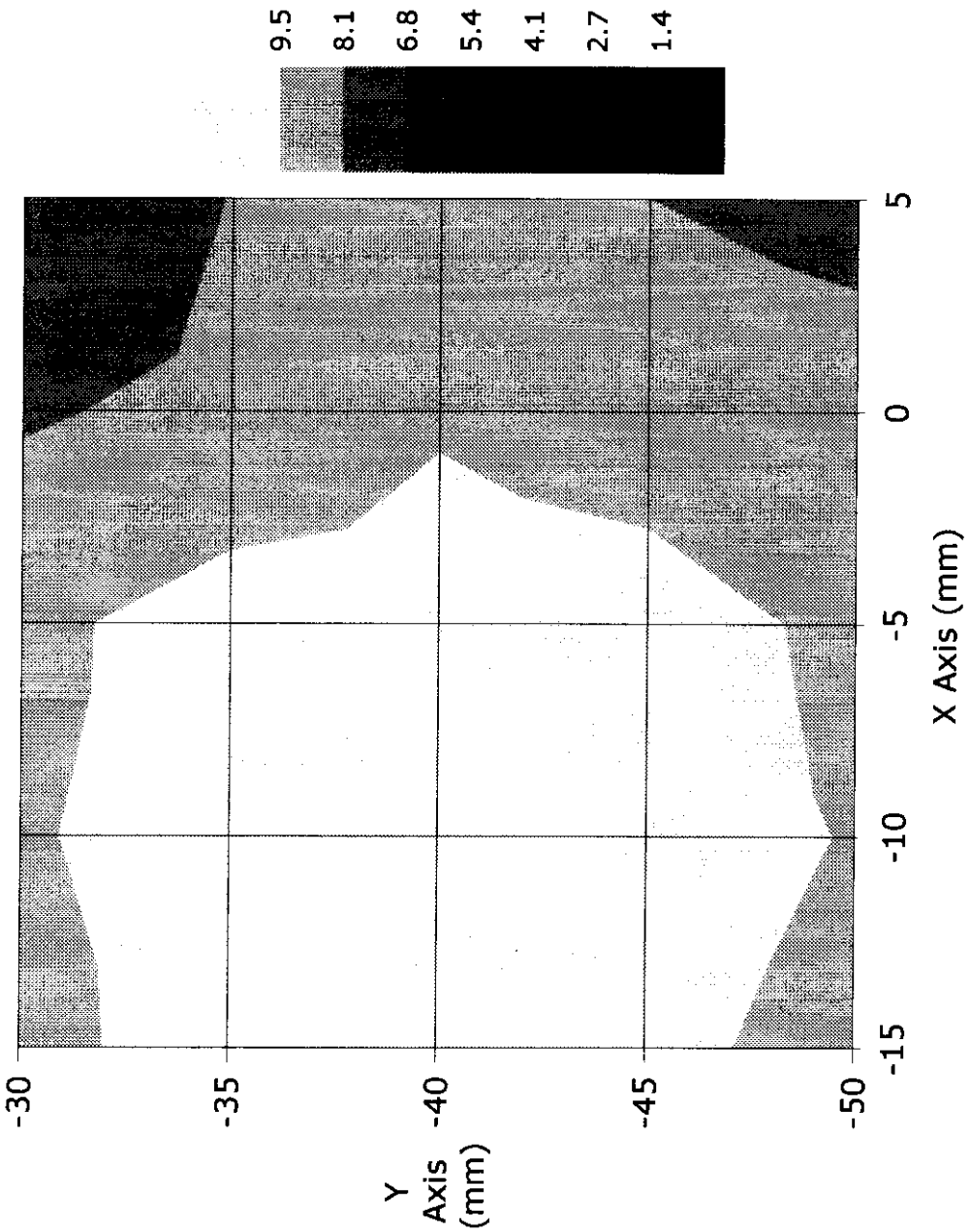
10.67	7.95	6.11	4.71	3.65	2.84
2.24	1.76	1.35	1.02	0.81	

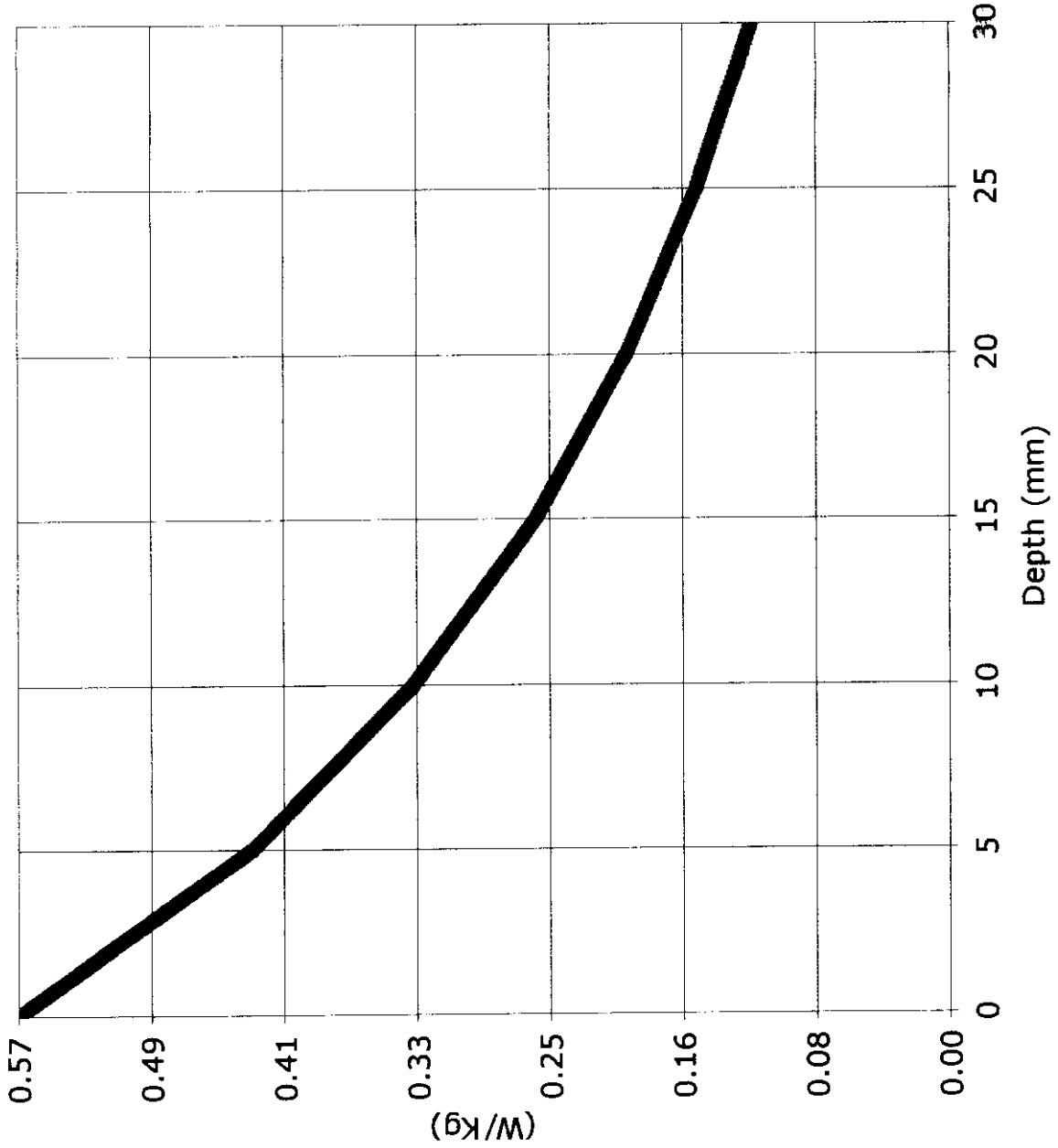
Peak Voltage (mV) : 12.61 **1 Cm Voltage (mV)** : 7.13 **SAR (W/Kg)** : 0.57


Y Axis (mm)
60
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
X Axis (mm)
30
20
10
0
-10
-20
-30


30
35
40
45
50
Y Axis (mm)
5
0
-5
-10
-15
X Axis (mm)


9.5
8.1
6.8
5.4
4.1
2.7
1.4
60
50
40
30
20
10
0
-10
-20
-30
-40
-50
-60
Y Axis (mm)
30
20
10
0
-10
-20
-30
X Axis (mm)


9.5
8.1
6.8
5.4
4.1
2.7
1.4
5
0
-5
-10
-15
X Axis (mm)
-30
-35
-40
-45
-50
Y Axis (mm)


0.57
0.49
0.41
0.33
0.25
0.16
0.08
0.00
(W/Kg)
0
5
10
15
20
25
30
Depth (mm)

From: Kwok Chan
To: ECHANG
Subject: EAS 93204

Errol:

This is the Shintom phone, EAS 93204, FCC ID BFYM3047 -

1. They are requesting 600 mW maximum output on the 731 form. After looking through the data, the 600 mW appears to be based on conducted measurements. Part 22, subpart H, requires ERP ratings to be listed on the grant. Something needs to be revised to get the ratings to match.

2. Descriptions in the application indicate 600 mW with +2/-4 dB tolerance. The rating provided on the FCC grant does not provide any tolerance, it is the maximum output (ERP for Part 22) the device will be authorized to transmit. We may consider listing 600 mW ERP nominal for Part 22, Class III handsets and in addition a maximum rating within the 2 dB tolerance recommended by industry standards provided there is SAR to support that. This does not mean there is any change in either FCC rules or industry standards. The 600 mW ERP nominal rating remains the same for normal ambient operation conditions. Tolerances provided by industry standards may be accepted provided there is SAR data to support that, otherwise, 600 mW ERP is the top limit on grant including tolerances and everything.

3. The field strength data for the spurious and ERP measurements, at the fundamental frequencies of the transmission band, seem to have large discrepancies. For example, at 848.97 MHz, carrier emission has 130.8 dBuV/m which converts to an ERP of 2.2 W; where as the ERP measurement by substitution method showing similar meter readings but only 676.1 mW ERP. Other frequencies need to be check as well. These need to be clarified in order to evaluate SAR compliance with respect to the maximum output rating listed on the grant.

4. SAR was tested at conducted output levels that are lower than those shown in other parts of the application. We either need new SAR data to support the higher outputs with respect to 600 mW ERP nominal output and maximum output within a tolerance limit, or grant this phone at lower output levels, supported by the SAR data, after the above items on output discrepancies have been clarified.

5. Please clarify if the SAR numbers shown at the bottom of page 3 in the SAR report are for antenna IN or OUT test conditions. We also need similar numbers for the other condition, i.e., If IN we also need OUT or if OUT, we need IN for those two frequencies.

6. The users manual indicates that there is a 3 W booster amplifier for this phone, for vehicle use. Please be aware that this booster is not a part of this application, it needs to comply with MPE limits for use with this phone. See 2.1091 of FCC rules. MPE evaluation is categorically excluded for less than 1.5 W ERP only. At 3 W, it needs to demonstrate MPE compliance for vehicle use.

7. (FYI only) There are 2 battery options. If the final SAR does not have at least 10-15 % margin, variations in radiated performance of the device due to battery options may need to be addressed. We will request for such clarifications, if necessary, when final SAR numbers and output levels are determined.

8. (FYI only) We have recently informed the SAR lab (through another occasion) to provide SAR plots etc. in units of W/kg. We are not requesting similar changes in this application but we will be expecting those changes in subsequent filings.

Kwok Chan

From: Kwok Chan
To: ECHANG
Date: 4/16/99 5:17pm
Subject: EAS 93204 - FCC ID: BFYM3047 (SHINTOM MVX605) -Reply

Errol:

The revised SAR information is O.K. The applicant will reduce the output to a maximum of 525 mW conducted at mid-band, lower at high and low channels as indicated in the response. This will result in a maximum ERP of 600 mW.

The grant rating should be 600 mW ERP. Please also indicate on the external comments of the grant that device rating is in ERP.

If this is a paper filing, the revised information should be included in the filing and to be scanned into the EAS system. If this is an electronic filing, Mr. Saito should upload the information into the EAS system to keep all the information together.

Kwok Chan

>>> Kenichi Saito <knsaito@ibm.net> 04/13/99 05:28am >>>
Dear Mr.Kwok Chan,

The followings are our answer to your comments
regarding our equipment,EAS 93204,FCC ID:BFYM3047.

Items 1 and 2:
Our application document shows that this quipment
has following conducted power output and ERP.

Frequency (MHz)	Conducted power output (mW)	ERP (mW)
824.04	551	631.0
836.49	600 (=27.8dBm)	676.1
848.97	478	676.1

To keep ERP of the equipment less than 600mW, at
the factory of Shintom Co.,Ltd.,we will align the
conducted power of this equipment for the Power
Level 0 (maximum level) to be 27.2dBm which is
0.6dB lower than the original level described in
the application document.
After this modification, the conducted power output
and ERP would be expected as follows.

Frequency (MHz)	Conducted power output (mW)	ERP (mW)
824.04	481.9	551.9
836.49	524.8 (=27.2dBm)	591.4
848.97	418.1	591.4

Item 3:
Please see a KEC's comment in the separate fax sent to you on April 12th.

Items 4 and 5:
Please see additional SAR data from 3D-EMC Laboratory,Inc. in the separate fax sent to you on April 12th.

Item 6:
We decided not to offer the 3W booter for this equipment. To make sure of this fact for all users, we will insert a paper with a description,"The 3W booster is not available at this time", into the users manual.

If you have any question on this matter, please let me know.

Best regards,

Kenichi Saito
Director
Shintom Co., Ltd.
Phone: 516-233-3393 (Audiovox)
Fax: 516-233-3438 (Audiovox)
E-mail: knsaito@ibm.net

CC: FCCMAIL.SMTPNLM."knsaito@ibm.net", kchan

AK2336

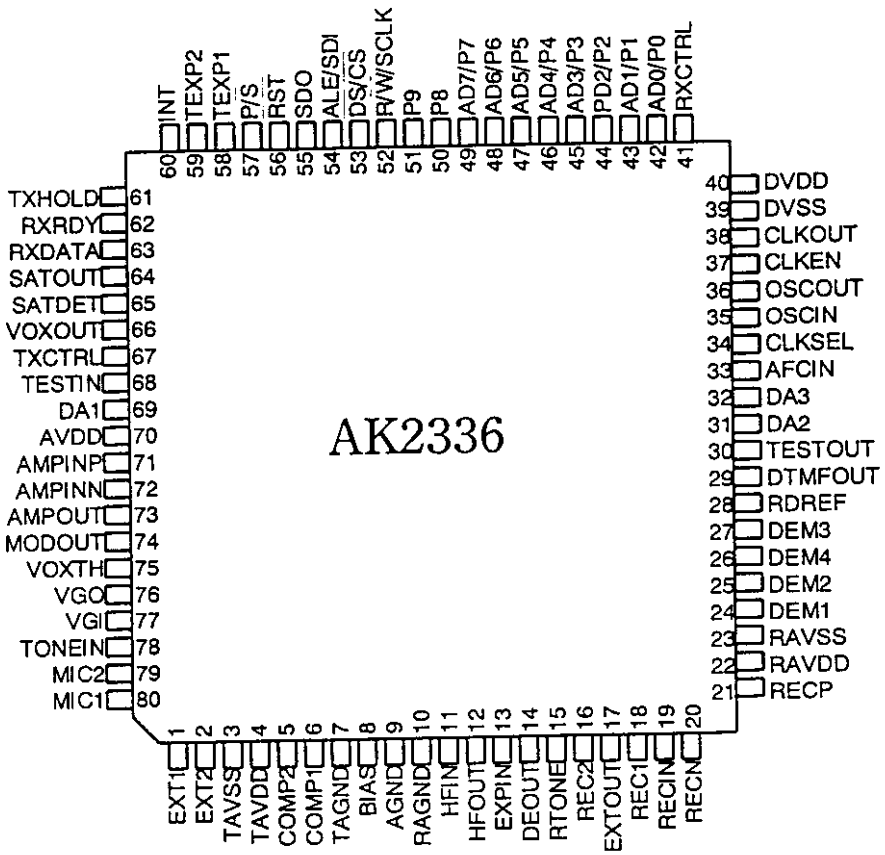
CMOS Base Band Processor for AMPS / TACS / NAMPS / NTACS

The AK2336 is a low power CMOS device incorporating all base band functions for AMPS, TACS, NAMPS and NTACS. All the functions needed for base band signal processing in a cellular telephone, not only audio related functions but also data related functions, are integrated into a single chip. The AK2336 can handle all base band functions only in conjunction with a micro-controller. The AK2336 even handles FOCC data by itself during idle mode. The AK2336 also generates interrupt if first 3 consecutive FOCC data are the same and the RF block may be shutdown duaring the remaining period. Therefore, theAK2336 is suitable for hand-held portable cellular phones, in which power consumption is a key concern.

Features

- ☐ Single chip base band LSI for AMPS, NAMPS, TACS and NTACS.
- ☐ Linearity Adjustable CMOS COMPANDOR.
- ☐ Voice signal processing circuits.
- ☐ Error handling, up to 2 bit error correction.
- ☐ Busy/Idle bit extraction.
- ☐ Majority voting.
- ☐ Discontinuous Reception Support.
- ☐ Wide band data processing.
- ☐ SAT decoding and transponding circuits.
- ☐ DSAT/DST generating and transponding circuits.
- ☐ DTMF and ST generator.
- ☐ Digital gain control at various points.
- ☐ Serial/Parallel bus control.
- ☐ 10 bit programmable I/O ports.
- ☐ Ceramic receiver driver.
- ☐ VOX circuit.
- ☐ Uncommitted 8 bit linear DAC × 3.
- ☐ Uncommitted OP-AMP × 1.
- ☐ Uncommitted Timer × 2.
- ☐ Six modes of operation for meticulous power management.
- ☐ 4.8 MHz oscillator circuit / 14.4/4.8 MHz clock input.
- ☐ AFC Counter.
- ☐ Low power CMOS, 1.4mA(TYP;VDD=3V) at Rx Data Mode.
- ☐ Sidetone path circuits.
- ☐ Single 2.7V to 5.5V power supply.
- ☐ 80 pin LQFP package.

■ Pin Configuration



Block Diagram Description

Block	Functions
Transmitter Section	
AMP1	An OP-AMP to adjust the transmit voice(MIC) signal level. Set the proper gain (≦ 30dB) with external resistors.
AMP2	An OP-AMP to adjust the external input signal level. Set the proper gain (≦ 30dB) with external resistors.
SUM1	Summing junction of MIC input signal and EXT input signal.
SW1, 2	SUM1 input signal select switches.
TONE LEVEL	Trnsmit DTMF signal level adjust for TACS/NTACS.
SW3	Transmit voice signal select switch.
AAF1	Anti-aliasing filter.
STGAIN	Gain control(-29dB) circuit to adjust the sidetone level.
SW16	Sidetone signal mute switch.
TXBPF	Band-pass filter (300～3300 Hz) for transmit voice signal.
VOX	Transmit voice signal detection circuit. May be disabled from control register.
COMP	Compressor circuit. Compress the amplitude of transmit voice signal with square root characteristic. Linearity can be adjusted from the control register
SW4	Compressor bypass switch.
VR1x (x = 1, 2)	Digital gain control circuit to set the deviation level. Adjustable from +2.1dB to -2.4dB by 0.3dB step from the control register. VR11 is for MICIN and EXTIN, VR12 is for TONEIN. That selection is linked with SW3.
P／E	Pre-emphasis circuit. Emphasize the higher frequency spectrum of the transmit voice signal in order to improve the signal-to-noise ratio of transmit modulated signal.
SW5	Transmit voice signal mute switch.
LIMITER	Limiting circuit for transmit voice signal amplitude in order to confine the maximum deviation of transmit modulated signal.
LIMSW	Limiter bypass switch.
SPLAT FIL	Low pass filter to reject the higher frequency (> 3kHz) spectrum from the transmit voice signal.
SUM2	Summing junction of transmit voice signal, transmit data and transmit SAT signal.
TDATA LPF	Low pass filter to reject the higher frequency (AMPS: >20kHz, TACS: >16kHz) spectrum from the transmit data signal.
VR4	Digital gain control circuit to set the maximum frequency deviation. Adjustable from 6.2dB to -6.4dB by 0.2dB step from the control register.
SMF1	Smoothing filter for transmit signal.
TRANSMIT BUFFER	38 bits transmit data buffer. Write "[DCC (2 bits)] + [transmit data (36 bit)]"
ENCODER	Add parity to the transmit data, then frame them properly to add Dotting Pattern(Wide), Sync Word(Wide/Narrow) and DCC(Wide), and encode them to Manchester code except Narrow Sync Word.

DSAT/DST GEN	Seven valid transmit DSAT/DST data generator. One DSAT data pattern and DSAT or DST are selected from the conrol register. These generated data are 24-bit NRZ data.
DSAT SELECT	Select either DSAT/DST or data/sync words for the transmit Narrow data. DSAT/DST data is selected while data and sync words are not transmitted at Narrow Analog Mode.
SW6	Select either Transmit data signal or Signaling Tone.
LEVEL TRANS1	Transmit data level translator.
VR2	Digital gain control circuit to set the transmit data signal level. Adjustable from + 3.0dB to -3.2dB by 0.2dB step from the control register.
DTXAMP	Gain Amp(12dB) for DTX low-state.
DTXSW	DTX low-state select switch.
WNSW1	Wide/Narrow mode for transmit data select switch.
TDATA LPF2	Low pass filter(fc=144Hz) to reject the higher frequency spectrum from the transmit data signal.
SW7	Transmit data signal mute switch.
STGEN	Signaling Tone generator.
SATCLKGEN	Transmit SAT signal and SATBPF clock generator.
SW8	Select either receive SAT signal or generated SAT signal(for test) for transmit SAT signal.
LEVEL TRANS2	Transmit SAT signal level translator.
VR3	Digital gain control circuit to set the transmit SAT signal level. Adjustable from + 1.4dB to -1.6dB by 0.2dB step from the control register.
TSATLPF	Low pass filter to reject the higher frequency spectrum of transmit SAT signal.
SW9	Transmit SAT signal mute switch.
Receiver Section	
AMP3	An OP-AMP to adjust the receive signal level. Set the proper gain (≦ 30dB) with external resistors.
AMP8	An OP-AMP to adjust the receive narrow data signal. Set the proper gain (≦ 30dB) with external resistors.
WNSW3	Wide(AMP3)/Narrow(AMP8) mode for receiver input AMP select switch. It is controlled from the control register add. 01 and 28.
AAF2	Anti-aliasing filter for receive signal.
RDATA LPF	Low pass filter to reject the higher frequency spectrum of receive signal.
VR5	Digital gain control circuit to set the receive signal level. Adjustable from + 3.0dB to -3.2dB by 0.2dB step from the control register.
RXBPF	Band-pass filter (300Hz～3300Hz) for receive voice signal.
D/E	De-emphasis circuit. Equalize the pre-emphasized voice signal to the original.
SW10	Receive voice signal mute switch.
EXP	Expander circuit. Expand the compressed voice signal to the original. Linearity can be adjusted from the control register.

SW11	Expander bypass switch.
SWHF	Hands-free system select switch.
VR6	Digital gain control circuit to set the RTONE signal level. Adjustable from + 0dB to -18dB by 6dB step from the control register.
SW12	RTONE signal mute switch.
SUM3	Summing junction of receive voice signal and RTONE signal.
VR7	Digital gain control circuit to set the level of REC1 output and EXTOUT output Adjustable from + 0dB to -21dB by 3dB step from the control register.
SUM4	Summing junction of receive voice signal and sidetone signal.
SW13	REC1 output mute switch.
AMP4	REC1 output buffer. Can drive 10kΩ or larger load.
SW14	EXTOUT output mute switch.
AMP5	EXTOUT output buffer. Can drive 10kΩ or larger load.
VR8	Digital gain control circuit to set the level of REC2 output Adjustable from + 0dB to -21dB by 3dB step from the control register.
SW15	REC2 output mute switch.
AMP6	REC2 output buffer. Can drive 10kΩ or larger load.
RECAMP	Ceramic receiver driver.
SMF2	Smoothing filter for receive data signal.
CMP1	Quantize the receive wide band data signal.
WDMSW	Quantized the receive wide band data output mute switch.
DATA RECOVERY	Receive wide band data recovery circuit. Recover clock from the received data and decode Manchester code to NRZ data.
WORD SYNC	Frame synchronization circuit.
DOTTING DETECTOR	Detect the Dotting Pattern of FVC and mute receive section during data burst after frame synchronization.
WNSW2	Wide/Narrow mode for receive data output select switch.
MAJORITY VOTING	3/5 majority voting circuit. Also, support Discontinuous Reception.
ERROR CORRECTION	Error correction circuit. Correct up to 2 bits error.
DATA PROCESSOR	Data Processor. Monitor the FOCC messages and generate interrupt at proper condition. Also, monitor the RECC status (BUSY/IDLE) .
RECEIVE BUFFER	30 bits receive data buffer. Buffer Error Status (2 bits) and 1 word (28 bits) .
RDATA LPF2	Low pass filter(fc=150Hz) to reject the higher frequency spectrum of receive signal.
SMF4	Smoothing filter for Narrow band receive data signal.
CMP3	Quantize the receive narrow band receive data signal.
SATBPF	High-Q band-pass filter to select receive SAT signal.

SMF3	Smoothing filter for receive SAT signal.
CMP2	Quantize the received SAT signal.
SATSW	Quantized the receive SAT signal output mute switch.
SAT DETECT	SAT signal detector. Detect the selected SAT signal.
The others	
OSC	Oscillator circuit. Generate 4.8 MHz main clock with quartz crystal, external resistor and cap. Or input 14.4/4.8 MHz clock to OSCIN pin.
DIV (1/3)	Clock divider. (1/3) Generate 4.8 MHz main clock from external 14.4MHz clock.
CLK BUF	4.8MHz clock output buffer.
CLKGEN	Internal clock generator.
DTMFGEN	Tone (include DTMF) signal generator.
TIMER1	Uncommitted 8 bits Timer 1.
TIMER2	Uncommitted 8 bits Timer 2.
DA1	Uncommitted 8 bits linear DAC 1.
DA2	Uncommitted 8 bits linear DAC 2.
DA3	Uncommitted 8 bits linear DAC 3.
AMP7	Uncommitted OP-AMP.
AFC	Auto Frequency Control Circuit.
REGISTER & DATA BUFFER	8 bit data bus interface circuit and 2 bit programmable I/O ports at parallel mode. At serial interface mode, AD0/P0～AD7/P7 pins are available for 8 bit programmabl I/O ports. P8 and P9 pins are available for 2 bit programmable I/O ports at any time.
BIAS	OP-AMP bias current generator.
AGNDGEN	Analog ground (1/2 VDD) generator.

Pin / Functions

NOTE: The value inside ( ) at the column I/O indicates the the value after RESET.

Pin No.	Pin Name	I/O	Function
Power			
40	DVDD	-	Power supply for digital section.
39	DVSS	-	GND for digital section.
22	RAVDD	-	Power supply for receiver analog section.
23	RAVSS	-	GND for receiver analog section.
4	TAVDD	-	Power supply for transmitter analog section.
3	TAVSS	-	GND for transmitter analog section.
70	AVDD	-	Power supply for substrate.
9	AGND	-	Analog ground (1/2 AVDD), connect capacitor.
10	RAGND	O	Analog ground (1/2 AVDD) for receiver section.
7	TAGND	O	Analog ground (1/2 AVDD) for transmitter section.
8	BIAS	I	Bias current setting pin. Connect to VSS through a specified resistor below: R_{BIAS} = 20×VDD [kΩ]
Transmit			
80	MIC1	I	MIC input (Inverting input of AMP1). Input impedance > 1MΩ. Set the MIC AMP (AMP1) gain with external resistors.
79	MIC2	O	MIC AMP output (output of AMP1). This output can drive50kΩ or larger, and 15pF or smaller.
78	TONEIN	I	Transmit DTMF Tone input. Input impedance > 1MΩ.
1	EXT1	I	EXT input (Inverting input of AMP2). Input impedance > 1MΩ. Set the EXT AMP (AMP2) gain with external resistors.
2	EXT2	O	EXT AMP output (output of AMP2). This output can drive50kΩ or larger, and 15pF or smaller.
61	TXHOLD	I	Transmit data hold input.
75	VOXTH	I	VOX threshold input.
66	VOXOUT	O (L)	VOX output. ("H":detect)
77	VGI	I	VOX gain stage input. Connect external resisters and a capacitor to set the sensitivity and the recovery time.
76	VGO	O	VOX gain stage output. Connect external resisters and a capacitor to set the sensitivity and the recovery time.
6	COMP1	I	Compressor capacitor connect pin. Connect a 0.047μF capacitor between COMP1 and COMP2.
5	COMP2	O	Compressor output.
74	MODOUT	O	Transmit output. This output can drive 10kΩ or larger, and 50pF or smaller.

Receive 24	DEM1	I	Receive signal input (inverting input of AMP3). Input impedance > 1MΩ. Set the receive input gain with external resistors.
25	DEM2	O	Output of AMP3. This output can drive 50kΩ or larger, and 15pF or smaller.
27	DEM3	I	Receive signal input (inverting input of AMP8). Input impedance > 1MΩ. Set the receive input gain with external resistors.
26	DEM4	O	Output of AMP8. This output can drive 50kΩ or larger, and 15pF or smaller.
65	SATDET	O (L)	Receive SAT detect output. ("H":detect)
64	SATOUT	O (L)	Receive SAT signal output.
28	RDREF	O	CMP3 off-set cancelation reference. Connect capacitor for off-set cancellation.
63	RXDATA	O (L)	Receive Wide/Narrow data output.
41	RXCTRL	O (H)	RF Receiver control. (refer to p71)
67	TXCTRL	O (H)	RF Transmitter control.
60	INT	O (L)	Interrupt output.
62	RXRDY	O (L)	Receive data ready.
14	DEOUT	O	De-emphasis output. Connect a 0.047μF capacitor between DEOUT and EXPIN.
13	EXPIN	I	Expander input. Connect a 0.047μF capacitor between DEOUT and EXPIN.
12	HFOUT	O	Receive voice signal output for Hands-free system. This output can drive 50kΩ or larger and 150pF or smaller
11	HFIN	I	Receive voice signal input for Hands-free system. This pin is connected RAGND with internal resister. Input impedance > 100kΩ
29	DTMFOUT	O	DTMF tone output. This output can drive 10kΩ or larger and 50pF or smaller.
15	RTONE	I	DTMF Tone input for the receiver. Input impedance > 1MΩ
17	EXTOUT	O	External receive signal output. This output can drive 10kΩ or larger and 50pF or smaller.
18	REC1	O	Receive signal output 1. This output can drive 10kΩ or larger and 50pF or smaller.
16	REC2	O	Receive signal output 2. This output can drive 10kΩ or larger and 50pF or smaller.
19	RECIN	I	Ceramic receiver driver input.
21	RECP	O	Ceramic receiver driver positive output.
20	RECN	O	Ceramic receiver driver negative output.
DAC/AMP 69	DA1	O	DAC 1 output. This output can drive 50kΩ or larger, and 50pF or smaller.
31	DA2	O	DAC 2 output. This output can drive 50kΩ or larger, and 50pF or smaller.
32	DA3	O	DAC 3 output. This output can drive 50kΩ or larger, and 50pF or smaller.

73	AMPOUT	O	AMP7 output. This output can drive 10kΩ or larger, and 50pF or smaller.
71	AMPINP	I	AMP7 non-inverting input.
72	AMPINN	I	AMP7 inverting input.
Control			
57	P/S	I	Parallel/Serial interface select.
53	DS/CS	I	Data strobe input / Chip select input.
54	ALE/SDI	I	Address latch enable input / Serial data input.
52	R/W/SCLK	I	Read/Write Select input / Serial clock input.
55	SDO	O(Z)	Serial data output.
42-49	AD0~AD7/ P0~P7	I/O	Parallel interface mode: 8 bit Adress/Date bus. Serial interface mode : 8 programmable I/O ports.
50-51	P8~P9	I/O	2 programmable I/O ports.
56	RST	I	Reset input. "L" active. Minimum pulse width is 100ns.
58	TEXP1	O(L)	Timer 1 expire output.
59	TEXP2	O(L)	Timer 2 expire output.
Clock			
35	OSCIN	I	4.8 MHz Oscillator input/14.4/4.8MHz clock input.
36	OSCOUT	O	4.8 MHz Oscillator output.
34	CLKSEL	I	Clock selection pin. (14.4 MHz("L") / 4.8 MHz("H"))
38	CLKOUT	O	4.8 MHz clock output. ("L": disable)
37	CLKEN	I	Clock output enable ("L": enable, "H": disable)
33	AFCIN	I	IF signal input pin for AFC.
Test			
68	TESTIN	I	Test input pin. (Connect to AVSS at normal operation)
30	TESTOUT	O	Test output pin. (Connect nothing at normal operation)

Z: High-Z

Absolute Maximum Ratings

TAVSS, RAVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VA+	-0.3	6.5	V
Input Current (except power supply pin)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.3	V
Storage Temperature	Tstg	-55	130	℃

Note 1: All voltage values are with respect to VSS pin.

WARNING: Operations at or beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

TAVSS, RAVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Ambient Operating Temperature		Ta	-30		85	℃
Power Supply		VDD	2.7		5.5	V
Analog Ground		AGND		1/2VDD		V
[VDD=3V]						
Power Consumption	mode 0	Idd0		0.7		mA
(Note 2)	mode 1	Idd1		1.4		
	mode 2	Idd2		2.9		
	mode 3	Idd3		2.3		
	mode 4	Idd4		3.8		
	mode 5	Idd5		7.0		
[VDD=5V]						
Power Consumption	mode 0	Idd0		1.0	1.3	mA
(Note 2)	mode 1	Idd1		2.0	2.8	
	mode 2	Idd2		3.5	5.0	
	mode 3	Idd3		2.9	4.0	
	mode 4	Idd4		4.4	6.1	
	mode 5	Idd5		7.9	11.2	

Note 1: All voltage values are with respect to VSS pin.

Note 2: Oscillator: 14.4MHz input, DACs, AMP7, VOX, AFC: OFF

Digital Characteristics

■ DC Specifications

Parameter	Pin	Symbol	min	typ	max	Units
High Level Input Voltage	(1)	V_{IH}	70%VDD			V
Low Level Input Voltage	(1)	V_{IL}			30%VDD	V
High Level Input Current V_{IH}=VDD	(1)	I_{IH}			10	μA
Low Level Input Current V_{IL}=0V	(1)	I_{IL}	-10			μA
High Level Output Voltage I_{OH}=-400μA	(2)	V_{OH}	90%VDD			V
Low Level Output Voltage I_{OL}=400μA	(2)	V_{OL}			0.4	V

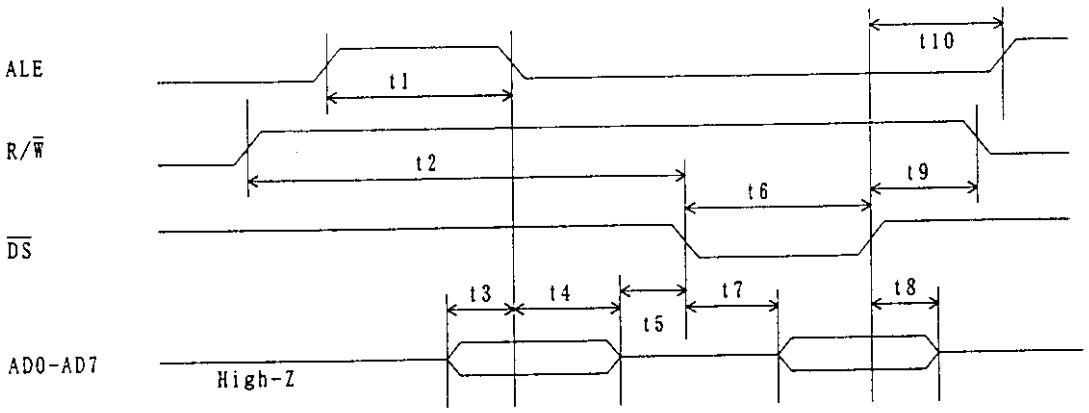
(1) All digital inputs ($\overline{RST}$, P/$\overline{S}$, SDI/ALE, $\overline{CS}$/$\overline{DS}$, SCLK/R/$\overline{W}$, CLKEN, CLKSEL, TXHOLD, P0~P7/AD0~AD7, P8, P9)

(2) All digital outputs (SDO, TEXP1, TEXP2, VOXOUT, CLKOUT, RXRDY, INT, TXCTRL, SATDET, P0~P7/AD0~AD7, P8, P9, RXDATA, RXCTRL, SATOUT)

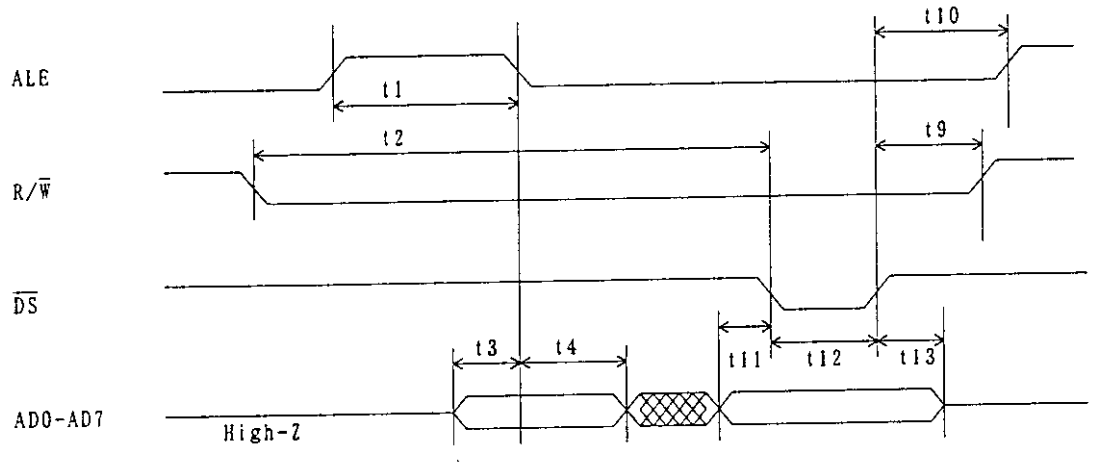
■ AC Specifications

Parameter	Pin	Symbol	min	typ	max	Units
Master Clock Frequency	OSCIN					
(CLKSEL=1)		F_{CK1}		4.8		MHz
(CLKSEL=0)		F_{CK2}		14.4		
4.8MHz Clock Duty Cycle	OSCIN	F_{CKDTY}	40		60	%
Input Level (H)		F_{CKVH}	20			V
Input Level (L)		F_{CKVL}			0.3	V
14.4MHz Clock Input Level	OSCIN	F_{OSCIN}	0.3		1.5	V_{P-P}
AFCIN Input Frequency	AFCIN	F_{AFCIN}		450		kHz
AFCIN Input Level	AFCIN	V_{AFCIN}	0.3		1.5	V_{P-P}
Parallel Interface Timing						
ALE Pulse Width "H"	ALE	t1	1000			ns
R/$\overline{W}$ Setup Time		t2	100			ns
Address Setup Time		t3	100			ns
Address Hold Time		t4	100			ns
$\overline{DS}$ Setup Time		t5	0			ns
$\overline{DS}$ Pulse Width "L"		t6				
Status and Event Register			1000			ns
Data Register			2000			ns
DS "↓" to Data Valid (Note 1)		t7			100	ns
Data Hold Time		t8	0			ns
R/$\overline{W}$ Hold Time		t9	100			ns
DS "↑" to ALE "↑"		t10	1000			ns
Data Setup Time		t11	100			ns
$\overline{DS}$ Pulse Width "L"		t12	1000			ns
Data Hold Time		t13	100			ns
$\overline{DS}$ CYCLE Time <WRITE>			2000			ns
(Status & Event) <READ>			2000			ns
(Data) <READ>			3000			ns
Serial Interface Timing						
$\overline{CS}$ "↓" to SCLK "↓"	$\overline{CS}$, SCLK	t1	100			ns
SCLK Pulse width "L"	SCLK	t2	350			ns
SCLK Pulse width "H"	SCLK	t3	350			ns
SDI data set-up time	SDI	t4	100			ns
SDI Data hold time	SDI	t5	100			ns
SCLK "↑" to $\overline{CS}$ hold time	$\overline{CS}$, SCLK	t6	600			ns
$\overline{CS}$ Pulse width "H"	$\overline{CS}$	t7	400			ns
SCLK Pulse width of	SCLK	t8				
R/$\overline{W}$ bit "H"			400			ns
(Status & Event)			2000			ns
(Data)						
SCLK "↓" to SDO Data Valid (Note)	SDO	t9			100	ns
$\overline{CS}$ "↑" to SDO Hi-Z		t10			100	ns

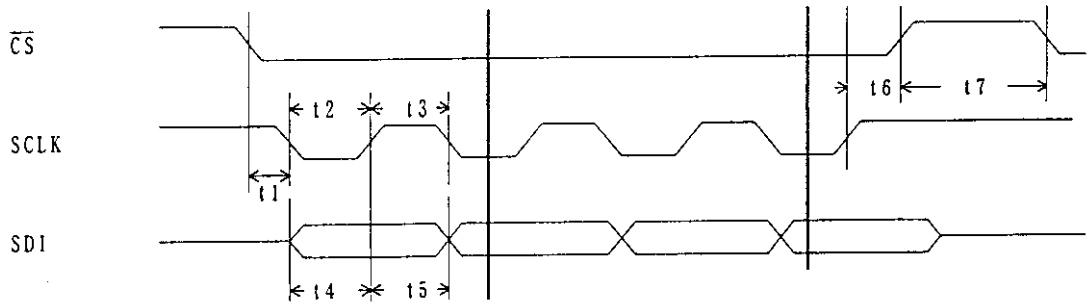
Note: Load Cap < 20pF



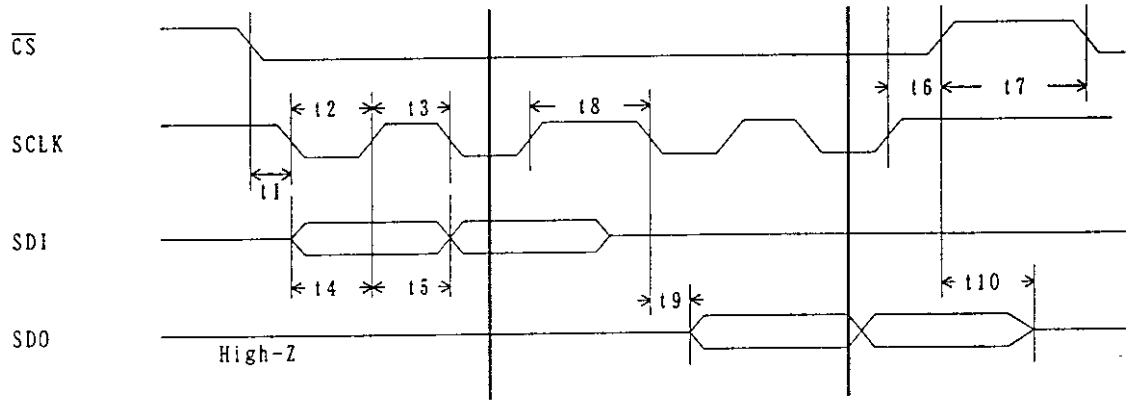
Parallel Interface Timing - Read



Parallel Interface Timing - Write



Serial Interface Timing - WRITE



Serial Interface Timing - READ

Analog Characteristics

AVDD=3.0V
AVSS=0V
Ta=-30～+85℃

■ Transmitter

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Gain	MIC2 ↓ MODOUT	MIC2=-22.0dBV @ 1kHz VR11=0dB, VR4=-5dB COMPRESSOR ON	-2.0	0.0	+2.0	dB	AMPS/ TACS
			-7.7	-5.7	-3.7	dB	NAMPS
			-5.7	-3.7	-1.7	dB	NTACS
	EXT2 ↓ MODOUT	EXT2=-22.0dBV @ 1kHz VR11=0dB, VR4=-5dB COMPRESSOR ON	-2.0	0.0	+2.0	dB	AMPS/ TACS
			-7.7	-5.7	-3.7	dB	NAMPS
			-5.7	-3.7	-1.7	dB	NTACS
	TONEIN ↓ MODOUT	TONEIN=-13.2dBV @ 1kHz VR12=0dB, VR4=-5dB COMPRESSOR OFF	-7.0	-5.0	-3.0	dB	AMPS
			-11.3	-9.3	-7.3	dB	TACS
			-14.5	-12.5	-10.5	dB	NAMPS
			-11.7	-9.7	-7.7	dB	NTACS
SINAD (S/N+D)	MIC2 ↓ MODOUT	MIC2=-8.0dBV @ 1kHz VR1=0dB VR4=-5dB COMPRESSOR ON C-message weighted	35			dB	
Noise Level	MODOUT	VR1=0dB VR4=-5dB COMPRESSOR ON C-message weighted			-42	dBV	Note 1)
Volume Step Deviation		VR1	-0.3		+0.3	dB	
		VR2, VR3, VR4	-0.2		+0.2		
Limitter Level	MODOUT		0.584	0.619	0.656	Vp-p	
SAT Output Level	MODOUT	VR3=-12dB VR4=-5dB	-26.7	-25.2	-23.7	dBV	
Data Output Level	MODOUT	VR2=0dB VR4=-5dB	-14.7	-13.2	-11.7	dBV	AMPS/ TACS
			-35.8	-34.3	-32.8	dBV	NAMPS
			-33.8	-32.3	-30.8	dBV	NTACS
DTMF Output Level	DTMFOUT	Single Tone	-14.2	-13.2	-12.2	dBV	
DTMF Twist DTH - DTL	DTMFOUT	AMPS		0		dB	
		TACS		2			
DTMF Frequency Deviation	DTMFOUT		-1.5		+1.5	%	
DTMF Tone SINAD	MODOUT	Single tone output	20			dB	
VOX Sensitivity VOX Attack Time VOX Recovery Time		(refer to P69)					

Note 1) Connect voice band input (TONEIN, MICIN, EXTIN) to TAGND through external resistor.

ASAHI KASEI [AK2336]

■ Receiver

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Gain	DEM2 ↓ EXTOUT	DEM2=-20dBV @ 1kHz VR5=0dB, VR7=0dB EXPANDOR ON	-10.0	-8.0	-6.0	dB	AMPS/ TACS
			+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	DEM4 ↓ EXTOUT	DEM2=-20dBV @ 1kHz VR5=0dB, VR7=0dB EXPANDOR ON	+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	DEM2 ↓ REC2	DEM2=-20dBV @ 1kHz VR5=0dB, VR8=0dB EXPANDOR ON	-10.0	-8.0	-6.0	dB	AMPS/ TACS
			+1.4	+3.4	+5.4	dB	NAMPS
			-2.6	-0.6	+1.4	dB	NTACS
	RTONE ↓ REC1	RTONE=-20dBV @ 1kHz VR6=0dB VR7=0dB	-1.0	0	+1.0	dB	
SINAD (S/N+D)	DEM2 ↓ REC1	DEM2=-11.2dBV @ 1kHz VR5=0dB VR7=0dB EXPANDOR ON C-message weighted	35			dB	
Noise Level	REC1	VR5=0dB VR7=0dB EXPANDOR ON C-message weighted		-80	-70	dBV	Note 1)
Volume Step Deviation		VR5	-0.2		-0.2	dB	
		VR6, VR7, VR8	-0.5		+0.5		
SAT Detect Level	DEM2	f=6kHz VR5=0dB	-35.2			dBV	Note 2)

Note 1) Connect DEM1 to RAGND through external resistor.
Note 2) measured with SAT frequency of 6kHz

ASAHI KASEI [AK2336]

■ Cross Talk

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Crosstalk	DEM2 ↓ MODOUT	DEM2 = -11.2dBV COMPRESSOR ON EXPANDOR ON VR1, VR5, VR7 = 0dB VR4 = -5dB			-60	dB	NOTE 1)
	MIC2 ↓ REC1	MIC2 = -8.0dBV COMPRESSOR ON EXPANDOR ON VR1, VR5, VR7 = 0dB VR4 = -5dB			-60	dB	NOTE 1)

Note 1) Connect the other analog input to RAGND/TAGND with an external resister respectively.

■ Filter Specification

Filter Name	Pin	Frequency Response	Condition		
			Input level	Reference Frequency	
RX OVERALL	DEM2 ↓ REC1	Fig-1	-20dBV	1 kHz	VR5: 0dB VR7: 0dB EXPANDOR: OFF
TX OVERALL	MIC2 ↓ MODOUT	Fig-2	-22dBV	1 kHz	VR1: 0dB VR4:-5dB COMPRESSOR:OFF
Splatter Filter	(SPLAT FIL) ↓ MODOUT	Fig-3			
TDATA LPF	(TDATA LPF) ↓ MODOUT	Fig-4			
RDATA LPF2	DEM2 ↓ (RDATALPF2)	Fig-5			
TDATA LPF2	(TDATALPF2) ↓ MODOUT	Fig-6			
TX Sat Pass	(TSAT LPF) ↓ MODOUT	Fig-9			VR4:-5dB
TX Data Pass	(SUM2) ↓ MODOUT	Fig-10			VR4:-5dB

■ Compandor Specification(Not adjusted linearity from control register)

AVDD=3.0V f=1kHz

Item	Pin	Conditions	MIN	TYP	MAX	Units	Remarks
Compressor							
Unity Gain Level	COMP2	MIC2 = -12.0dBV	-13.0	-12.0	-11.0	dBV	
Output Level	COMP2	MIC2 = -2.0dBV	4.0	5.0	6.0	dB	Note 1)
		MIC2 = -52.0dBV	-22.0	-20.0	-18.0	dB	Note 1)
Attack Time	COMP2	MIC2 = -24.0dBV → -12.0dBV 1.5 times of final value	2	3	5	ms	
Recovery Time	COMP2	MIC2 = -12.0dBV → -24.0dBV 0.75 times of final value	7	13.5	20	ms	
Expander							
Unity Gain Level	HFOUT	EXPIN = -12.0dBV	-13.0	-12.0	-11.0	dBV	
Output Level	HFOUT	EXPIN = -7.0dBV	9.0	10.0	11.0	dB	Note 2)
		EXPIN = -32.0dBV	-43.0	-40.0	-37.0	dB	Note 2)
Attack Time	HFOUT	EXPIN = -18.0dBV → -12.0dBV 0.75 times of final value	7	13.5	20	ms	
Recovery Time	HFOUT	EXPIN = -12.0dBV → -18.0dBV 1.5 times of final value	7	13.5	20	ms	

Note 1) Relative value to unity gain level, without register adjustment (Fig-7)
Note 2) Relative value to unity gain level, without register adjustment (Fig-8)

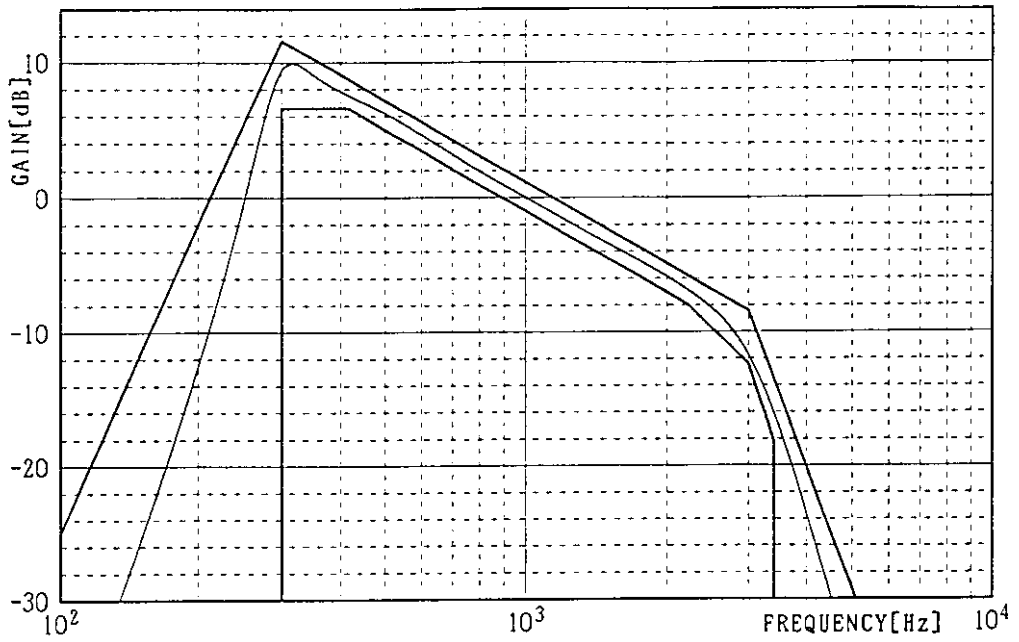


Fig - 1 Total Frequency Response of Receiver Section

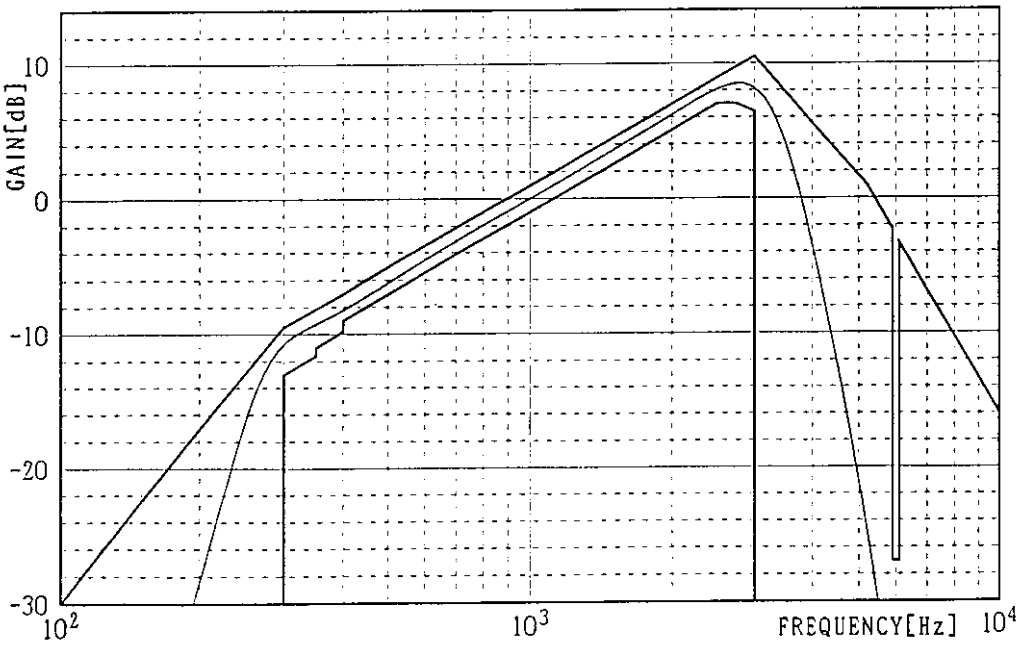


Fig - 2 Total Frequency Response of Transmitter Section

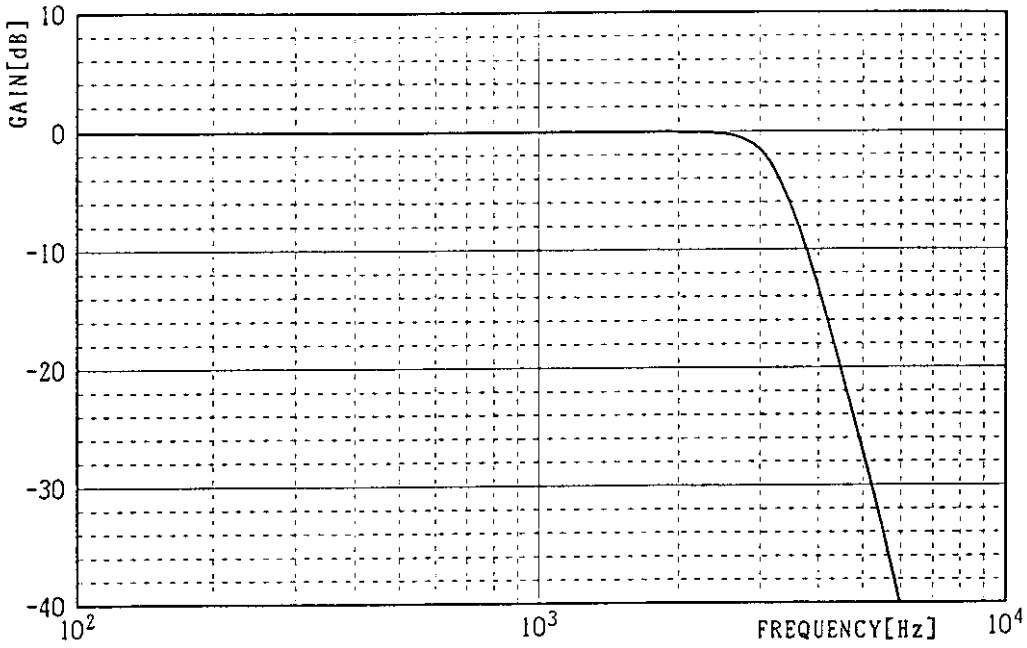


Fig - 3 Frequency Response of Splatter Filter

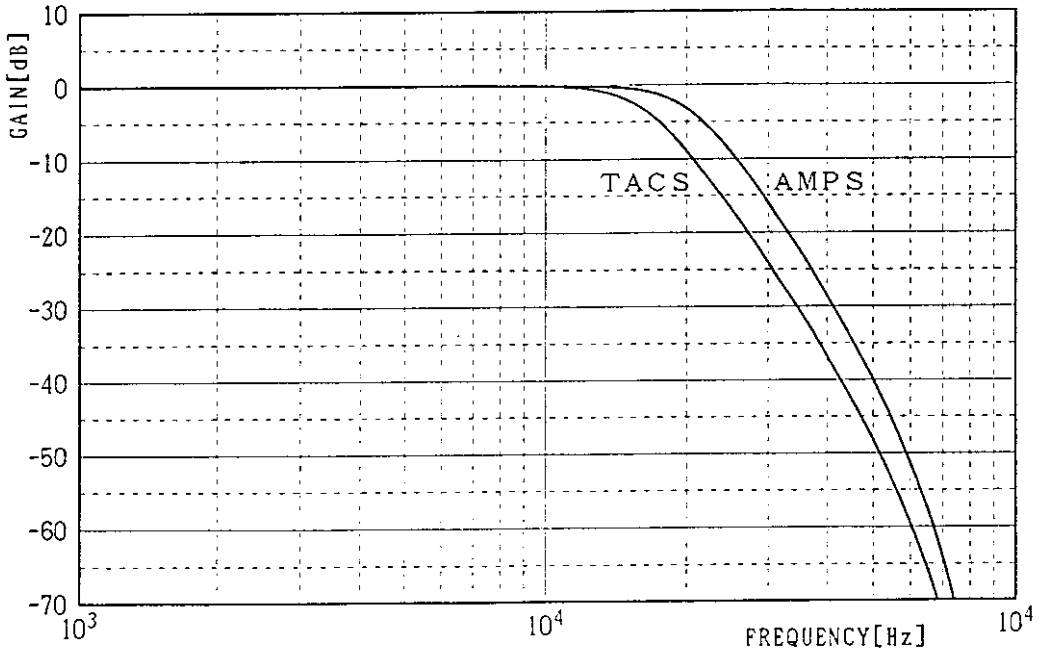


Fig - 4 Frequency Response of Transmitter Data Filter

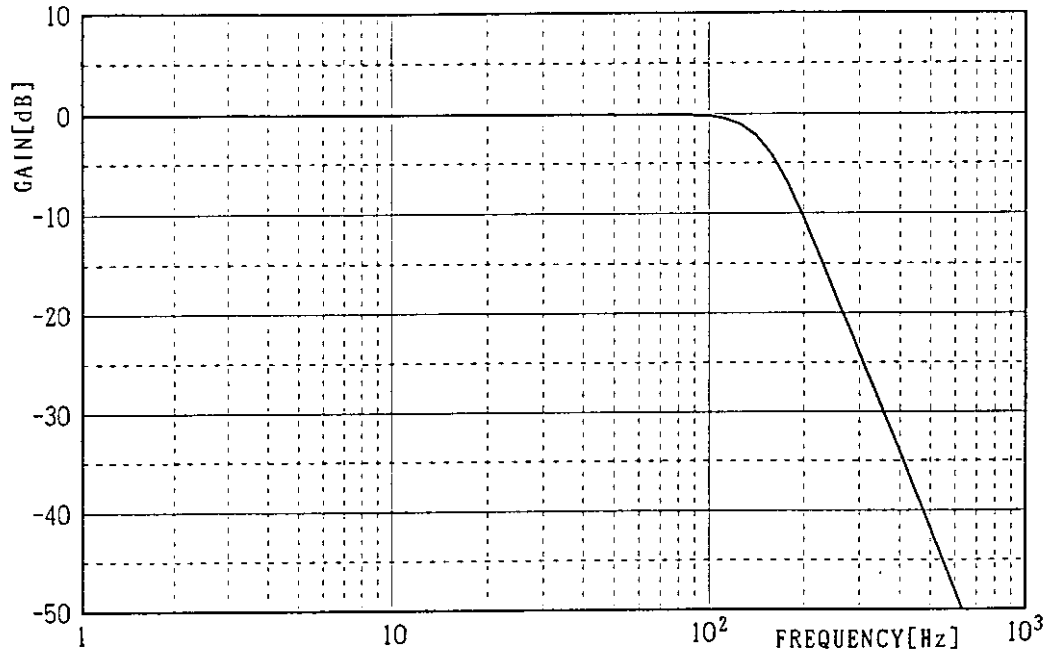


Fig - 5 Frequency Response of Receiver Data Filter2

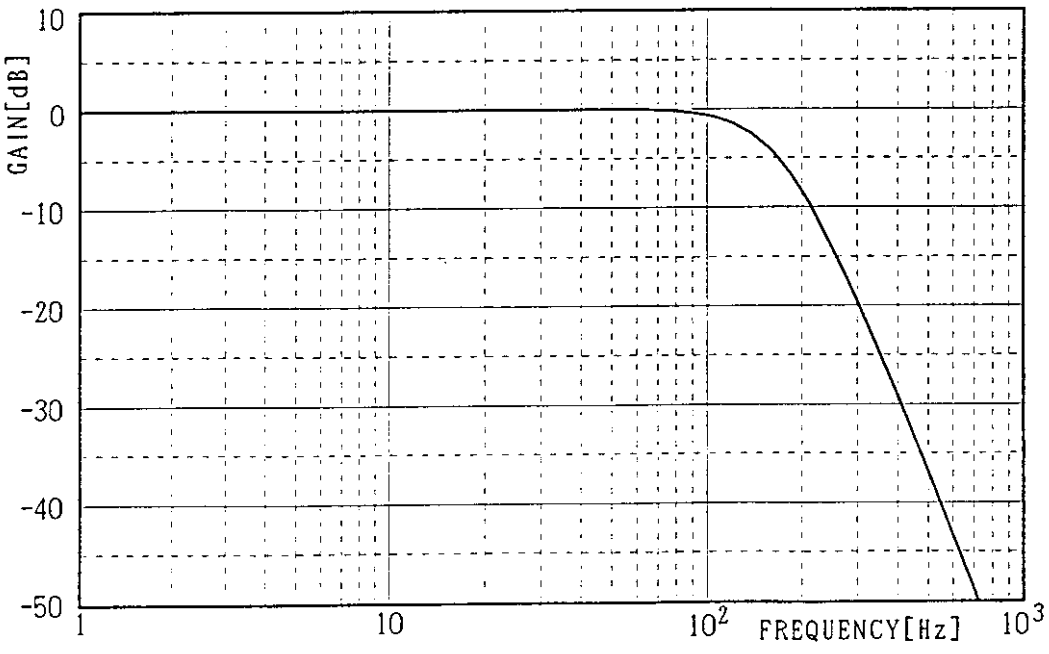


Fig - 6 Frequency Response of Transmitter Data Filter2

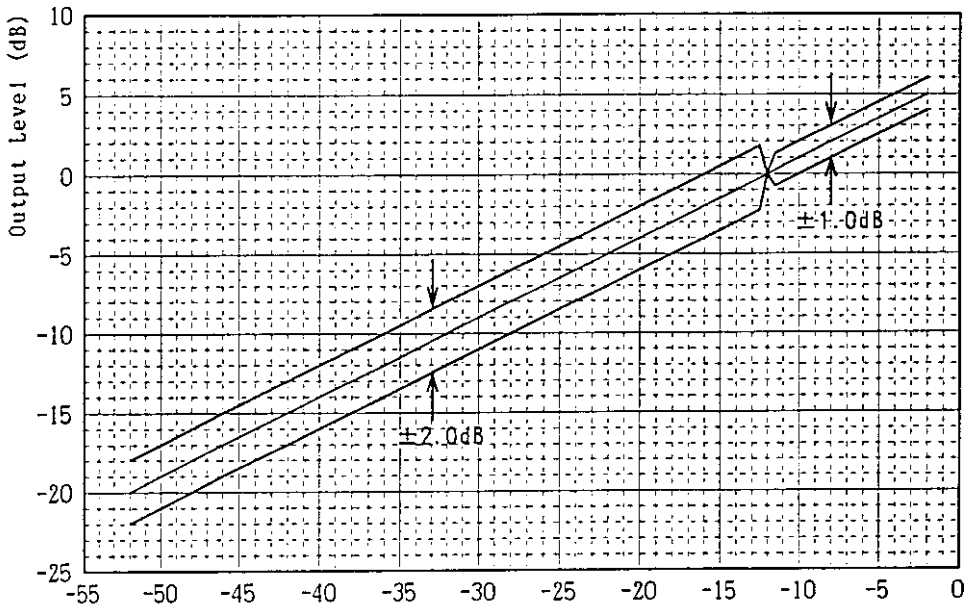


Fig-7 COMPRESSOR LINEARITY

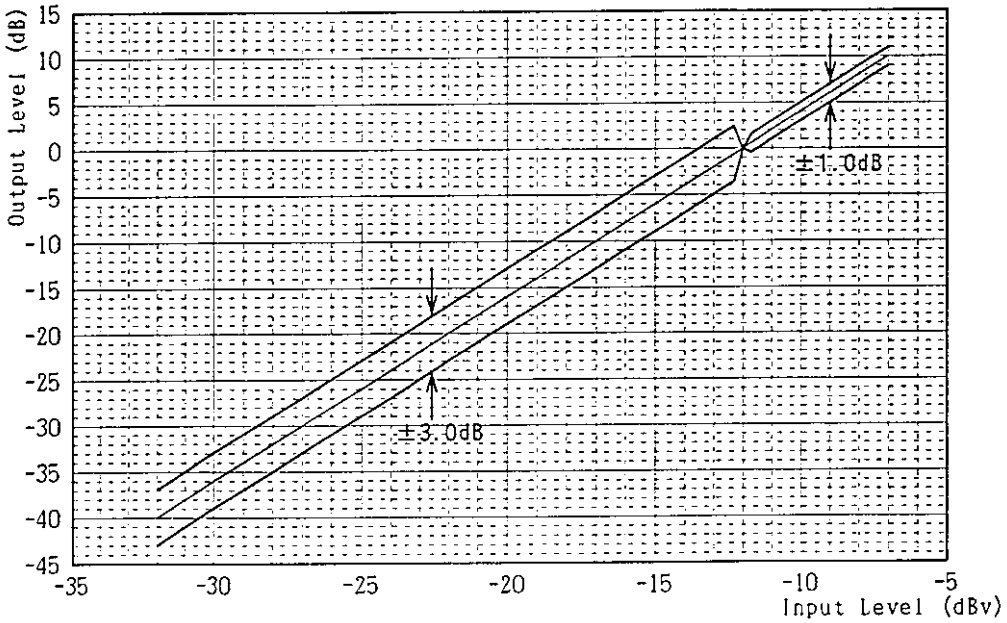


Fig-8 EXPANDER LINEARITY

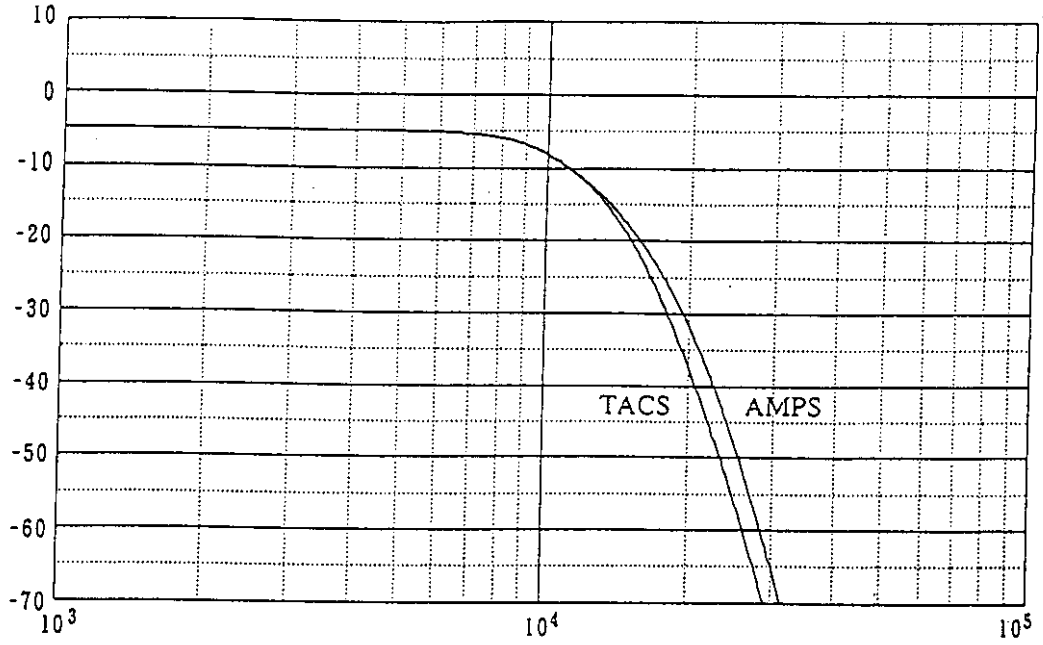


Fig - 9 Frequency Response of Transmitter Sat Pass

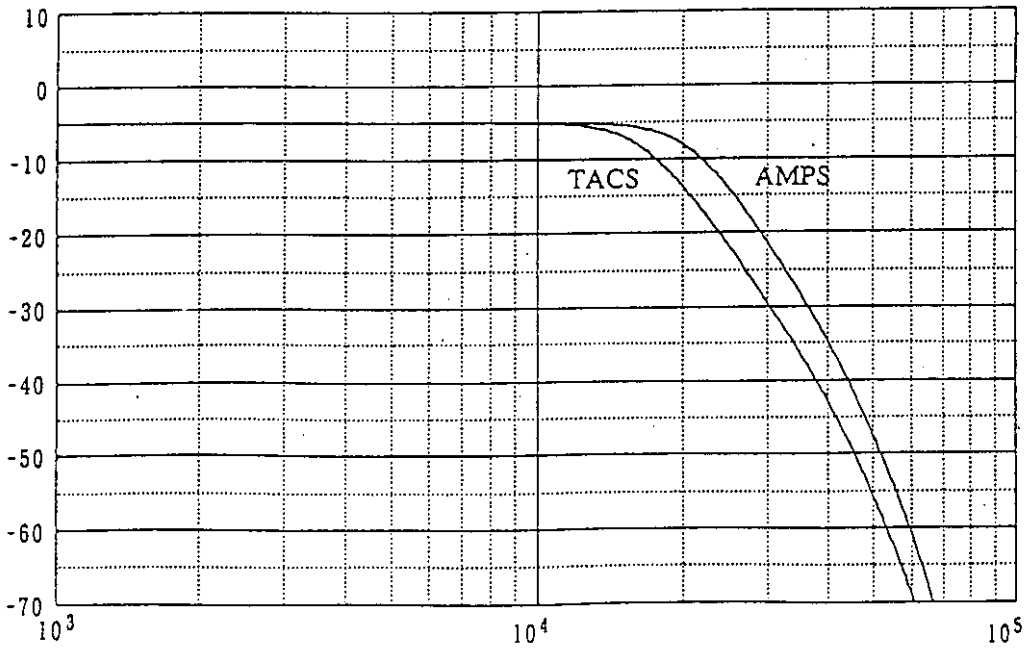
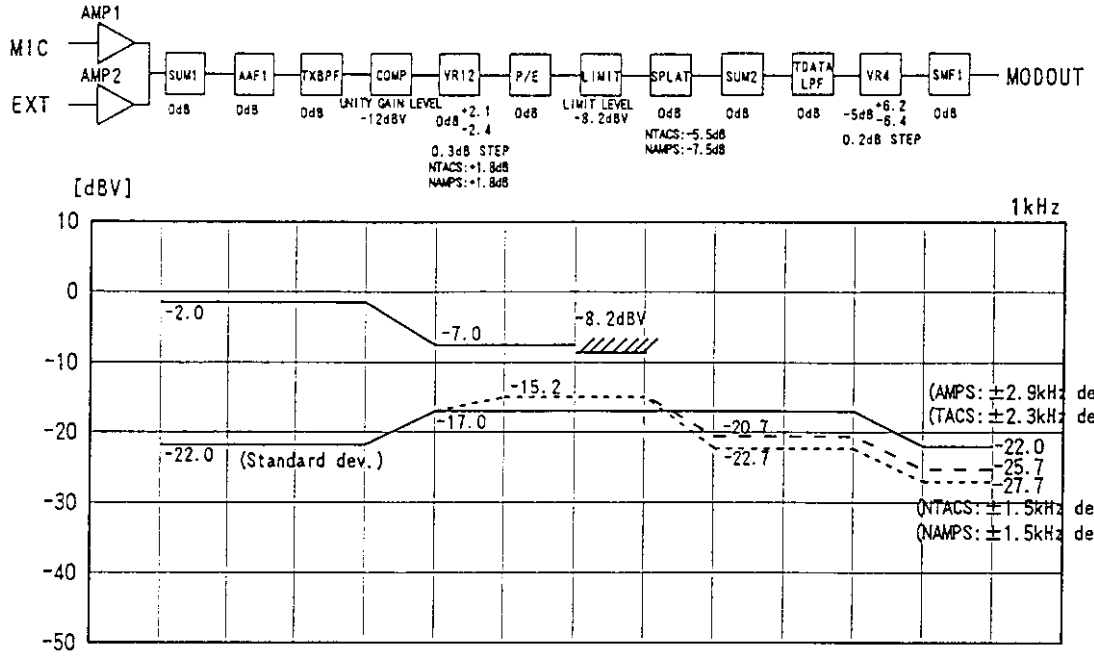


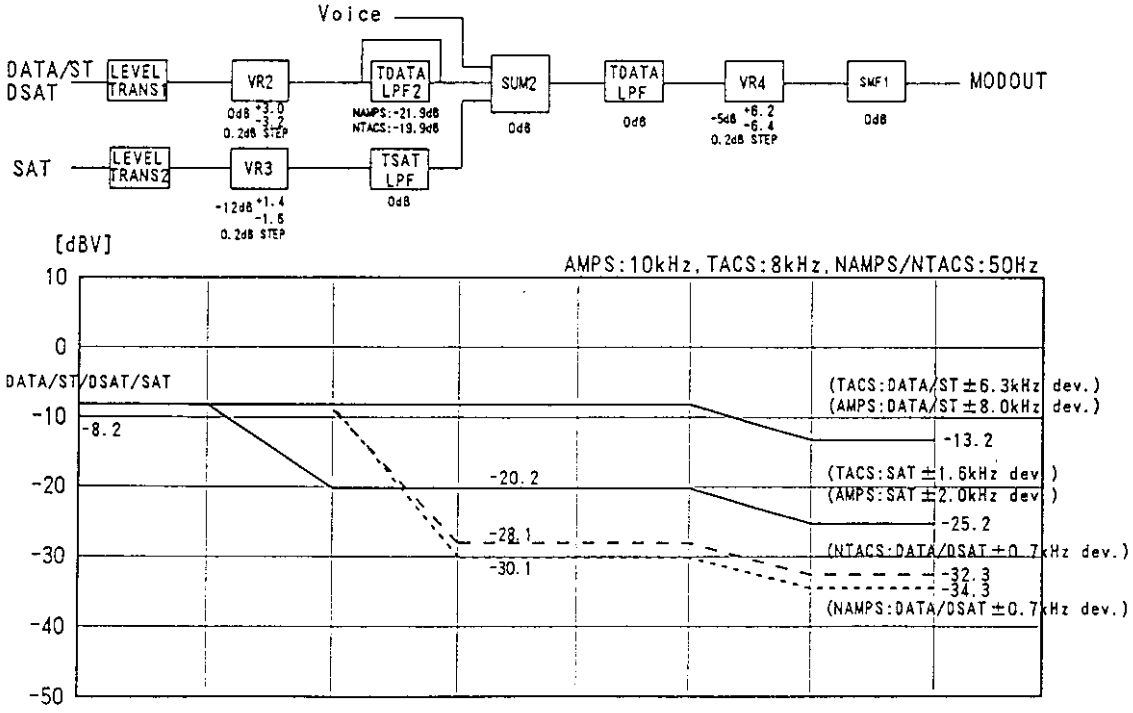
Fig - 10 Frequency Response of Transmitter Data Pass

Level Diagrams

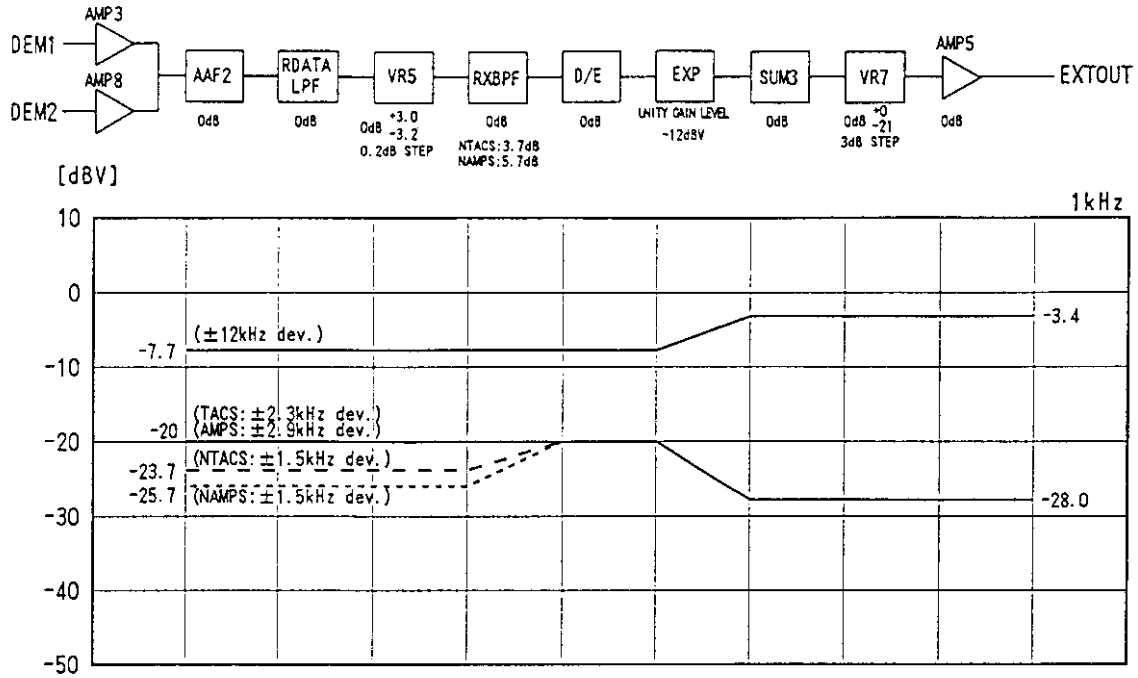
VDD=3.0V, 0dBV=1Vrms



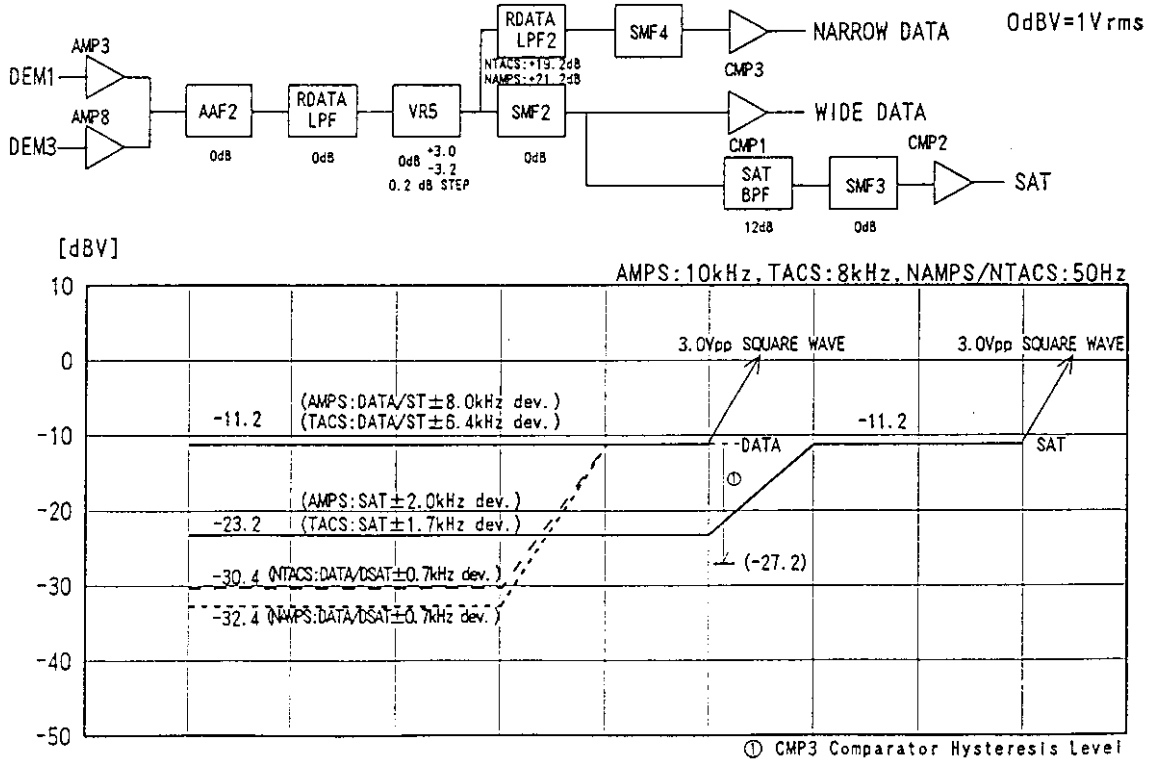
Transmit Voice Signal Level Diagram



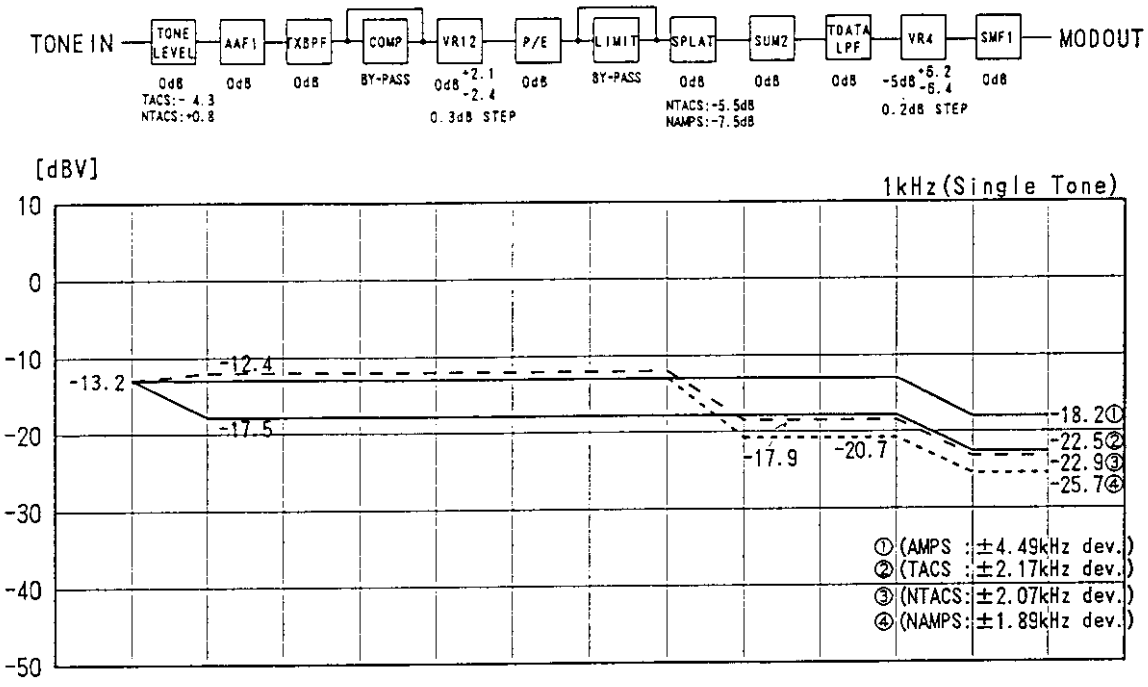
Transmit Data Signal and SAT Signal Level Diagram



Receive Voice Signal Level Diagram



Receive Data Signal and SAT Signal Level Diagram



Transmit DTMF Signal Level Diagram

Circuit Description

■ Power Management

The AK2336 has six modes of operation, described in the Register Map "POWER DOWN MODE CONTROL" (address 00) for a meticulous power management. So its power consumption is only 1.4mA (TYP) at the "RX DATA Mode", when VDD is 3V. The AK2336 can handle FOCC data by itself and the conjunctive micro-controller could be in sleep mode during Idle mode. Therefore, the total stand by time could be extended as long as 1.5 times of the conventional solution.

■ Data Transmitter

Wideband RECC/RVC Data

The AK2336 provides the following treatments to the 38 bits incoming data (Message:36 bits + DCC:2 bits).

1) BCH Encode
2) Dotting Pattern
3) Synchronization Word
4) 7 bits Coded DCC (RECC only)
5) 48 bits code word
6) Message Construction
7) Manchester Encode

Narrow RVC Data

The AK2336 provides the following treatments to the 36 bits incoming data.

1) BCH Encode
2) NRZ Synchronization Word
3) 48 bits code word
4) Message Construction
5) Manchester Encode (Data Word only)

The AK2336 is transparent to the 36 bits data of Reverse Control Channel and Wideband /Narrow Reverse Voice Channel.

RECC Data Transmit Timing

Fig-7 shows Reverse Control Channel(RECC) data transmit timing.

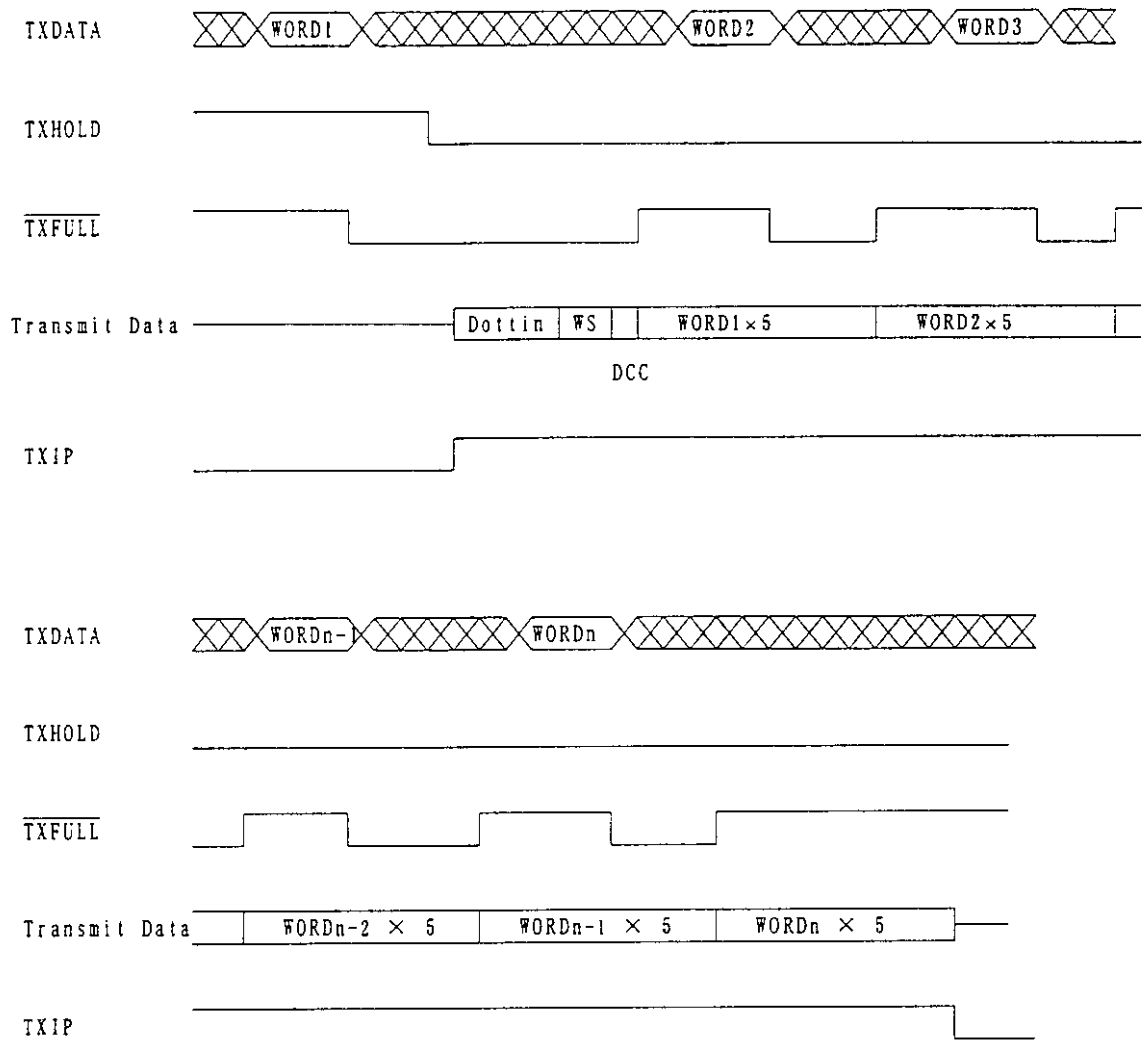
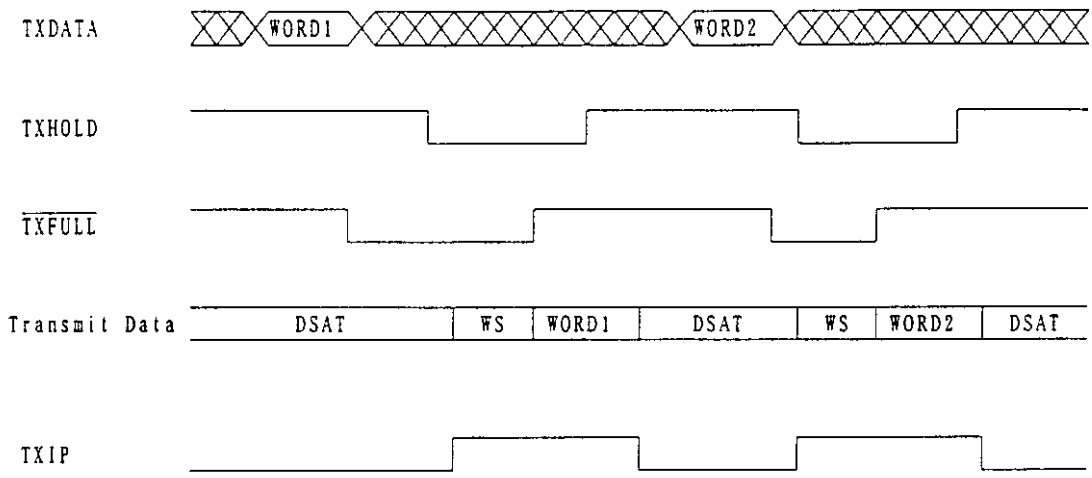


Fig-7 RECC Data Transmit Timing

Narrow RVC Data Transmit Timing

Fig-8 shows Narrow Reverse Voice Channel data transmit timing.



*DSAT phase is maintained so that when it is discontinued for transmission of data and sync words it is at the proper phase.

Fig-8 Narrow RVC Data Transmit Timing

DSAT/DST Generator

The AK2336 can generate seven valid DSAT/DST(24 bit) patterns. One of them, that was selected from the control register, is generated repeatedly, when Narrow Analog Mode is selected from the control register. When the polarity(DSAT↔DST) changes is desired from the control register(address 03) at Narrow Analog Mode, polarity will not be changed until next allowable phase, which is given as a Bit-Mask. For each mask bit that is set, a polarity inversion is allowed on that bit.
When DSAT/DST pattern changes is desired from the control register at Narrow Analog Mode, also the polarity that is the same address is set at the same time. And then the pattern and polarity will changed within 5ms.
NOTE: When the TXINV(address 01, bit1) change will be desired from the control register, the transmit data polarity is change immediately.

RECC Access Arbitration

TXCTRL pin goes "L" and INTERRUPT pin goes "H" simultaneously in order to stop transmission, if B/I bit alters to "Busy" from "Idle" by 56th bit or remains "Idle" until 104th bit after the transmission start.
The AK2336 adds unmodulated carrier(MODOUT pin output goes AGND level) automatically after transmitting the last data and TXIP goes "L" to inform no data transmission in progress.

■ **Receiver**

Wideband FOCC/FVC Data

The AK2336 performs the following treatments and outputs 28 bit data through the receive buffer.

1) Bit synchronization and word synchronization
2) Busy/Idle bit extraction
3) Majority Voting
4) Error Correction

The AK2336 is transparent to 28 bits data of FOCC and FVC.
When "DATA PROCESSOR ENABLE" (address 02) is set to "H", AK2336 Data Processor performs as described in the next chapter "Data Processor".

Narrow FVC Data

The AK2336 quantize the received data signal and outputs it without any processing.

DATA RECOVERY

The Data Recovery block performs clock recovery, manchester decoding and data regeneration. There are two mode of operation in clock recovery: high speed pull-in mode and low jitter mode. Once the word sync is detected, PLL goes to low jitter mode automatically.

DOTTING DETECTOR

The Dotting Detector block detect 32 bit continuous Dotting Pattern in FVC and generate interrupt. If "RX AUTO MUTE ENABLE" (addles 01) is set, receive voice circuits are muted after frame synchronization automatically. The external controller have to write address 6 7 (RXCTRL RESET) to be released from the mute and also the Dotting Detector block is reset.

WORD SYNC

The Word Sync block performs the frame synchronization and Busy/Idle bit extraction. The Word Sync block goes into In-frame mode after two consecutive Sync Word detection and goes into Out-of-frame mode after five consecutive miss-detection.

REVERSE CONTROL CHANNEL STATUS

The status of the reverse control channel is determined by register setting of "Busy/Idle MODE SELECT" (address 02)

"B/I MODE SELECT" = 1 : BUSY/IDLE detect by 1 bit data directly
"B/I MODE SELECT" = 0 : BUSY/IDLE detect by continuous 2 bit data

MAJORITY VOTING

Forward Control Channel:
The Majority Voting block performs bit-wise majority decision on five words of system A or B according to the Serving System (A/B) register after valid Word Sync detection.
Forward Voice Channel:
The Majority Voting block performs bit-wise majority decision on five consecutive word after the just before valid Word Sync detection.

ERROR CORRECTION

The Error Correction block corrects up to two bits error according to the control register by 12 parity bit in majority voted 40 bit data. If the more error(that is set correctional bit by register) occurs, it generates interrupt for uncorrection.

RECEIVE BUFFER

The Receive Buffer maintains corrected 28 bits data. RXRDY pin goes to "H" when the data is ready to read. RXRDY goes to "L" after reading the data or after majority voting of the next word being completed. The AK2336 over-writes the buffer when new data is received, even the previous data is not read yet.

■ Data Processor

The AK2336 Data Processor monitors Overhead Message and Control Message of Forward Control Channel (FOCC), and generates interrupt in proper manner. Therefore, the micro-controller may be in sleep mode until the AK2336 generates the interrupt. The AK2336 stores all the data needed during Idle Mode, and the micro-controller can read the data, which are received during sleeping, from the data register (address 90~DF) of the AK2336 after interrupt occurs.

This unique feature makes it possible to save the total power consumption during Idle Mode and could extend the standby time as long as 1.5 times of the conventional solution.

Rx Data Mode Operation

The AK2336 Data Processor has five modes of operation and each mode is independently set by "DP CONTROL"(address 30) except the folowing condition.

(1) Either OHM Train Mode or SPM mode is selectable. If both mode are selected, SPM mode is neglected because SPM mode is a subset of OHM Train mode.
(2) Both CFM mode and MSCM mode are selectable independently.
(3) If All mode is selected, the other mode is neglected.
(4) OHM Train mode, SPM mode and MSCM mode processing are not to be done, if CFM is received

NOTE: The Data Processor must be disabled (address 02, "RECEIVE DATA CONTROL") once, whenever the Data Processor mode is altered.

The interrupt condition is different in each mode as shown below.

(1) OHM Train Mode

Interrupt Conditions:
- Both SPM1 and SPM2 reception
  &
- OHM, whose END field = 1, reception
  &
- Different OHM(after 2nd OHM)

(2) SPM mode

Interrupt Condition:
- Both SPM1 and SPM2 reception
  &
- Different SPM(after 2nd SPM)

(3) MSCM Mode

Interrupt Conditions:

If MSCM mode is MIN1,
- MIN1r=MIN1p (One Word Page) reception
- MIN1r=MIN1p and MSCM (Except One Word Page) reception
- on and after MSCM3 reception

If MSCM mode is MIN1 & MIN2,
- MIN1r=MIN1p and MIN2r=MIN2p (Except One Word Page) reception
- on and after MSCM3 reception

If MSCM mode is OFF, (no MIN check)
- One Word Page reception
- MSCM1 and MSCM2 reception
- on and after MSCM3 reception

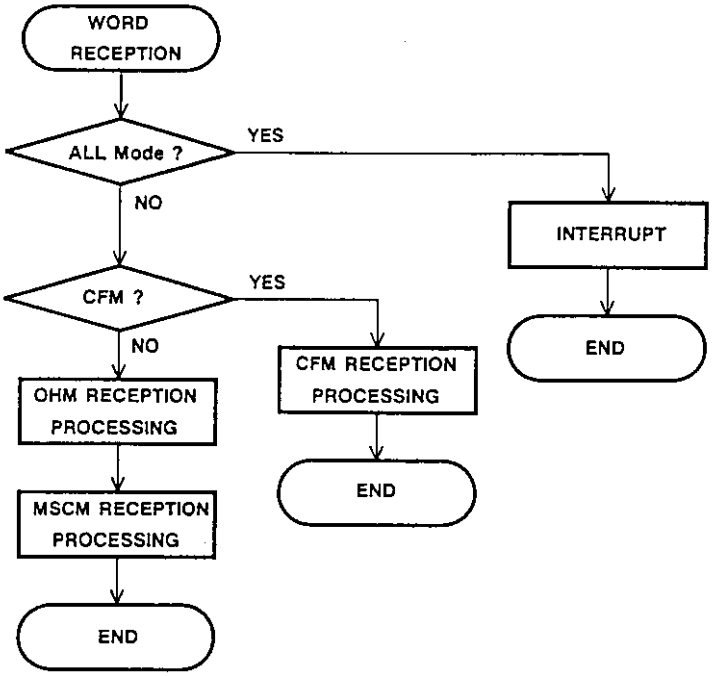
(4) CFM Mode

Interrupt Conditions:
- First CFM reception
- Different CFM detection

(5) ALL Mode

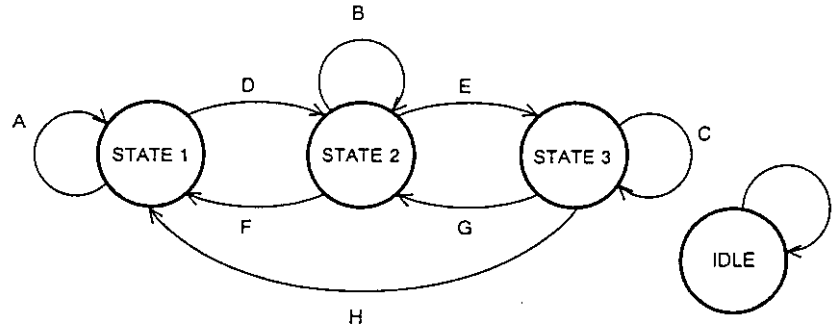
Interrupt Conditions:
- Every word reception

The flow chart of the data processing is described bellow:



The state diagram of each processing is described below.

(1) OHM RECEPTOIN PROCESSING



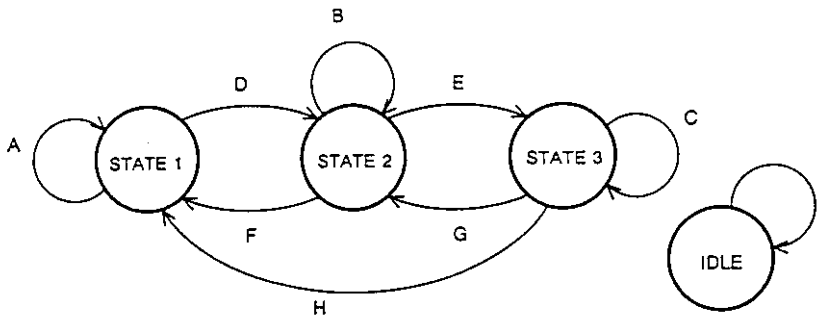
STATE 1: WAIT FOR SPM1
STATE 2: WAIT FOR SPM2
STATE 3: WAIT FOR END

```
IF (SPM = ON or OHM TRAIN = ON)
      CF ← ON                          /* CF: Compare Flag */
   NEXT STATE "STATE 1"

IF (SPM = OFF and OHM TRAIN = OFF)
   NEXT STATE "IDLE"
```

```
"STATE 1"
        IF (MESSAGE = SPM1)
                IF (SPM1r ≠ SPM1s) {
                    CF ← ON
                    SPM1s ← SPM1r
                }
                NEXT STATE "STATE 2"                    /* STATE TRANSITION D */
        ELSE
            NEXT STATE "STATE 1"                        /* STATE TRANSITION A */

"STATE 2"
        IF (MESSAGE = SPM1)
                IF (SPM1r ≠ SPM1s) {
                    CF ← ON
                    SPM1s ← SPM1r
                }
                NEXT STATE "STATE 2"                    /* STATE TRANSITION B */

        IF (MESSAGE = SPM2)
                IF (SPM2r ≠ SPM2s) {
                    CF ← ON
                    SPM2s ← SPM2r
                }
                AW ← 1                                  /* AW: Additional Word */

        IF (OHM TRAIN = ON)
                        IF (END FIELD = 1 and CF = ON) {
                            INTERRUPT ID ← OHM TRAIN
                            INTERRUPT
                            CF ← OFF
                            NEXT STATE "STATE 1"        /* STATE TRANSITION F */
                        }
                        ELSE
                            NEXT STATE "STATE 3"        /* STATE TRANSITION E */
                ELSE {
                        IF (CF = ON) {
                            INTERRUPT ID ← SPM
                            INTERRUPT
                            CF ← OFF
                        }
                    NEXT STATE "STATE 1"                /* STATE TRANSITION F */
                        }
            ELSE
                NEXT STATE "STATE 1"                    /* STATE TRANSITION F */

"STATE 3"
        IF (MESSAGE = SPM1)
                IF (SPMr ≠ SPMs) {
                    CF ← ON
                    SPMs ← SPMr
                }
```

```
        NEXT STATE "STATE 2"                    /* STATE TRANSITION G */

    IF (MESSAGE = SPM2)
        NEXT STATE "STATE 1"                    /* STATE TRANSITION H */

    IF (MESSAGE = MSCM)
        NEXT STATE "STATE 3"                    /* STATE TRANSITION C */

    IF (BCH ERROR)
        AW ← AW + 1
            IF (AW = 15)
                NEXT STATE "STATE 1"            /* STATE TRANSITION H */
            ELSE |
                CF ← ON
                OHMs(AW) ← OHMr
            |
                NEXT STATE "STATE 3"            /* STATE TRANSITION C */

    IF (MESSAGE = OHM and ≠ SPM1, SPM2, CFM)
            AW ← AW + 1
            IF (OHMr ≠ OHMs(AW)) |
                CF ← ON
                OHMs(AW) ← OHMr
            |
            IF (END FIELD =1 and CF = ON) {
                INTERRUPT ID ← OHM TRAIN

                INTERRUPT
                CF ← OFF
                NEXT STATE "STATE 1"            /* STATE TRANSITION H */
            |
            ELSE
                    IF (AW = 15)
                        NEXT STATE "STATE 1"    /* STATE TRANSITION H */
                    ELSE
                        NEXT STATE "STATE 3"    /* STATE TRANSITION C */
```

(2) MSCM RECEPTION PROCESSING



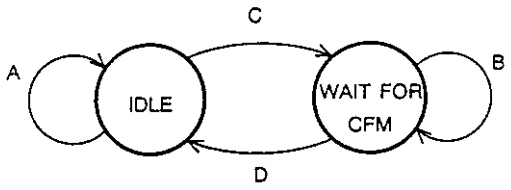
STATE 1: WAIT FOR MSCM1
STATE 2: WAIT FOR MSCM2
STATE 3: WAIT FOR ON AND AFTER MSCM3

```
IF (MSCM = ON)
    NEXT STATE "STATE 1"

IF (MSCM = OFF)
    NEXT STATE "IDLE"


"STATE 1"
        IF (MESSAGE = MSCM1)
                IF (((MIN CHECK = MIN1 or MIN1&2) and MIN1r = MIN1p)
                or MIN CHECK = OFF)
                    MSCM1s ← MSCM1r
                    NEXT STATE "STATE 2"                /* STATE TRANSITION D */
                ELSE
                    NEXT STATE "STATE 1"                /* STATE TRANSITION A */

        IF (MESSAGE = 1 WORD PAGE)
                IF ((MIN CHECK = MIN1 and MIN1r = MIN1p) or MIN CHECK = OFF) {
                    MSCM1s ← MSCM1r
                    INTERRUPT ID ← MSCM
                    MSCM ID ← 1 WORD

                    INTERRUPT
                    NEXT STATE "STATE 1"                /* STATE TRANSITION A */
                }

        IF (MESSAGE = ON AND AFTER MSCM2)
            NEXT STATE "STATE 1"                        /* STATE TRANSITION A */

"STATE 2"
        IF (MESSAGE = MSCM1)
                IF (((MIN CHECK = MIN1 or MIN1&2) and MIN1r = MIN1p)
```

```
                    or MIN CHECK = OFF)
                        MSCM1s ← MSCM1r
                        NEXT STATE "STATE 2"                /* STATE TRANSITION B */
                    ELSE
                        NEXT STATE "STATE 1"                /* STATE TRANSITION F */

                IF (MESSEGE = 1 WORD PAGE)
                    IF ((MIN CHECK = MIN1 and MIN1r = MIN1p)
                    or MIN CHECK = OFF) {
                        MSCM1s ← MSCM1r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 1 WORD
                        INTERRUPT
                        NEXT STATE "STATE 1"                /* STATE TRANSITION F */
                    }

                IF (MESSAGE = ON AND AFTER MSCM2)
                    IF (((MIN CHECK = MIN1 or MIN1&2) and MIN2r = MIN2p)
                    or MIN CHECK = OFF) {
                        MSCM2s ← MSCM2r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 2 WORD
                        INTERRUPT
                        NEXT STATE "STATE 3"                /* STATE TRANSITION E */
                    }
                    ELSE
                        NEXT STATE "STATE 1"                /* STATE TRANSITION F */

                ELSE
                    NEXT STATE "STATE 1"                    /* STATE TRANSITION F */

            "STATE 3"
                IF (MESSAGE = MSCM1)
                    IF (((MIN CHECK = MIN1 or MIN1&2) and MIN1r = MIN1p)
                    or MIN CHECK = OFF)
                        MSCM1s ← MSCM1r
                        NEXT STATE "STATE 2"                /* STATE TRANSITION G */
                    ELSE
                        NEXT STATE "STATE 1"                /* STATE TRANSITION H */

                IF (MESSEGE = 1 WORD PAGE)
                    IF ((MIN CHECK = MIN1 and MIN1r = MIN1p)
                    or MIN CHECK = OFF) {
                        MSCM1s ← MSCM1r
                        INTERRUPT ID ← MSCM
                        MSCM ID ← 1 WORD
                        INTERRUPT
                        NEXT STATE "STATE 1"                /* STATE TRANSITION H */
                    }

                IF (MESSAGE = ON AND AFTER MSCM2)
                    MSCM3s ← MSCM3r
```

```
                INTERRUPT ID ← MSCM
                MACM ID ← ON AND AFTER WORD 3
                INTERRUPT
                NEXT STATE "STATE 3"                    /* STATE TRANSITION C */

            ELSE
                NEXT STATE "STATE 1"                    /* STATE TRANSITION H */
```

(3) CFM RECEPTION PROCESSING




```
"IDLE"
        IF (MESSAGE = CFM)
            NEXT STATE "IDLE"                           /* STATE TRANSITION A */

        IF (CFM = ON)
            CF ← ON
            NEXT STATE "WAIT FOR CFM"                   /* STATE TRANSITION C */

"WAIT FOR CFM"
        IF (MESSAGE = CFM)
            IF (CFMr ≠ CFMs) {
                CF ← ON
                CFMs ← CFMr
            }
            IF (CF = ON) {
                INTERRUPT ID ← CFM
                INTERRUPT
                CF ← OFF
            }
            NEXT STATE "WAIT FOR CFM"                   /* STATE TRANSITION B */

        IF (CFM = OFF)
            NEXT STATE "IDLE"                           /* STATE TRANSITION D */
```

■ SAT Signal Reception and Transponding

The AK2336 has a on-chip SAT signal receiver and transponder. The receive SAT signal frequency is determined to specify one SAT frequency out of three by the control register.

The AK2336 does not support the SAT phase angle adjustment.

■ Serial Interface

Control Register, Status Register and Data Register of AK2336 are read through serial interface. The serial interface timing is shown in figure Fig-8.

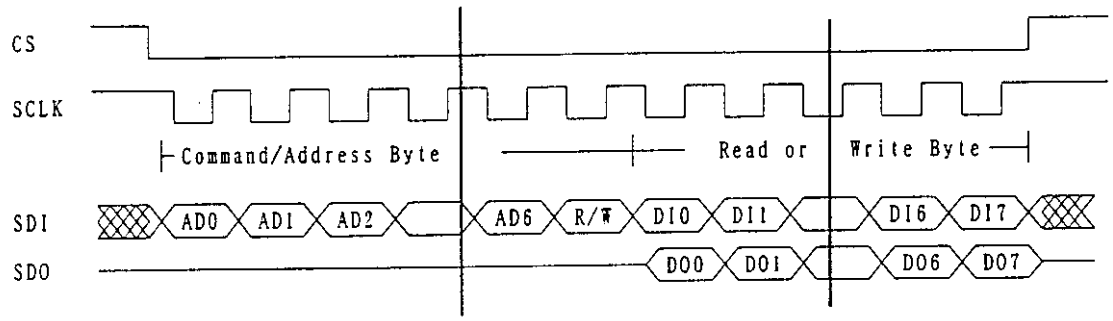


Fig-8 Serial Interface Timing 1

If SCLK is clocked continuously, AK2336 increments the address automatically and input/output next address data as shown in figure Fig-9.

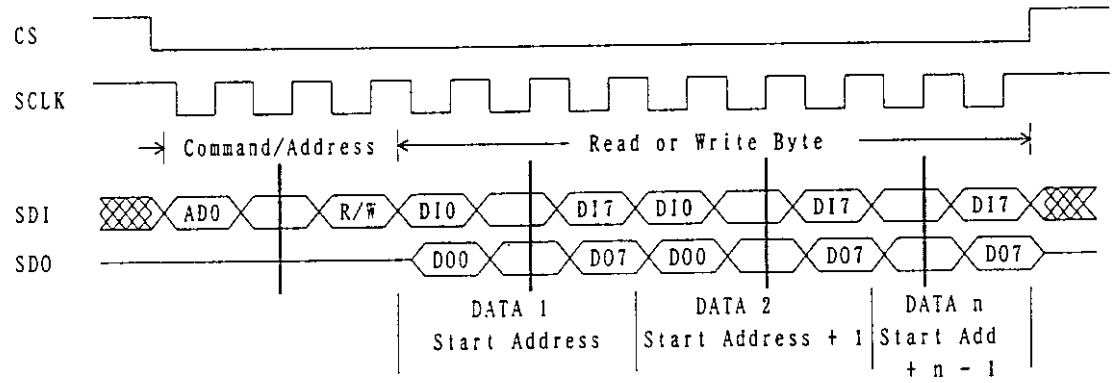


Fig-9 Serial Interface Timing 2

* Parallel Interface also has the same feature.

■ Uncommitted DAC／OP-AMP／Timer

DAC

The AK2336 has three on-chip 8 bits linear DACs.

Resolution : 8bit linear
Output Voltage : 0.02×VDD(00)～0.98×VDD(FF)
DNL : ≦ ±1/2 LSB (No Load)
Settling Time : ≦ 10μs
Output Current : I_{OUT}=50μA(MAX)

OP-AMP

The AK2336 has an uncommitted OP-AMP (AMP7).

Timer

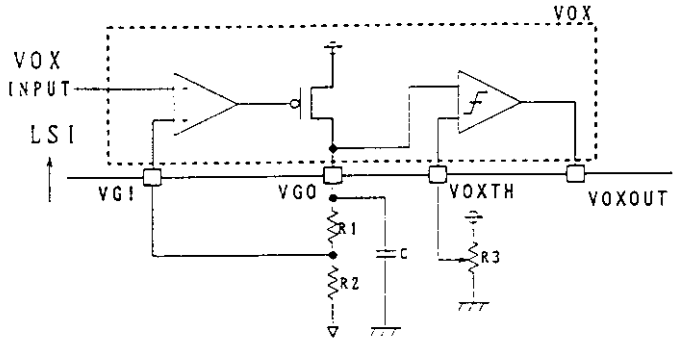
The AK2336 has two uncommitted 8 bits Timers. The main clock and preset value of the timer are set from the control register. Also, the timers have a repeat mode. For example: The initial timer value is set to 50. At the point that the timer reaches 0, it generates an interrupt and TEXPI/2 pin goes to "Hi". At a same time, it resets to 50 and starts to count down automatically. TEXPI/2 pin goes to "Lo" after one main clock cycle.
Note, the interrupt line has to stay in the interrupt state until the event register with the timer are read.

T1: Clock ..... 12.5kHz, 6.25kHz, 3.125kHz or 1.5625kHz
Counter Value ..... 0～255

T2: Clock ..... 781.25Hz, 390.625Hz, 195.3125Hz or 97.65625Hz
Counter Value ..... 0～255

■ VOX

The VOX circuit of the AK2336 is shown bellow. The sensitivity, attack time and recovery time of the circuit are defined by external resistors and a capacitor.



Operation; The signal at VGO is described as belows:

$$(1/2\ VDD) + |(R1+R2)/R2| * V_{O-P}$$

V_{O-P} described above is the voltage of VOX INPUT's V_{O-P}.
And VOXOUT is determined by comparing VGO with VOXTH that is set by R3.
ATTACK/DECAY TIME are under the control of external capacitor C.

■Automatic Frequency Control (AFC)

AK2336 provides a controlling voltage for VCXO. The μC determines the control voltage from counts of the 1.2MHz and the 2nd IF (typ 450kHz) clocks. The μC writes the control voltage of the D/A converter to the register. AK2336 D/A converts the register value and output it. AK2336 provides the following for AFC. Figure in the next page shows the block diagram of the AFC.

1. AFC block diagram description

- AFC Input Buffer for the 2nd IF(450kHz)
- 4bit Shift Register(450kHz)
- 2bit Shift Register(1.2MHz)
- AFC (16bit) counter clocked by 450kHz
- 1 sec counter clocked by 1.2MHz
- 8 bit D/A converter

2. Operational sequence

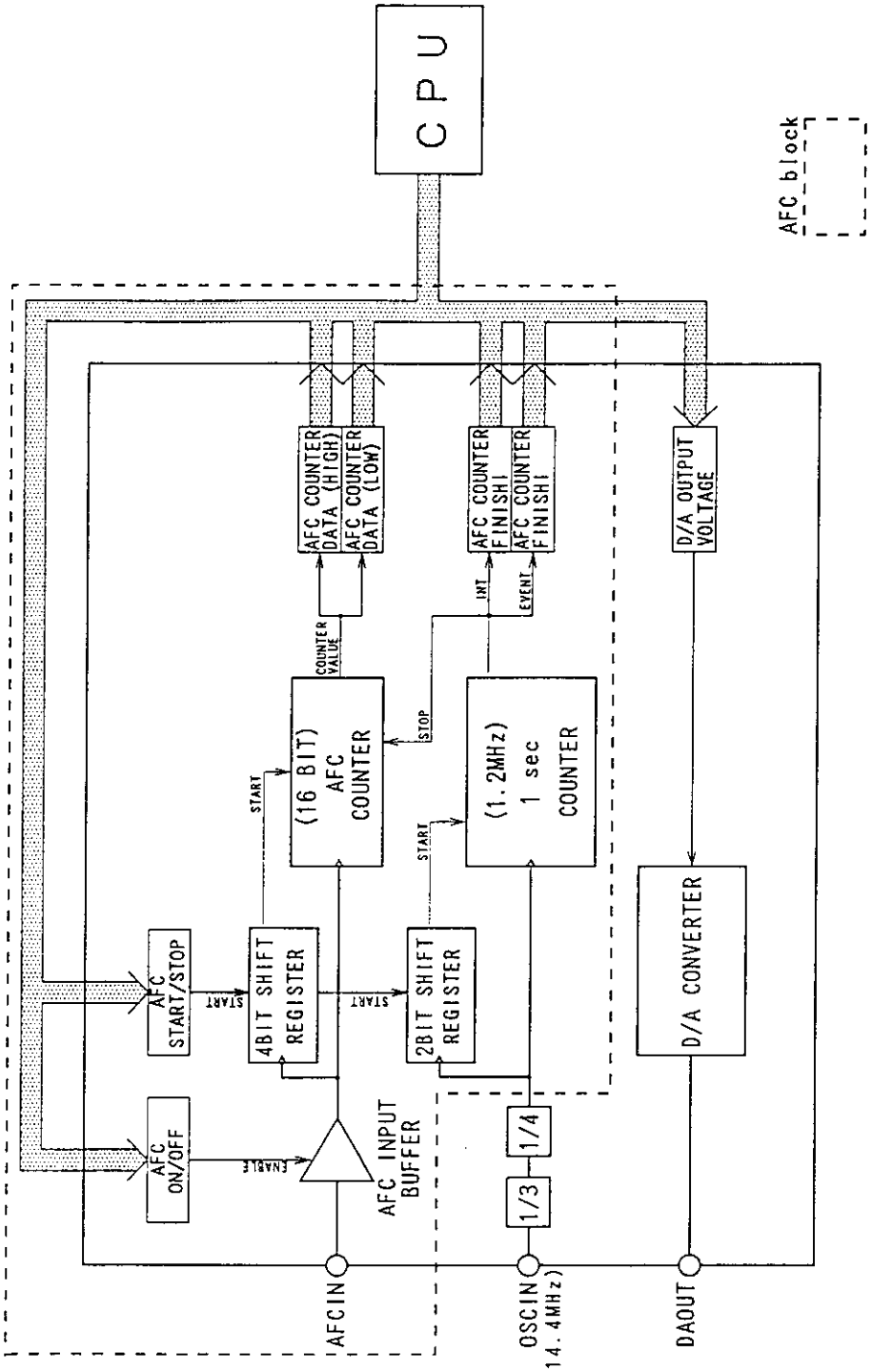
——— Pre - SET ———

1 Power ON.
2 System Reset.
3 Enable D/A and AMP7.
4 Set the D/A output to the center level.
5 Enable AFC INPUT BUFFER(by setting the AFC ON/OFF bit = "1"). *

——— AFC START ———

①Start AFC (by setting the AFC START/STOP bit = "1").
②After four (4) 450kHz clocks, AFC COUNTER and 2 BIT SHIFT REGISTER starts.
③And then after two (2) 1.2MHz clocks, 1 sec COUNTER starts.
④After 1 sec, AFC COUNTER stops and generates a interrupt to μC.
⑤μC reads the EVENT REGISTER and then reads AFC COUNTER DATA register.
⑥AK2336 stops AFC automatically (by setting AFC START/STOP bit = "0") and resets the counter value.
⑦In consideration of the counter value, μC writes the control voltage of the D/A converter to the register. Go to ①.
⑧Disable AFC (by setting the AFC ON/OFF bit = "0").

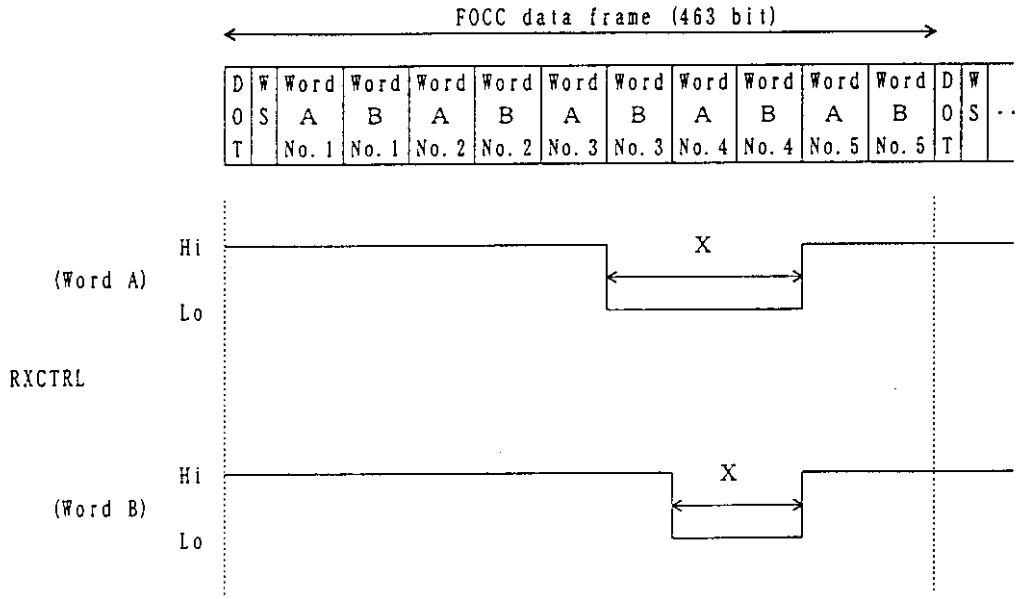
*AFC INPUT BUFFER must be enabled at least 5ms prior to the AFC start.


CPU
AFC block
AFC COUNTER DATA (HIGH)
AFC COUNTER DATA (LOW)
AFC COUNTER FINISHI
AFC COUNTER FINISHI
D/A OUTPUT VOLTAGE
INT
EVENT
COUNTER VALUE
STOP
START
(16 BIT) AFC COUNTER
(1.2MHz) 1 sec COUNTER
AFC START/STOP
4BIT SHIFT REGISTER
2BIT SHIFT REGISTER
D/A CONVERTER
AFC ON/OFF
ENABLE
AFC INPUT BUFFER
1/4
1/3
AFCIN
OSCIN (14.4MHz)
DAOUT

■DISCONTINUOUS RECEPTION (DRX)

Regarding to the FOCC, AK2336 performs bit-wise majority decision on repeated five words normally. However, when DISCONTINUOUS RECEPTION(DRX) is set from the control register(address 01), if the first three* received data of the five words are matched, receive data is settled without receiving the rest data. At the same time AK2336 generates a interrupt and RXCTRL pin goes to "Lo". Therefore, RF block in the system could be power down. And then RXCTRL pin go to "Hi" after the time(X) that is set from the control register(address 26) and AK2336 generates a interrupt. If the first three data word are not matched, AK2336 performs bit-wise majority decision normally. RXCTRL pin status is also controlled from the command register(address 66/67) by force.

*The first three or two: that is set from the control register.

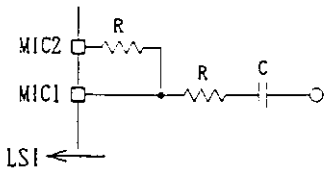


Note:When DRX is set during FOCC reception, DRX takes effect from the next frame data.
At Narrow analog mode, RXCTRL pin is fixed with "Hi" level.

Application Circuit Example

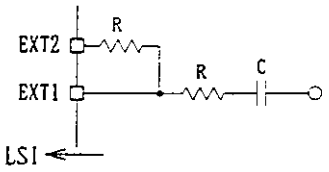
External circuit examples

1.AMP1



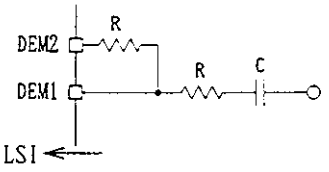
R: 100KΩ
C: 0.1μF

2.AMP2



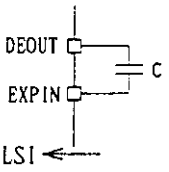
R: 100KΩ
C: 0.1μF

3.AMP3/8



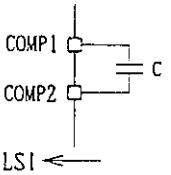
R: 100KΩ
C: 0.1μF (AMP3)
0.33μF (AMP8)

4.AC Coupling Capacitor



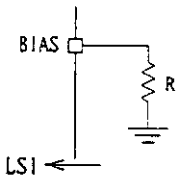
C: 0.047μF ±50%

5.Capacitor For Compressor



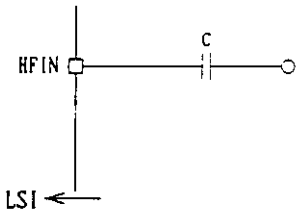
C: 0.047μF ±50%

6. Bias-current Setting Resistor



R: 61KΩ (VDD=3V±10%) ±5%
R: 100KΩ (VDD=5V±10%) ±5%

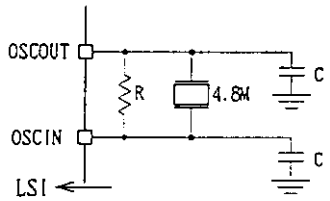
7. HFIN Input



C: 0.1μF ±20%

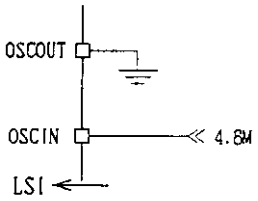
8. Main Clock Input

(1) Crystal Oscillator

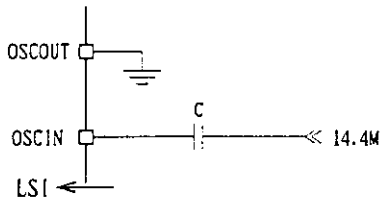


C: 22pF ±20%
R: 1MΩ

(2) 4.8M Input

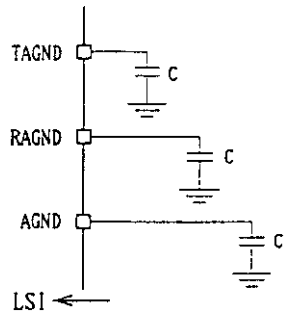


(3)14.4M Input



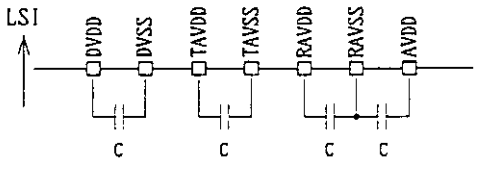
C: 100pF ±20%

9.AGND Stabilization Capacitor



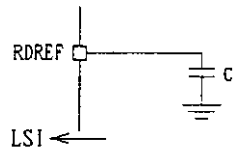
C: 1μF (≧0.8μF)

10.Power Supply Stabilization Capacitor



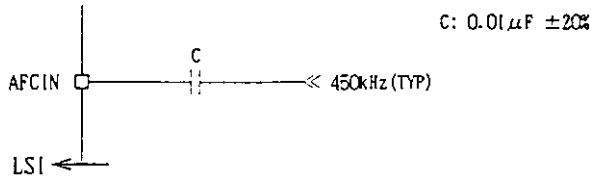
C: 0.1μF

11.CMP3 Capacitor For Offset Cancellation



C: 1μF ±20%

12.AFC 2nd IF signal input



Supplement

■Analog Characteristics that Depend on the Power Supply Voltage

Analog characteristics in the AK2336 data sheet are specified at VDD=3V.
Analog characteristics described below are in proportion to the supply voltage.

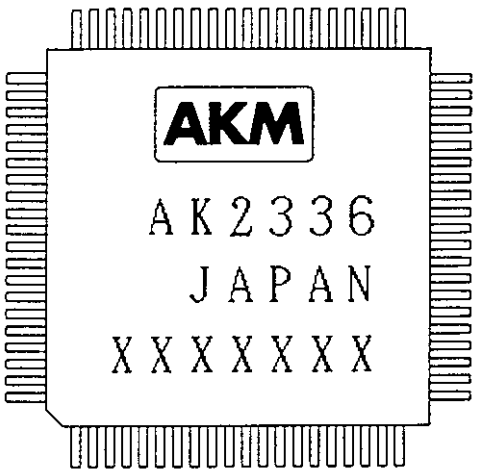
Difference from VDD=3.0V : 20log(VDD/3) [dB]

Item	VDD=3.0V	VDD=4.0V	VDD=5.0V
Compandor Unity Gain Level (TYP)	-12.0dBV	-9.5dBV	-7.56dBV
Limiter Level (TYP)	-8.2dBV	-5.7dBV	-3.76dBV
SAT Output Level (TYP)	-25.2dBV	-22.7dBV	-20.76dBV
Data (AMPS/TACS) Output Level (TYP)	-13.2dBV	-10.7dBV	-8.76dBV
Data (NAMPS) Output Level (TYP)	-34.3dBV	-31.8dBV	-29.9dBV
Data (NTACS) Output Level (TYP)	-32.3dBV	-29.8dBV	-27.9dBV
DTMF Output Level (TYP)	-13.2dBV	-10.7dBV	-8.76dBV
SAT Detect Level (MIN)	-35.2dBV	-32.7dBV	-30.76dBV
DAC Output Level (TYP)	0.06V～2.94V	0.08V～3.92V	0.10V～4.90V

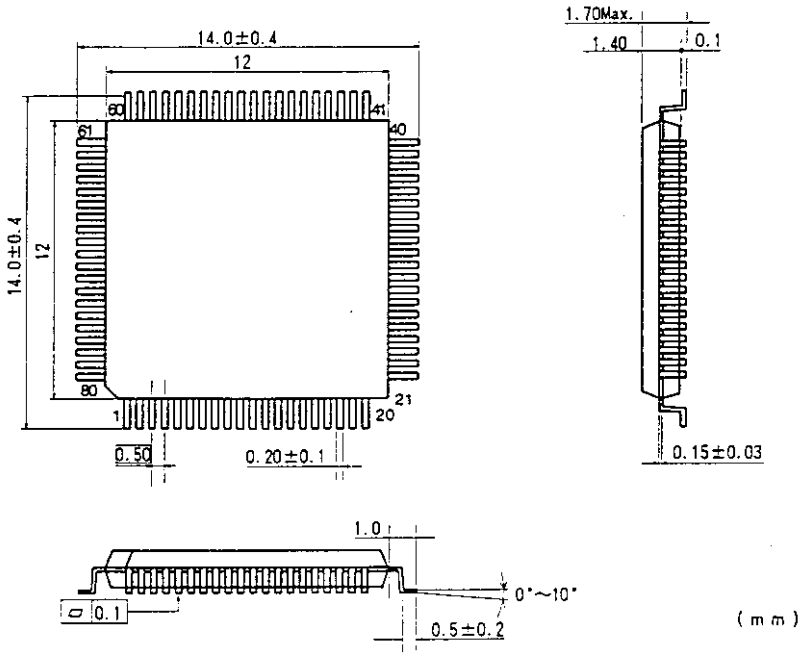
Package

■ Marking

(1) Pin #1 indication
(2) Date Code : XXXXXX (7 Digits)
(3) Marketing Number : AK2336
(4) Country of Origin : JAPAN
(5) Asahi Kasei Logo



■ Package Outline



Spec No.	IS-971066

S P E C I F I C A T I O N

NJM2904V (TE2)

JULY 11, 1997
NEW JAPAN RADIO CO., LTD.
IC QUALITY ASSURANCE DIVISION
DOCUMENT CONTROL SECTION

AUTHORIZED Y. AIDA

[SHPPING INSPECTION]

SHPPING LOT SHOULD BE INSPECTED FOLLOWING TABLE
SAMPLING ANSI/ASQC Z1.4-1993 (EQUAL TO MIL-STD-105D)
AMBIENT TEMPERATURE 25±3℃
HUMIDITY ≦75%

INSPECTION ITEM	QUALITY CHARACTERISTICS	LEVEL	A Q L
MAJOR DEFECT	OPEN , SHORT , OPPOSITE AND NO MARK	II	0.25
EXTERNAL VISUAL	LEAD PLATING , MARKING	II	2.5
ELECTRICAL CHARACTERISTICS	PER APPLICABLE ELECTRIC TEST SPECIFICATION	II	0.65

[A STATE OF OZONE DEPLETING CHEMICALS]

《No object ODC》
Those deviceis are processed and assembled without ODC, and do not contain any ODC.

OBJECT ODC :

Flon (Freon)	CFC-11, -12, -113, -114, -115
H a l o n	Halon-1211, -1301, -2402
Other Flon	CFC-13, -111, -112, -211, -212, -213, -214, -215, -216, -217
Carbon Tetrachloride	
1.1.1-Trichloethane (Methyl Chloroform)	

[A STATE OF SPECIAL BROMIC FRAMERETARDANT CHEMICALS]

《No Object Chemical》
Those deviceis are not include without following chemicals.

OBJECT CHEMICAL :

P B B O s	PBDO, PBDPO, PBDE, PBDPE, OBDO, DBDO, TBDO
P B B s	

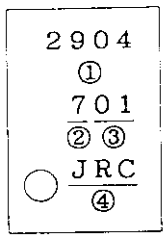
NJM2904V

[DUAL SINGLE-SUPPLY OPERTIONAL AMPLIFIERS]

[STRUCTURE]
EQUIVALENT CIRCUIT, CONNECTION INFORMATION
PACKAGE OUTLINE, PACKING SPECIFICATION,
SOLDERING METHOD

[NOTE]
For this device, soldering technique is recommended Reflow.

MARKING



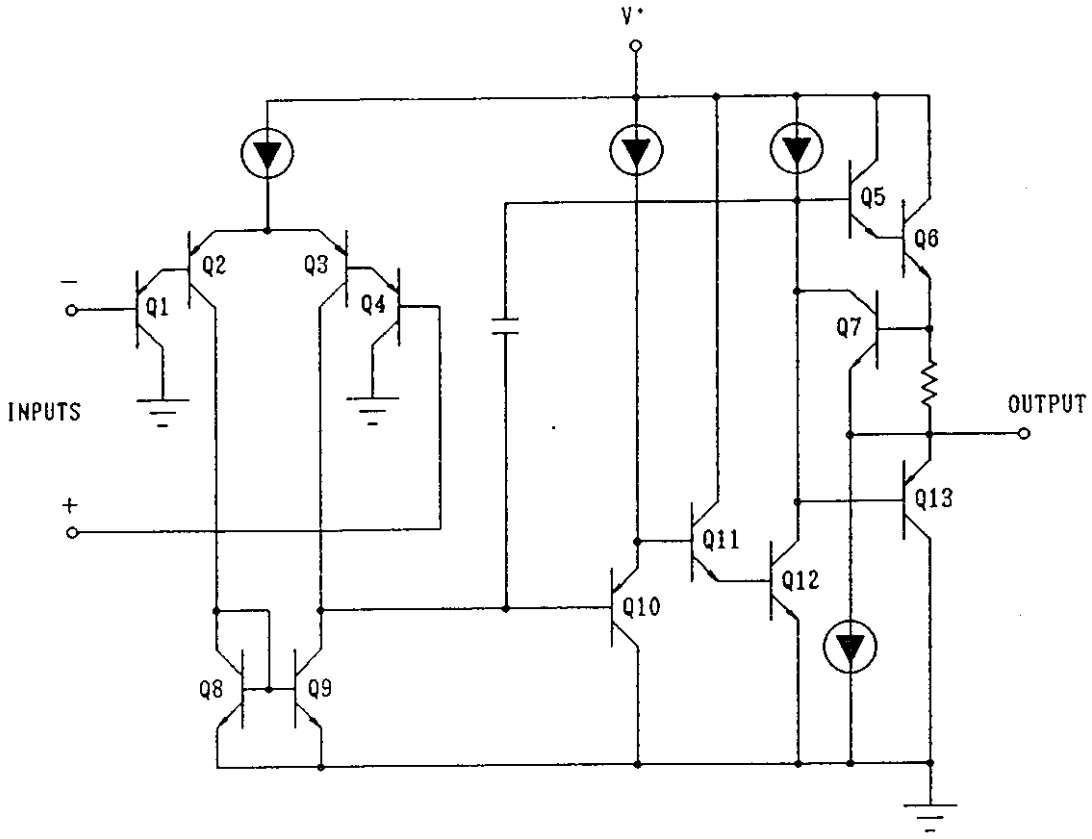
①DEVICE No.
②LAST DIGIT OF THE CALENDAR YEAR
③LOT No.
④MANUFACTURE'S SYMBOL

ABSOLUTE MAXIMUM RATINGS Ta=25°C

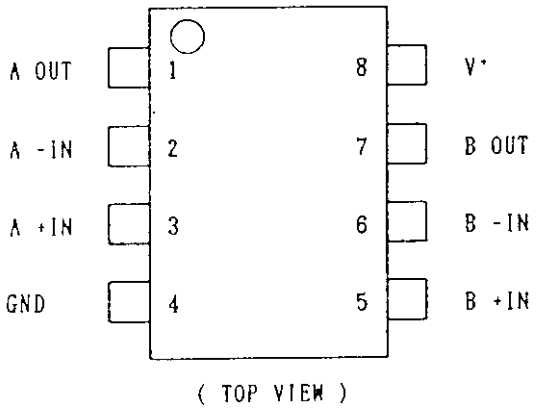
SUPPLY VOLTAGE..... 32 or ±16 [V]	OPERATING TEMPERATURE RANGE
INPUT VOLTAGE ..... -0.3 to +32 [V]	-40 ~ +85°C
POWER DISSIPATION..... 250 [mW]	STORAGE TEMPERATURE RANGE
DIFFERENTIAL INPUT VOLTAGE... 32 [V]	-50 ~ +125°C

ELECTRICAL CHARACTERISTICS $V^+=5V$, Ta=25°C

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S=0\Omega$	V_{IO}	—	—	7	mV
Input Bias Current		I_B	—	—	250	nA
Input Offset Current		I_{IO}	—	—	±50	nA
Input Common-Mode Voltage Range		V_{ICM}	3.5	—	—	V
Supply Current	$R_L=\infty$	I_{CC}	—	—	1.2	mA
Large Signal Voltage Gain	$R_L\geqq 2k\Omega$	A_V	—	100	—	dB
Output Voltage Swing	$R_L=2k\Omega$	V_{OM}	3.5	—	—	V
Common Mode Rejection Ratio		CMR	—	85	—	dB
Supply Voltage Rejection Ratio		SVR	—	100	—	dB
Channel Separation	f=1kHz to 20kHz (Input Referred)	CS	—	120	—	dB
Output Source Current	$V_{IN}^+=1V$, $V_{IN}^-=0V$	I_{SOURCE}	20	—	—	mA
Output Sink Current	$V_{IN}^+=0V$, $V_{IN}^-=1V$	I_{SINK}	8	—	—	mA

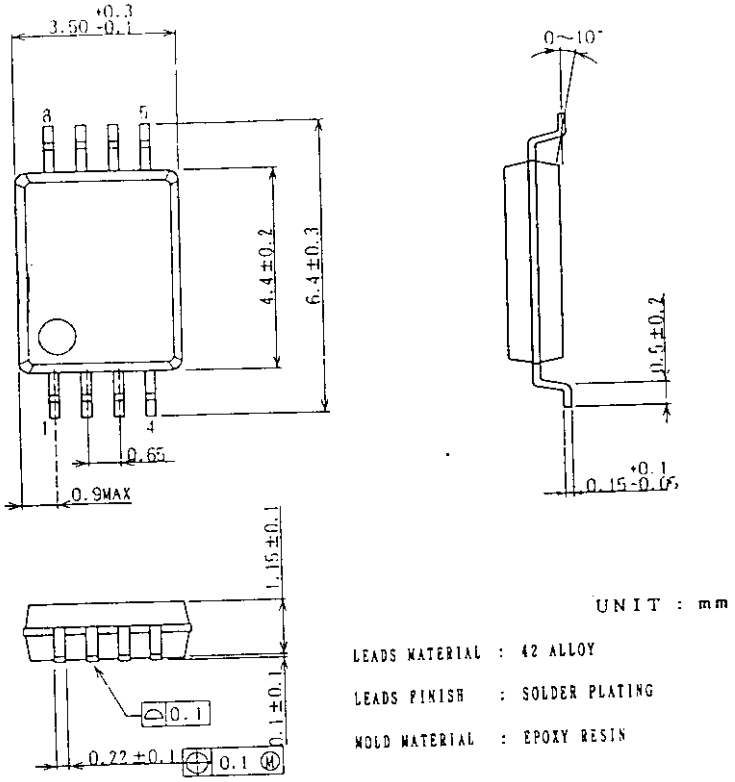


EQUIVALENT CIRCUIT



CONNECTION INFORMATION

《SSOP-8PIN PACKAGE OUTLINE》



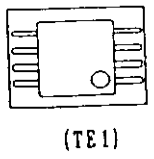
Applicant: Shintom Co., Ltd. Transmitter Type: BFYM3047

《SSOP-8PIN PACKING SPECIFICATION》

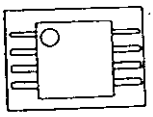
UNIT mm

【TAPING DIMENSION】

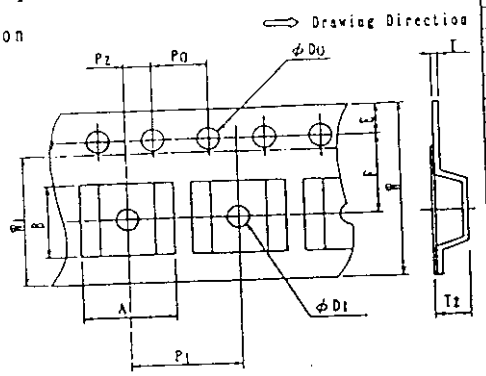
Insert direction



(TE1)



(TE2)

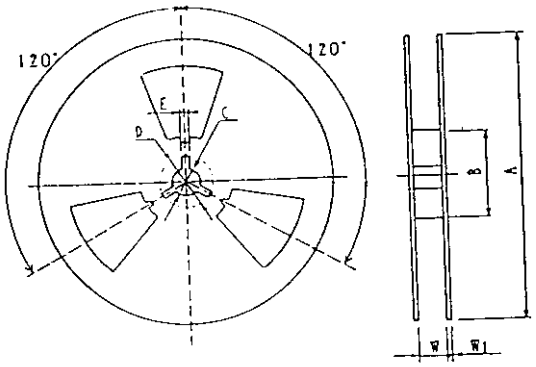


SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	DIMENSION
B	3.9±0.1	DIMENSION
D0	1.55±0.05	
D1	1.55±0.1	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T1	2.2	
W	12.0±0.3	
W1	9.5	DIMENSION

※MATERIAL FOR A TAPE : Conductive PVC

Based on device No. of cover.

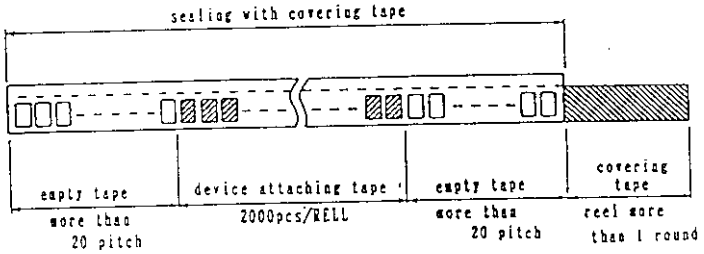
【REEL DIMENSION】



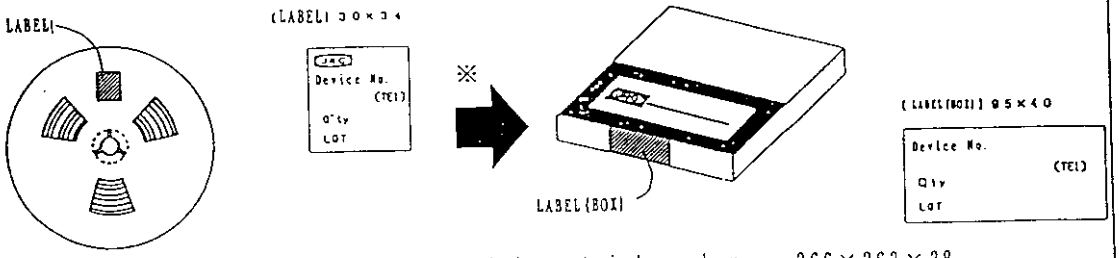
SYMBOL	DIMENSION
A	φ255±1
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	14±1.5
W1	2±0.2

※MATERIAL:PLASTIC

【TAPING SPECIFICATION】



【PACKING STAGE】



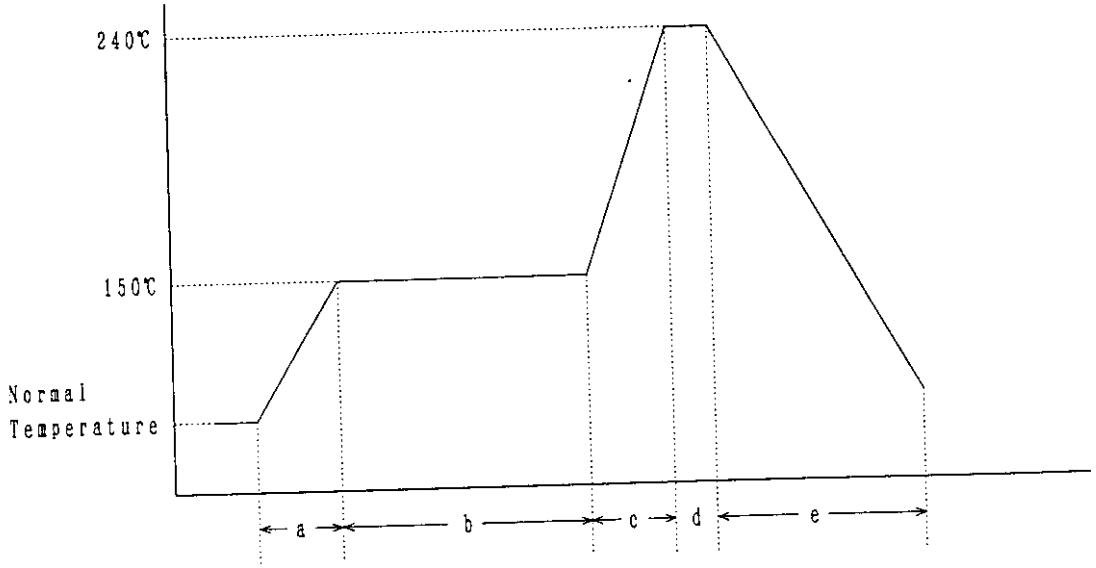
φ255×18W

※The reel is put into a box 266×263×28

Emboss Carrier Taping

Recommended Soldering Method

Soldering temperature profile is as follows:



a:Temperature ramping rate 1℃～7℃/s
b:Pre-heating Temperature:150℃
Time : 60～120s
c:Temperature ramping rate 1℃～7℃/s
d:Main heating Temperature:under 240℃
Time:within 10s
e:Ramping rate under 7℃/s

The temperature indicates the surface of mold package.

At above reflow soldering condition
It is no problem to twice reflow soldering at above condition.

☆MANUFACTURING PROCESS

Wafer Process

- New Japan Radio Co., Ltd.

  IC Factory. (JAPAN)

Assembly Process

- Saga Electronics Co., Ltd.

  Saga Factory. (JAPAN)

1. Taping standards for surface mount devices.

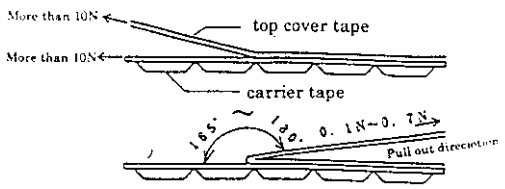
①Tensile strength of carrier tape More than 10N.

②Tensile strength of top cover tape More than 10N.

③Adherence of top cover tape 0.1N~0.7N.

(Angle=165~180° Speed=300mm/min.)

④Conform to JIS C 0806



2.Ultrasonic cleaning standards

①Frequency 28~40kHz(Secure the device not to vibrate)

②Output Less than a 15W/liter

③Duration Shorter than 60 seconds

④Cleaners.

Alternative Freon or alcoholic cleaning.

: IPA(Isopropyl alcohol)

HCFC-225

Water soluble cleaners.

: Surface active agents (Clean through 750H)

Hydrocarbon (Techno cleaner 335)

Fatty alcohol (Pine alpha ST-100S)

Alkali saponifier (Aqua cleaner 240)

Applicant: Shintom Co., Ltd. Transmitter Type: BFYM3047

RELIABILITY REPORT

Device No. NJM2904V

TEST RESULTS

TEST	MIL STANDARD	CONDITIONS	SAMPLE SIZE	FAILURES	CHECK ITEM
High Temperature Storage	MIL STD883 1008	Cond. B, 125℃, 1000h	45	0	1
humidity	MIL STD883 103B	85℃, 85%, 1000h	45	0	1
Steady State Life	N/A	125℃, V^+=32V, 1000h	45	0	1
Temperature Humidity - Bias	N/A	85℃, 85%, V^+=32V, 1000h	45	0	1
Pressure Cooker	N/A	121℃, 2.03×10^5Pa, 100h	45	0	1
Soldering Heat (Reflow)	MIL STD750 2031	MAX 260℃, 10s	45	0	1
Thermal Shock	MIL STD750 1011	Cond. A, 0℃, 5min～100℃, 5min 10cycles	45	0	1, 2
Temperature Cycling	MIL STD750 1010	-50℃, 30min～25℃, 5min～125℃, 30min 100cycles	45	0	1, 2
Solderability	MIL STD750 2003	230℃, 5s with flux	45	0	2

1. ELECTRICAL CHARACTERISTICS 2. OUTWARD

FAILURE CRITERIA (End Point Electrical Parameters)

PARAMETER	CONDITION	CRITERIA
Electrical characteristics is shown in the specification. Testing will be done for the parts which has either maximum or minimum value.		The failure criteria is out of the limit of electrical characteristics shown in the specification.
Outward	Visual Inspection	Resin crack, Resin Break, Terminal Break, Vanished Mark.
Solderability	Visual Inspection	The case terminal is coated with solder under 95% of soldering area.

Applicant: Shintom Co., Ltd. Transmitter Type: BFYM3047

E. S. D. DATA

PRODUCT : NJM2904

*THIS TEST WAS CONFORMED TO EIAJ ED-4701 (TEST METHOD C-111, TEST CONDITION CODE A).

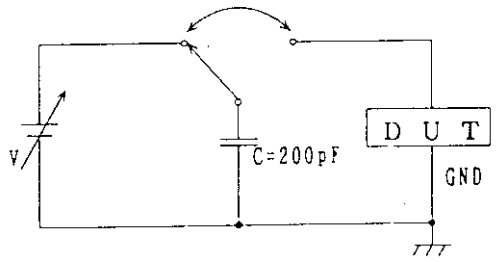
+SURGE

pin/v	100	150	200	250	300	350	400	450	500	550	600
A OUTPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
A -INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	1/5	1/5
A +INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	2/5	2/5	2/5
GND	CONNECT GND (CF. TEST CIRCUIT)										
B +INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	4/5	4/5	4/5
B -INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	2/5	4/5	4/5
B OUTPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
V+	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5

-SURGE

pin/v	-100	-150	-200	-250	-300	-350	-400	-450	-500	-550	-600
A OUTPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
A -INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
A +INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
GND	CONNECT GND (CF. TEST CIRCUIT)										
B +INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
B -INPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
B OUTPUT	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5
V-	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5	0/5

TEST CIRCUIT



2SC4903

Silicon NPN Bipolar Transistor

Application

VHF & UHF wide band amplifire

Features

- High gain bandwidth product
  f_T = 6 GHz typ
- High gain, low noise figure
  PG = 12.0 dB typ,
  NF = 1.6 dB typ at f = 900 MHz

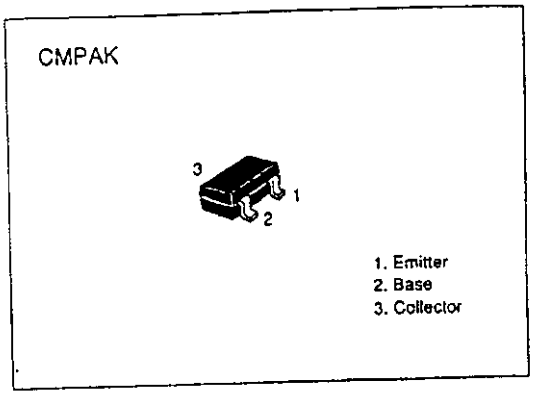


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	20	V
Collector to emitter voltage	V_{CEO}	12	V
Emitter to base voltage	V_{EBO}	2	V
Collector current	I_C	30	mA
Collector power dissipation	P_C	100	mW
Junction temperature	T_j	150	°C
Storage temperature	Tstg	–55 to +150	°C

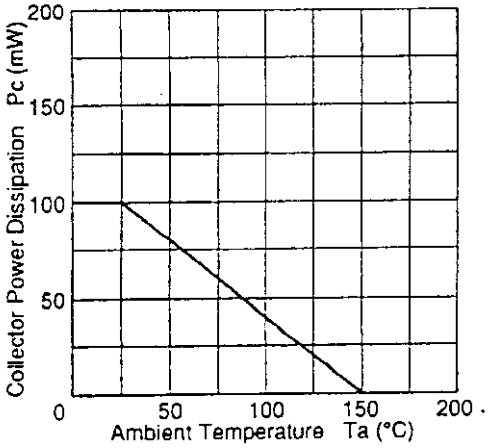
Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Collector cutoff current	I_{CBO}	—	—	10	μA	V_{CB} = 20 V, I_E = 0
	I_{CEO}	—	—	1	mA	V_{CE} = 12 V, R_{BE} = ∞
Emitter cutoff current	I_{EBO}	—	—	10	μA	V_{EB} = 2 V, I_C = 0
DC current transfer ratio	h_{FE}	50	120	250		V_{CE} = 5 V, I_C = 10 mA
Output capacitance	Cob	—	0.6	1.0	pF	V_{CB} = 5 V, I_E = 0, f = 1 MHz
Gain bandwidth product	f_T	4.0	6.0	—	GHz	V_{CE} = 5 V, I_C = 10 mA
Power gain	PG	9.5	12.0	—	dB	V_{CE} = 5 V, I_C = 10 mA, f = 900 MHz
Noise figure	NF	—	1.6	3.0	dB	V_{CE} = 5 V, I_C = 5 mA, f = 900 MHz

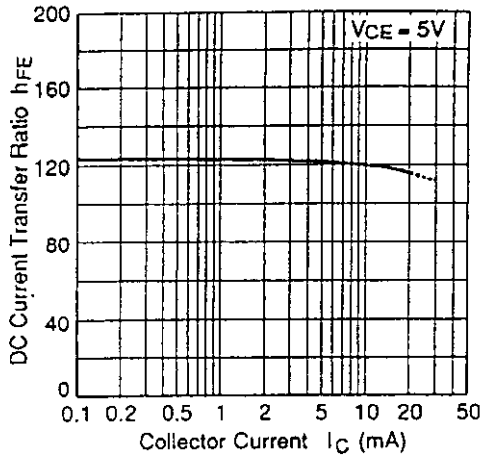
Marking for 2SC4903 is "YL–".
Attention: This is electrostatic sensitive device.

2SC4903

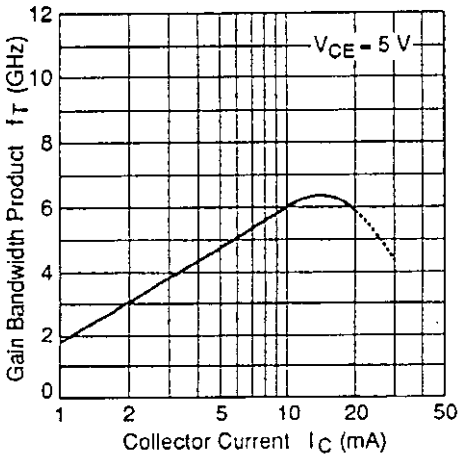
Maximum collector power dissipation curve



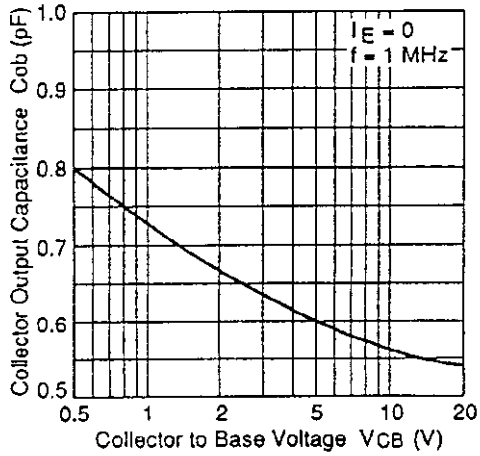
DC current transfer ratio vs. collector current



Gain bandwidth product vs. collector current

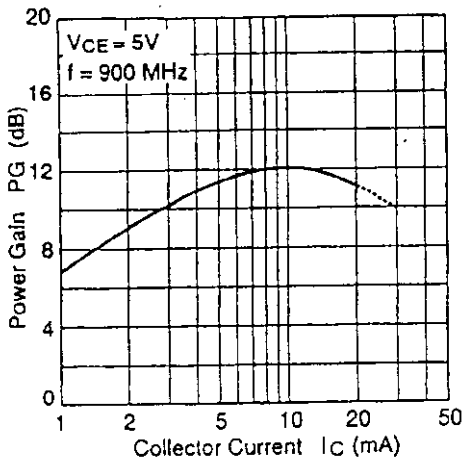


Collector output capacitance vs. collector to base voltage

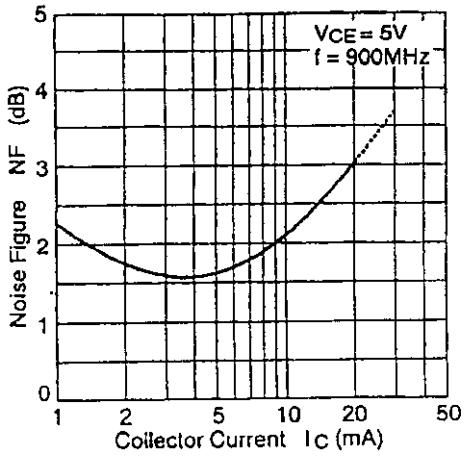


2SC4903

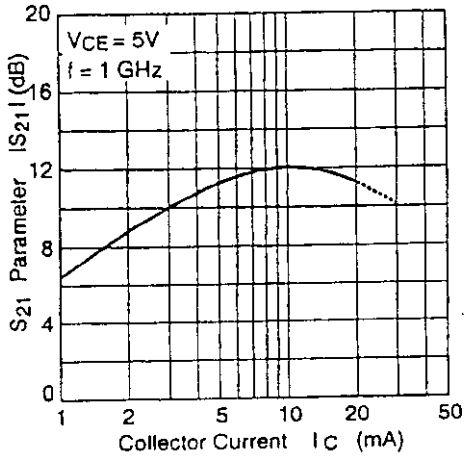
Power gain vs. collector current



Noise figure vs. collector current

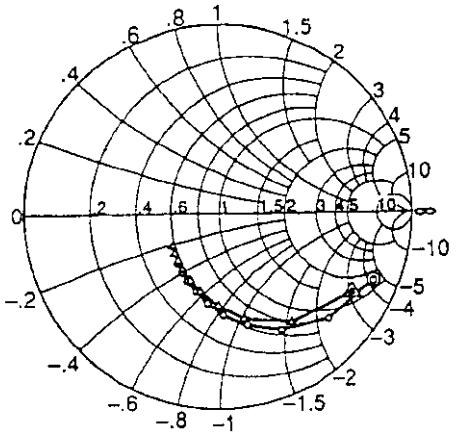


S21 parameter vs. collector current



2SC4903

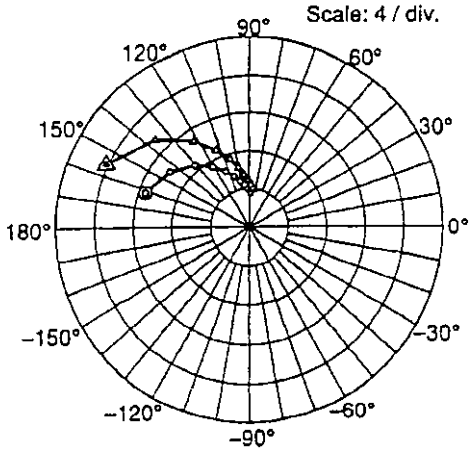
S11 parameter vs. frequency



Condition: V_{CE} = 5 V , Zo = 50 Ω
100 MHz to 1000 MHz (100 MHz step)
(IC = 5 mA)
(IC = 10 mA)

S21 parameter vs. frequency

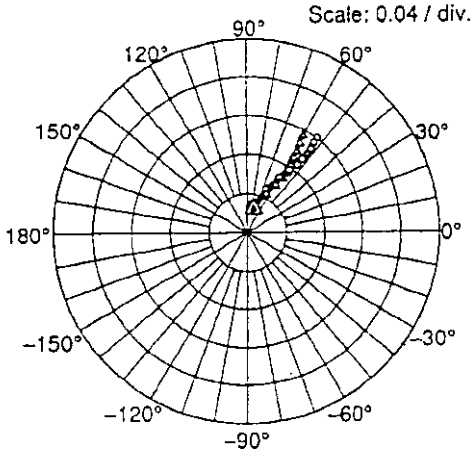
Scale: 4 / div.



Condition: V_{CE} = 5 V , Zo = 50 Ω
100 MHz to 1000 MHz (100 MHz step)
(IC = 5 mA)
(IC = 10 mA)

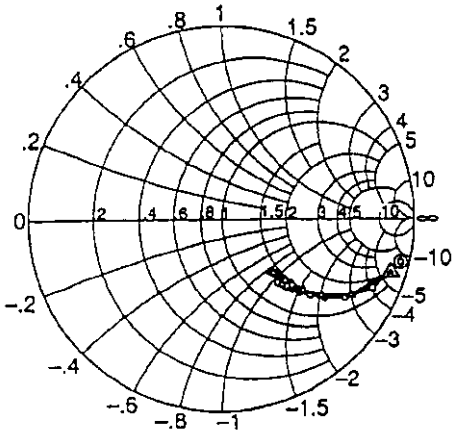
S12 parameter vs. frequency

Scale: 0.04 / div.



Condition: V_{CE} = 5 V , Zo = 50 Ω
100 MHz to 1000 MHz (100 MHz step)
(IC = 5 mA)
(IC = 10 mA)

S22 parameter vs. frequency



Condition: V_{CE} = 5 V , Zo = 50 Ω
100 MHz to 1000 MHz (100 MHz step)
(IC = 5 mA)
(IC = 10 mA)

Table 3 S Parameter (V_{CE} = 5 V, I_C = 5 mA, Z_O = 50 Ω, Emitter common)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	0.872	–23.3	11.28	161.2	0.0266	77.9	0.956	–13.4
200	0.777	–43.6	10.03	144.3	0.0493	67.3	0.862	–24.4
300	0.672	–62.0	8.59	130.8	0.0661	60.2	0.759	–32.4
400	0.586	–75.7	7.36	121.0	0.0777	56.0	0.672	–37.4
500	0.517	–88.0	6.34	112.8	0.0866	53.6	0.604	–40.7
600	0.462	–98.0	5.52	106.4	0.0941	53.1	0.553	–43.0
700	0.417	–107.3	4.88	101.1	0.102	52.5	0.514	–44.6
800	0.384	–115.9	4.39	96.5	0.108	52.7	0.483	–46.0
900	0.359	–122.7	3.97	92.2	0.115	53.3	0.460	–46.9
1000	0.336	–130.8	3.63	88.5	0.121	53.4	0.441	–48.3

Table 4 S Parameter (V_{CE} = 5 V, I_C = 10 mA, Z_O = 50 Ω, Emitter common)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100	0.798	–30.5	16.22	155.6	0.0254	74.9	0.921	–17.5
200	0.666	–56.4	13.39	136.1	0.0442	63.8	0.780	–30.3
300	0.550	–76.4	10.76	122.3	0.0569	58.9	0.652	–37.3
400	0.470	–90.8	8.80	113.0	0.0663	57.1	0.561	–41.0
500	0.412	–104.2	7.39	105.6	0.0741	56.5	0.500	–43.1
600	0.373	–114.0	6.33	100.3	0.0821	57.2	0.456	–44.1
700	0.345	–123.6	5.53	95.5	0.0899	57.9	0.425	–44.9
800	0.322	–131.5	4.91	91.6	0.0973	58.5	0.401	–45.4
900	0.307	–138.7	4.41	87.8	0.106	59.4	0.384	–46.0
1000	0.294	–145.5	4.02	84.8	0.114	59.9	0.371	–46.8

DATA SHEET

NEC

SILICON TRANSISTOR
2SC5015

HIGH FREQUENCY LOW NOISE AMPLIFIER
NPN SILICON EPITAXIAL TRANSISTOR
4 PINS SUPER MINI MOLD

FEATURES

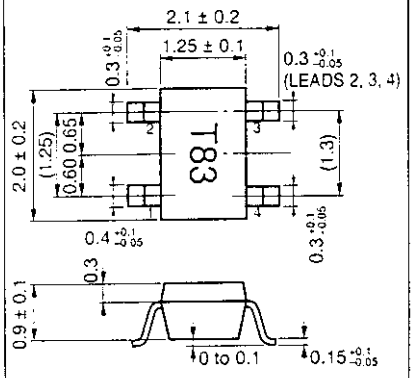
- Small Package
- High Gain Bandwidth Product (f_T = 12 GHz TYP.)
- Low Noise, High Gain
- Low Voltage Operation

ORDERING INFORMATION

PART NUMBER	QUANTITY	PACKING STYLE
2SC5015-T1	3 Kpcs/Reel.	Embossed tape 8 mm wide. Pin3 (Base), Pin4 (Emitter) face to perforation side of the tape.
2SC5015-T2	3 Kpcs/Reel.	Embossed tape 8 mm wide. Pin1 (Collector), Pin2 (Emitter) face to perforation side of the tape.

* Please contact with responsible NEC person, if you require evaluation sample. Unit sample quantity shall be 50 pcs. (Part No.: 2SC5014)

PACKAGE DIMENSIONS
in millimeters



PIN CONNECTIONS
1. Collector
2. Emitter
3. Base
4. Emitter

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Collector to Base Voltage	V_{CBO}	9	V
Collector to Emitter Voltage	V_{CEO}	6	V
Emitter to Base Voltage	V_{EBO}	2	V
Collector Current	I_C	30	mA
Total Power Dissipation	P_T	150	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to + 150	°C

Caution: Electrostatic Sensitive Device

Document No. P10394EJ2V0DS00 (2nd edition)
(Previous No. TD-7938)
Date Published August 1995 P
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Collector Cutoff Current	I_{CBO}			0.1	μA	V_{CB} = 5 V, I_E = 0
Emitter Cutoff Current	I_{EBO}			0.1	μA	V_{EB} = 1 V, I_C = 0
DC Current Gain	h_{FE}	75		150		V_{CE} = 3 V, I_C = 10 mA*1
Gain Bandwidth Product	f_T		12		GHz	V_{CE} = 3 V, I_C = 10 mA
Feed-back Capacitance	C_{re}		0.3	0.5	pF	V_{CB} = 3 V, I_E = 0, f = 1 MHz*2
Insertion Power Gain	$\|S_{21e}\|^2$	9	11		dB	V_{CE} = 3 V, I_C = 10 mA, f = 2.0 GHz
Noise Figure	NF		1.5	2.5	dB	V_{CE} = 3 V, I_C = 3 mA, f = 2.0 GHz

*1 Pulse Measurement; PW ≤ 350 μs, Duty Cycle ≤ 2 % Pulsed.

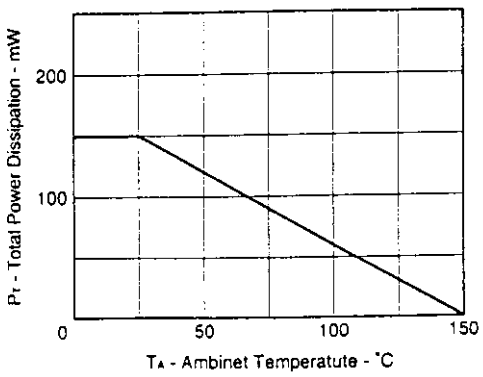
*2 Measured with 3 terminals bridge, Emitter and Case should be grounded.

h_{FE} Classification

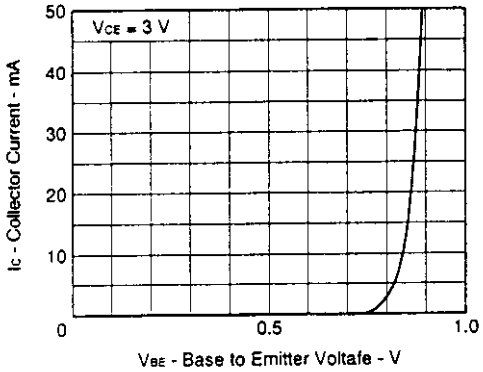
Rank	KB
Marking	T83
h_{FE}	75 to 150

TYPICAL CHARACTERISTICS (T_A = 25 °C)

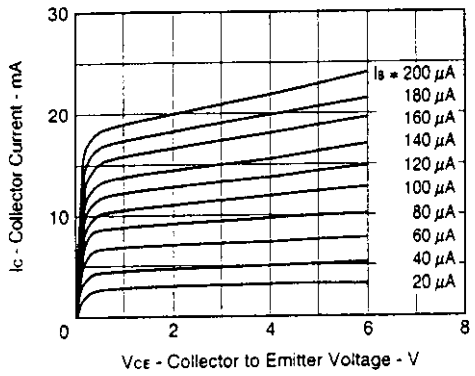
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



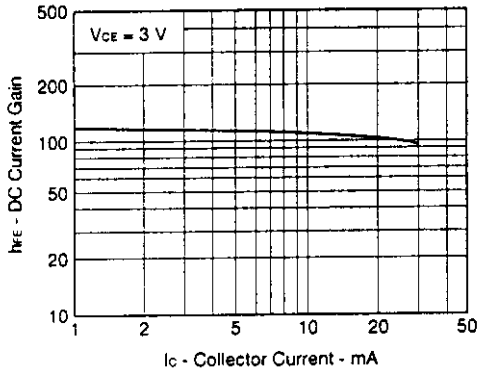
COLLECTOR CURRENT vs. BASE TO EMITTER VOLTAGE



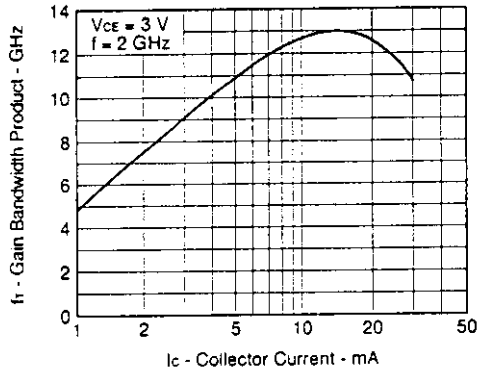
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



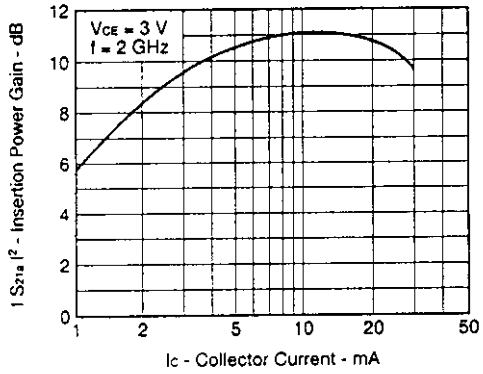
DC CURRENT GAIN vs. COLLECTOR CURRENT



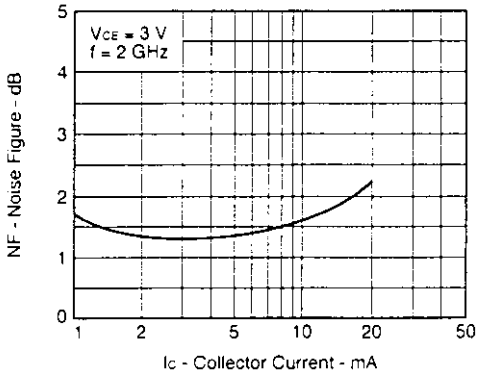
GAIN BANDWIDTH PRODUCT vs. COLLECTOR CURRENT



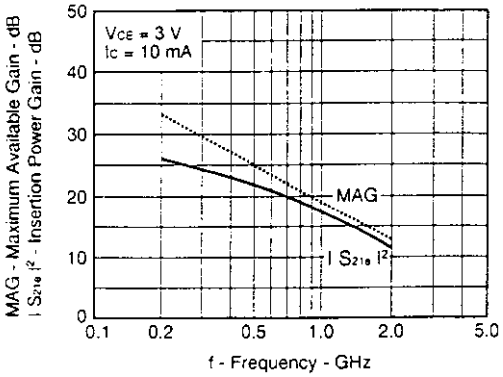
INSERTION POWER GAIN vs. COLLECTOR CURRENT



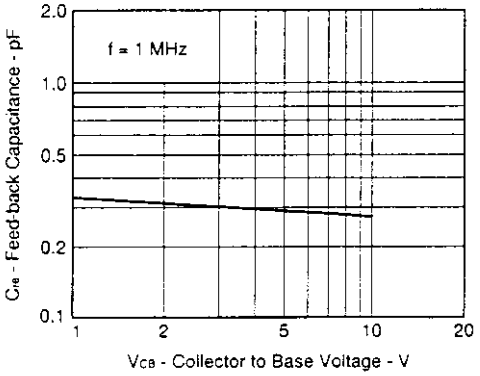
NOISE FIGURE
vs. COLLECTOR CURRENT



MAXIMUM AVAILABLE GAIN/INSERTION POWER GAIN
vs. FREQUENCY



FEED-BACK CAPACITANCE vs.
COLLECTOR TO BASE VOLTAGE



S-PARAMETER

V_{CE} = 3 V, Ic = 10 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100.00	.727	-22.0	22.084	159.4	.011	87.5	.934	-13.1
200.00	.640	-42.3	19.220	142.1	.029	70.7	.832	-24.3
300.00	.537	-57.8	16.333	129.2	.041	69.4	.735	-31.7
400.00	.452	-70.0	13.716	119.6	.046	60.9	.642	-35.6
500.00	.374	-82.3	11.834	111.2	.051	59.6	.562	-39.2
600.00	.332	-91.0	10.355	105.6	.060	61.7	.520	-40.7
700.00	.293	-101.5	9.190	100.2	.066	61.0	.479	-42.0
800.00	.255	-109.0	8.182	95.6	.072	61.3	.443	-44.4
900.00	.231	-119.1	7.376	91.9	.076	60.5	.413	-44.0
1000.00	.211	-128.8	6.751	87.9	.086	61.2	.394	-43.9
1100.00	.200	-136.1	6.171	84.9	.095	62.6	.376	-45.7
1200.00	.184	-143.4	5.658	81.7	.099	58.8	.363	-47.1
1300.00	.184	-154.3	5.286	79.0	.103	60.1	.342	-48.3
1400.00	.180	-162.4	4.932	76.2	.111	54.6	.332	-48.3
1500.00	.174	-171.5	4.630	73.3	.115	56.8	.310	-51.6
1600.00	.180	-178.4	4.347	70.9	.123	58.2	.303	-53.2
1700.00	.192	176.8	4.128	68.7	.131	54.1	.292	-51.8
1800.00	.193	169.1	3.914	66.0	.132	55.6	.292	-54.2
1900.00	.191	165.2	3.734	64.0	.139	51.7	.285	-55.3
2000.00	.209	161.0	3.561	61.1	.151	53.8	.281	-60.1
2100.00	.212	154.0	3.386	59.3	.154	51.9	.268	-61.0
2200.00	.219	148.1	3.242	56.7	.165	50.8	.267	-64.1
2300.00	.230	147.0	3.117	54.9	.169	49.2	.259	-63.5
2400.00	.230	141.3	2.986	53.0	.172	51.0	.240	-66.9
2500.00	.243	140.6	2.891	50.2	.186	48.5	.239	-68.9
2600.00	.254	135.8	2.790	48.6	.188	47.7	.249	-67.8
2700.00	.247	135.4	2.703	47.4	.193	47.9	.242	-73.3
2800.00	.251	132.3	2.610	44.0	.203	45.5	.237	-75.5
2900.00	.254	131.9	2.525	42.6	.207	44.0	.232	-77.9
3000.00	.269	123.9	2.435	40.5	.213	42.1	.236	-82.2

V_{CE} = 3 V, Ic = 5 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100.00	.854	-15.0	13.962	166.0	.014	83.0	.966	-9.2
200.00	.795	-29.7	13.063	152.7	.033	76.1	.917	-17.9
300.00	.724	-41.9	11.975	141.5	.046	71.1	.856	-25.0
400.00	.648	-53.1	10.690	132.1	.054	65.0	.785	-30.0
500.00	.569	-63.9	9.702	123.1	.063	62.7	.711	-34.8
600.00	.516	-72.9	8.789	116.6	.070	58.8	.656	-38.4
700.00	.457	-81.9	8.009	110.2	.078	55.8	.611	-40.8
800.00	.411	-88.9	7.240	104.7	.085	54.3	.562	-44.1
900.00	.374	-96.5	6.634	100.2	.094	55.3	.525	-45.7
1000.00	.331	-105.0	6.145	95.6	.095	52.9	.500	-46.6
1100.00	.310	-111.5	5.664	91.9	.102	53.3	.468	-48.0
1200.00	.277	-118.1	5.207	88.1	.108	50.6	.453	-50.0
1300.00	.260	-126.8	4.898	84.8	.112	51.5	.425	-51.2
1400.00	.249	-134.2	4.595	81.6	.119	52.3	.411	-52.6
1500.00	.232	-143.5	4.329	78.3	.121	50.2	.386	-54.8
1600.00	.232	-150.4	4.085	75.4	.133	48.7	.378	-55.2
1700.00	.234	-158.5	3.892	72.7	.134	46.4	.360	-57.5
1800.00	.216	-164.6	3.678	69.8	.140	47.9	.359	-58.6
1900.00	.211	-171.3	3.514	67.6	.145	45.5	.343	-60.4
2000.00	.230	-176.6	3.368	64.5	.151	46.0	.336	-63.1
2100.00	.224	174.1	3.207	62.2	.161	46.4	.319	-64.7
2200.00	.227	168.9	3.064	59.2	.166	45.9	.317	-66.7
2300.00	.229	165.3	2.942	57.3	.168	44.3	.314	-67.4
2400.00	.230	158.8	2.838	55.3	.174	44.3	.291	-68.4
2500.00	.253	156.1	2.742	52.5	.181	42.8	.290	-71.4
2600.00	.250	150.1	2.656	50.7	.184	44.0	.289	-69.8
2700.00	.248	149.2	2.558	49.0	.189	43.8	.281	-74.2
2800.00	.254	145.7	2.484	45.9	.195	40.9	.283	-77.3
2900.00	.262	143.7	2.405	44.2	.203	39.8	.276	-77.7
3000.00	.264	135.7	2.317	41.7	.208	39.4	.294	-83.9

S-PARAMETER

V_{CE} = 3 V, Ic = 3 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100.00	.908	−11.7	9.519	169.3	.020	77.7	.984	−7.3
200.00	.872	−22.9	9.147	158.9	.036	74.3	.951	−13.7
300.00	.825	−33.1	8.721	149.4	.050	68.7	.920	−19.7
400.00	.767	−42.7	8.085	141.0	.061	66.4	.866	−24.9
500.00	.701	−52.2	7.623	132.2	.073	61.0	.813	−30.0
600.00	.656	−61.0	7.104	125.7	.082	57.4	.764	−33.9
700.00	.598	−69.4	6.670	119.0	.088	54.9	.721	−37.3
800.00	.551	−76.2	6.145	113.1	.097	52.4	.671	−41.2
900.00	.494	−84.0	5.719	108.0	.101	51.7	.631	−42.9
1000.00	.458	−90.7	5.371	102.9	.111	49.3	.602	−45.0
1100.00	.422	−97.4	5.005	98.6	.117	47.6	.570	−47.0
1200.00	.388	−104.1	4.642	94.3	.118	46.3	.538	−49.4
1300.00	.356	−110.7	4.396	90.5	.124	45.3	.512	−51.3
1400.00	.341	−117.6	4.148	86.8	.129	42.6	.491	−52.7
1500.00	.318	−124.9	3.933	83.0	.135	44.0	.463	−55.2
1600.00	.305	−132.3	3.713	79.8	.140	43.7	.445	−56.4
1700.00	.291	−140.3	3.563	77.0	.141	42.0	.430	−57.1
1800.00	.282	−145.0	3.382	73.6	.149	42.2	.424	−59.1
1900.00	.269	−151.9	3.234	71.2	.149	41.8	.413	−60.7
2000.00	.277	−160.1	3.108	67.7	.155	41.4	.401	−64.2
2100.00	.262	−167.5	2.956	65.1	.162	40.4	.386	−65.3
2200.00	.255	−172.8	2.838	61.9	.169	38.9	.377	−66.8
2300.00	.260	−177.4	2.722	60.0	.169	38.1	.373	−68.2
2400.00	.249	175.5	2.635	57.5	.173	37.9	.352	−68.1
2500.00	.266	171.8	2.553	54.5	.182	38.2	.351	−71.9
2600.00	.263	164.2	2.459	52.0	.183	36.7	.347	−70.9
2700.00	.270	164.0	2.383	50.6	.192	36.7	.341	−75.1
2800.00	.272	159.9	2.323	47.5	.195	36.4	.337	−79.8
2900.00	.278	155.5	2.241	45.6	.193	34.5	.316	−78.4
3000.00	.272	150.5	2.147	42.7	.200	35.0	.324	−82.3

V_{CE} = 3 V, Ic = 1 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
100.00	.973	−6.3	3.521	173.9	.015	82.1	.991	−3.5
200.00	.959	−13.5	3.484	167.3	.033	83.0	.985	−7.6
300.00	.947	−19.7	3.458	161.2	.055	79.6	.981	−11.3
400.00	.922	−26.2	3.360	155.2	.065	72.2	.962	−14.8
500.00	.898	−32.8	3.348	148.3	.084	69.4	.946	−18.9
600.00	.878	−39.1	3.287	143.3	.100	63.5	.925	−22.5
700.00	.848	−45.9	3.248	137.3	.109	60.2	.909	−25.5
800.00	.822	−51.7	3.136	131.4	.126	56.6	.875	−29.5
900.00	.772	−58.0	3.040	126.1	.134	55.0	.847	−32.4
1000.00	.752	−64.0	2.980	120.9	.150	50.0	.830	−34.6
1100.00	.708	−70.1	2.879	116.1	.158	46.1	.801	−38.1
1200.00	.676	−76.4	2.749	110.5	.163	43.5	.776	−40.7
1300.00	.644	−82.4	2.690	106.0	.172	44.1	.745	−43.5
1400.00	.617	−88.2	2.588	101.4	.176	38.2	.724	−46.8
1500.00	.579	−94.1	2.514	96.8	.181	36.3	.696	−49.2
1600.00	.559	−100.2	2.407	92.4	.186	33.2	.680	−50.2
1700.00	.536	−106.6	2.369	89.1	.188	31.7	.651	−52.6
1800.00	.509	−111.4	2.278	84.9	.191	30.5	.642	−54.9
1900.00	.490	−117.1	2.201	81.5	.192	28.4	.624	−57.0
2000.00	.478	−124.8	2.151	77.0	.195	27.2	.611	−59.7
2100.00	.442	−129.6	2.071	73.5	.198	25.4	.593	−62.2
2200.00	.423	−136.7	2.001	69.4	.201	25.8	.575	−63.7
2300.00	.429	−140.8	1.938	67.1	.203	23.5	.565	−65.5
2400.00	.401	−145.8	1.873	63.8	.202	21.3	.536	−66.3
2500.00	.406	−152.3	1.839	60.3	.204	20.3	.540	−69.0
2600.00	.388	−158.3	1.776	57.3	.201	20.6	.528	−68.7
2700.00	.400	−161.7	1.733	55.3	.204	20.6	.521	−72.7
2800.00	.385	−166.9	1.688	51.3	.203	19.0	.512	−75.5
2900.00	.389	−171.6	1.644	49.3	.201	17.8	.498	−75.6
3000.00	.368	−177.7	1.590	46.0	.209	17.2	.495	−80.4

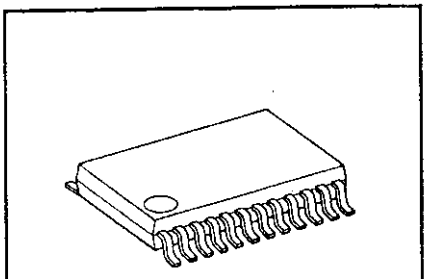
TOSHIBA TA31181FN

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA31181FN

FILTERLESS IF DETECTOR FOR MOBILE COMMUNICATION

This IF detector IC can extremely save space and depth of AMPS mobile telephone due to including 2nd IF filter, which previously made by ceramic device. High speed mixer, demodulator, wide dynamic range RSSI function and RSSI AMP are also built-in.

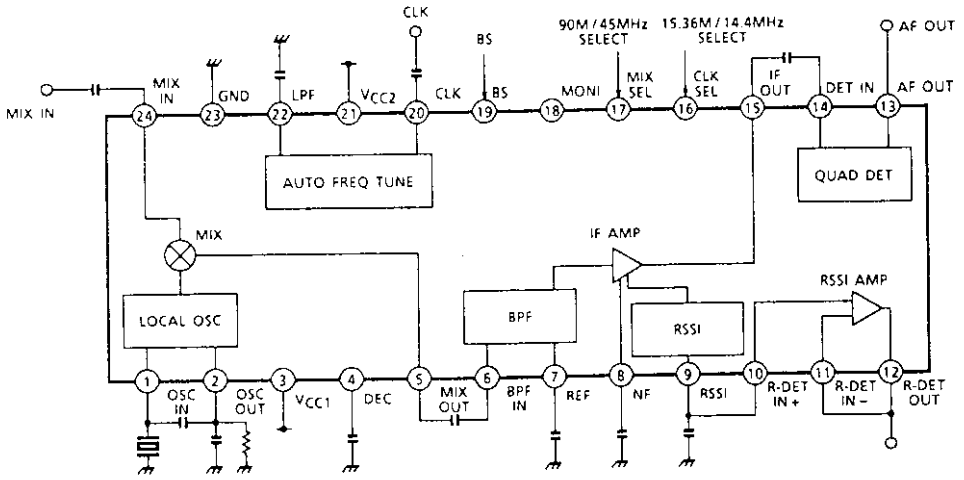


SSOP24-P-300-0.65A

Weight : 0.14g (Typ.)

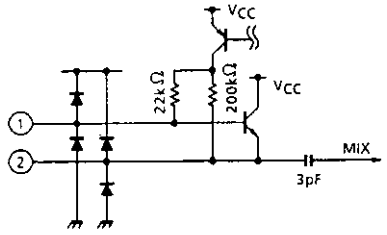
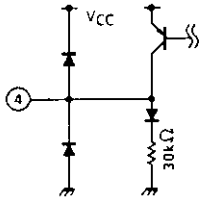
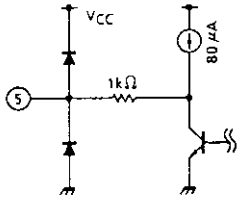
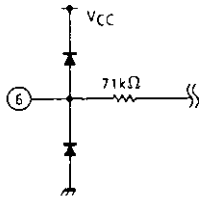
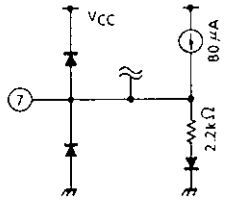
FEATURES

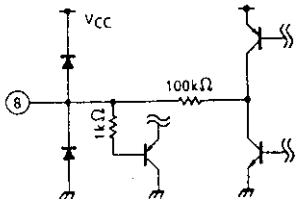
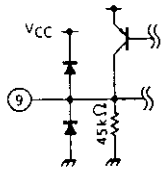
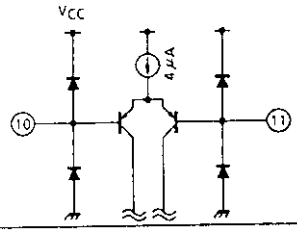
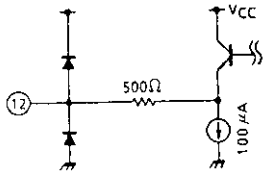
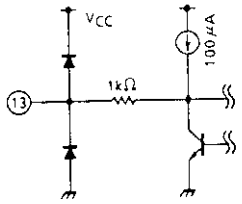
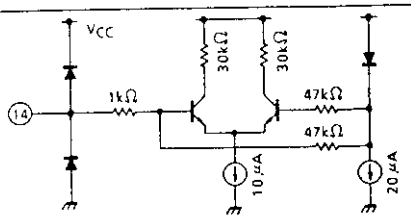
- Wide operating frequency mixer including image canceler : 40~50MHz, 80~100MHz
- High demodulating output level : 245mV$_{rms}$
- Operating voltage range : 2.3~5.5V
- Low current consumption : 7mA (Typ.)
- Small package : SSOP24pin (0.65mm pitch)

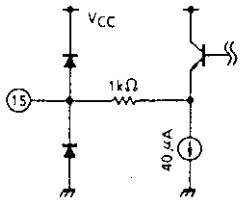
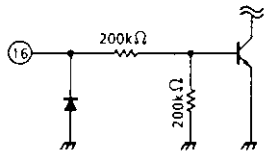
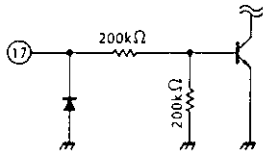
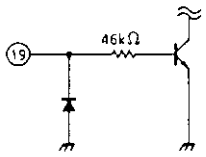
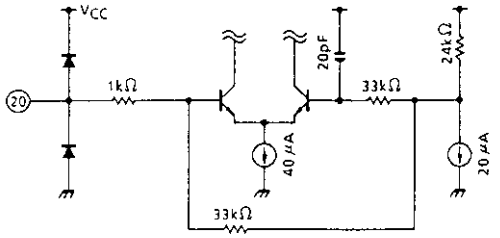


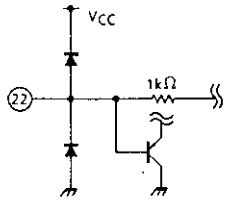
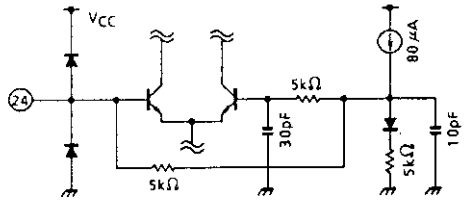
961001EBA2

PIN FUNCTION (The values of resistor and capacitor are typ..)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	OSC IN	LOCAL OSC input/output terminals. Colpitts oscillator is formed by internal emitter follower and external crystal. And external local signal injection is possible from pin 1 or pin 2.	
2	OSC OUT		
3	V_{CC1}	Power supply terminal.	—
4	DEC	AGC terminal for MIX conversion gain. This terminal connects capacitor to GND.	
5	MIX OUT	MIX output terminal. Output impedance is around 1.1kΩ.	
6	BPF IN	Internal BPF input terminal.	
7	REF	Internal BPF decoupling terminal for DC bias. This terminal connects capacitor to GND.	

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
8	NF	IF AMP decoupling terminal for DC bias. This terminal connects capacitor to GND.	
9	RSSI	This terminal outputs DC level according to input signal level to IF AMP. Dynamic range is around 80dB.	
10	R-DET IN +	RSSI AMP input terminal.	
11	R-DET IN −	RSSI AMP inverted input terminal.	
12	R-DET OUT	RSSI AMP output terminal.	
13	AF OUT	Demodulate signal output terminal. Output impedance is around 1.1kΩ.	
14	DET IN	QUAD DET input terminal.	

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
15	IF OUT	Output terminal of IF AMP.	
16	CLK SEL	CLK frequency signal (input pin 20) selection terminal. "H" : f_{CK} = 15.36MHz. "L" : f_{CK} = 14.40MHz.	
17	MIX SEL	MIX operating frequency selection terminal. "H" : f_{IN} = 80~100MHz. "L" : f_{IN} = 40~50MHz.	
18	MONI	Connected internal circuit. Externally non-connection.	—
19	BS	Power down mode selection terminal. "H" : Active mode. "L" : Power down mode.	
20	CLK	CLK frequency signal (15.36 / 14.40MHz) for AUTO FREQ TUNE input terminal.	
21	V_{CC2}	Power supply terminal for AUTO FREQ TUNE block.	—

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
22	LPF	AUTO FREQ TUNE function decoupling terminal. This terminal connects capacitor to GND.	
23	GND	GND terminal.	—
24	MIX IN	1st IF signal input terminal.	

DESCRIPTION

1. Setting input frequency

- Setting MIX input frequency
  MIX SEL terminal (pin17) selects two operating frequency range for MIX.

MIX SEL	MIXER INPUT FREQUENCY (MHz)
L	40~50
H	80~100

It is not recommended MIX SEL terminal is non-connection.

- Setting LOCAL OSC frequency
  On-chip 2nd IF filter is fulfilled by active filter that works on 60kHz 2nd local frequency. Therefore local frequency fixed to (1st IF - 60kHz) is required.

2. LOCAL OSC external injection method

Input from pin1 as shown in Fig.1, add resistor R21 and set the input signal so that signal level at pin1 is 95~105dBμV. A built-in BUFFER amp minimizes leakage from MIX.
Input from pin2 as shown in Fig.2, setting the injection level at pin2 between 95dBμV and 105dBμV.

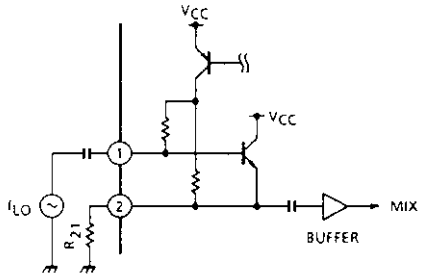


Fig.1

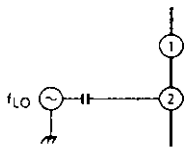


Fig.2

3. BPF (band pass filter)

Internal BPF for channel selection (center frequency $f_0 = 60kHz$, cut-off frequency $f_{CK} = 10kHz$, rejection level at adjacent channel $ATT_{ADJ} = 60dB$) is cause of selectivity characteristics and demodulation output distortion characteristics.

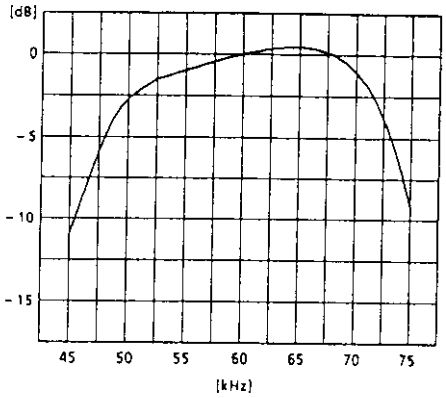


Fig.3 BPF characteristics

4. Automatic frequency tuning system

Automatic frequency tuning system stabilizes center frequency f_0 drift of internal BPF by temperature and parameter tolerance. External clock signal, as reference frequency signal for automatic frequency tuning system, inputs to CLK terminal (pin20). Two kinds of clock frequency signal can be chosen by CLK SEL terminal (pin16).

CLK SEL	CLOCK INPUT FREQUENCY (MHz)
L	14.40
H	15.36

It is not recommended CLK SEL terminal is non-connection.
Clock frequency signal source should be required high accuracy such as TCXO, because selectivity characteristics and demodulation output distortion characteristics depend on clock frequency regulation.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	7	V
Power Dissipation	P_D	780	mW
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~150	°C

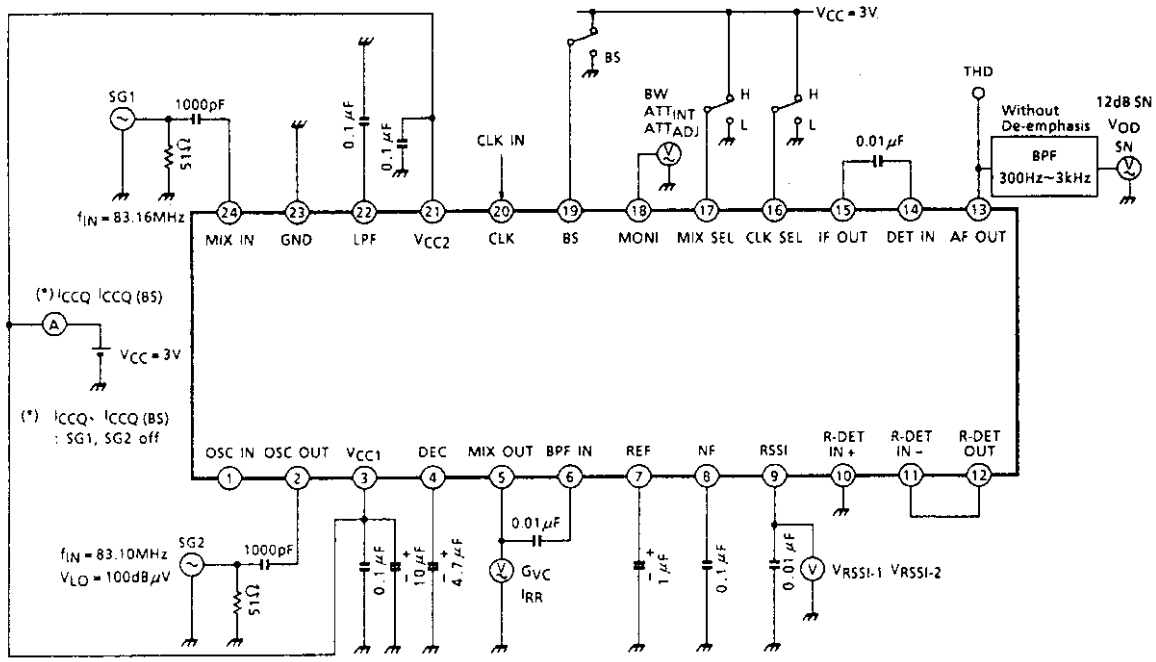
ELECTRICAL CHARACTERISTICS (Unless otherwise specified V_{CC} = 3.0V, f_{IN} = 83.16MHz, Δf = ±8kHz, f_{MOD} = 1kHz, f_{CK} = 15.36MHz, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	V_{CC}	—	—	2.3	3.0	5.5	V
Current Consumption	I_{CCQ}	1	MIX SEL, CLK SEL = H	4.2	7	9.8	mA
Battery Saving Current Consumption	$I_{CCQ\ (BS)}$	1	MIX SEL, CLK SEL = L	—	0	10	μA
MIX Operating Frequency	f_{IN-1}	—	MIX SEL = L	40	—	50	MHz
	f_{IN-2}	—	MIX SEL = H	80	—	100	MHz
MIX Image Rejection Ratio	I_{RR}	1	V_{IN} = 70dBμVEMF, Pin4 → GND	20	30	—	dB
MIX Conversion Gain	G_{VC}	1	V_{IN} = 60dBμVEMF, Pin4→GND	27	29.5	32	dB
MIX Intercept Point	I_P	—	V_{IN} = 80dBμVEMF, Pin4→GND	—	103	—	dBμVEMF
MIX Input Impedance	R_{IN}	—	—	—	4.5	—	kΩ
	C_{IN}	—	—	—	3	—	pF
LOCAL OSC Input Level	V_{LO}	—	—	95	100	105	dBμV
12dB Sensitivity	12dB SN	1	—	—	15	20	dBμVEMF
Demodulation Output Level	V_{OD}	1	V_{IN} = 80dBμVEMF	190	245	300	mV_{rms}
SN Ratio	SN	1	V_{IN} = 80dBμVEMF	45	66	—	dB
AM Rejection Ratio	AMR	—	V_{IN} = 80dBμVEMF	—	45	—	dB
Demodulation Output Distortion	THD	1	V_{IN} = 80dBμVEMF	—	−30	−26	dB
Pass Band Width	BW	1	−6dB	±11	±13	—	kHz
Demodulation Output Cut-off Frequency	f_C	—	−3dB	—	10	—	kHz
Rejection Level at Inter Leave Channel	ATT_{INT}	1	±30kHz (*1)	30	45	—	dB
Rejection Level at Adjacent Channel	ATT_{ADJ}	1	±60kHz (*1)	50	60	—	dB
RSSI Output Voltage	V_{RSSI-1}	1	V_{IN} = 15dBμVEMF	230	380	530	mV
	V_{RSSI-2}	1	V_{IN} = 90dBμVEMF	1.6	2.0	2.4	V

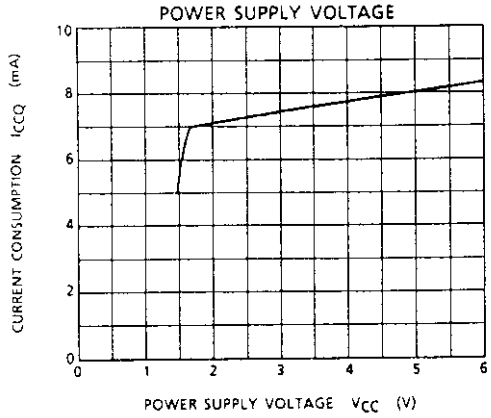
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Input Level	V_{IN} CK	—	—	94	100	106	dBμV
Low Level Input Voltage	V_L	—	BS, CLK SEL, MIX SEL	—	—	0.2	V
High Level Input Voltage	V_H	—	BS, CLK SEL, MIX SEL	2.0	—	V_{CC}	V
Input Voltage Range to RSSI AMP	V_{IN}	—	—	0	—	V_{CC} − 1	V

(*1) $\Delta f = \pm 8kHz$, $f_{MOD} = 400Hz$

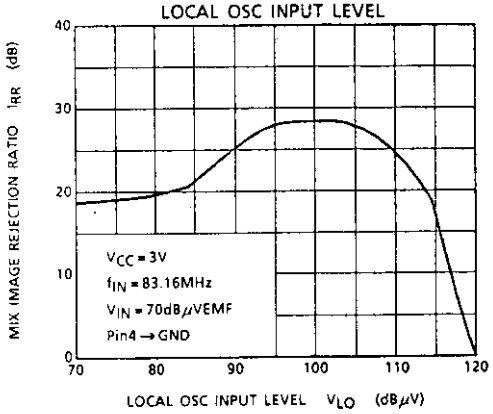
TEST CIRCUIT 1



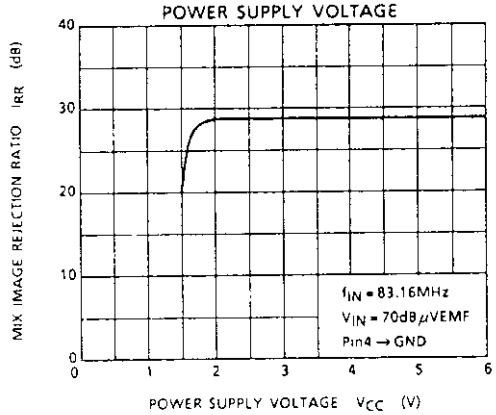
CURRENT CONSUMPTION – POWER SUPPLY VOLTAGE



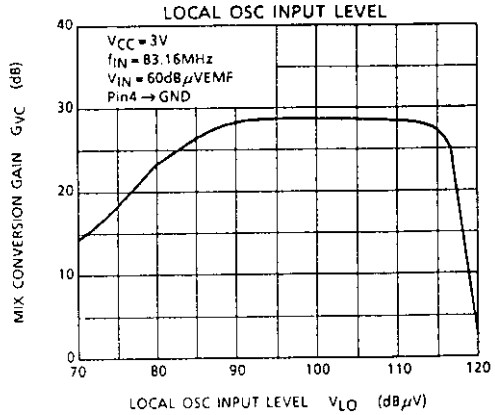
MIX IMAGE REJECTION RATIO – LOCAL OSC INPUT LEVEL



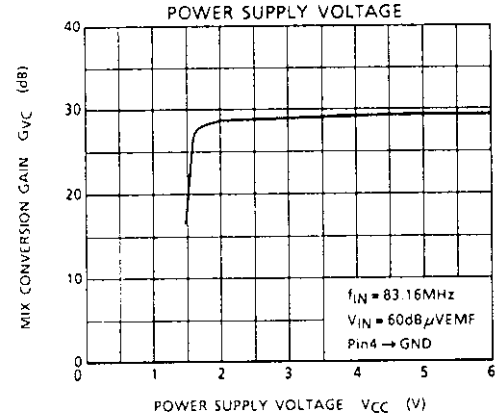
MIX IMAGE REJECTION RATIO – POWER SUPPLY VOLTAGE



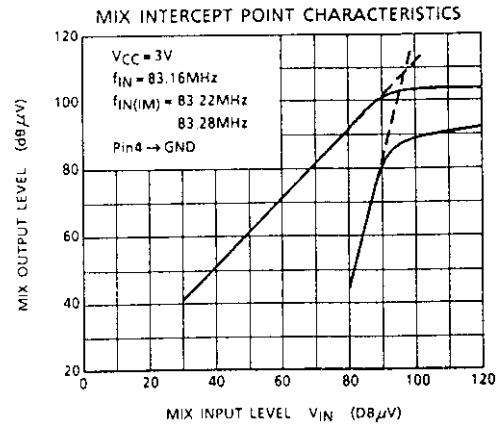
MIX CONVERSION GAIN – LOCAL OSC INPUT LEVEL



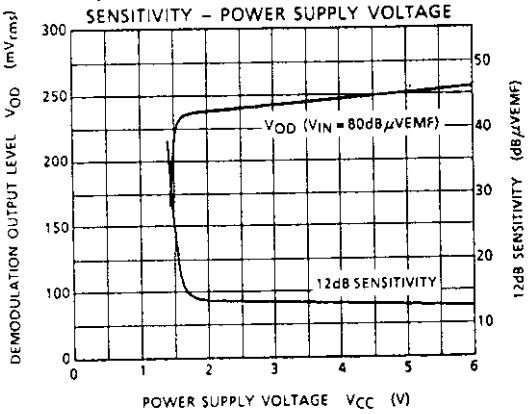
MIX CONVERSION GAIN – POWER SUPPLY VOLTAGE



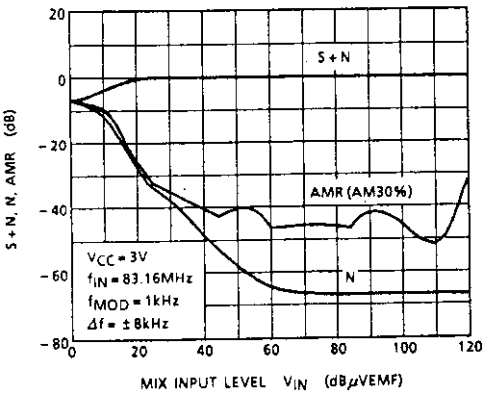
MIX INTERCEPT POINT CHARACTERISTICS



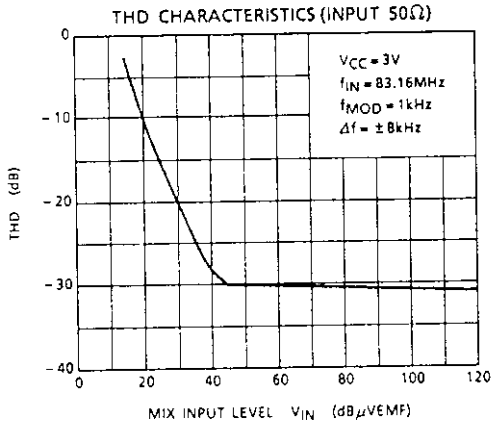
DEMODULATION OUTPUT LEVEL, 12dB SENSITIVITY – POWER SUPPLY VOLTAGE



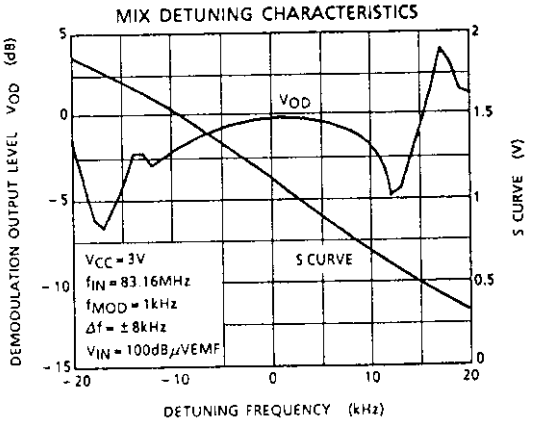
MIX + IF CHARACTERISTICS (INPUT 50Ω)



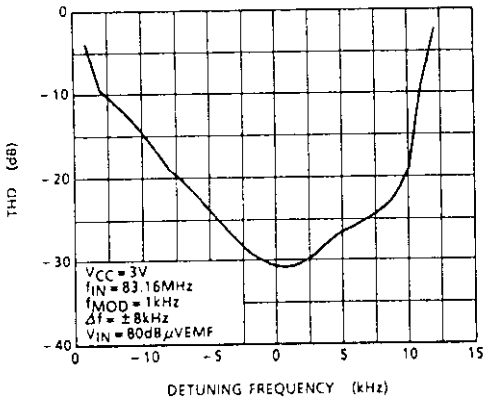
THD CHARACTERISTICS (INPUT 50Ω)



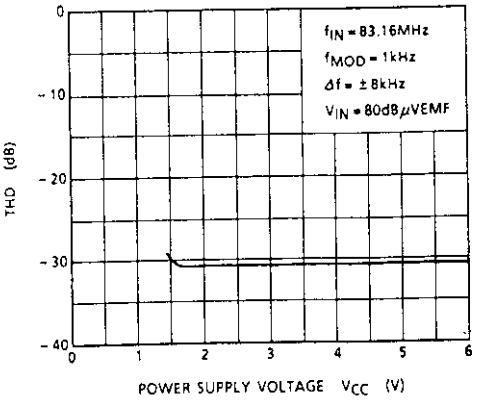
MIX DETUNING CHARACTERISTICS

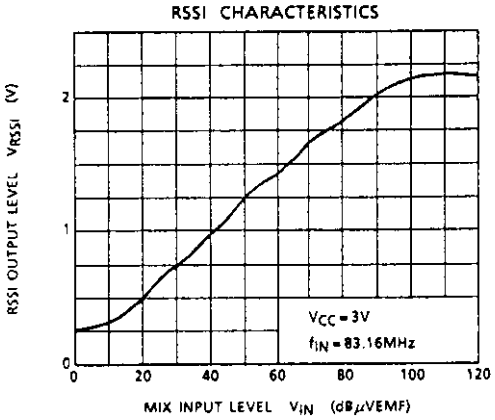


THD DETUNING CHARACTERISTICS

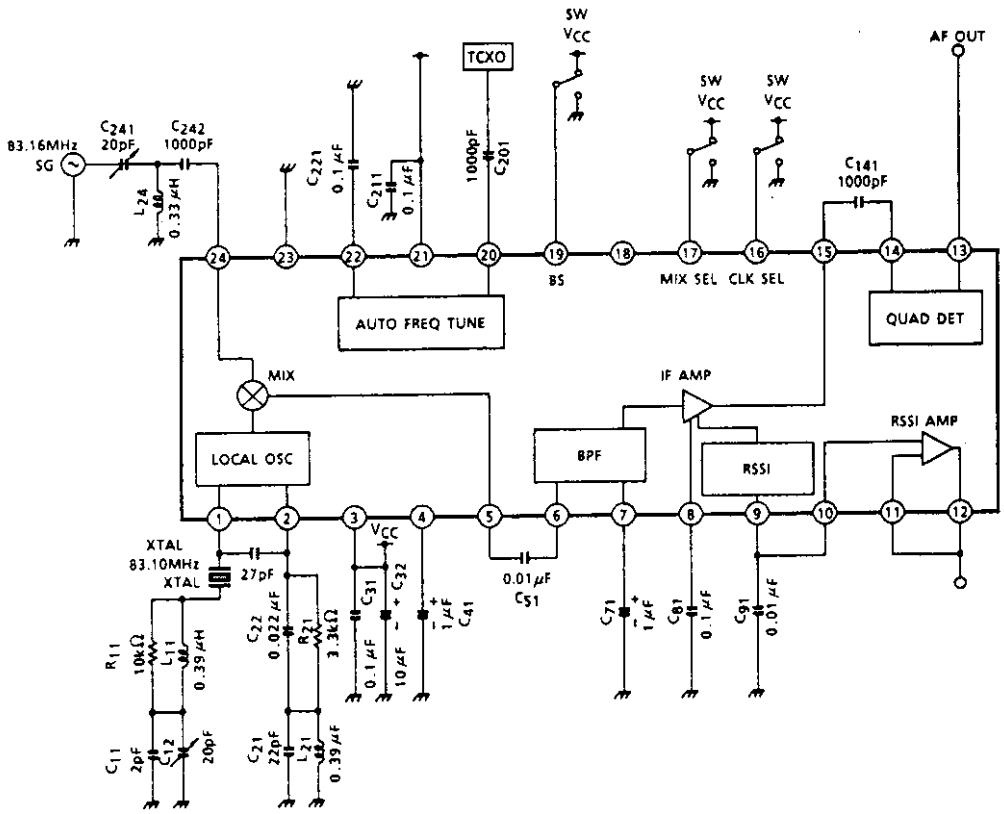


THD – POWER SUPPLY VOLTAGE




RSSI CHARACTERISTICS
RSSI OUTPUT LEVEL V_{RSSI} (V)
2
1
0
0
20
40
60
80
100
120
V_{CC} = 3V
f_{IN} = 83.16MHz
MIX INPUT LEVEL V_{IN} (dBμVEMF)

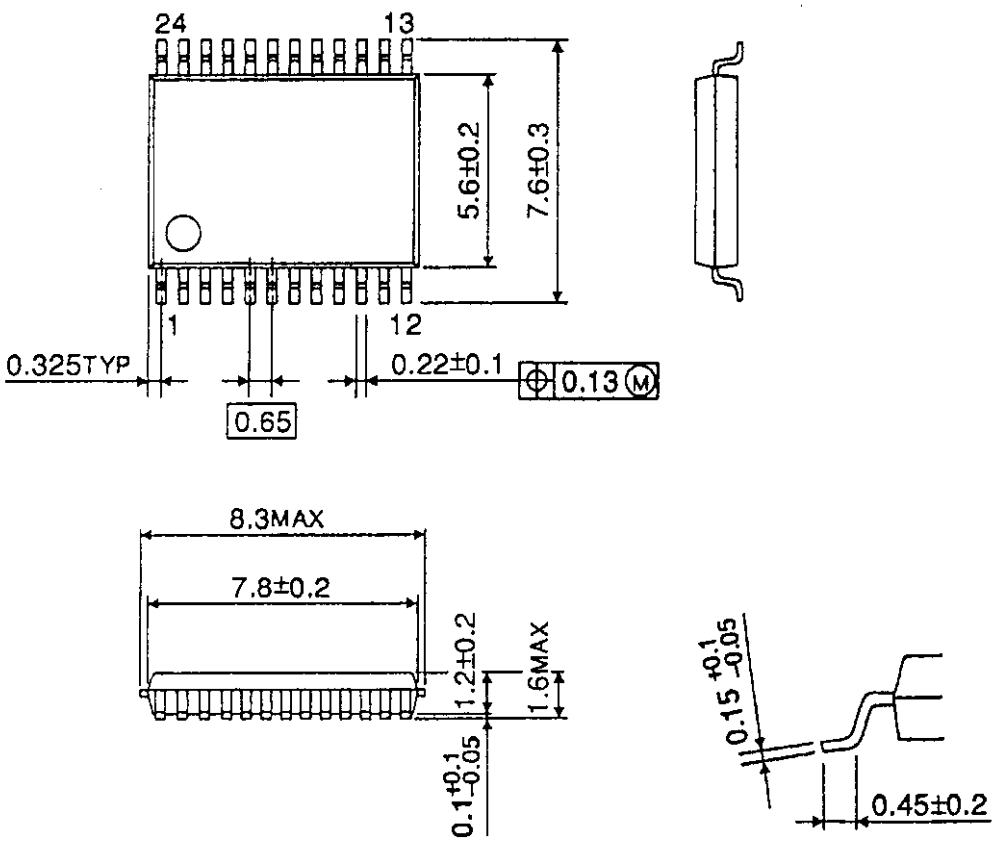
APPLICATION CIRCUIT



OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)

KINSEKI, LTD.

SPECIFICATION

No. H1101-97041-012 1/6

1. PURPOSE AND SCOPE

This document contains specifications related to Quartz Crystal Model CX-91F for TALK.

2. APPEARANCE AND STRUCTURE :

2. 1 Model : CX-91F

2. 2 Marking & Dimension : per H1101-97041-012 6/6

3. ELECTRICAL CHARACTERISTICS :

3. 1 Nominal frequency : 14400 kHz

3. 2 Mode of vibration : Fundamental

3. 3 Operating temperature range : −30°C to +70°C

3. 4 Storage temperature range : −40°C to +100°C

3. 5 Frequency tolerance : 10×10^{-6} (25±3°C)

3. 6 Frequency temperature characteristics :

	−10°C	+60°C
Lank A	$+3.1$ to $+9.2\times10^{-6}$	-10.3 to -4.3×10^{-6}
Lank B	-2.9 to $+3.2\times10^{-6}$	-4.9 to $+1.1\times10^{-6}$

3. 7 Equivalent series resistance : 50 Ω max.

3. 8 Shunt capacitance : 7.0 pF max.

3. 9 Insulation resistance : 500 MΩ min./DC 100±15V

3.10 Test condition

3.10.1 Test method : HP4194A or HP4195A

3.10.2 Load capacitance : 17pF

3.10.3 Drive level : 200μA

2.11 Aging Tolerance : $\pm2\times10^{-6}$/year

4. MECHANICAL CHARACTERISTICS;

4. 1 Leakage : No bubbles shall appear when units are placed in hot water (70-75°C) having depth of 100-150 mm for 5 minutes.

4. 2 Dry heat After the following test , outline appearance, electrical characteristics shall be satisfied.
The quartz crystal unit shall be stored at a temperature of 100±3°C for 500h. Then it shall be subjected to standard atmospheric conditions for 30 minutes, after which measurement shall be made.

4. 3 Cold After the following test , outline appearance, electrical characteristics shall be satisfied.
The quartz crystal unit shall be stored at a temperature of -40±3°C for 500h. Then it shall be subjected to standard atmospheric conditions for 30 minutes, after which measurement shall be made.

4. 4 Successive change of temperature cycle test
After following test, outline appearance, electrical characteristics shall be satisfied.
The quartz crystal unit shall be subjected to 500 successive change of temperature cycles, each as shown in fig.1 below.

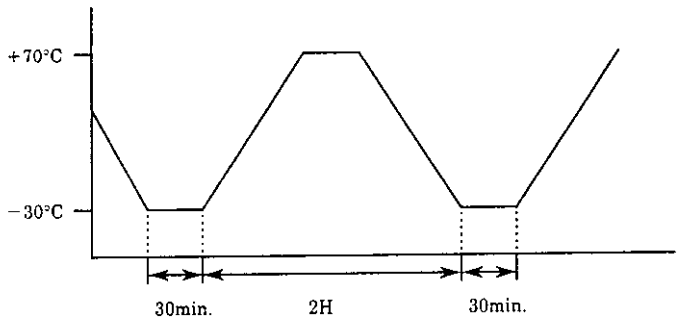


Fig.1

4. 5 Shock of temperature

After following test, outline appearance, electrical characteristics shall be satisfied.
The quartz crystal unit shall be subjected to 500 successive change of temperature cycles, each as shown in fig.2 below. Then it shall be subjected to standard atmospheric conditions for 24 h, after which measurements shall be made.

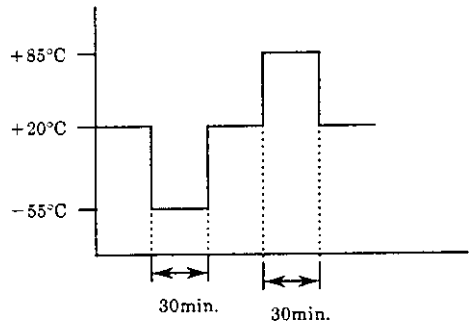


Fig.2

4. 6 Damp heat

(Steady State)

After the following test , outline appearance, electrical characteristics shall be satisfied.
The quartz crystal unit shall be stored at a temperature of 40±3°C with relative humidity of 90% to 95% for 96h. Then it shall be subjected to standard atmospheric conditions for 30 minutes, after which measurement shall be made.

4. 7 Shock

: After following test, outline appearance, electrical characteristics shall be satisfied.
Test condition : Randomly dropped from height of 86.7 cm onto concrete board surface in 3 times.

4. 8 Vibration

After the following test, outline appearance, electrical characteristics shall be satisfied.

Test condition :

Amplitude	: 1.5 mm
Frequency	: 10-55Hz
Sweep time	: 1 minute
Duration	: 3 mutually perpendicular planes
	: in each 2 hour.

4. 9 Resistance to soldering heat

(Reflow test)

After reflow twice on conditions of fig.3. , outline appearance, electrical characteristics shall be satisfied.

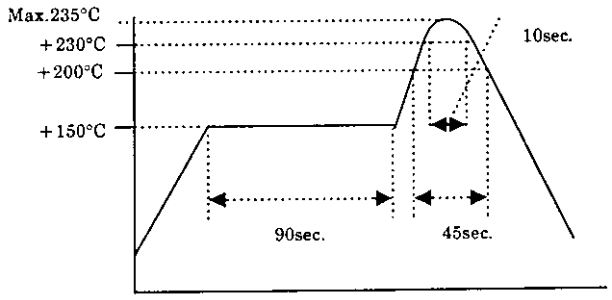


Fig.3

(Solder iron)

Solder all terminals by a solder iron whose temperature is 350 ± 10°C , for 3 ± 1 seconds once per terminal.
Then , the specimen should be subjected to standard atmospheric conditions for 2 hours.
After the above , outline appearance , electrical characteristics should be satisfied.

4.10 Ultrasonic wave washing standard

Frequency	: 28-40kHz
Ultrasonic wave output	: 15W/ℓ max.
Time	: 60 sec.
Washing liquid	: IPA

5. Inspection All products are Inspected. Clause 3.5 to 3.7 , 3.9 shall be satisfied.Besides we guarantee the quality of Clause 3.8 , 3.11 , 4.1 to 4.10.
Inspection data is not appended.

6. Package
Less than 1000 :Pack
1000 or More than : Taping (Refer to H1102-93070-012)

7. Manufacturing place

Nation of manufacturing :Japan
Factory of manufacturing :KINSEKI LIMITED CHIBA PLANT

8. Assurance term after products being delivered

Within a year [The quartz crystal unit shall be stored at a temperature of 25±10°C with relative humidity of 50±10%.]

9. The minimum quantity for an order : 1000 piece

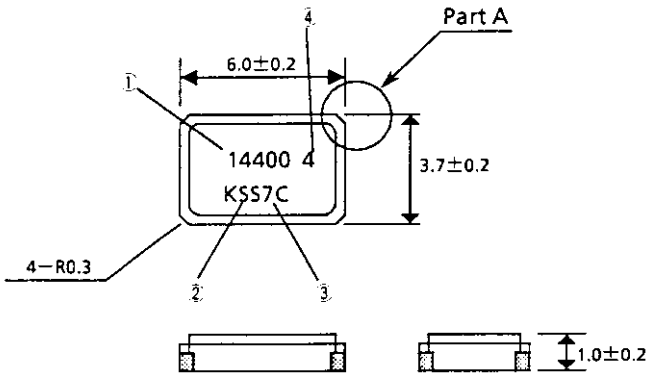
10. Contact method when specification is changed

In the case that specification shall be changed , we will decide together after marking contact with you before the specification will be changed.

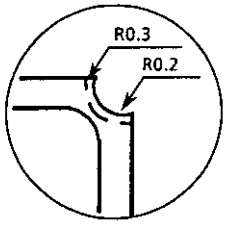
11. Shipping inspection standard

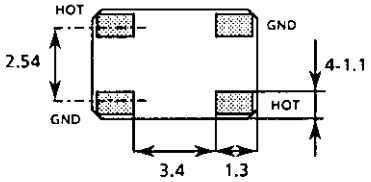
Inspection level : ANSI/ASQC Z 1.4 an ordinart inspection level Ⅰ AQL 0.4%
Inspection item : Frequency , CI
Test method : HP4195A

CX-91F

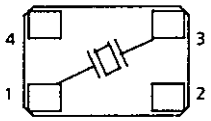


Magnifying drawing of Part A(Top view)



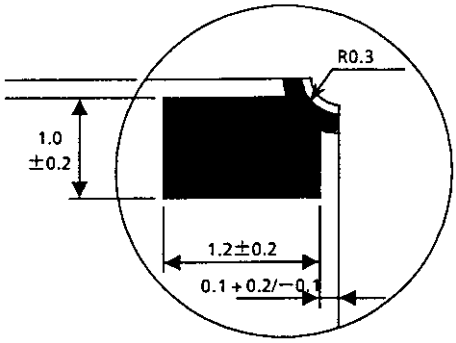


CONNECTION (TOP VIEW)



Terminal 2 and 4 is connected with the case

Magnifying drawing of Electrode



Finish : Ni plated / 4±2μm
Au plated / 0.5μm以下

Marking

Unit : mm

① Nominal frequency
② Manufacturer's name
③ Lot No.
④ Symbol of Frequency temperature characteristics lank
4 = Lank A
5 = Lank B

0.08g/a piece

*Year
The last digit of the year of the Christian Era should be corresponded to the Arabic figures.
*Month
The month should be corresponded to the below table.

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.
Symbol	1	2	3	4	5	6	7	8	9	10	11	12

CRYSTAL UNITS SPECIFICATION

OUR SPEC No. QA0510500
DATE : DEC 1, 1998

NIKKO DENSHI CO., LTD.

Applicant: Shintom Co., Ltd. Transmitter Type: BFYM3047

SPECIFICATION OF CRYSTAL UNIT	Spec No.QA0510500	Page 1/3

1.Nominal Frequency — 14.400 MHz

2.Holder type — TOP-B (Outline Dimension : as per XD-4053)

3.Load capacitance — 17.8 ± 0.1 pF

4.Frequency stablity in operating temperature range referred to +25°C

Temp.(°C)	Group 4	Group 5
-35	-14.77 to -8.42	-16.25 to -11.74
0	- 0.10 to 7.12	- 1.78 to 5.23
+60	- 8.65 to -2.09	- 6.92 to 0.12
+80	- 4.72 to 1.30	- 1.08 to 6.40

Unit:ppm

5.Frequency tolerance(at +25±2℃) — ± 8 ppm max

6.Drive level — 1.0 ± 0.2 mA

7.Equivalent series resistance — 30.0Ω max

8.Spurious
Within ±200kHz of main response, impedance ratio of spurious response to main response is to be more than 3:1

9.Insulation resistance — 500 MΩ min.at DC100±15V

10.Shunt capacitance — 7.0 pF max

11.Temperature range
Operating — - 30℃ to + 70℃
Storage — - 40℃ to +100℃

12.Aging — (1) Frequency : ±2.0 ppm / Year
(2) ESR : 30Ω max

13.Mode of oscillation — Fundamental

14.Drive level dependance
At the drive level of 0.1, 0.5, 1.0mA, deviations are to be as folloes.
(1) Frequency : ± 2.0×10^{-6} max
(2) ESR : ± 20% max

15.Mechanical Characteristics

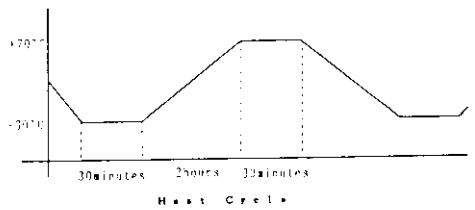
Test	Method and Condition	Judgement
15.1 Shock	Free drops onto hard wooden board from 1.2m height with 130 grams weight 10times 3 each directions.	Meets Electrical Characteristics in individual specifications and no appearance change.
15.2 Vibration	Amplitude 1.5mm, vibration 10 to 55Hz sine wave for 1 minutes, 3 each directions for 2 hours.	Same as above.
15.3 Leakage	Slow leak test Helium leak detector. Gross leak test Immersed into flourinert of 120±5°c.	Below 1×10^{-3} μpa·m³/sec. No continuous bubble for 5 minutes.
15.4 Humidity	240±8 hours in atmosphere of 40±2°C, 90 to 95%RH, remove drops of water, leave it at ambient for 2 hours.	Meets electrical characteristics and no appearance change. Insulation resistance should be more 20% of initial value.
15.5 Cold resistance	500 hours in atmosphere of -30°C, remove drops of water, leave it at ambient for 2 hours.	Meets electrical characteristics and no appearance change.
15.6 Heat resistance	500 hours in atmosphere of 70±2°C, leave it at ambient for 2 hours.	Same as above.

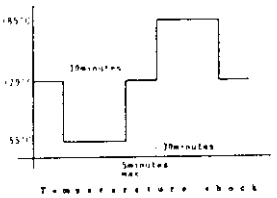
	DATE	APPROVED	CHECKED	CHECKED	DRAWN	REVISED
00	Nov. 30 1998					00

NIKKO DENSI CO., LTD

SPECIFICATION OF CRYSTAL UNIT	Spec No.QA0510500	Page 2/3

15.7 Heat resistance of terminals when soldering.	After touch to surface of solder bath of 350±10°C for 3±½ seconds,wipe off.	Meets electrical characteristics and no appearance change.
15.8 Solderability	Touch to surface of solder bath of 250±10°C for 3±½ seconds.	More then 3/4 of surface is covered by solder.
15.9 Heat cycle	500 cycles of temperature -30 and +85°C leave it st ambient for 2 hours.	Meets electrical Characteristics and no apperrance change.
15.10 Temperature shock	500 cycles of temperature -55, +20 and +85°C as shown below, leave it at ambient for 24hours.	Same as above





16. Cleaning — No deterioration in electrical characteristics and marking by using organic solvent

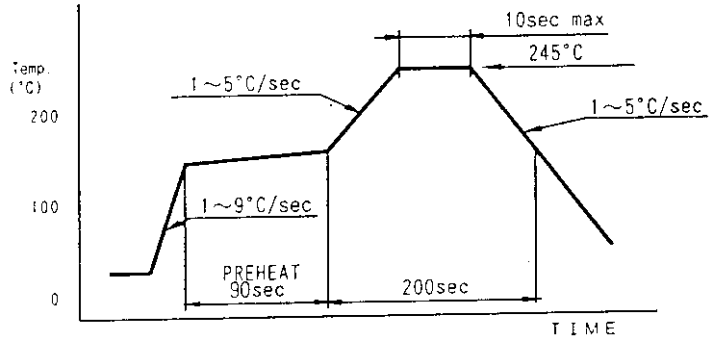
17. Ultrasonic-wave cleaning
- Frequency : 25±4 , 40±4 KHz
- Output : 10~30 W/l
- Time : 60±5 sec
- Cleaning liquid : IPA(Isopropyl alcohol),PINE ALPHA ST-100S

18. Soldering condition

Soidering Condition	Temperature (max)	Time (the number of times)
Refrow	260°C	10sec × 2
Flow	260°C	10sec
Soldering Iron	260°C	6sec

- Frequency : $\pm 2.0 \times 10^{-6}$ max
- ESR : ±15% max or 2Ω max whichever bigger

Reflow Profile



DATE	APPROVED	CHECKED	CHECKED	DRAWN	REVISED
00 Nov. 30 1998	H. Eguchi	H. Uozumi	M. Nakayama	M. Omine	00

NIKKO DENSI CO., LTD

SPECIFICATION OF CRYSTAL UNIT	Spec No.QA0510500	Page 3/3

19. Test circuit and references
    5.1 Frequency and ESR : Fr meter
    5.2 Country of manufacture : Japan
        Place of manufacture : Nikko Denshi Co.,Ltd.
    5.3 Net weight : 0.06g/unit

20. Marking
    Marked by lazer sculpture.
    Leave space 0.5mm each from longer ends and 0.3mm each from shortor ends

Nominal Frquency, Number of Group
Munufacture Code, Date Code

For example

NKD 8 K

Mounth code(A to M,except I)
Last digit of year
Manufacture code

21.Packing
    21.1 Taping specifications : as per XZ-0675
    21.2 SMD packing specifications : as per XZ-0676
    21.3 SMD packaging specifications : as per XZ-0677

22.Taping
    22.1 Reel dimensions : as per X0-2163
    22.2 Carrier tape dimensions : as per X0-2166

23. Storage
    Units are to be kept in temperature between -40 to +85°C,humidity below 75%,dark,and clean place.

24.These units are not under control of COCOM(Nothing to do with COCOM)

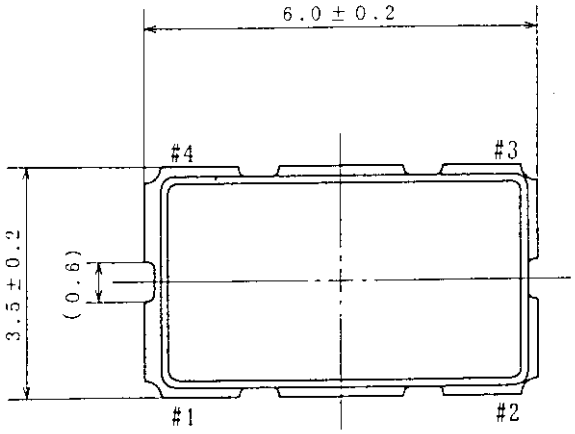
25.These units do not contain illegal materials nor legulated materials.

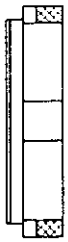
26.When useing, please pay attention to the Reliability Test Conditions and Soldering Conditions.

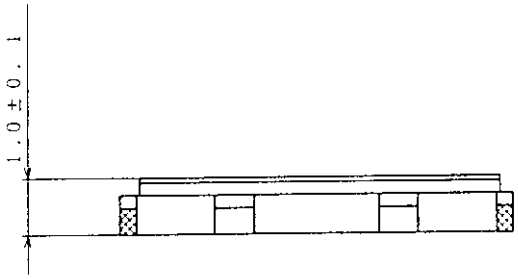
27.These units do no include bromine type uninflammable materials.

	DATE	APPROVED	CHECKED	CHECKED	DRAWN	REVISED
00	Nov. 30 1998		H. Horiuchi	M. Nakayama	M. Omine	00

NIKKO DENSI CO., LTD







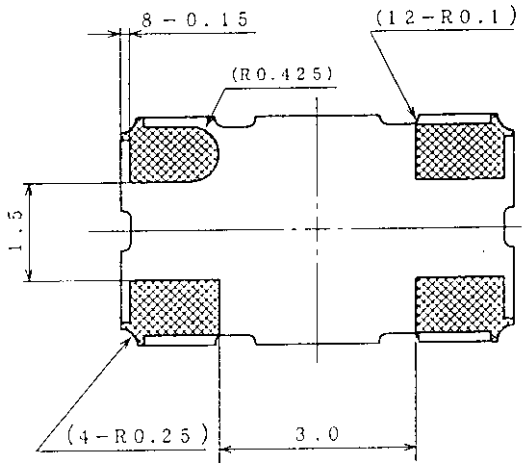
CONNECTION

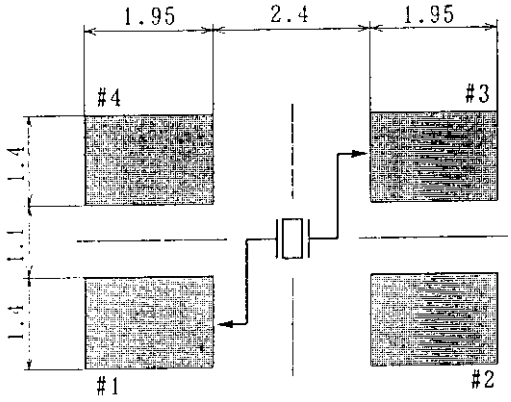
#1 : INPUT

#2 : NC

#3 : OUTPUT

#4 : GROUND





SUGGESTED PADS (TOP VIEW)

※Tolerance shall be ±0.2mm unless otherwise specified

UNITS : mm

APPROVED	CHECKED	RESPONSIBLE	DRAWN	D.DATE		TITLE	TOP−B OUTLINE DIMENSION	
				00	'96. 2. 5			
				03	'96. 6.14	DRAWING NO	XM−4053	03

NIKKO DENSHI CO., LTD

ROHM | Products Semiconductor IC | Type BH4435FV | Page 1 8

構　造／STRUCTURE　シリコンモノリシック集積回路 ／Silicon Monolithic Integrated Circuit

型　名／TYPE　**BH4435FV**

製品名／PRODUCT SERIES　温度センサー内蔵　水晶発振用IC ／Crystal oscillator IC, temperature sensor is built in.

外形図／PACKAGE OUTLINES　図－1（プラスチックモールド）／*Figure 1* (Plastic Mold)

回路図／BLOCK DIAGRAM　図－2／*Figure 2*

機　能／FUNCTIONS
- 発振回路及び温度センサー内蔵 ／Oscillator circuit, temperature sensor circuit are built in.
- 広い動作電圧範囲(2.7～5.5V) ／Wide voltage operation (2.7～5.5V).
- 低消費電流(1.35mA TYP Vcc=3.0V). ／Low current (1.35mA TYP Vcc=3.0V).
- 小型パッケージ:SSOP-B8 ／Small package:SSOP-B8

発振部／Oscillator section
- 20MHzまでの水晶発振に対応。 ／Crystal oscillator deal to 20MHz.
- 発振起動時間が短い(1.5mS TYP Vcc=3.0V)。 ／Stertup time is short (1.5mS TYP Vcc=3.0V).
- 電源電圧変動に対して安定。 ／It works a stability to voltage chenge.

温度センサー部／Temperature sensor section
- 温度特性のﾘﾆｱﾘﾃｨが良い。 ／A lenearity of temperature charecteristic is good.
- 温度傾度 6.0mV/℃ ／Temperature coefficent 6.0mV/℃.

用　途／USE
- TCXO等,温度補償の必要な発振回路。 ／TCXO, on oscillator which need temperature compensation.

使用上の注意
応用回路例は推奨すべきものと確信しておりますが，御使用に当たっては更に特性の御確認を十分に願います。
外付回路定数を変更して御使用になる時は，静特性のみならず過渡特性も含め外付部品及び当社ＩＣのバラツキ等を考慮して十分なマージンを見て決定して下さい。
また，特許権に関しましては当社では十分な確認は出来ておりませんので御了承ください。

本製品は，一般的な電子機器への使用を意図しています。
極めて高度な信頼性が要求され，その製品の故障や誤動作が直接人命に関わるような機器・装置へのご使用を検討される際は，事前に弊社営業窓口までご相談願います。

本仕様に記載しております応用回路等は製品の特性及び性能を引き出す上で性格かつ信頼できるものと確信しております。
ただしその使用に起因する回路上及び工業所有権に関する諸問題につきましては当社は一切その責任は負いません。

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Design	Check	Approval	Date	Specification
			ROHM CO., LTD.	Specification No.

動作範囲／OPERATING RANGE

項目 Parameter	記号 Symbol	定格 Limits	単位 Unit	条件 Conditions
動作温度範囲 Operating temperature range	T_{opr}	−40 ～ +85	℃	
動作電源電圧範囲 Operating supply voltage range	V_{BAT}	2.7 ～ 5.5	V	

絶対最大定格／ABSOLUTE MAXIMUM RATINGS

Ta=25℃、測定回路において／Ta=25℃, In test circuit

項目 Parameter	記号 Symbol	定格 Limits	単位 Unit	条件 Conditions
電源電圧 Supply voltage	V_{DD}	−0.3～+7.0	V	
入力電圧 Input voltage	V_{DUT}	−0.3～V_{DD}+0.3	V	
出力電圧 Output voltage	V_{OUT}	−0.3～V_{DD}+0.3	V	
出力電流 Output current	I_{OUT}	±10.0	mA	
許容損失 Power dissipation	T_{PT}	300	＊ mW	(注1) (NOTE1)
保存温度範囲 Storage temperature	T_{stg}	−55 ～ +125	℃	

(注1) ＊Ta=25℃以上で使用する場合は，1℃につき3.0mWを軽減する。
(NOTE1) To use at a temperature higher than Ta=25℃, derate 3.0mW per 1℃.

電気的特性／ELECTRICAL CHARACTERISTICS

特に指定のないかぎり，Ta=25℃, V_{DD}=3.0V／Unless otherwise specified, Ta=25℃, V_{DD}=3.0V

発振部／Oscillator section

項目 Parameter	記号 Symbol	規格値 Limits 最小 Min.	標準 Typ.	最大 Max.	単位 Unit	条件 Conditions	測定回路 Test cir.
発振部動作電流 Oscillator working current	I_{CC2}	--	1.25	1.6	mA	発振周波数 14.4MHz ／Osillator frequency 14.4MHz 負荷容量 10KΩ//10pF Load 10KΩ//10pF	1
発振出力電圧 Oscillator output voltage	V_{OUT}	0.8	1.35	--	V_{P-P}	発振周波数 14.4MHz ／Osillator frequency 14.4MHz 負荷 10KΩ//10pF Load 10KΩ//10pF	1
発振起動時間 Oscillator start up time	T_{ST}	--	2.5	--	mS		2

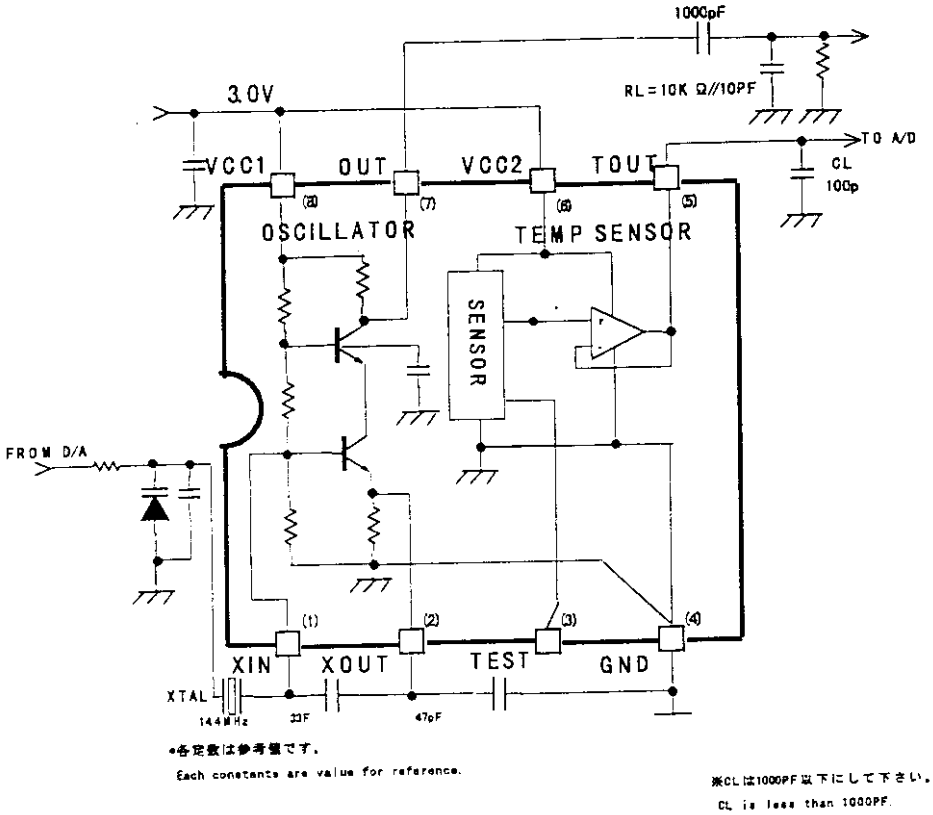
センサー部／Sensor section

項目 Parameter	記号 Symbol	規格値 Limits 最小 Min.	標準 Typ.	最大 Max.	単位 Unit	条件 Conditions	測定回路 Test cir.
センサー部電流 Sensor current	I_{CC1}	--	90	120	μA		1
出力電圧 1 Output voltage 1	V_{O1}	1.77	1.790	1.81	V	Ta=25℃	1
出力電圧 2 Output voltage 2	V_{O2}	--	2.091	--	V	Ta=75℃	1
出力電圧 3 Output voltage 3	V_{O3}	--	1.488	--	V	Ta=−25℃	1
負荷安定度 Load stability	V_R	--	0	1.0	mV	負荷 10KΩ～∞ Load 10KΩ～∞	1
温度傾斜 Temperature slope	V_T	--	6.0	--	mV/℃	Ta=−40～85℃	1

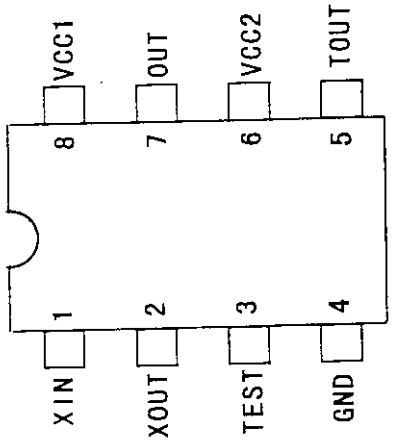
Date | Specification

ROHM CO., LTD. | Specification No.

ブロック図&応用例／BLOCK DIAGRAM & APPLICATION CIRCUIT

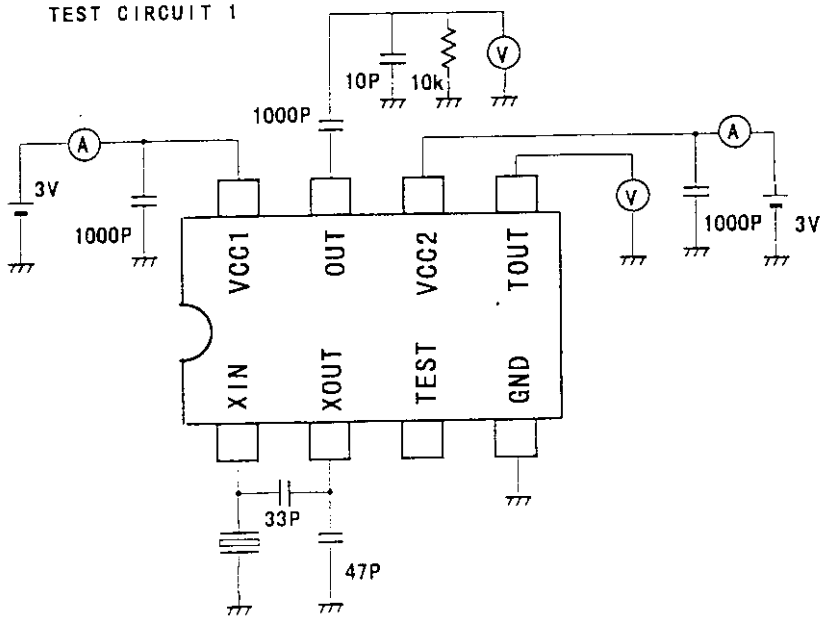


ピン配置図／PIN ARRENGMENT

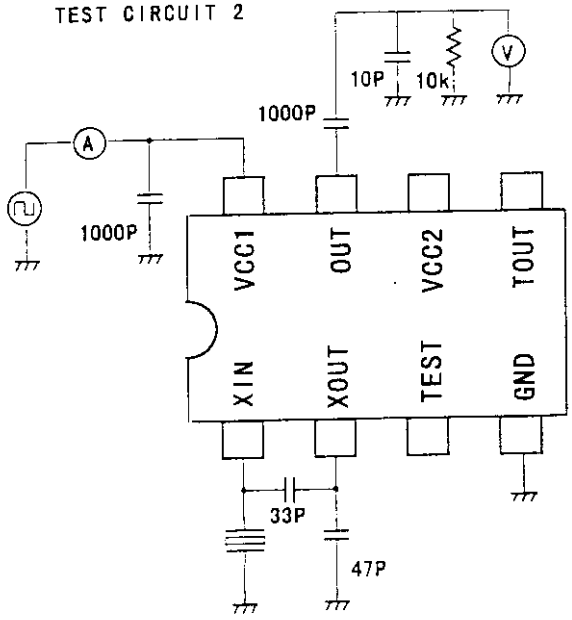


Date	Specification
ROHM CO., LTD.	Specification No.

測定回路 1
TEST CIRCUIT 1



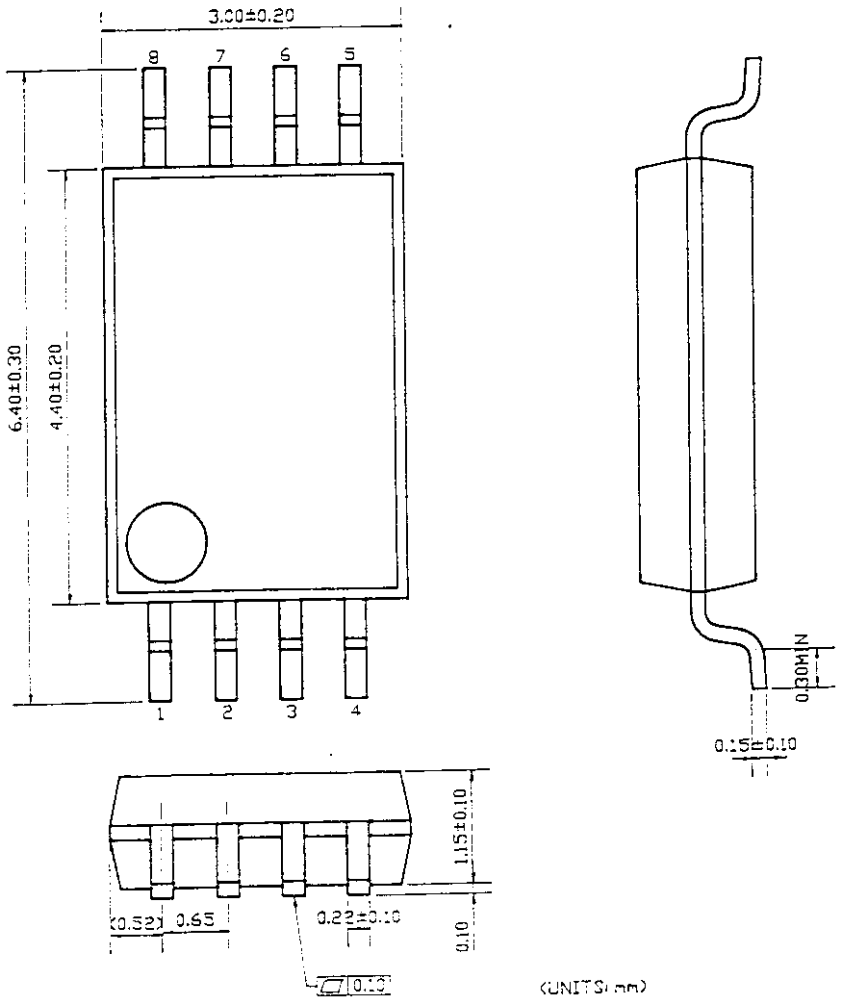
測定回路 2
TEST CIRCUIT 2



Date	Specification
ROHM CO., LTD.	Specification No.

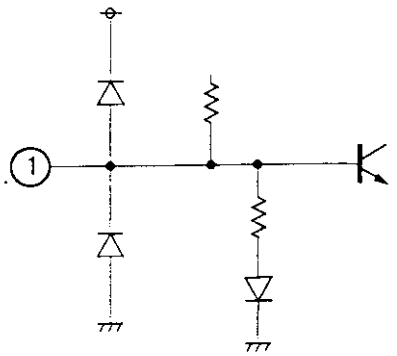
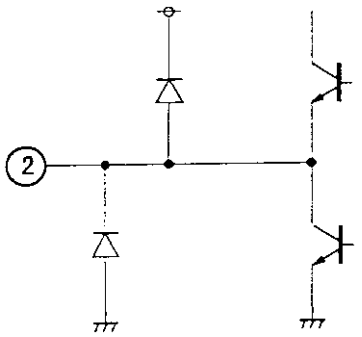
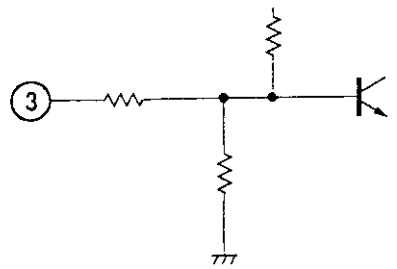
外形寸法図／PACKAGE OUTLINES (mm)

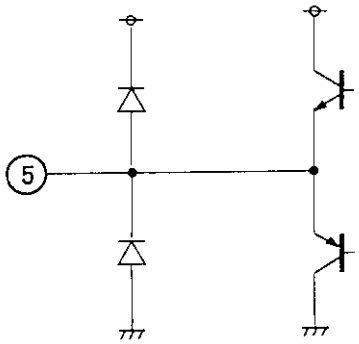
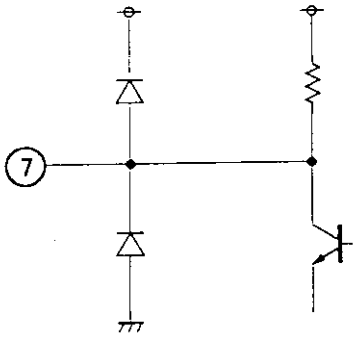
図－2／Figure 2



Date	Specification
ROHM CO., LTD.	Specification No.

端子説明／EXPLANATION FOR TERMINAL FUNCTION

番号 No.	端子名 Name	端子説明 Description	内部周辺回路 Equivalent circuit
1	XIN	発振入力端子 Oscillator input terminal コンデンサーとクリスタルを接続します。 Connect capacitor and crystal.	
2	XOUT	発振出力端子 Oscillator output terminal コンデンサーを接続します。 Connect capacitor.	
3	TEST	テスト端子 Test terminal この端子はオープンにして下さい。 Open this terminal.	

番 号 No.	端子名 Name	端 子 説 明 Description	内 部 周 辺 回 路 Equivalent circuit
4	GND	グランド端子 GND terminal	
5	TOUT	温度センサー出力端子 Temperature sensor output terminal	
6	Vcc2	センサー部の電源端子 Power supply terminal to sensor section	
7	OUT	TCXO出力端子 TCXO output terminal	

Date	Specification
ROHM CO., LTD.	Specification No.

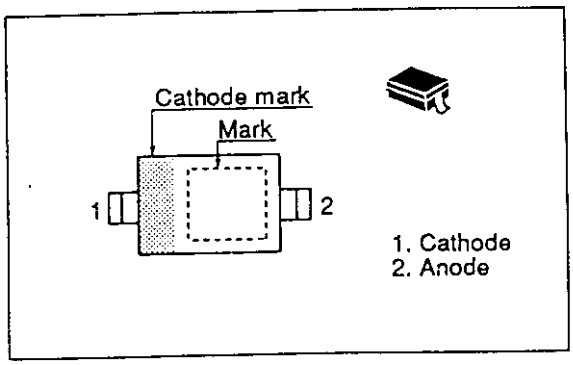
HVU358

Variable Capacitance Diode for VCO

Features

- Low series resistance. (r_s=0.4Ω max)
- High capacitance ratio. (n=2.0min at C1/C4)
- Good linearity of C-V curve.
- Ultra small Resin Package (URP) is suitable for surface mount design.

Outline



Ordering Information

Type No.	Laser Mark	Package Code
HVU358	R	URP

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	15	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I_{R1}	—	—	10	nA	V_R = 15 V
	I_{R2}	—	—	100		V_R = 15 V , Ta = 60 °C
Capacitance	C_1	19.0	—	21.0	pF	V_R = 1 V , f = 1 MHz
	C_4	8.5	—	10.0		V_R = 4 V , f = 1 MHz
Capacitance ratio	n	2.0	—	—	—	C_1 / C_4
Series resistance	r_s	—	—	0.40	Ω	V_R = 1 V , f = 470MHz

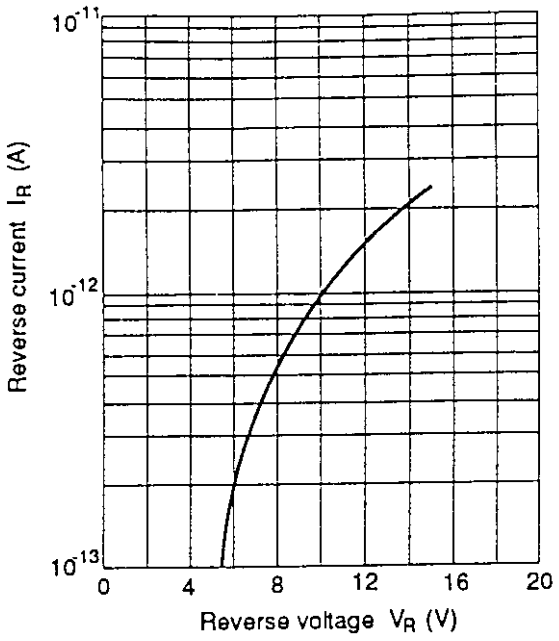


Fig.1 Reverse current Vs. Reverse voltage

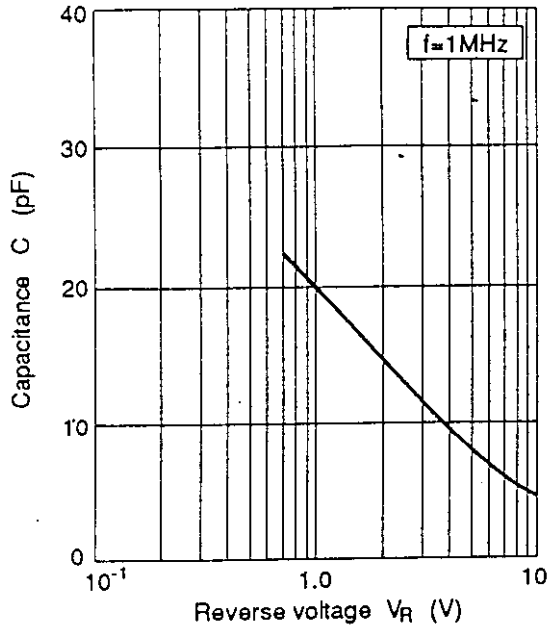


Fig.2 Capacitance Vs. Reverse voltage

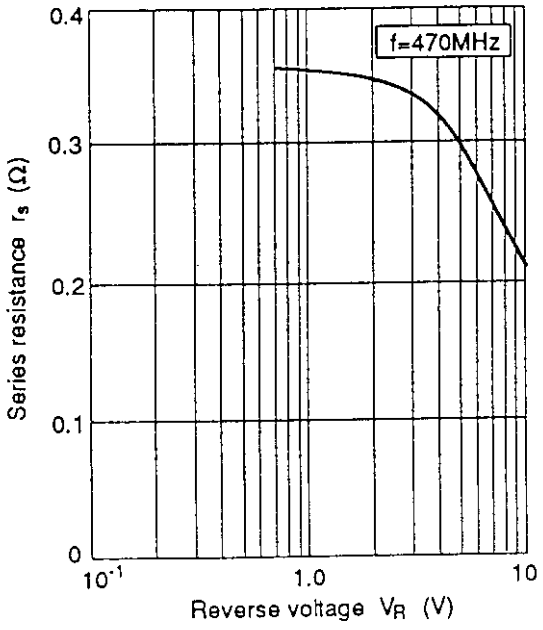


Fig.3 Series resistance Vs. Reverse voltage

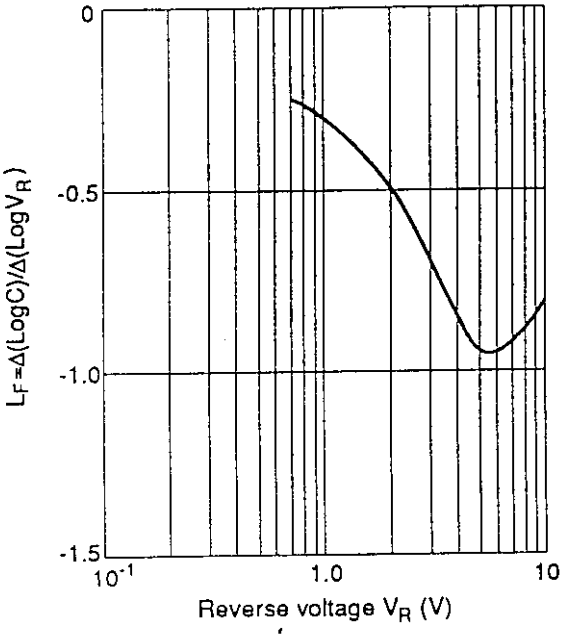


Fig.4 Linearity factor Vs. Reverse voltage

INTEGRATED CIRCUITS

DATA SHEET

UMA1015AM
Low-power dual frequency synthesizer for radio communications

1997 Sep 03

Product specification
Supersedes data of 1997 Jun 10
File under Integrated Circuits, IC17

Philips Semiconductors

PHILIPS

Low-power dual frequency synthesizer for radio communications

UMA1015AM

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports
- Crystal input frequency signal inverted and buffered output on separate pin.

APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

GENERAL DESCRIPTION

The UMA1015AM is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz.

The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 (I_{SET}). The BiCMOS device is designed to operate from 2.7 V (3 NiCd cells) to 5.5 V at low current. Digital supplies V_{DD1} and V_{DD2} must be at the same potential. The charge pump supply (V_{CC}) can be provided by an external source or on-chip voltage doubler. V_{CC} must be equal to or higher than V_{DD1}.

Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.7	–	6.0	V
V_{CCvd}	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DD1} + I_{DD2} + I_{CC}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	8.7	–	mA
$I_{DDpd} + I_{CCpd}$	total current in power-down mode	doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	3	–	µA
I_{DDpd}	current in power-down mode from supply V_{DD1} and V_{DD2}	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.25	–	mA
f_{RF}	RF input frequency for each synthesizer		50	–	1100	MHz
f_{XTALIN}	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency		–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency		–	750	–	kHz
T_{amb}	operating ambient temperature		-30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1015AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

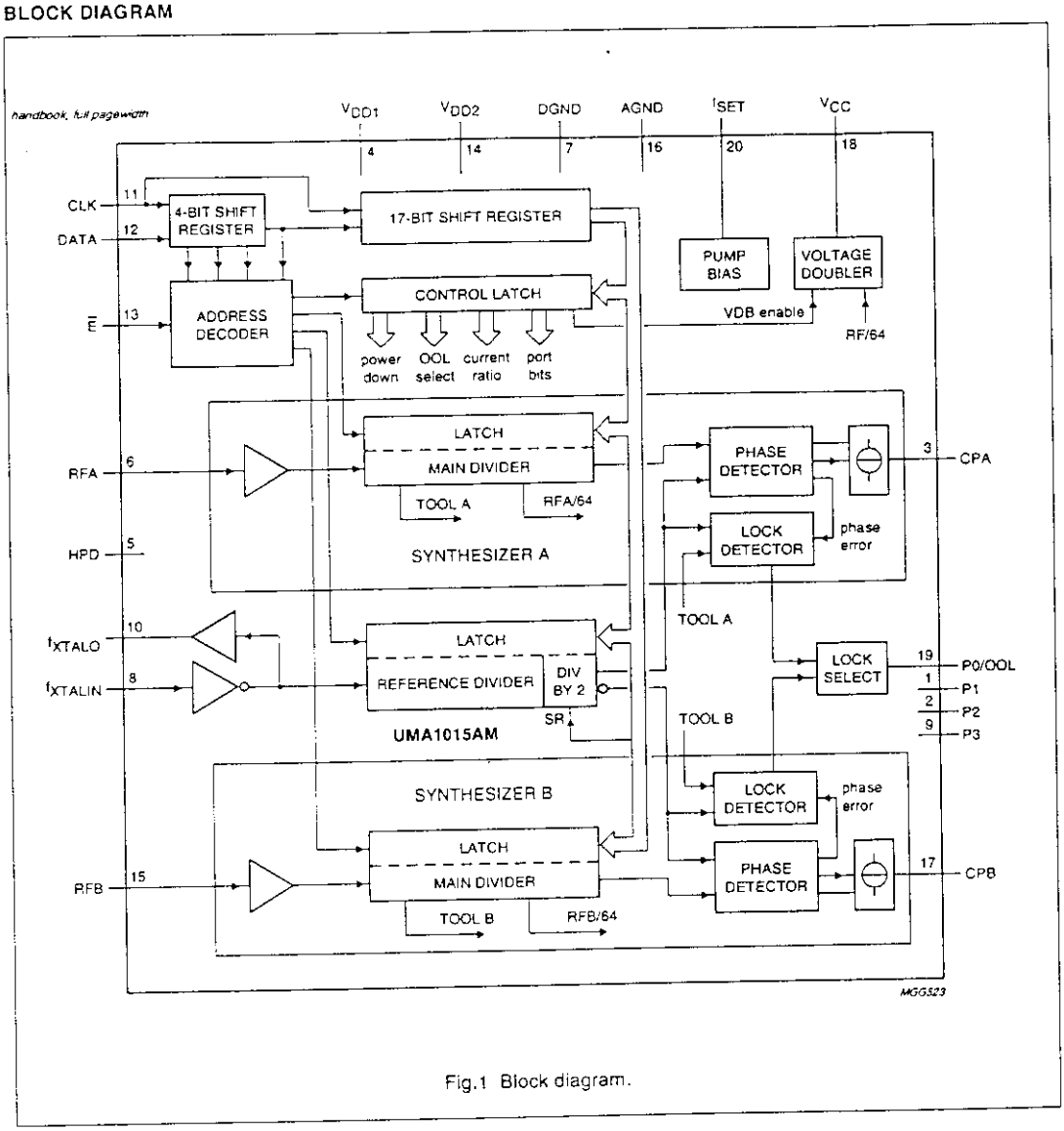


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge pump output synthesizer A
V_{DD1}	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common crystal frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	open-drain output of f_{XTAL} signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input (active LOW)
V_{DD2}	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I_{SET}	20	regulator pin to set charge pump currents

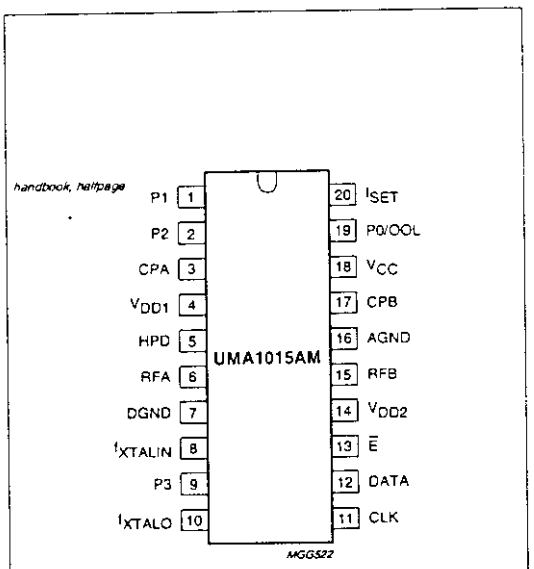


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f_{XTALIN} drives a pre-amplifier to provide the clock input for the reference divider. This clock signal is also inverted and output on pin f_{XTALO} (open drain). A crystal connected between f_{XTALIN} and f_{XTALO} with suitable feedback components can be used to make an oscillator. An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half the frequency of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

Table 1 Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature-independent voltage of 1.1 V is generated. R_{SET} should be between 12 and 60 kΩ.
The charge pump current, I_{CP}, can be programmed to be either ($12 \times I_{SET}$) or ($24 \times I_{SET}$) with a maximum of 2.3 mA.
The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply, V_{CC}, which helps to reduce the interference on the charge pump output from other parts of the circuit. V_{CC} can be higher than V_{DD1} if a wider range on the VCO input is required. V_{CC} must not be less than V_{DD1}.

Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply V_{DD1}, and is internally limited to a maximum output of 6 V.
An external capacitor is required on pin V_{CC} for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit VDON to logic 0, in order to allow an external charge pump supply to be used.

Out-of-lock indication/output ports

There is a common lock detector on-chip for the synthesizers. The lock condition of each, or both loops, is output via an open-drain transistor which drives pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4).

An out-of-lock condition is flagged when the phase error is greater than T_{OOL}, which is approximately 30 ns.
The out-of-lock flag is only released after the first reference cycle where the phase error is less than T_{OOL}.
The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as a port output. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and $\overline{E}$ (enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive (HIGH). This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 (f_{XTALIN}) for correct programming.

Data format

Data is entered with the most significant bit first.
The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch.
To ensure that data is correctly loaded on first power-up, $\overline{E}$ should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

Table 2 Bit allocation

FIRST	REGISTER BIT ALLOCATION																					LAST
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS			
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT															MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT															MB0	0	1	1	0
	RESERVED FOR TEST[1]																0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	sPBF	0	0	1	0	0	0

Note

1. The test register should not be programmed with any other values except all zeros for normal operation.

Table 3 Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
sPBF	software power-on for f_{xtal} buffer (1 = buffer on)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to I_{SET} ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

Table 4 Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

Table 5 Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

Table 6 Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits sPDA and sPDB, logic 0 = power-down).

The synthesizers are powered up when both hardware and software Power-down signals are at logic 1. When only one synthesizer is powered down, the functions common to both will be maintained (independent of the state of sPBF). When both synthesizers are powered down, the f_{xtal} buffer can be maintained in an active state by setting sPBF to logic 1. This will allow any system clock derived from the f_{XTALO} buffered output to remain on in power-down. Note that sPBF is independent of the state of HPD. When both synthesizers are switched off, the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}, V_{DD2}	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
V_{CC}	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
ΔV_{CC-DD}	difference in voltage between V_{CC} and V_{DD1}, V_{DD2}	−0.3	+6.0	V
V_n	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	V_{DD1} + 0.3	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	V_{CC} + 0.3	V
ΔV_{GND}	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−30	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 6.0 V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; (V_{DD1}, V_{DD2} and V_{CC}) voltage doubler disabled, external supply on V_{CC}						
V_{DD1}, V_{DD2}	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 3 V	–	8.7	–	mA
		f_{XTAL} = 12.8 MHz; both synthesizers on; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	12.5	mA
I_{DDpda}, I_{DDpdb}	total digital supply current from V_{DD1} and V_{DD2} with one synthesizer in power-down mode	f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 3 V	–	5.0	–	mA
		f_{XTAL} = 12.8 MHz; one synthesizer powered down; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	7.5	mA
$I_{DD(xtal)}$	digital supply current from V_{DD1} with both synthesizers powered down and crystal buffer on	f_{XTAL} = 12.8 MHz; V_{HPD} = 0 V; sPBF = 1; $V_{DD1} = V_{DD2}$ = 3 V	–	0.5	–	mA
		f_{XTAL} = 12.8 MHz; V_{HPD} = 0 V; sPBF = 1; $V_{DD1} = V_{DD2}$ = 5.5 V	–	–	1.15	mA
I_{DDpd}	digital supply current in power-down mode	both synthesizers powered down; V_{HPD} = 0 V; sPBF = 0	–	–	60	µA
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	6.0	V
I_{CC}	charge pump supply current	both synthesizers on and in lock; f_{ref} = 12.5 kHz	–	–	25	µA
I_{CCpd}	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	µA
Voltage doubler enabled						
I_{DD}	total digital supply current from V_{DD1} and V_{DD2}	f_{XTAL} = 12.8 MHz; both synthesizers on and in lock; V_{DD1} = 3 V; f_{RF} = 900 MHz	–	9.2	12	mA
I_{DDpd}	total digital supply current in power-down mode from V_{DD1} and V_{DD2}	both synthesizers powered down; V_{DD1} = 3 V; V_{HPD} = 0 V; sPBF = 0	–	0.25	0.4	mA
V_{CCvd}	charge pump supply voltage	DC current drawn from V_{CC} = 50 µA; f_{RF} > 100 MHz	4.2	$2V_{DD1} - 0.6$	6.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RF main divider input; RFA and RFB						
f_{RF}	RF input frequency		50	–	1100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	R_s = 50 Ω; f_{RF} = 400 to 1100 MHz	50	–	250	mV
		R_s = 50 Ω; f_{RF} = 80 to 400 MHz	150	–	400	mV
		R_s = 50 Ω; f_{RF} = 50 to 80 MHz	225	–	400	mV
Z_I	input impedance (real part)	f_{RF} = 1 GHz; indicative, not tested	–	300	–	Ω
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{pm}	principle main divider ratio		512	–	131071	
Reference divider input; f_{XTALIN}						
f_{XTALIN}	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
Z_I	input impedance (real part)	f_{XTALIN} = 12.8 MHz; indicative, not tested	–	10	–	kΩ
C_I	input capacitance	indicative, not tested	–	1	–	pF
R_{rd}	reference divider ratio		8	–	4095	
Charge pump current setting resistor input; I_{SET}						
V_{SET}	voltage output on I_{SET}	R_{SET} = 12 to 60 kΩ	–	1.1	–	V
Charge pump outputs; CPA and CPB						
I_{cp}	charge pump sink or source current	R_{SET} = 15 kΩ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	1.3	1.75	2.3	mA
		R_{SET} = 15 kΩ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$; V_{cp} = 0.4 V to V_{CC} – 0.5 V	0.7	0.9	1.2	mA
I_{LI}	charge pump off leakage current	V_{cp} = 0.4 V to V_{CC} – 0.5 V	–5	±1	+5	nA
Logic input signal levels; DATA, CLK, $\overline{E}$ and HPD						
V_{IH}	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	V_{DD1} + 0.3	V
V_{IL}	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
I_{bias}	input bias currents	at logic 1 or logic 0	–5	–	+5	μA
C_I	input capacitance	indicative, not tested	–	1	–	pF
Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and f_{XTALO} - open drain outputs						
V_{OL}	LOW level output voltage	I_{sink} < 0.4 mA	–	–	0.4	V

SERIAL TIMING CHARACTERISTICS

V_{DD1} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r, t_f	input rise and fall times	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	−20	–	–	ns
t_W	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

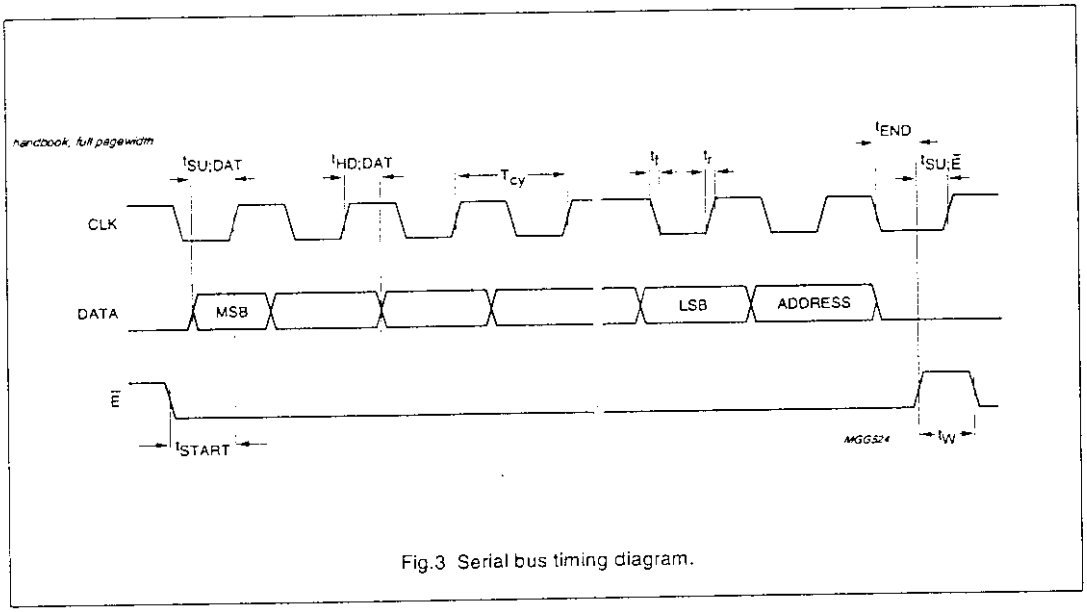
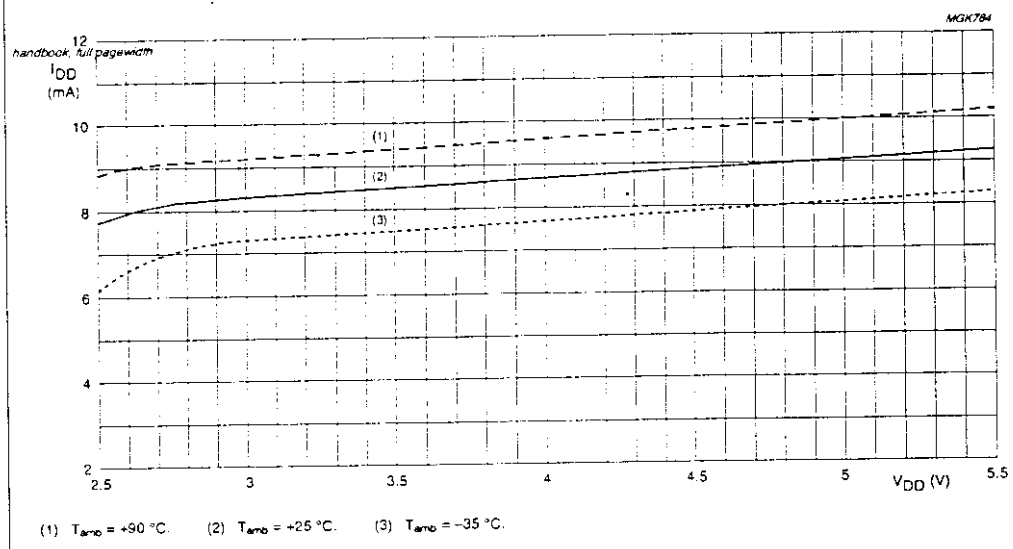


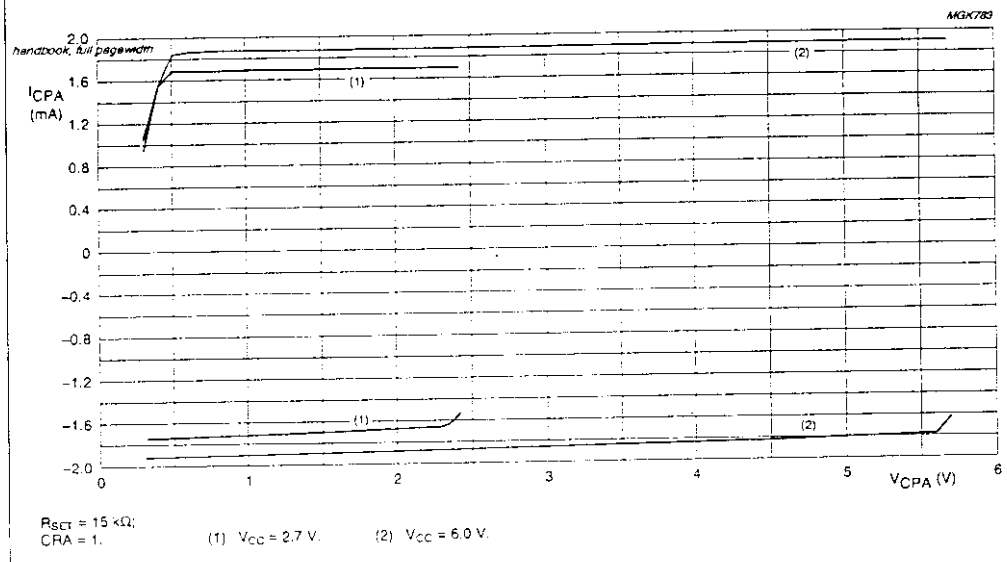
Fig.3 Serial bus timing diagram.

TYPICAL PERFORMANCE CHARACTERISTICS



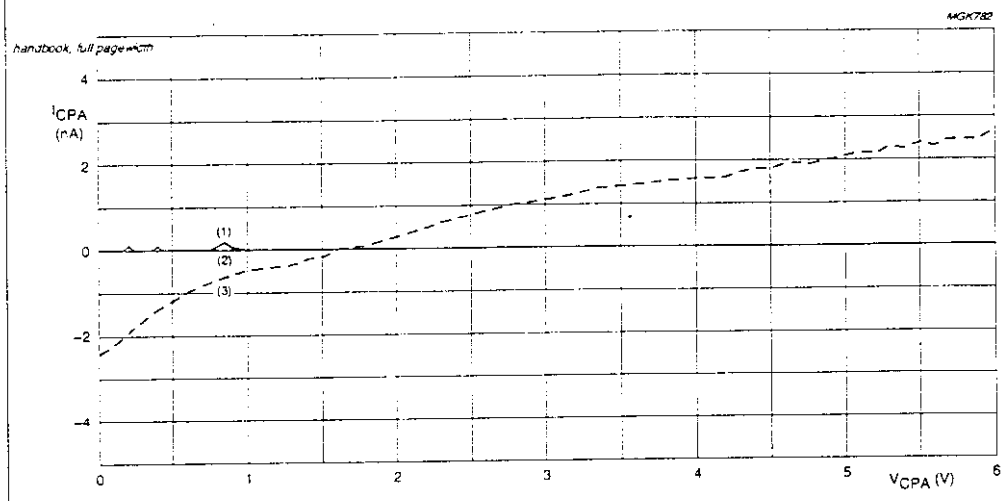
(1) T_{amb} = +90 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = −35 °C.

Fig.4 Typical I_{DD} as a function of V_{DD} with both synthesizers on and voltage doubler disabled.



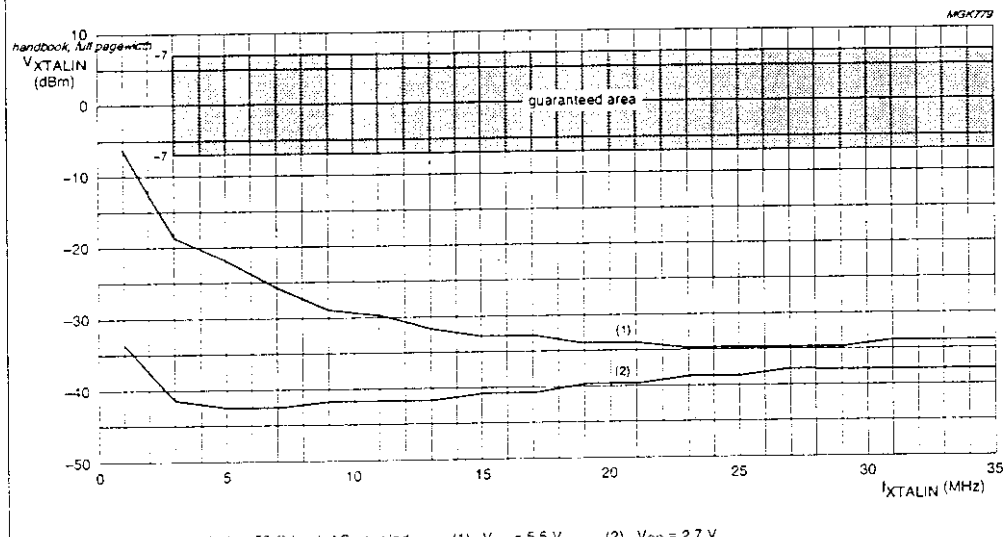
R_{SET} = 15 kΩ; CRA = 1. (1) V_{CC} = 2.7 V. (2) V_{CC} = 6.0 V.

Fig.5 Typical charge pump current as a function of CPA voltage with T_{amb} = 25 °C.



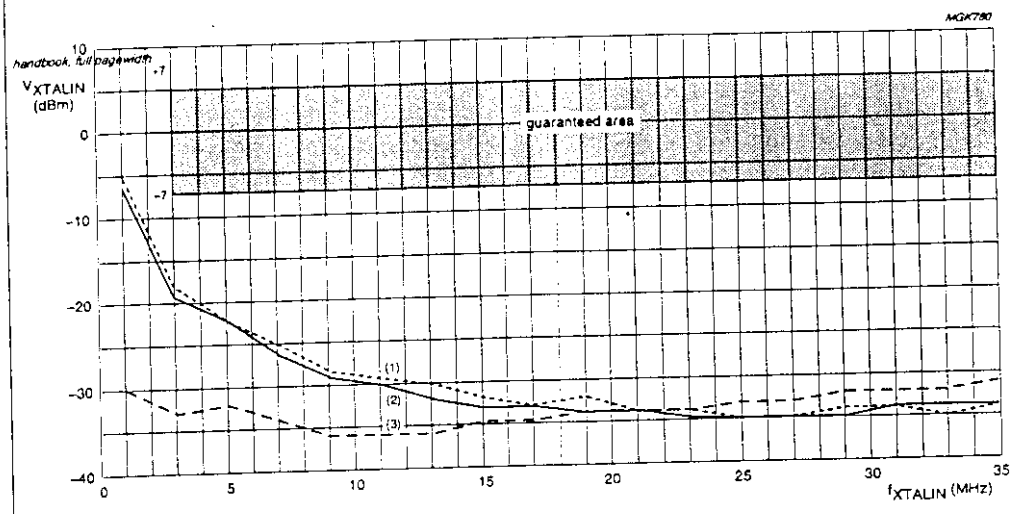
$V_{CC} = V_{DD} = 6$ V; $R_{SET} = 15$ kΩ; CRA = 1. (1) $T_{amb} = +25$ °C. (2) $T_{amb} = -35$ °C. (3) $T_{amb} = +90$ °C.

Fig.6 Typical charge pump 3-state current as a function of CPA voltage.



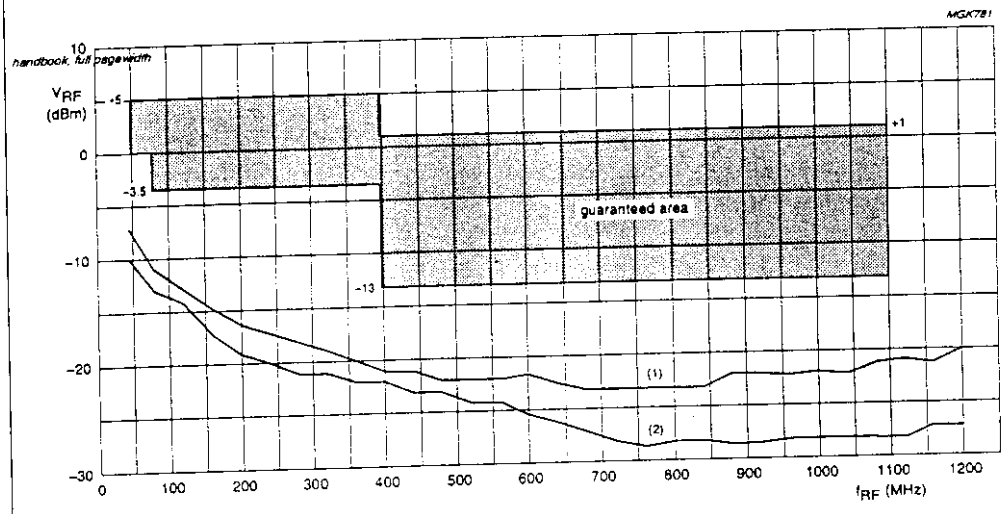
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled. (1) $V_{DD} = 5.5$ V. (2) $V_{DD} = 2.7$ V.

Fig.7 Typical crystal input sensitivity as a function of input frequency with $T_{amb} = 25$ °C.



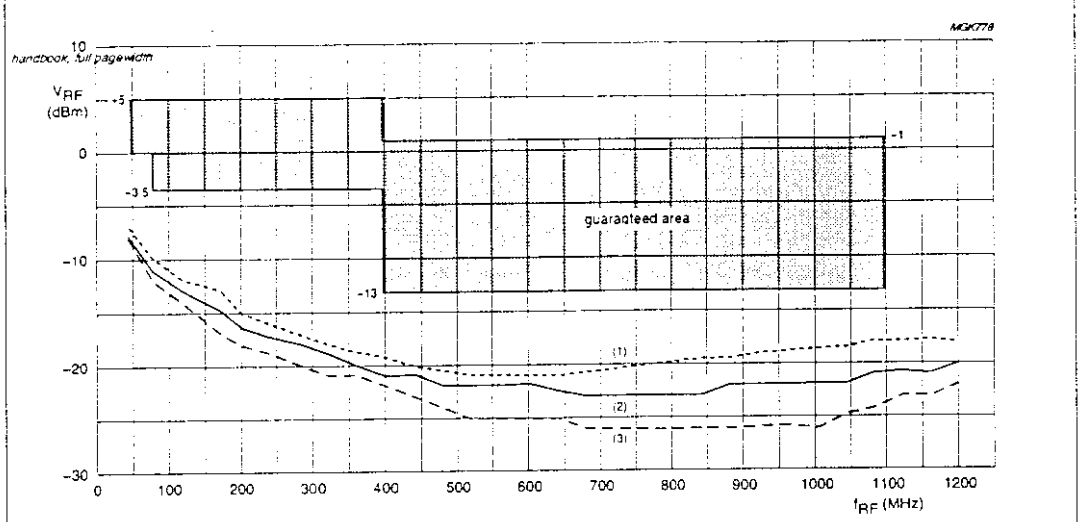
f_{XTALIN} externally terminated by 50 Ω load; AC-coupled. (1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.8 Typical crystal input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



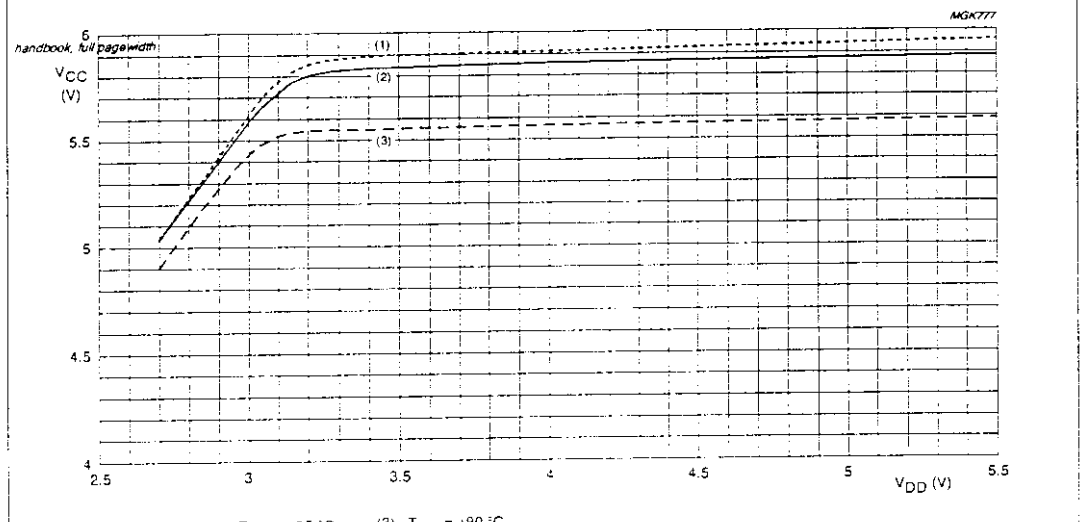
RF input externally terminated by 50 Ω load; AC-coupled. (1) V_{DD} = 5.5 V. (2) V_{DD} = 2.7 V.

Fig.9 Typical RF input sensitivity as a function of input frequency with T_{amb} = 25 °C.



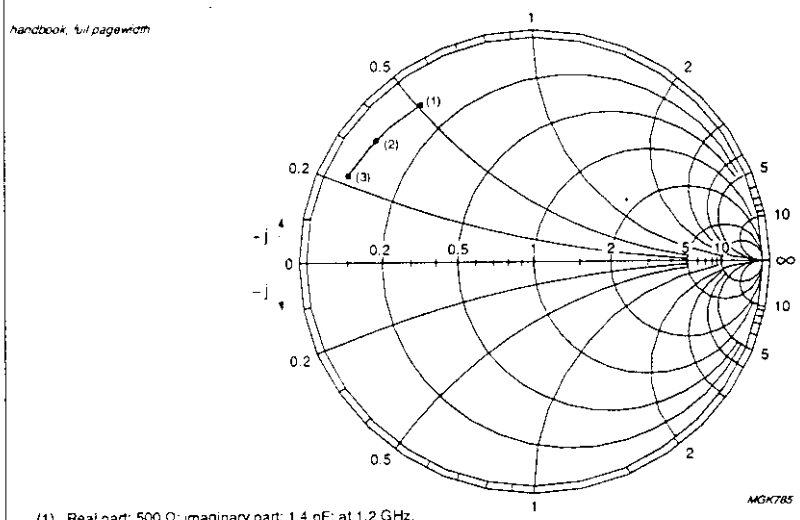
RF input externally terminated by 50 Ω load; AC-coupled. (1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.10 Typical RF input sensitivity as a function of input frequency with V_{DD} = 5.5 V.



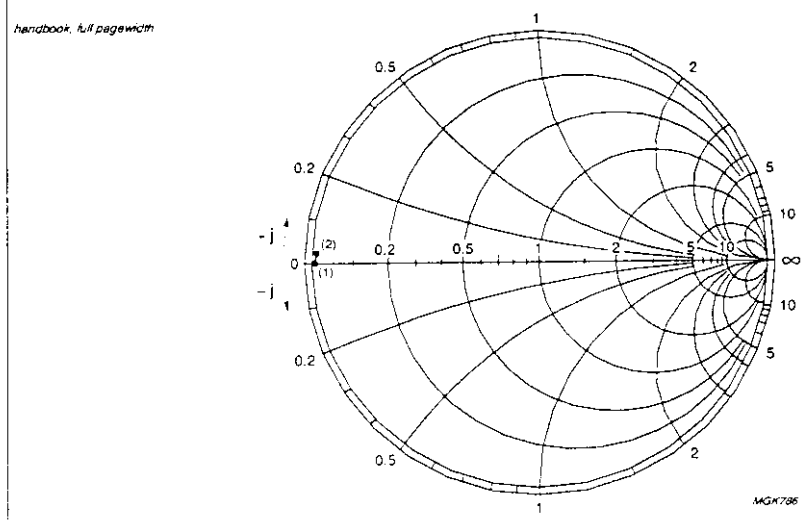
(1) T_{amb} = −35 °C. (2) T_{amb} = +25 °C. (3) T_{amb} = +90 °C.

Fig.11 Typical charge pump supply voltage as a function of V_{DD} voltage with voltage doubler enabled.



(1) Real part: 500 Ω; imaginary part: 1.4 pF; at 1.2 GHz.
(2) Real part: 800 Ω; imaginary part: 1.1 pF; at 1.0 GHz.
(3) Real part: 830 Ω; imaginary part: 0.9 pF; at 800 MHz.

Fig.12 Typical RF input admittance (IC powered on).



(1) Real part: 7.8 kΩ; imaginary part: 0.9 pF; at 3 MHz.
(2) Real part: 9.8 kΩ; imaginary part: 1.0 pF; at 35 MHz.

Fig.13 Typical crystal input admittance (IC powered on).

APPLICATION INFORMATION

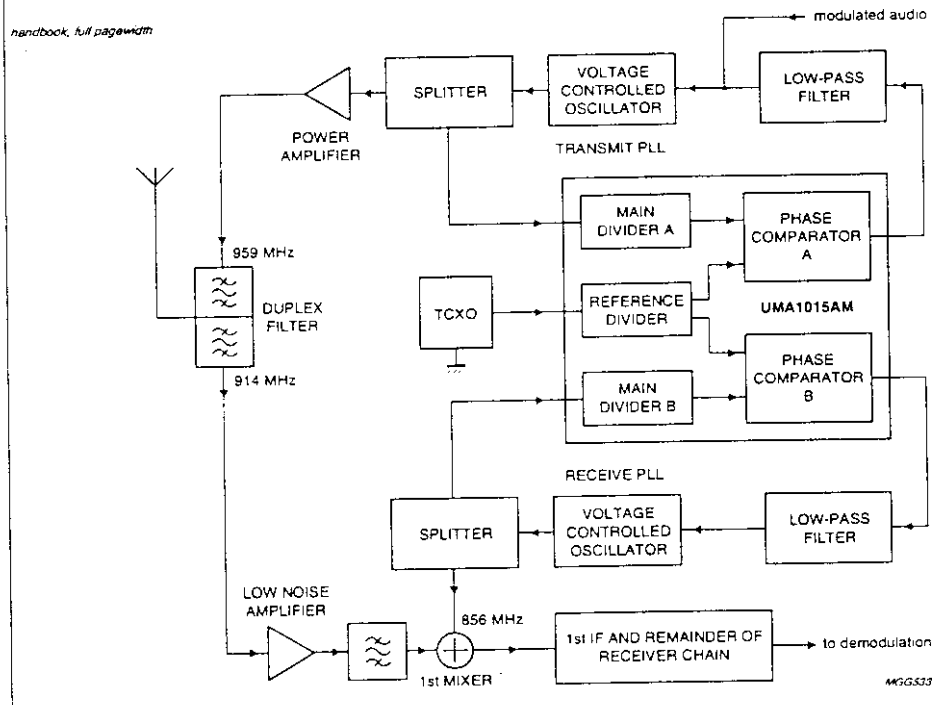


Fig.14 Typical application block diagram.

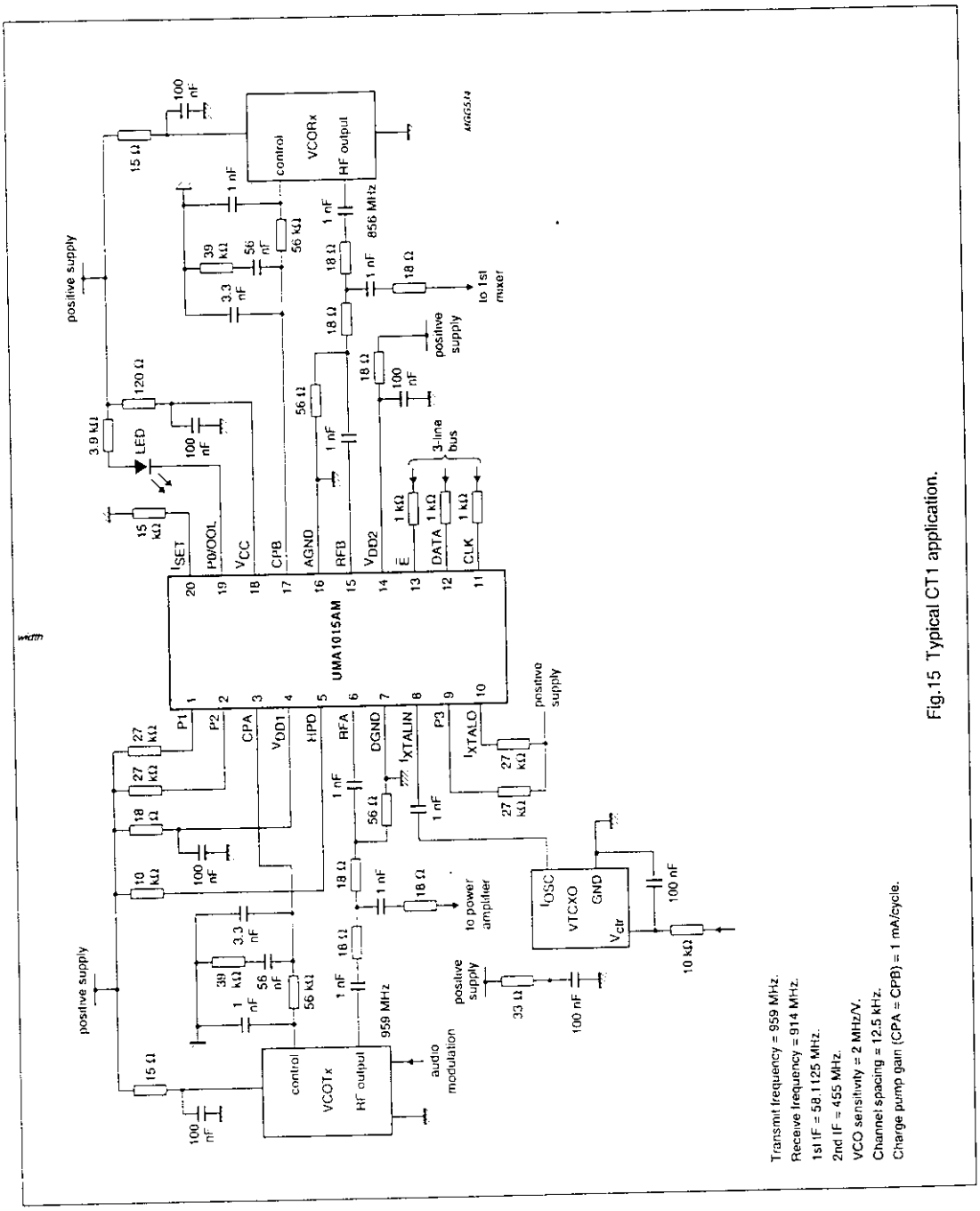
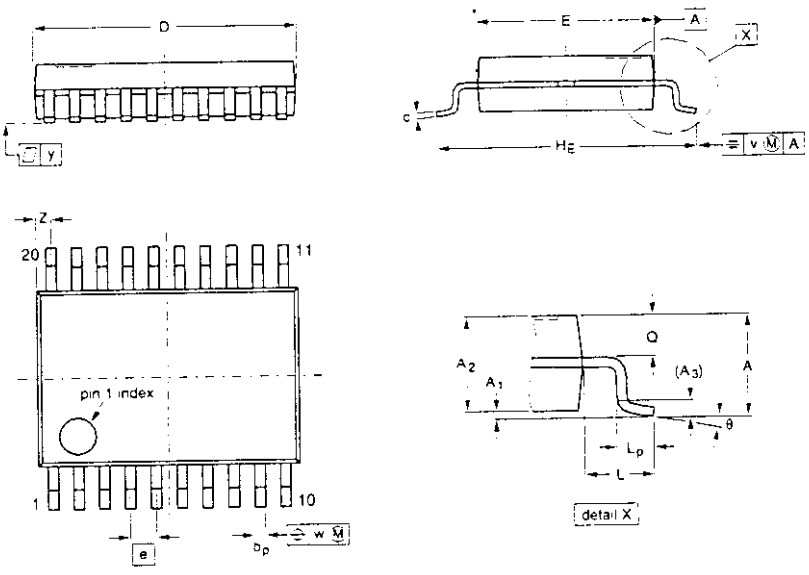


Fig.15 Typical CT1 application.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT266-1					~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

1. Application

This specification applies to the VCO IL108 for SHINTOM CO., LTD.

2. Name of product

FDK Corporation part number is IL108

3. Dimensions and marking

Dimensions and marking are shown in Fig. 1.

4. Appearance

VCO shall have no distortion, crack, stain and so on which will disfigure its appearance.

5. Absolute maximum rating (Ta=25℃)

No.	Item	Condition	Rating	Unit
1	Supply voltage		-0.3 ~ 5.0	V
2	Control voltage		-0.3 ~ 5.0	
3	Operating temperature range		-30 ~ +70	℃
4	Storage temperature range		-40 ~ +85	
5	Operating humidity range	Dew must not fall.	85 MAX	%RH
6	Storage humidity range	Dew must not fall.	95 MAX	

6. Promoted operating condition

No.	Item	Condition	Rating	Unit
1	Supply voltage		3.3 ± 0.16	V
2	Control voltage		1.0 ~ 2.8	

7. Electrical characteristics(Vcc=3.3V, Vc=1.9V, Ta=+25℃ unless otherwise specified)

No.	Item	Condition	Rating	Inspection
1	Oscillating frequency	Vcc=3.3V , Vc=1.0V	≦ 824.0 MHz	100 % inspection
		Vcc=3.3V , Vc=2.8V	≧ 849.0 MHz	
2	Control voltage sensitivity	Note 1	20.0~28.0MHz/V	
3	Power output	50Ω	-3.0±3.0dBm	
4	Supply current		≦ 8.0 mA	
5	S／N	fm=1kHz, Dev.=±3kHz, BW=50～15kHz Without vibration	≧ 36 dB	
6	Pushing figure	Vcc=3.3 ± 0.16 V	±0.5MHz	Sampling inspection
7	Frequency stability for temp.	-30 ～ +70℃	±3.0MHz	
8	Pulling figure	VSWR=2.0 at all phases	±1.5MHz	
9	C／N	Δf= 60kHz, BW=30kHz	≧ 70 dBc	
10	Spurious characteristic	till third harmonic	≧ 15 dBc	
11	Audio modulation sensitivity	fm=1kHz, 1Vp-p	10±2 kHz/Vp-p	
12	Audio modulation sensitivity deviation	824.0 ～ 849.0MHz	±10%	

Note 1) Cont. volt. sensitivity=(f(2.8)-f(1.0))/(2.8-1.0):[F(Vc):Oscillating frequency at Vc]

8. Reliability

Reliability assurance tests are shown below.

Group	Test item	n	Test condition	Measurement
I	Temperature cycle	11	-30℃ ⇔ RT ⇔ +100℃ (30min) (10min) (30min) 30cy	Electrical characteristic
II	Vibration	5 ↓ 5 ↓ 5	10 ~ 500Hz, 2G, 1oct/min X, Y, Z Direction, each 1 Hr	Electrical characteristic
	Constant acceleration		5000G, 1 min, Y Direction	Electrical characteristic
	Natural drop		On board 75 cm, each 1 time (X, Y, Z Direction)	Electrical characteristic
III	High temperature storage	11	+100 ℃, storage, 96 Hrs	Electrical characteristic
IV	High temperature bias	22	+ 85 ℃, bias, 96 Hrs	Electrical characteristic Appearance
V	High temperature and high humidity bias	22	+ 85 ℃, 85 %, bias, 96 Hrs	Electrical characteristic Appearance
VI	Low temperature storage	11	- 30 ℃, storage, 96 Hrs	Electrical characteristic
VII	Resistance to solvents	5	IPA 3times Dipping, 30sec each	Electrical characteristic Appearance

9. Product warranty

The VCO is guaranteed by the manufacturer FDK for a period of 12 months from the date of customer's purchase. However our guarantee does not cover damage cased by misuse or mishandling by the customer.

10. Inspection report

Inspection report shall be attached to the first lot only.
The following items will be included in our inspection report.

(1) Part product.
(2) Lot number.
(3) Test quantity.
(4) Summary of result.

11. Packaging

VCO is delivered in the embossed carrier tape for automatic mounting. (cf. BQ10006). Customer code, Part No., Quantity and Lot No. are indicated by label or printing on reel, dampproof bag, inner carton and outer carton.

FDK	PRODUCT	IL108	
CHECK	DATE	Jun. 7, 1997	
T. SATO	LOT No. /Q'TY		
	0001/1000		

[Taping]
- Tape break force : MIN. 10N
- Top cover tape strength : MIN. 10N
- Top cover tape peel force : 0.1~0.7N, at a peel speed of 300mm/min.
- Angle between the cover tape and the direction of during peel off : 160~180°

[Weight]
0.38g MAX. /pc.

12. Production location/ Manufacturing plant

1). Production location : Japan.

2). Manufacturing plant : Iwaki Electronics Co., Ltd.

13. Change specification.

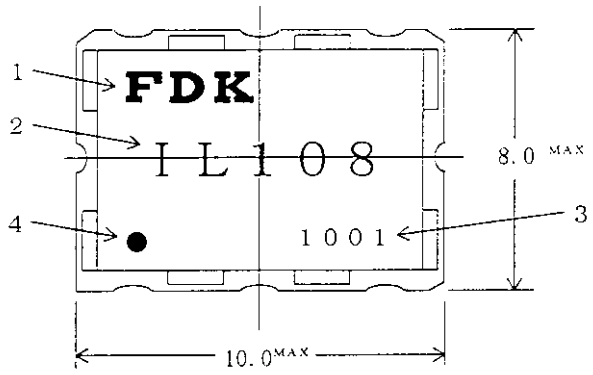
Whenever change or updating of the requirements in this specification is deemed necessary, decision of consent shall be made by FDK, sales agent and user.

FDK CORPORATION Tokyo, Japan

TITLE

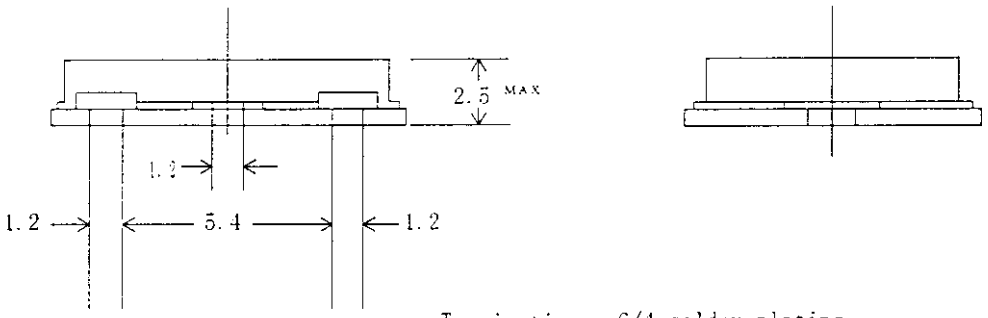
SPEC. NUMBER AL14186 Rev. 01

14. Outline

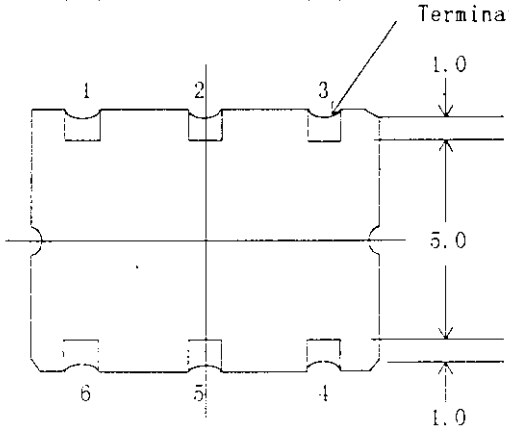


Marking

1. Manufacturer brand
2. Product number
3. Production lot number
4. Index dot



Termination 6/4 solder plating



1 —— Vc
2 —— GND
3 —— Vcc
4 —— OUT
5 —— GND
6 —— Audio Modulation

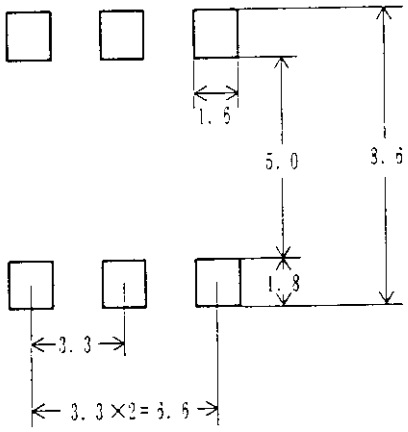
Bottom View

Fig. 1

15. Recommendable mounting condition for VCO.

1). Recommendable material of PCB : FR−4

2). Recommendable pattern of PCB

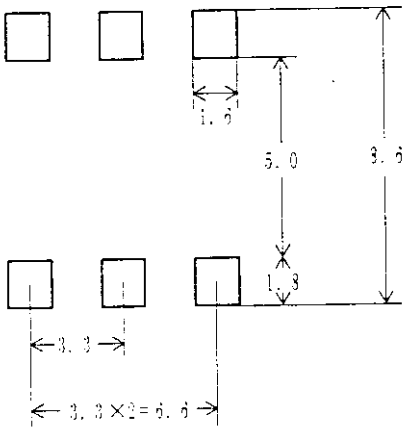


Unit : mm

3). Mask to print solder

Thickness of metal mask : 150μm

Figure of opening part



Unit : mm

The center of opening part of mask must fit to the pattern of PCB.

1 6. Recommendable solder material

1). Solder paste is designed to use fine-line screen printing.

2). Composition Sn :63%wt Pb :37%wt

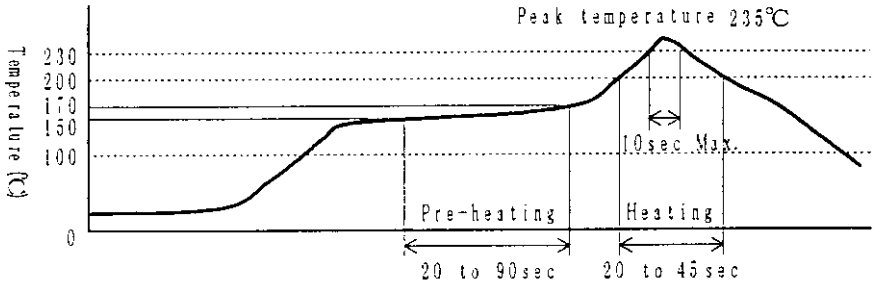
3). Flux Content of flux :9%
Content of chlorine in flux is less then 0.2%.

4). Particle size of solder 10 ~ 53 μm

5). Viscosity of solder paste 1,800 Poise

For example ; OZ-63-177F(6)-50-9 (Senju Metal Industry Co.,ltd)

1 7. Recommendable temperature profile of reflow soldering



1) 30sec. is needed for the profile to reach 150℃.

2) Pre-heating time 150 to 170℃, must be kept at 20 to 90sec.

3) Heating time, more than 200℃, must be kept at 20 to 45sec., and peak temperature must be 235℃. (Fusion time of solder more than 230 ℃, must be kept under 10 sec.)

Caution : Please don't vibrate VCO during reflow soldering process.

: Please don't pass VCO at upside down into reflow soldering process.

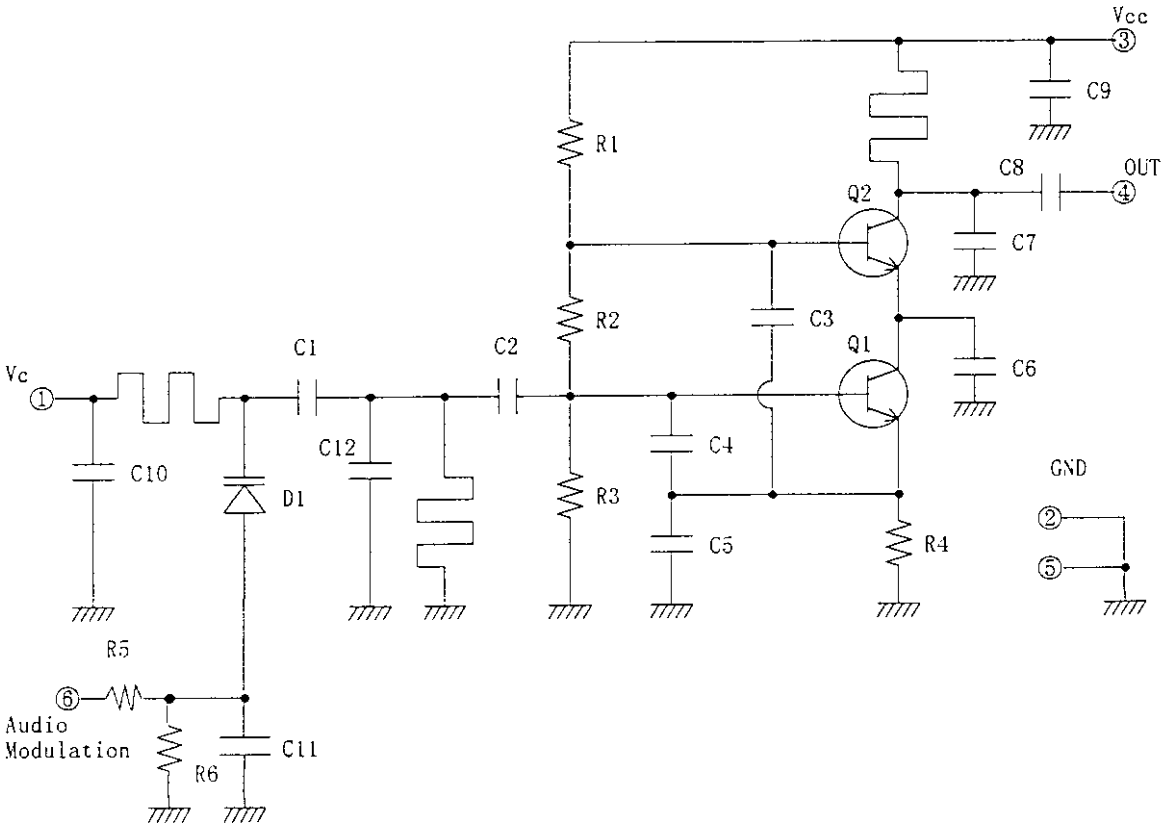
: Reflow soldering process : Maximum twaice.

F D K C O R P O R A T I O N Tokyo, Japan

TITLE

SPEC. NUMBER A L 1 4 1 8 6 Rev.01

1 8. Circuit



SPECIFICATION OF VCO FOR AMPS

CUSTOMER P/N	:	
ALPS P/N	:	URAA8-D22A
SAMPLE P/N	:	URAA8XD22A

SYMB.	DATE	APPD.	CHKD.	DSGD.

ALPS ELECTRIC CO.,LTD.

APPD.	CHKD.	DSGD.
Nov.'96	Nov.'96	Nov.'96

URAA8-D22A

TITLE PRODUCT SPECIFICATION

DOCUMENT No. (1/14)

1. PURPOSE AND SCOPE

This document contents specifications pertinent to AMPS VCO module.
It includes GENERAL MECHANICAL, ELECTRICAL and RELIABLITY REQUIREMENTS.

2. STANDARD OPERATING CONDITIONS

2-1. ELECTRICAL AND ENVIRONMENT OPERATING CHARACTERISTICS

ITEM		UNIT	NOTE
Vcc	+3.30 ±0.16	V	+8V MAX.
Vctl	+1.0 to +2.8	V	
OUTPUT IMPEADANCE	NOMINAL 50	ohm	

2-2. OPERATING TEMPERATURE RANGE : -30deg.C to +70deg.C

2-3. STORAGE TEMPERATURE RANGE : -40deg.C to +85deg.C

3. GENERAL MECHANICAL CHARACTERISTICS

3-1. ASPECT
There should not be contamination, scratches nor strains body.

3-2. DIMENSIONS
Refer to ASSEMBLY DRAWING

3-3. WEIGHT
Approx. 0.6g

3-4. TAPING METHOD
Refer to Fig-1.

3-5. SOLDERING CONDITION
Refer to Fig-2.

PRELIMINARY

SYMB.	DATE	APPD.	CHKD.	DSGD.

ALPS ELECTRIC CO.,LTD.

APPD.	CHKD.	DSGD.

URAA8-D22A

TITLE PRODUCT SPECIFICATION

DOCUMENT No. (2/)

3-6. MANUAL SOLDERING USING SOLDERING IRON

Tip diameter	Selected to fit application
Maximum tio temoerature	+350deg.C
Antistatic protection	Required
Maximum exposure time	6s

4. GENERAL ELECTRICAL CHARACTERISTICS

4-1. REQUIREMENT SPECIFICATIONS

PARAMETER	SPEC	UNIT	CONDITIONS
1) FREQUENCY RANGE	Vctl=1.0V : 954 MAX. Vctl=2.8V : 981 MIN.	MHz	
2) CONTROL VOLTAGE SENSITIVITY	33±7	MHz/V	Vctl=1.0 to 2.8V
3) OUTPUT POWER	0±3	dBm	Ta=+25 deg.C
4) SSB PHASE NOISE	-76TYP	dBc/Hz	60kHz offset:30KHz B.W.
5) CURRENT CONSUMPTION	12 MAX. (9 typ.)	mA	
6) HARMONICS	-10 MAX.	dBc	for carrier
*7) PULLING FIGURE	3 MAX.	MHzp-p	For VSWR=2:1 at all phases, reference load 50 ohm
*8) PUSHING FIGURE	±1.0 MAX.	MHz	Vcc=+3.30V±0.16V
*9) TEMPERATURE DRIFT	±3.0 MAX.	MHz	Ta=-30 to +70 deg.C Ref. +25deg.C

PRELIMINARY

SYMB	DATE	APPD	CHKD	DSGD

ALPS ELECTRIC CO.,LTD.

APPD	CHKD	DSGD	URAA8-D22A
			TITLE PRODUCT SPECIFICATION
			DOCUMENT No. (3/)

4-2. ENVIRONMENTAL REQUIREMENTS FOR MEASUREMENT

Measurement shall be based on STANDARD CONDITIONS.
In case of no objection to judgment, it shall be conformed to GENERAL CONDITONS.

STANDARD CONDITIONS	:	TEMPERATURE	25deg.C
		HUMIDITY	65%
STANDARD CONDITIONS	:	TEMPERATURE	10 to 35deg.C
		HUMIDITY	45 to 85%

5. GENERAL RELIABILITY TEST

TABLE-1 : POST ENVIRONMENT

ITEM		NOTE
FREQUENCY LIMIT	+/- 5MHz	
OUTPUT LEVEL	Original	Shall meet original limits of 4-1.
CNR	Original	Shall meet original limits of 4-1.

5-1. HIGH TEMPERATURE TEST

The sample shall meet the performance of TABLE-1 after storage +85+/-3deg.C for 96 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 4 hours prior to test.

5-2. LOW TEMPERATURE TEST

The sample shall meet the performance of TABLE-1 after storage -40+/-3deg.C for 96 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 4 hours prior to test.

PRELIMINARY

5-3. TEMPERATURE CYCLING TEST

The sample shall meet the performance of TABLE-1 after storage for 10cycle (1cycle : 40 minutes) at temperature range -20+/-3deg.C to +80+/-3deg.C.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 4 hours prior to test.

5-4. HUMIDITY TEST

The sample shall meet the performance of TABLE-1 after storage +60+/-2deg.C for and 90% for 96 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 4 hours prior to test.

5-5. VIBRATION TEST

The sample shall meet the performance of TABLE-1 after the following.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 1 hours prior to test.

VIBRATION FREQUENCY : 10 to 55 to 10Hz (1 cycle : 1 minute)
TOTAL AMPLITUDE : 1mm
DIRECTION : X.Y.Z (each direction 20 minutes)

PRELIMINARY

SYMB.	DATE	APPD.	CHKD.	DSGD.	ALPS ELECTRIC CO.,LTD.		
					APPD.	CHKD.	DSGD.
					URAA8-D22A		
					TITLE PRODUCT SPECIFICATION		
					DOCUMENT No. (5/)		

5-6. DROP SHOCK TEST

The shall sample meet the performance of TABLE-1 after the following.

DROP POINT(HEIGHT) : 1m
RECEIVING BORD : WOOD BOARD (20×20×3cm)
DROP TIME : 1 TIME

5-7. THE RESISTANCE TO REFLOW SOLDERING

The sample shall meeet the performance of 4-1. (GENERAL ELECTRICAL CHARACTERISTICS), after reflow soldering on the profile of Fig-2 based on the following conditions.

- SMD VCO should not be vibrated during the test.
- SMD VCO should not be mounted up side down.

5-8. SUBSTRATE BENDING TEST

SMD VCO should be mounted on Print Circuit Board.
(Glass Fabric Epoxy Resin, thickness : 1.6mm, W×L : 100mm×100mm)
When the vaule of PCB's bowing is 2mm, there should be no crack in soldering portion.

PRELIMINARY

SYM.	DATE	APPD.	CHKD.	DSGD.

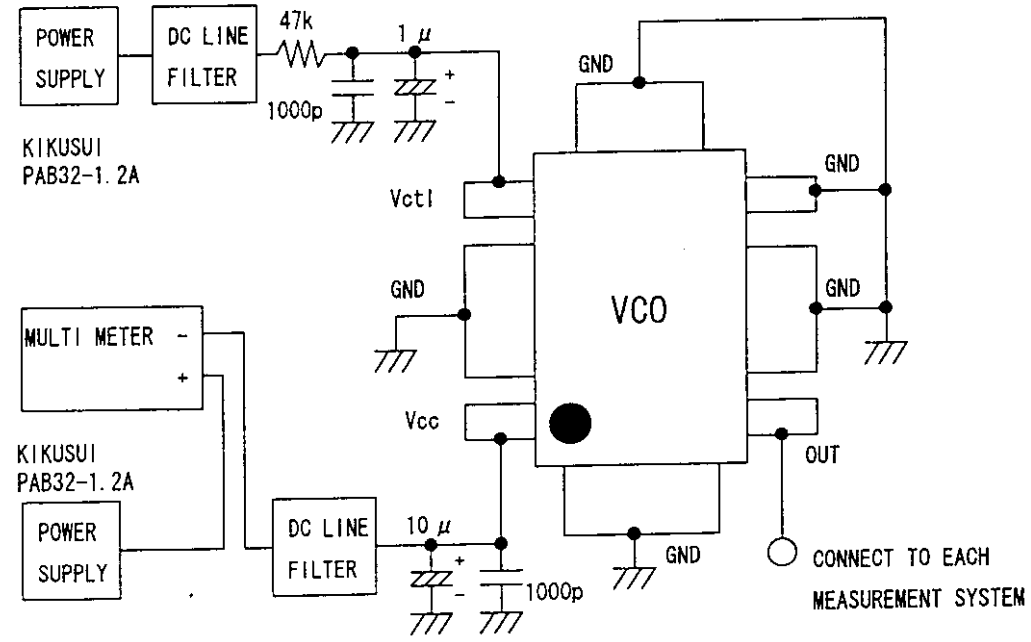
ALPS ELECTRIC CO.,LTD.

APPD.	CHKD.	DSGD.	URAA8-D22A
			TITLE PRODUCT SPECIFICATION
			DOCUMENT No. (6/)

6. MEASUREMENT METHOD

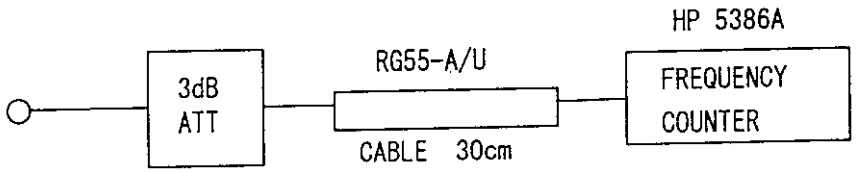
Measurement shall be based on 6-1. STANDARD CIRCUIT FOR MEASUREMENT. VCO TEST JIG and DC LINE FILTER (Refer to 6-3.)shall be used in STANDARD CIRCUIT.

6-1. STANDARD CIRCUIT FOR MEASUREMENT



6-2. MEASUREMENT SYSTEM

1) FREQUENCY and TUNING SENSITIVITY MEASUREMENT



PRELIMINARY

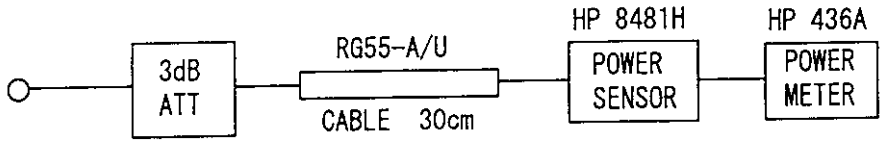
					ALPS	ALPS ELECTRIC CO.,LTD.	
					APPD.	CHKD.	DSGD.
SYM.	DATE	APPD.	CHKD.	DSGD.			

URAA8-D22A

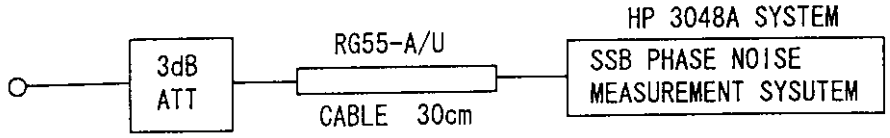
TITLE PRODUCT SPECIFICATION

DOCUMENT No. (7/)

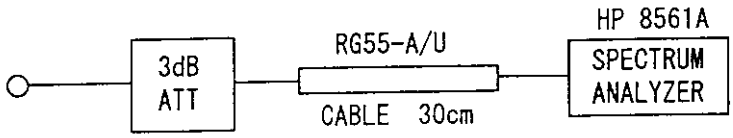
2) OUTPUT LEVEL MEASUREMENT



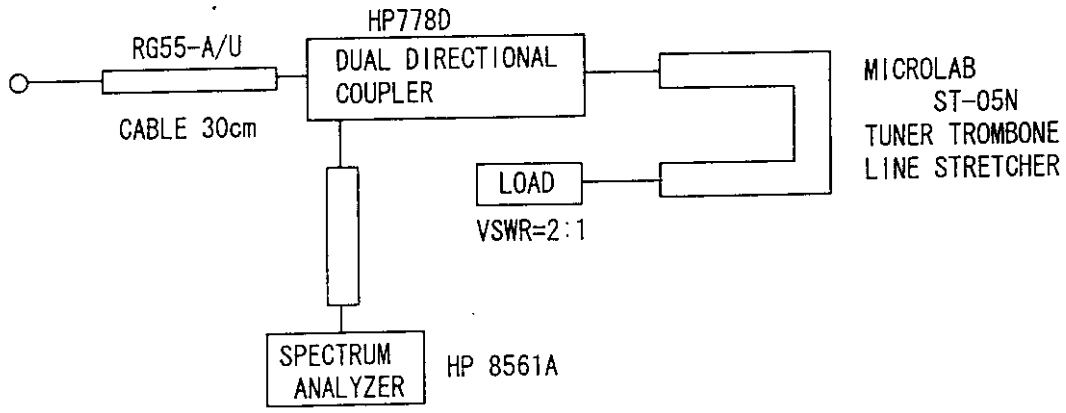
3) SSB PHASE NOISE MEASUREMENT



4) HARMONIC MEASUREMENT



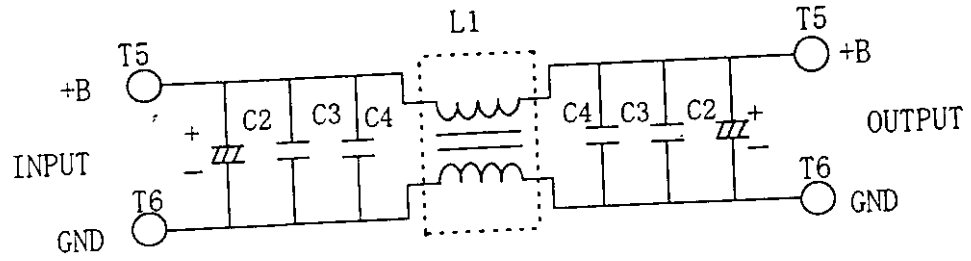
5) PULLING FIGURE MEASUREMENT



PRELIMINARY

					ALPS ELECTRIC CO.,LTD.		
					APPD.	CHKD.	DSGD.
					URAA8-D22A		
					TITLE PRODUCT SPECIFICATION		
					DOCUMENT No. (8/)		
SYMB.	DATE	APPD.	CHKD.	DSGD.			

6-3. DC LINE FILTER

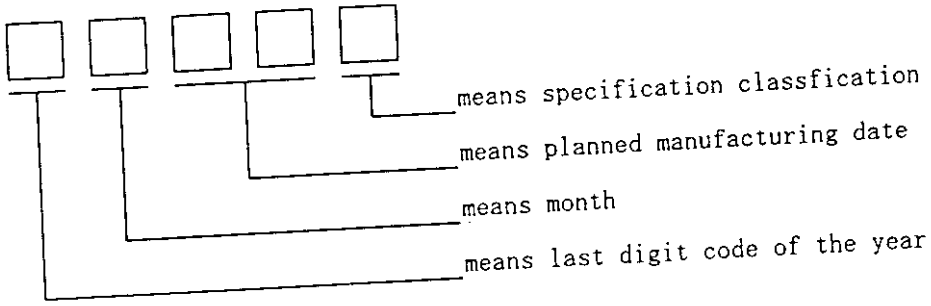


L1 : CHOCKING COIL SE25H-15100(10mH)
C2 : ELECTROLTIC CAPACITOR 2200 μ F / 25V
C3 : FILM CAPACITOR 0.47 μ F
C4 : CERAMIC CAPACITOR 1000pF

VOLTAGE	35(V) MAX.
CURRENT	30(mA) MAX.
NOISE REDUCTION	50Hz -52dB 60Hz -54dB

7. MARKING METHOD

We put number and description which are relatively controlled by assembly drawing on the products. Refer to 8-ASSEMBLY DRAWING .



month	1	2	3	4	5	6	7	8	9	10	11	12
mark	1	2	3	4	5	6	7	8	9	0	N	D

0=Oct. N=Nov. D=Dec.

PRELIMINARY

SYMB	DATE	APPD	CHKD	DSGD

ALPS ELECTRIC CO.,LTD.

APPD.	CHKD.	DSGD.	URAA8-D22A
			TITLE PRODUCT SPECIFICATION
			DOCUMENT No. (9/)

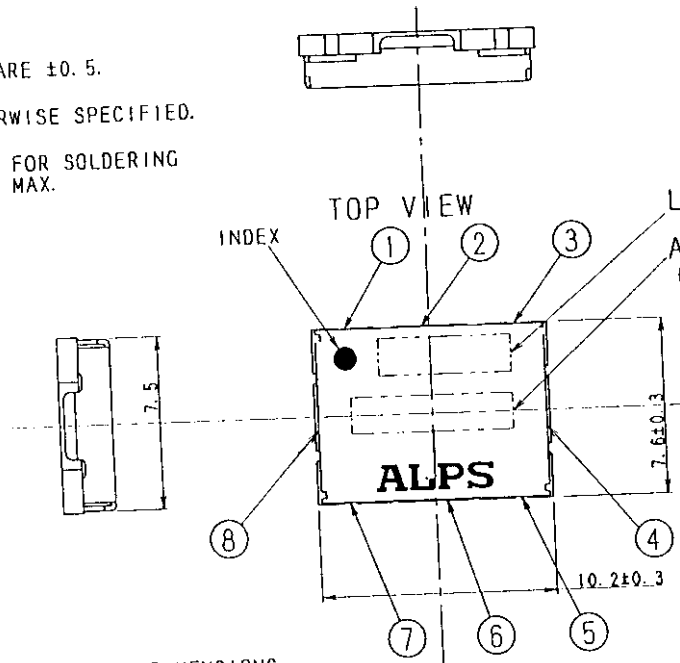
Applicant: Shintom Co., Ltd.

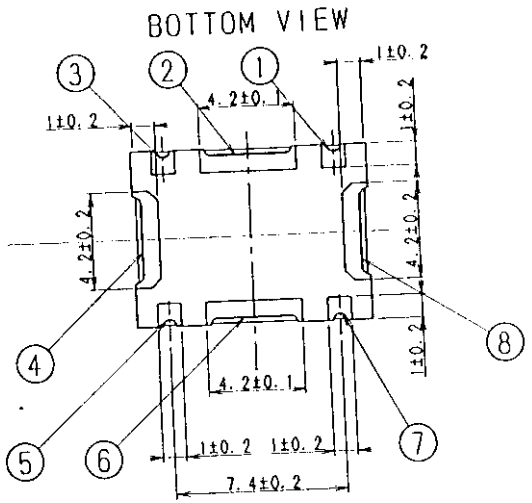
Transmitter Type: BFXM3017

PAD NO.	1	2	3	4	5	6	7	8
CONTENTS	VCC	GND	CTL	GND	GND	GND	OUT	GND

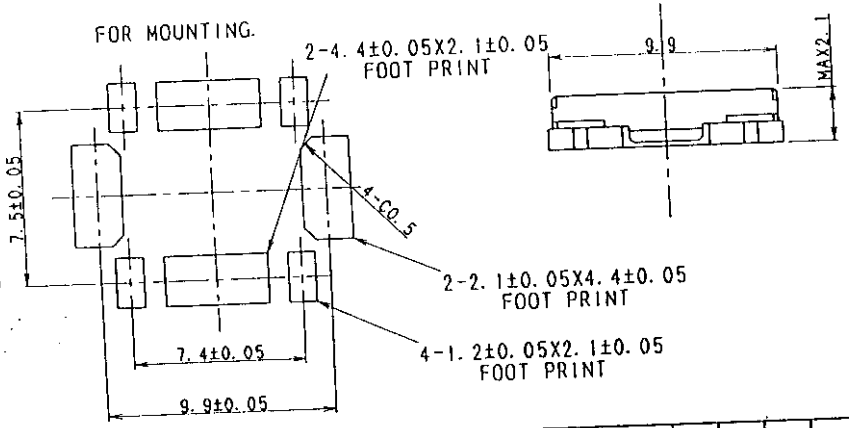
NOTE 1. TOLERANCES ARE ±0.5.
UNLESS OTHERWISE SPECIFIED.

2. COPLANARITY FOR SOLDERING PADS: 0.15mm MAX.





3. RECOMENDED FOOTPRINT DIMENSIONS FOR MOUNTING.



RX

PRELIMINARY

CUSTOMER'S MODEL NO.	A-D22A ALPS MODEL NO. (ABBREVIATION)	URAA8-D22A ALPS MODEL NO.

PART NO.	NAME	MATERIAL	SPEC.	FINISH

ALPS ELECTRIC CO., LTD.

ZONE	SYMB.	DATE OR NO.	APPD.	CHKD.	DSGD.

DSGD. Nov. 26'97 M. Enkou
CHKD.
APPD. Nov. 26'97 T. Inoue

SCALE 5:1
UNIT mm
KEY NO.

TITLE URAA8 ASSEMBLY DRAWING
DOCUMENT NO. (10/)

6 (A3ヤ変更無し)

PF0045A/PF0065A

MOS FET Power Amplifier Module for AMPS Handy Phone

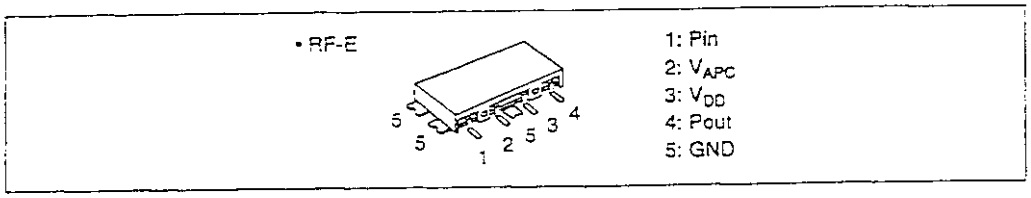
HITACHI

ADE-208-309B (Z)
Preliminary 3rd. Edition
July 1996

Features

- High efficiency
  PF0045A: 58 % Typ at 1.2 W
  PF0065A: 52 % Typ at 1.2 W
- Low voltage operation: 4.8 V
- High power gain: 1 mW input
- Low power control current: 500 µA Typ
- Reflowable surface mounted small package: 1 cc, 3 g

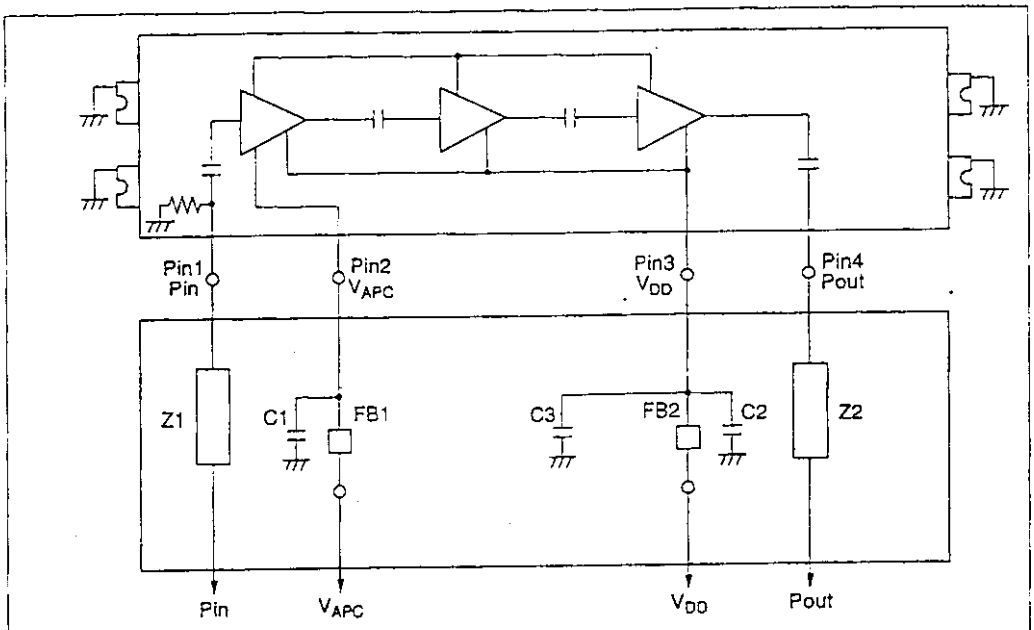
Pin Arrangement



Hitachi semiconductor

PF0045A/PF0065A

Internal Diagram and External Circuit



C1 = C2 = 0.01 µF (Ceramic chip capacitor)
C3 = 4.7 µF (Tantalum)
FB = Ferrite bead BL01RN1-A62-001 (Manufacture: MURATA) or equivalent
Z1 = Z2 = 50 Ω (Microstrip line)

Absolute Maximum Ratings (Tc = 25°C)

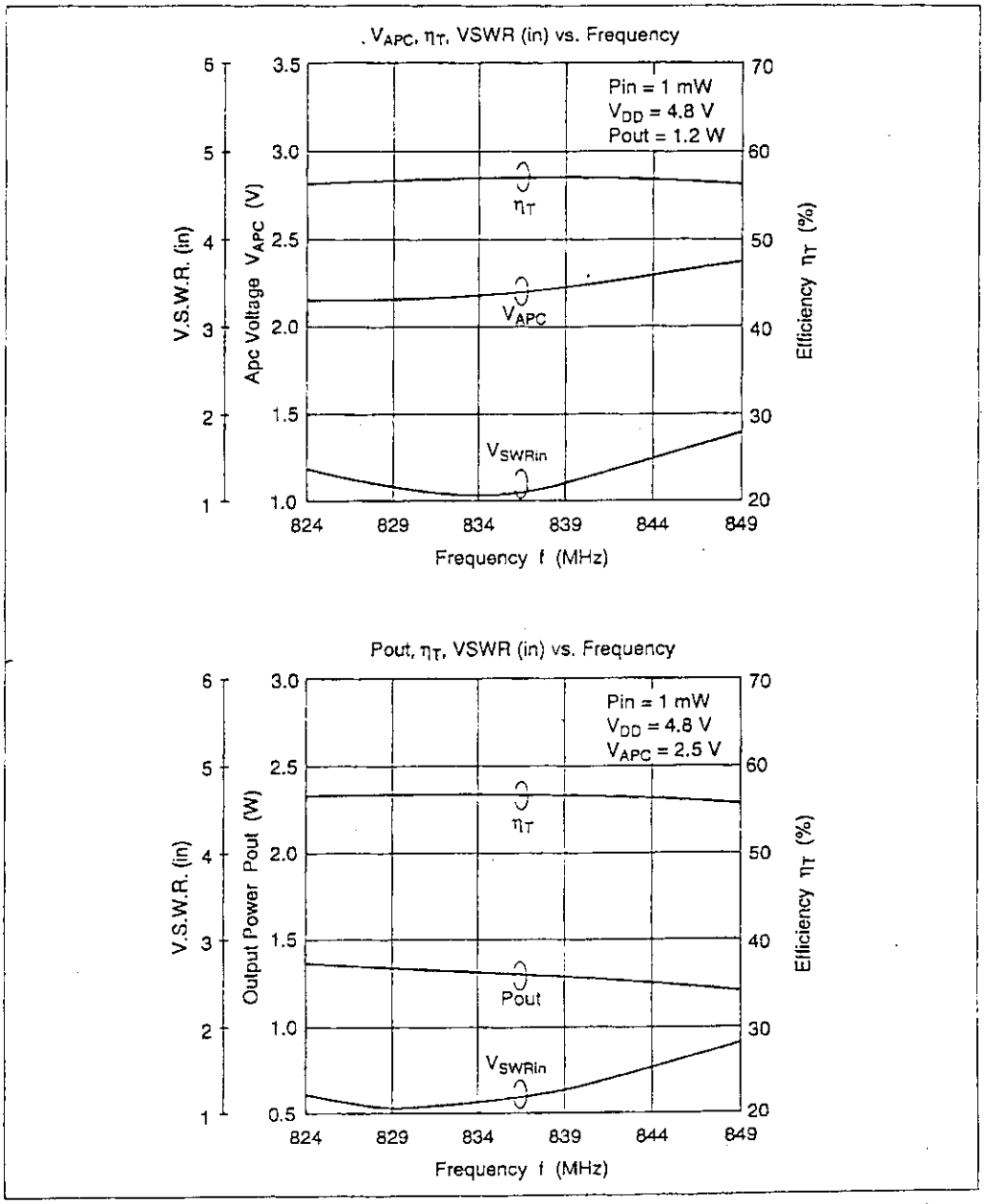
Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	10	V
Supply current	I_{DD}	1.5	A
V_{APC} voltage	V_{APC}	4.5	V
Input power	Pin	20	mW
Operating case temperature	Tc (op)	–30 to +100	°C
Storage temperature	Tstg	–30 to +100	°C

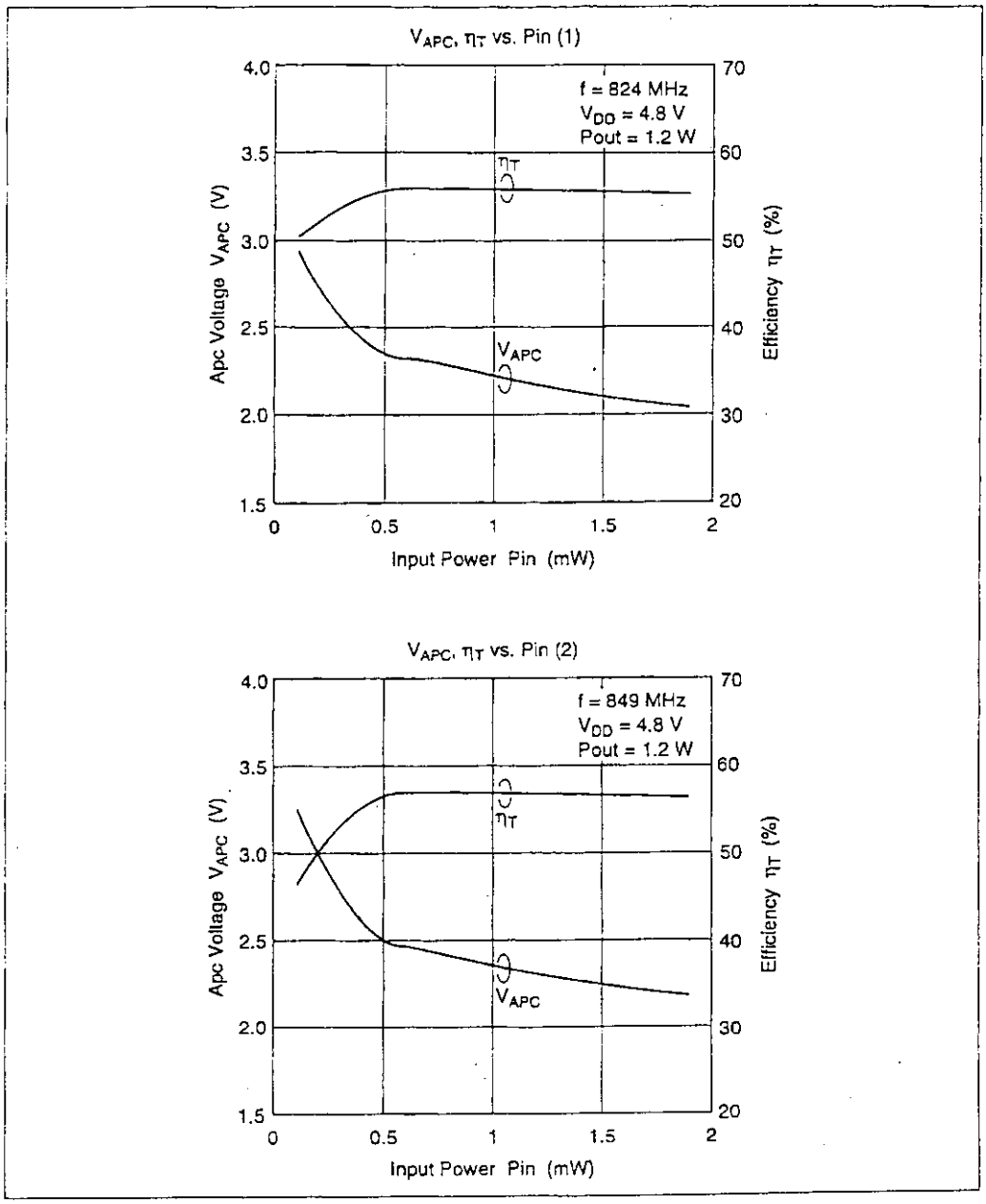
Electrical Characteristics (Tc = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Drain cutoff current	I_{DS}	—	—	100	µA	V_{DD} = 10 V, V_{APC} = 0 V, R_L = Rg = 50 Ω
Total efficiency (PF0045A)	η_T	50	58	—	%	f = 824, 849 MHz, Pin = 1 mW, V_{DD} = 4.8 V, Pout = 1.2 W (at V_{APC} controlled), R_L = Rg = 50 Ω
Total efficiency (PF0065A)	η_T	48	52	—	%	
2nd harmonic distortion	2nd H.D.	—	–35	–30	dBc	
3rd harmonic distortion	3rd H.D.	—	–40	–30	dBc	
Input VSWR	VSWR (in)	—	2	3	—	
Output power	Pout	1.25	1.4	—	W	f = 824, 849 MHz, Pin = 1 mW, V_{DD} = 4.8 V, V_{APC} = 4 V, R_L = Rg = 50 Ω
Isolation	—	—	–40	–35	dBm	f = 824, 849 MHz, Pin = 1 mW, V_{DD} = 4.8 V, V_{APC} = 0.5 V, R_L = Rg = 50 Ω
Stability	—	No parasitic oscillation			—	f = 824 to 849 MHz, Pin = 1 mW, V_{DD} = 4.3 to 6 V, Pout ≤ 1.4 W, Rg = 50 Ω, Load VSWR = 3:1 All phases angles
Load VSWR tolerance	—	No degradation			—	f = 824 to 849 MHz, Pin = 1 mW, t = 10 sec., V_{DD} = 4.3 to 6 V, Pout ≤ 1.4 W, Rg = 50 Ω, Load VSWR = 20:1 All phases angles

PF0045A/PF0065A

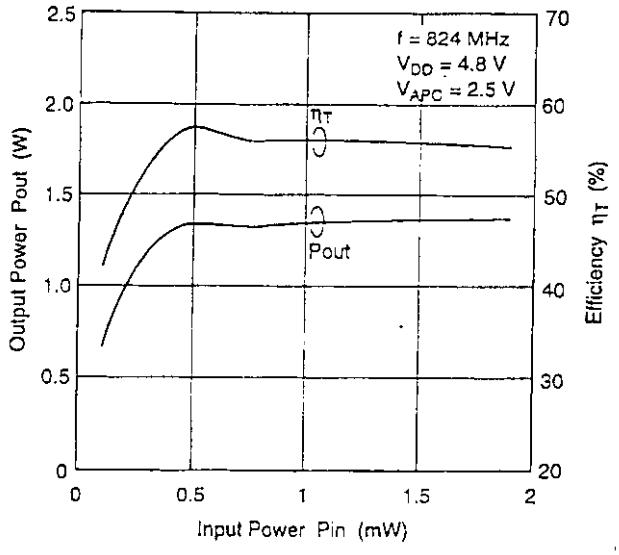
Characteristics Curve



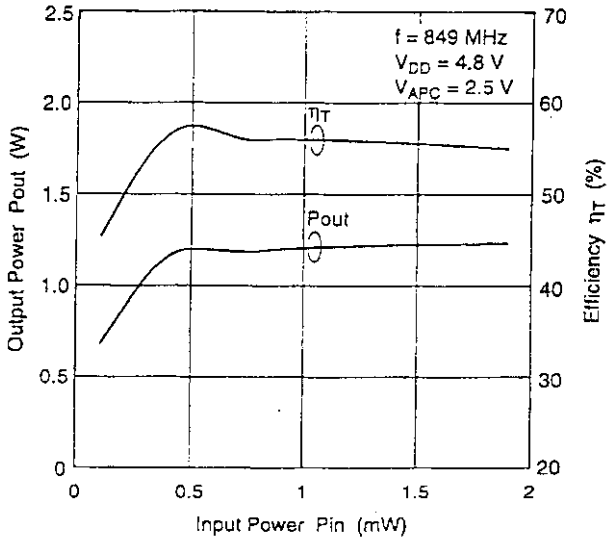

V_{APC}, η_T vs. Pin (1)
f = 824 MHz
V_{DD} = 4.8 V
Pout = 1.2 W
η_T
V_{APC}
Apc Voltage V_{APC} (V)
Efficiency η_T (%)
Input Power Pin (mW)
V_{APC}, η_T vs. Pin (2)
f = 849 MHz
V_{DD} = 4.8 V
Pout = 1.2 W
η_T
V_{APC}
Apc Voltage V_{APC} (V)
Efficiency η_T (%)
Input Power Pin (mW)

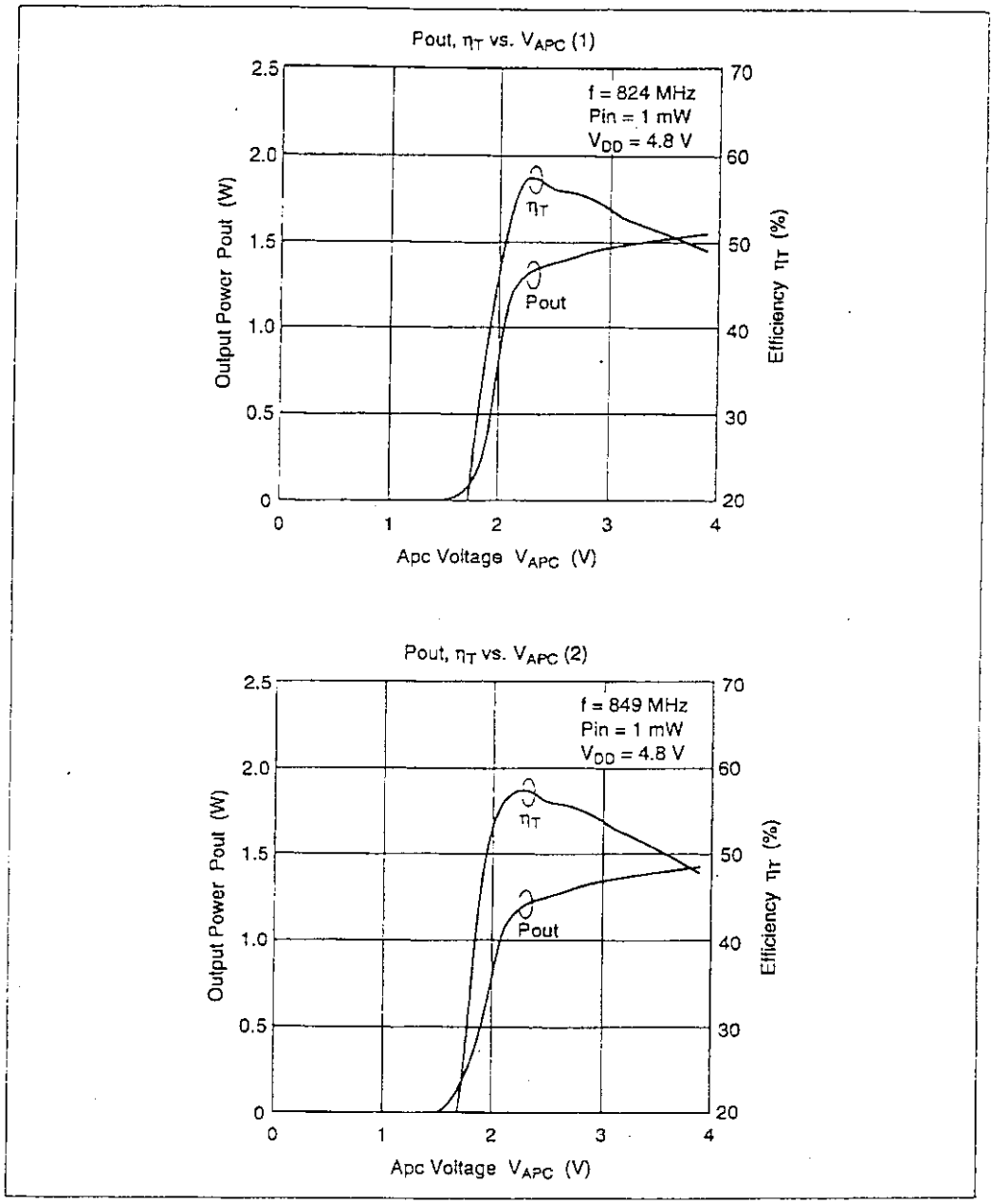
PF0045A/PF0065A

Pout, η_T vs. Pin (1)

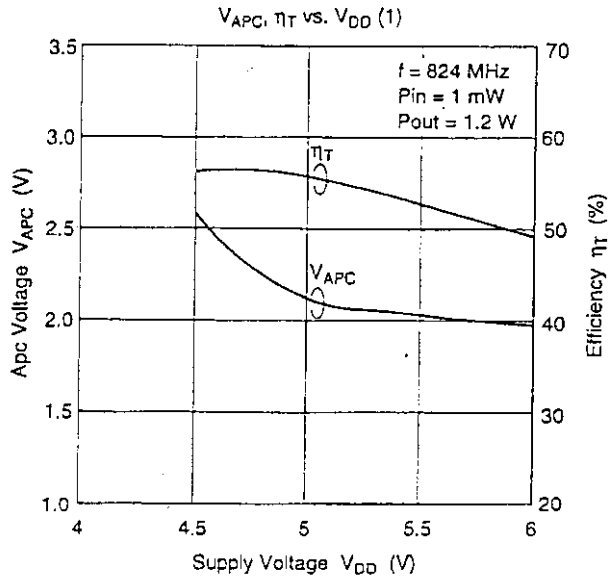


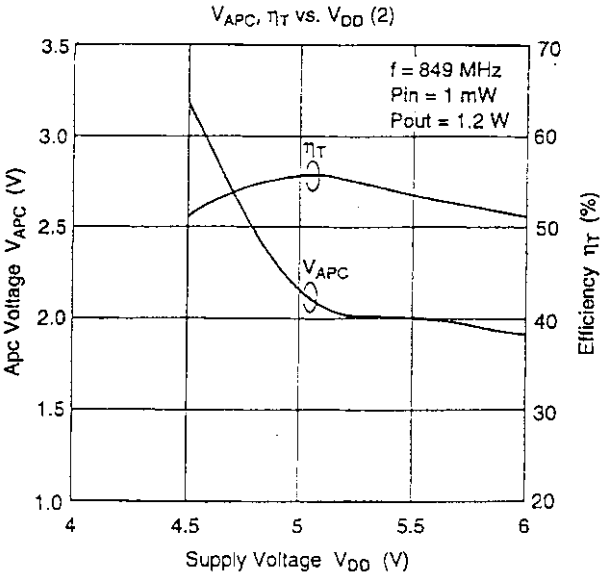
Pout, η_T vs. Pin (2)




Pout, ηT vs. VAPC (1)
f = 824 MHz
Pin = 1 mW
VDD = 4.8 V
ηT
Pout
Output Power Pout (W)
Efficiency ηT (%)
Apc Voltage VAPC (V)
Pout, ηT vs. VAPC (2)
f = 849 MHz
Pin = 1 mW
VDD = 4.8 V
ηT
Pout
Output Power Pout (W)
Efficiency ηT (%)
Apc Voltage VAPC (V)

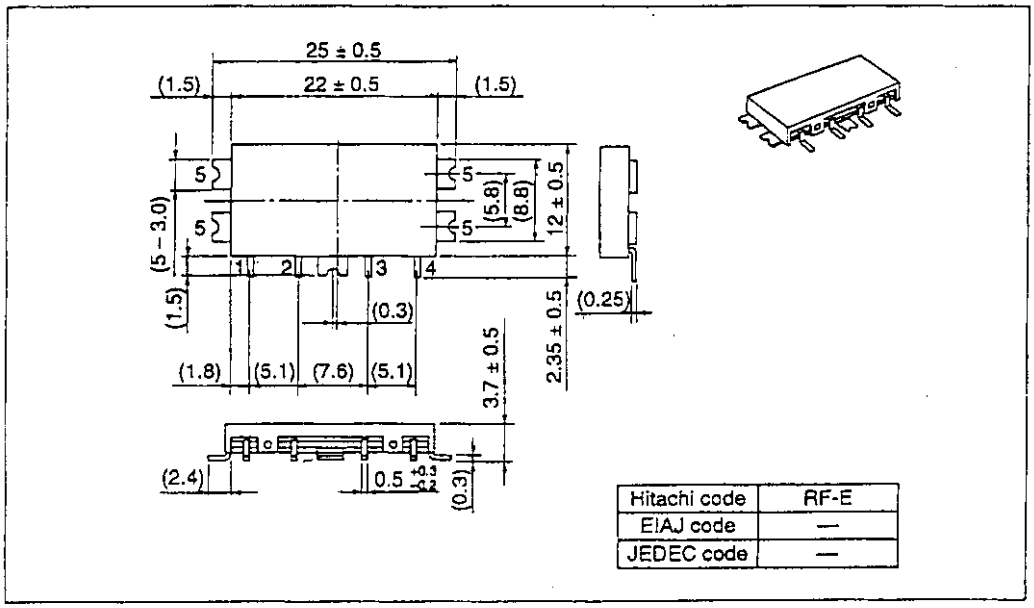
PF0045A/PF0065A





Package Dimensions

Unit: mm



Hitachi code	RF-E
EIAJ code	—
JEDEC code	—