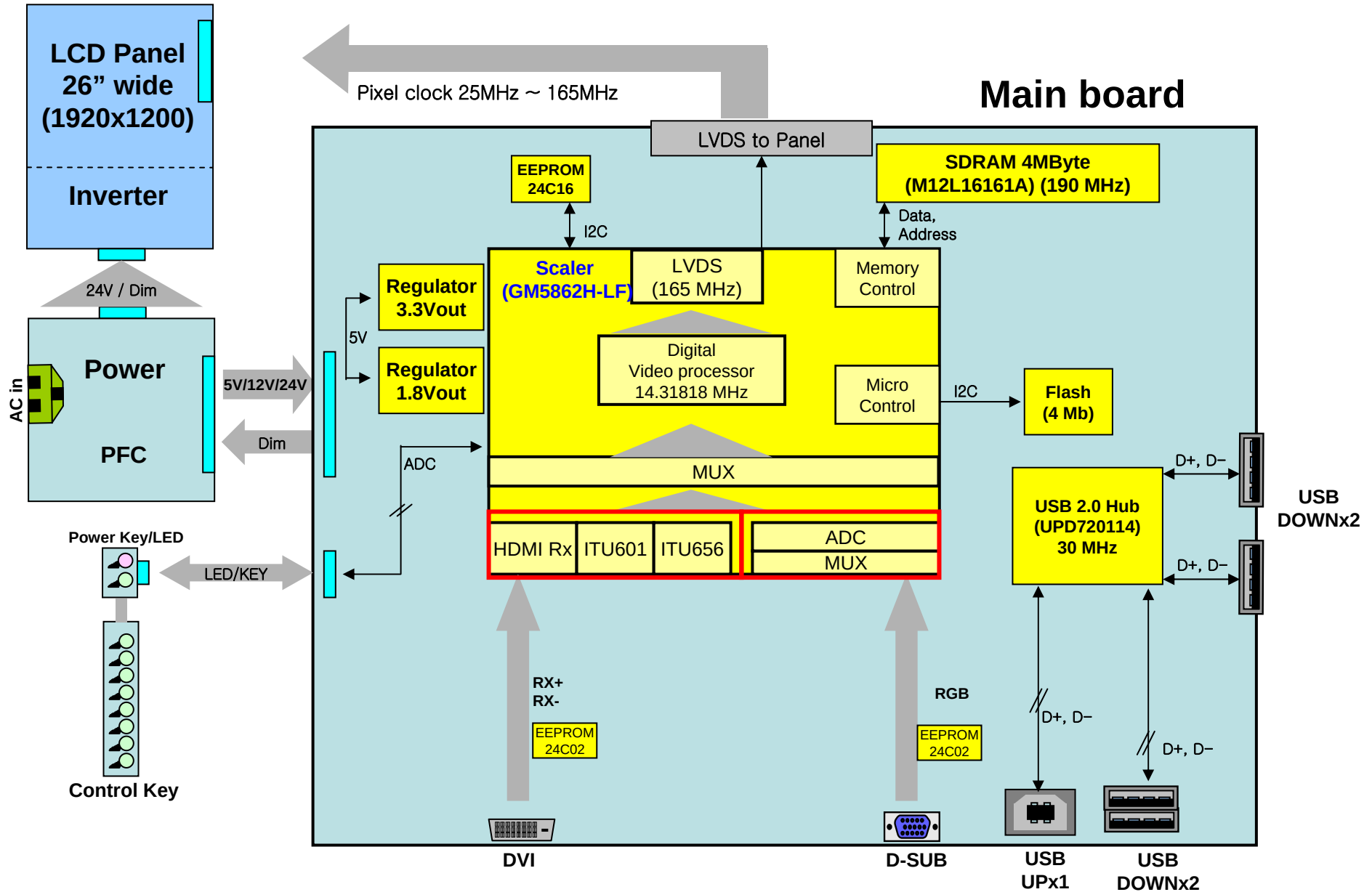


APPENDIX D
: BLOCK DIAGRAM

W2600H System Architecture



DESCRIPTION OF BLOCK DIAGRAM

1. Video Controller Part.

This part amplifies the level of video signal for the digital conversion and converts from the analog video signal to the digital video signal using a pixel clock.

The pixel clock for each mode is generated by the PLL.

The range of the pixel clock is from 25MHz to 165MHz.

This part consists of the Scaler, ADC and TMDS receiver .

The Scaler gets the video signal converted analog to digital, interpolates input to 1680 x 1050 resolution signal and outputs 8-bit R, G, B signal to transmitter.

2. Power Part.

This part consists of the 3.3V regulator to convert power which is provided 5V,

5V in Power board and Micom

5V is provided for LCD panel.

24V is converted 12V by DC/DC converter only for the speaker DC output(Optional).

Also, 5V is converted 3.3V by regulator and 3.3V is converted 1.8V by regulator.

Converted power is provided for IC in the main board.

3. MICOM Part.

This part consists of EEPROM IC which stores control data and the Micom.

The Micom distinguishes polarity and frequency of the H/V sync are supplied from signal cable.

The controlled data of each modes is stored in EEPROM.

*refer to the each frequency of crystal oscillators and working frequency.

-Video processor : 14.31818MHz.

-USB Hub : 30MHz

-LVDS Clock Freq. : 165MHz

-MEMORY Clock Freq. : 190MHz
