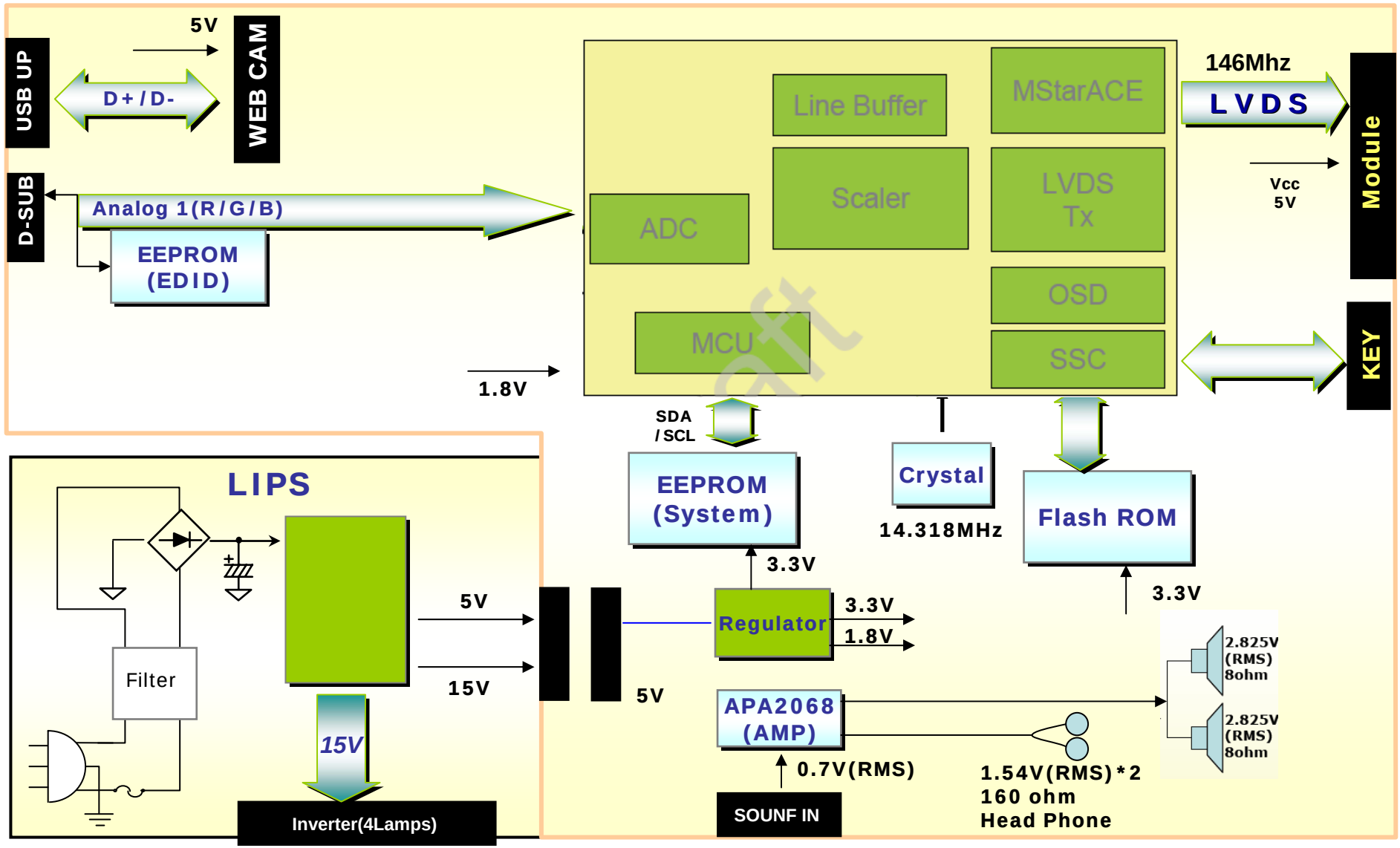
# APPENDIX D

## : BLOCK DIAGRAM

# Block diagram(회로)




**Crystal Location No : X501**

# DESCRIPTION OF BLOCK DIAGRAM

1. Video Controller Part.
This part amplifies the level of video signal for the digital conversion and converts from the analog video signal to the digital video signal using a pixel clock.
The pixel clock for each mode is generated by the PLL.
The range of the pixel clock is 25MHz to 140MHz
This part consists of the Scaler, ADC convertor, TMDS receiver and LVDS transmitter.
The Scaler gets the video signal converted analog to digital, interpolates input to 1680X1050 resolution signaland outputs 8-bit R, G, B signal to transmitter.
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2. Power Part.
This part consists of the one 3.3V, and one 1.8V regulators to convert power which is provided 5V in Power board.
15V is provided for inverter
Also, 5V is converted 3.3V and 1.8V by regulator. Converted power is provided for IC in the main board.
The inverter converts from DC 15V to AC 700Vrms and operates back-light lamps of module

3. MICOM Part.
This part is include video controller part. And this part consists of EEPROM IC which stores control data and Reset IC and the Micom.
The Micom distinguishes polarity and frequency of the H/V sync are supplied from signal cable.
The controlled data of each modes is stored in EEPROM.

*refer to the each frequency of crystal oscillators and working frequency.
-Video processor : 14.31818MHz.
-LVDS Clock Freq. : 146MHz