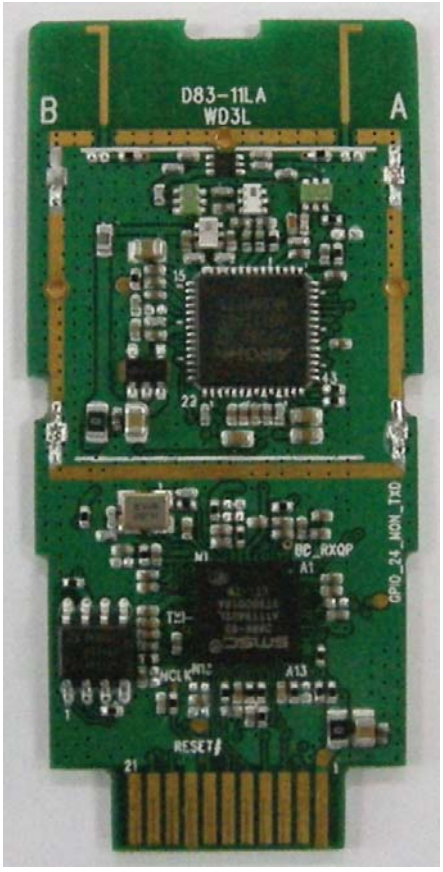
NAM-WD3L (DWAM83)

Digital Wireless Audio Transceiver Module
Preliminary Technical Product Specification
(Subject to change)



Revision History

Revision.	Author	Date	Detail.
0.0	SM/ET	27/1/2011	Preliminary

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1. Module

1.1. Product Description

The Module is an OEM module (35x35mm) based on the SMSC DARR83. It is an uncompressed wireless digital audio transceiver operating in the 2.4GHz, 5.2GHz and 5.8GHz bands. The wireless audio link supports up to 4 stereo audio streams and comes together with additional features such as: data encryption, pairing functionality, bi-directional control data messages, low power audio snooze mode, WLAN detection and Automatic Frequency Allocation. The DARR83 chip itself provides the basic functions of Audio Processing and buffering, Data Link Layer and Physical Layer. The module integrates all functionality for a wireless digital audio connection, comprising:

- DARR83 Wireless Audio Processor
- 2.4GHz/ 5.2GHz/ 5.8 GHz RF Transceiver
- Embedded Antennas
- Digital audio interfaces (I^2S and/or S/PDIF)
- I^2C control interface
- 26 pins interface connector (FFC) for power, digital audio and control interface and GPIOs
- Using a digital modulation

1.2. Basic Features

1.2.1. High Quality Audio

• Up to four stereo audio channels, fully bidirectional, up to 24-bit/96 ksps uncompressed audio
• Low latency <20ms for real-time audio and lip sync
• Low latency compression algorithm - optimized for voice applications, headphones
• Inter-speaker synchronization; Low-jitter audio clock sync
• Programmable digital audio gain

1.2.2. Networking and Connectivity

• 22Mbps Bandwidth in 2.4GHz, 5.2GHz and 5.8 GHz Bands
• In-room or multi-room network topology
• Point-to-Point and Point-to-Multipoint
• Bidirectional data channel (100 kbps)
• Simple Pairing and Association Function
• 4 I^2S Data pins, each provided with their own pair of BCK/LRCK signals or stereo S/PDIF input/output
• Master and Slave I2C bus for external control functions

1.2.3. Coexistence and Robustness

• Enhanced robustness against both in- and out of band interferers like: WiFi and cordless phones
• Coexistence with 802.11a, b, g and n
• Automatic receiver antenna diversity minimizes fading and multi-path effects
• Link quality monitoring
• Soft audio muting under poor link circumstances

1.2.4. Power Management

• Low power consumption
• Automatic RF output power control
• Power Down Duty Cycle mode: If no link is established, modules (both TX and RX) will enter a power down mode

1.2.5. Integrated 8052 MCU

The DARR83 integrates an 8052 MCU. This includes the following features:
• 45 kByte Code RAM
• 8 kByte Data RAM
• 4 Timer/Counters
• UART

1.2.6. Digital Audio Clock Synchronization

The digital audio clock synchronization is an additional more cost effective method for synchronization of audio samples on the receiving side with respect to the transmitted audio samples. The digital clock synchronization feature works for output audio sample rates of 96 and 48 ksps.

1.2.7. Sample Rate Converter (SRC) + Sample Rate Detector

The SRC can handle the following input sample rates [ksps]:
- 44.1
- 48
- 96
- 192 (using I^2S in slave mode)

2. Module Specifications

System Specifications				
ID	**Parameter**	**Value**	**Unit**	**Remarks**
RF Characteristics				
	RF frequency range	2400 – 2483.5 5150 - 5250 5725 - 5875	MHz MHz MHz	
	Number of RF channels	3		In each Frequency band.
Air framing				
	Addressing	24	Bit	
	Data message size	32	Byte	Application dependent
	CRC	16, 24 and 32	Bit	Hybrid
Control				
	Control interface	I^2C		Compliant with the I^2C protocol (slave), 0…400kbps. Base address 0x80.
Data				
	Data Bandwidth	100	Kbps	Bi-directional wireless data channel
	Data latency	5	ms	Minimum under good RF link conditions for applications that support the 100kbps data rate.
Interference Robustness				
	Fixed frequency devices (e.g. WLAN, microwave oven)			Fully coexistent[1]
	Frequency hopping devices (e.g. 5.8GHz cordless phones)			Fully coexistent[1]

[1] Laboratory tests have verified coexistence with interference sources collocated. Exact ranges are scenario dependent (function of latency, output power, audio compression, etc.). A mix of interference sources is allowed. Interference of fixed frequency devices may result in the loss of one useable RF channel.

Audio Interface				
	Available Interface Types	I^2S S/PDIF		Can be used simultaneously Incl. S/PDIF detection.
	Number of stereo audio output channels on Mobile Unit	1, 2, 3 or 4		Bidirectional, incl. audio loop
	Number of stereo audio input channels on Central Unit	1, 2, 3 or 4		Bidirectional, incl. audio loop
Audio Quality				
	Sample rate	44.1, 48 or 96	ksps	
	Sample width	16 or 24	bit	
	Latency	20	ms	Configurable from 10 to 23.6ms, depending on the application.
	Dynamic Range	98 146	dB dB	16 bit 48ksps, A-weighted 24 bit 48ksps, A-weighted
	THD+N	-96 -143	dB dB	16 bit 48ksps 24 bit 48ksps
	Frequency response	0	dB	20Hz…22kHz [2]
Dimensions				
	Module dimensions	35 x 35 x 4.3	mm	

[2] In applications where Digital Clock Sync is not used.

2.1. Absolute Maximum Rating

Symbol	Parameter	Min.	Typ	Max	Unit
VCC	Supply Voltage			3.8	V
$T_{storage}$	Storage Temperature	-25	–	85	°C
V_{ESD}	ESD Contact Discharge	-3	–	+3	kV

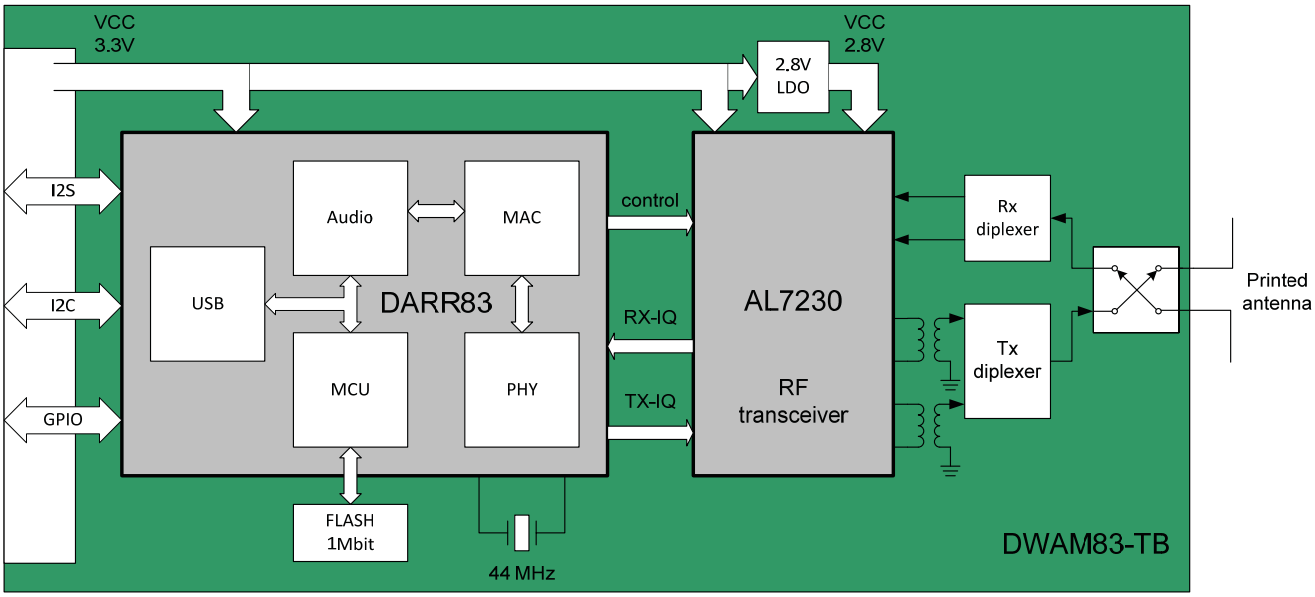
2.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
VCC	Supply Voltage	3.1	3.3	3.5	V
VCC Ripple	Peak to Peak Ripple (in circuit)	–	0	100	mV
T_{amb}	Operating Temperature	-10	25	60	°C

2.3. DC Characteristics

All digital IO levels are 3.3V CMOS. The digital IO ports are not 5V compliant.
Please refer to datasheet of DARR83 for more information.

2.4. Module Block Diagram



2.5. Power Consumption

(Vcc=3.3V, 25°C, Audio Clock:12.288MHz).

Application*	2.4GHz		5.2GHz		5.8GHz	
	MU (in mA)	CU (in mA)	MU (in mA)	CU (in mA)	MU (in mA)	CU (in mA)
Standby mode*	21	21	21	21	21	21
1 Stereo NACK	31	98	36	96	36	96
2-1 Stereo NACK BiDir	81	155	82	145	82	146
2 ACK	60	140	65	124	65	127
TX Continuous mode (peak current)	-	390	-	300	-	300

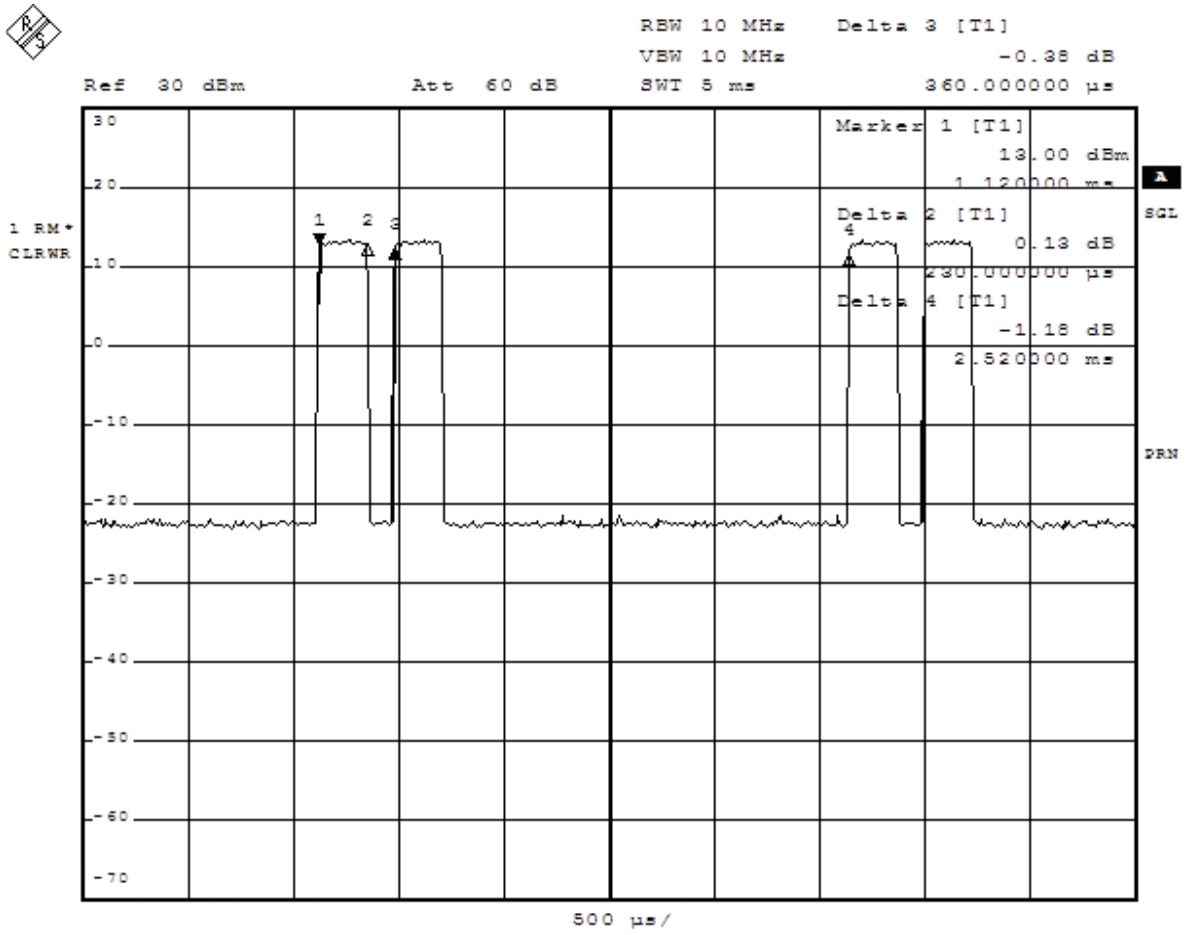
**Current consumption measurements based on External MCU using EVK. Standby mode can be wake up by CU*

For detailed current consumption for other applications mode, please contact our AE.

Note 1: The ACK applications have automatic RF power control therefore these applications will have variable (lower) power consumption depending on wireless link conditions.

Note 2: The above measurements are under un-interfered circumstances. When retransmissions are required, current consumption will change (e.g. ACK and CU NACK at 30 % and only MU NACK when there is interference)

Note 3: The duration of the peak current is depending on the application. For example, a 2 Stereo ACK CU has a peak power duration of two time slots of 230us in a 2.52ms frame period as depicted here below:


RBW 10 MHz
VBW 10 MHz
SWT 5 ms
Delta 3 [T1]
-0.38 dB
360.000000 µs
Ref 30 dBm
Att 60 dB
Marker 1 [T1]
13.00 dBm
1.120000 ms
Delta 2 [T1]
0.13 dB
230.000000 µs
Delta 4 [T1]
-1.18 dB
2.520000 ms
1 RM
CLRWR
SGL
PRN
30
20
10
0
-10
-20
-30
-40
-50
-60
-70
500 µs/

2.6. RF Performance

Vcc=3.3V, 25°C)

Parameter		Condition	Min.	Typ.	Max	Units
RF Frequency Range			2400	–	2483.5	MHz
Number of RF-channels		Carriers in the spectrum	–	3	–	
Channel Frequency (dynamic or fixed allocation)	CH1 CH2 CH3		–	2412 2438 2464	–	MHz
Channel Spacing			–	26	–	MHz
RF Bandwidth		Null-to-null	–	22	–	MHz
Rx sensitivity			–	-83	–	dBm
Antenna Diversity		TX/RX	–	ON	–	

For 5.2GHz application (Vcc=3.3V, 25°C)

Parameter		Condition	Min.	Typ.	Max	Units
RF Frequency Range			5150	–	5250	MHz
Number of RF-channels		Carriers in the spectrum	–	3	–	
Channel Frequency (dynamic or fixed allocation)	CH1 CH2 CH3		–	5180 5210 5240	–	MHz
Channel Spacing			–	30	–	MHz
RF Bandwidth		Null-to-null	–	22	–	MHz
Rx sensitivity			–	-81	–	dBm
Antenna Diversity		TX/RX	–	ON	–	

For 5.8GHz application (Vcc=3.3V, 25°C)

Parameter		Condition	Min.	Typ.	Max	Units
RF Frequency Range			5725	–	5875	MHz
Number of RF-channels		Carriers in the spectrum	–	3	–	
Channel Frequency (dynamic or fixed allocation)	CH1 CH2 CH3		–	5736 5762 5814	–	MHz
Channel Spacing			–	26	–	MHz
RF Bandwidth		Null-to-null	–	22	–	MHz
Rx sensitivity			–	-81	–	dBm
Antenna Diversity		TX/RX	–	ON	–	.

[3] With DARR83-ADC based Power Control Loop. Output power country/region dependent.

2.7. Pin out of 22pin Interface Slot

Specs of Slot: 1.27mm pitch PCB Slot

Pin Number	Pin Name	I/O	Description
1	VDD	Power	Regulated 3.3V input
2	GND	Ground	Ground
3	MCLK	In	12.288MHz audio clock In
4	DARR83_GPIO_4	I/O	Configurable. Please refer to the DARR83 datasheet
5	DARR83_GPIO_3	I/O	
6	I2C_SDA_SLV		I2C SLAVE (SDA)
7	I2C_SCL_SLV		I2C SLAVE (SCLK)
8	DARR83_GPIO_12	I/O	Configure as SDIO Z
9	DARR83_GPIO_6	I/O	Configure as SDIO Y
10	DARR83_GPIO_11	I/O	Configure as SDIO X
11	DARR83_GPIO_5	I/O	Configure as SDIO W
12	DARR83_GPIO_2	I/O	MUTE INTERRUPT
13	DARR_RST#		DARR RESET
14	DARR83_GPIO_8	I/O	Configure as BCK W
15	GND	Ground	Ground
16	DARR83_GPIO_10	I/O	Configure as LRCK W
17	DARR83_GPIO_24	I/O	Configure as MON_TXD
18	DARR83_GPIO_23	I/O	RED LED
19	DARR83_GPIO_13	I/O	BLUE LED
20	DARR83_GPIO_14	I/O	Configurable. Please refer to the DARR83 datasheet
21	NC		NOT CONNECTED
22	NC		NOT CONNECTED

2.8. Antenna

The module uses embedded PCB track Tri-Band antennas. RX and TX diversity antennas are used to avoid dropouts due to multipath fading.

- Antenna A (ANT A) fixed track antenna on the module
- Antenna B (ANT B) fixed track antenna on the module

Only ‘one’ antenna is selected for use at any one time, through the on-board Transmit-Receive/ Diversity RF switch.

3. Hardware Development

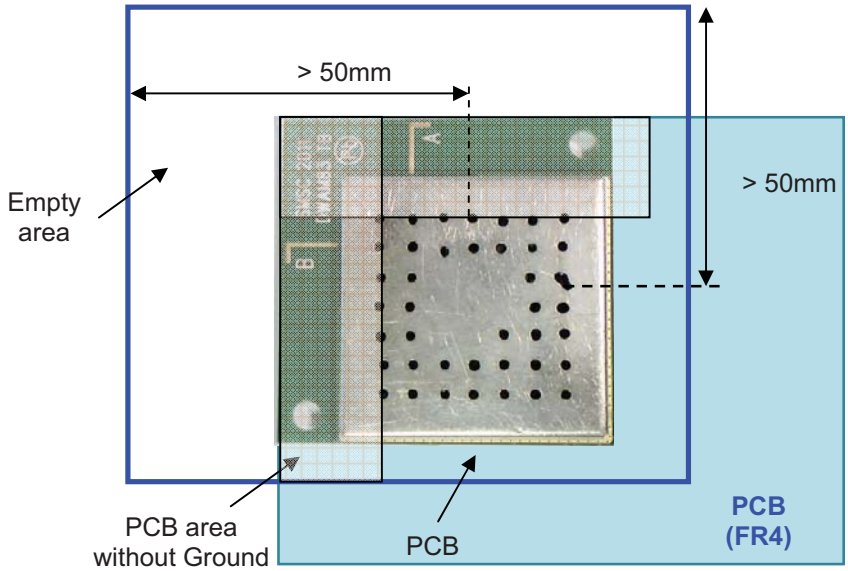
3.1. Module Placement

The module outputs typically RF Power of 18dBm @ 2.4GHz, 9.5dBm @ 5.2GHz and 16.5dBm @5.8GHz band. This holds both for the CU and the MU (in NACK mode, the MU transmits when a packet is lost and in ACK the MU acknowledges receipt of each message by RF transmission). This RF energy may be received by the application controller board and rectified by analog non-linear components (e.g. coupling capacitors) and this may eventually result in audible artifacts if not proper care is taken (especially since the air frame rate is in the audible range). It is therefore important that the RF module (especially the antennae) is separated from the analog circuitry as much as possible.

3.1.1. Potential Antenna Issues

This section goes for the embedded antennae only

- No ground plane of tracks must be placed on the application board underneath the module
- Antennas must not be placed close to metallic objects
- Antennas should not be placed in direct contact or close proximity to Plastic Casings/ objects to avoid Antenna detuning.
- Be careful not to place the wiring inside the finalized product close to the antennas.
- Please note that final antenna tuning may be required of the final product for optimal antenna performance (due to antenna detuning by the enclosure and/or surrounding components)
- Do not use a metallic enclosure or metalized plastic if the antennas are internal
- Ensure that the enclosure is tested for low RF losses when the antennas are placed internally (an easy test is to measure the heating of the enclosure when put by itself in a microwave oven)



Typical Module (RF) Placement: >30mm separation (all directions) from antennae is recommended.

3.2. General Power Supply Decoupling

The RF frame rate is in the audio frequency band. So the switching between TX and RX will cause a power supply ripple (because of the change in current between TX and RX mode) that is also in the audio frequency band. Therefore, it is important that the module power supply is isolated from the audio circuitry power supply.

Listed here below are some general guide lines:

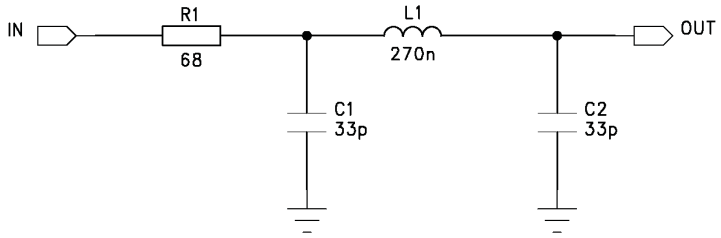
- Use a dedicated power supply for the module.
- Consider the Pi-network for power supply decoupling from the regulator to the module (large capacitor to ground, series bead inductor, large capacitor to ground).
- Isolate the control loop of the application board regulator from this 3.3V power supply domain
- Use a very short and solid ground connection from the star point of the power supply to the module.
- Isolate the module's ground from the analog ground.
- Use low ESR capacitors (e.g. Nichicon HDM)

With the above guide lines, it should be possible to suppress the switching peaks to well over 110dB below the full scale output.

3.3. Digital IO filtering

3.3.1. MCLK filtering

The audio clock signal runs over the flat foil cable to the module. The harmonics can easily radiate and exceed the regulatory limits if the drive strength is too strong and/or cable and/or PCB trace lengths are too long. To overcome this, the audio clock signal can be filtered at the source (i.e. at the crystal oscillator itself) by a simple filtering circuit such as depicted here below:

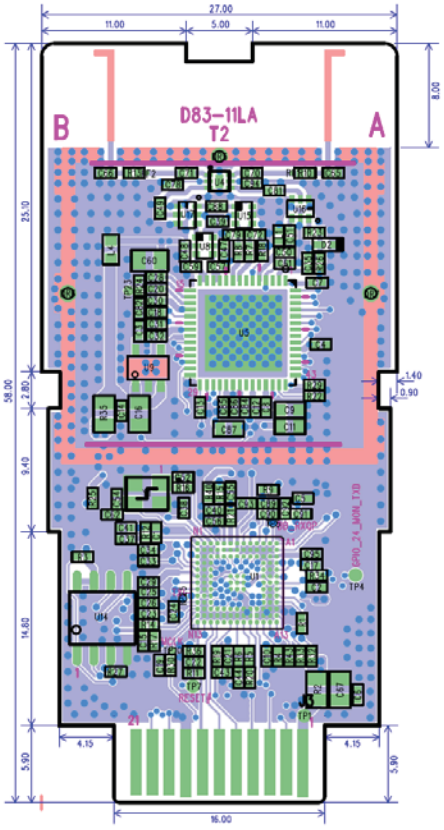


3.3.2. I^2S Bus

The I^2S bus signals are transported over the FFC. To overcome potential radiation problems, it is advised that the bus is filtered on the application board with a resistor array (e.g. 33…68Ohm) and small valued (e.g.10pF) capacitors.

3.4. Transceiver Dimension

- Module -size: 58 x 27 mm (±0.15), including 2-Printed Tri-Band antennas.



3.5. Module Picture