6.0 Electrical Specifications

6.1 GENERAL SPECIFICATIONS

Absolute Maximum Ratings (see Table 9) indicate limits beyond which damage to the device may occur. Operating Ratings (see Table 10) indicate conditions for which the device is intended to be functional.

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

The following conditions apply unless otherwise stated in the tables below:

- T_A = -40°C to +85°C
- VCC = 3.3V, IOVCC = 3.3V
- RF system performance specifications are guaranteed on National Semiconductor Austin Board rev1.0b reference design platform.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Core Logic Power Supply Voltage	-0.3	4.0	V
IOVCC	I/O Power Supply Voltage	-0.3	4.0	V
USB_VCC[1]	USB Power Supply Voltage	-0.5	3.63	V
V_I	Voltage on any pad with GND = 0V	-0.5	3.6	V
PinRF	RF Input Power		+15	dBm
T_S	Storage Temperature Range	-65	+125	°C
T_L	Lead Temperature (solder 4 sec)		+235	°C
ESD-HBM	ESD, Human Body Model		2000 [2]	V
ESD-MM	ESD, Machine Model		200	V

1. USB Interface not supported by LMX9820A firmware. Treat as no connect. Pad required for mechanical stability.
2. Antenna pin passes 1500V HBM.

Table 10. Recommended Operating Conditions[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
VCC[3]	Module Power Supply Voltage	2.85	3.3	3.6	V
IOVCC[4]	I/O Power Supply Voltage	2.85	3.3	3.6	V
t_R	Module Power Supply Rise Time			50	ms
T_O	Operating Temperature Range	-40		+85	°C
HUM_{OP}	Humidity (operating, across operating temperature range)	10		90	%
HUM_{NONOP}	Humidity (non-operating, 38.7°C web bulb temperature)	5		95	%

1. Maximum voltage difference allowed between VCC and IOVCC is 500 mV.
2. Typical operating conditions are VCC = 3.3V, IOVCC = 3.3V operating voltage and 25°C ambient temperature.
3. VCC internally regulated to VDD_ANA (see Table 11)
4. IOVCC internally regulated to VDD_DIG (see Table 11)

Table 11. Power Supply Electrical Specifications (Analog and Digital LDOs)

Symbol	Parameter	Min	Typ[1]	Max	Unit
VDD_ANA_OUT[2]	Analog Voltage Output Range		2.8		V
VDD_DIG_OUT[3]	Digital Voltage Output Range		2.5		V

1. Typical operating conditions are VCC = 3.3V, IOVCC = 3.3V operating voltage and 25°C ambient temperature. Values reflect voltages of internally generated, regulated voltages VDD_ANA and VDD_DIG
2. Output of internally generated regulated voltage VDD_ANA
3. Output of internally generated regulated voltage VDD_DIG

6.0 Electrical Specifications (Continued)

Note: The voltage regulators are optimized for the internal operation of the LMX9820A. Because any noise coupled into these supplies can have influence on the radio performance, it is highly recommended to have no additional load on their outputs.

Table 12. Power Supply Requirements[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
I_{CC-TX}	Power supply current for continuous transmit			68	mA
I_{CC-RX}	Power supply current for continuous receive			62	mA
I_{CC-Inq}	Inquiry		31		mA
I_{RXSL}	Receive Data in SPP Link, slave [3,4]		23		mA
I_{RXM}	Receive Data in SPP Link, master [3,4]		18		mA
I_{HV3}	Active HV3 SCO Audio Link		22		mA
I_{SnM}	Sniff Mode, sniff interval 1 second [3]		8		mA
$I_{SC-TLDIS}$	Scanning, no active link, TL disabled [3,5]		2.5		mA
I_{Idle}	Idle, scanning disabled, TL disabled [3,5]		0.15		mA

1. Power supply requirements based on Class II output power.
2. VCC = 3.3V, IOVCC = 3.3V, Ambient Temperature = +25°C.
3. Average values.
4. Based on UART Baudrate 115.2kbit/s.
5. TL: Transport Layer

6.2 DC CHARACTERISTICS

Table 13. Digital DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
VCC[1]	Core Logic Supply Voltage		2.85	3.6	V
IOVCC[2]	IO Supply Voltage		2.85	3.6	V
V_{IH}	Logical 1 Input Voltage		0.7 x VDD_ANA	VDD_ANA + 0.5	V
V_{IL}	Logical 0 Input Voltage		-0.5	0.2 x VDD_ANA	V
V_{HYS}	Hysteresis Loop Width[3]		0.1 x VDD_ANA		V
I_{OH}	Logical 1 Output Current	VDD_ANA = 2.8V	-1.6		mA
I_{OL}	Logical 0 Output Current	VDD_ANA = 2.8V	1.6		mA
I_{OHW}	Weak Pull-up Current	VDD_ANA = 2.8V	-10		µA
I_{IH}	High-level Input Current	V_{IH} = VDD_ANA = 2.8V	- 10	10	µA
I_{IL}	Low-level Input Current	V_{IL} = 0	- 10	10	µA
I_L	High Impedance Input Leakage Current	$0V \le V_{IN} \le$ VDD_ANA	-2.0	2.0	µA
$I_{O(Off)}$	Output Leakage Current (I/O pins in input mode)	$0V \le V_{OUT} \le$ VDD_DIG	-2.0	2.0	µA

1. VCC internally regulated to VDD_ANA (see Table 11)
2. IOVCC internally regulated to VDD_DIG (see Table 11)
3. Guaranteed by design.