B69SD25 OPERATIONAL DESCRIPTION

Operating frequencies - .190 to .535 Mhz

Modulation Modes - 2K04A2A and 6K00A3A

Operating Power levels – (5 to 25) Watts + 25%

The end user has five methods to vary operating power.

1. With the local control panel, see the user's manual Local Control Panel Diagram SLM10005 , the customer can change the output power in fine steps of 1Watt, using the outer most push buttons titled MOD/RF LEVEL ADJUST, or coarse steps of 10 Watts using the inner most push buttons.
2. This same method of adjustment is used when the local control panel is utilized as a remote control panel. The remote control panel communicates through its RS485 line back to the local control panel's RS485 line to exercise power changes.
3. With a local PC attached to the Local Control Port RS232, see pg. 65 of the user's manual for the Load Center Drawer Diagram, the customer uses a factory supplied program to enter any desired power level; with fine adjustments of 1 Watt; up to a maximum of +25% of rated power. With factory set program limits, the customer is not allowed to exceed the maximum rating of the transmitter.
4. With a remote PC communicating with the transmitter via modem, the above adjustments apply.
5. On the RF PA Power Supply, see the user's manual for SEP10003, potentiometer R4 is used at the factory for power adjustments to facilitate board test and setup. This control is jumper selectable, and it will be accessible to the customer. However, the customer can only adjust the power to their system's maximum rating due to factory set program limits.

(1) As per CFR 47 part 87.131, Radionavigation Land has various power levels. However, as per FAA Publication 6740.2D:

Class LOM Facilities are authorized output power of 25 Watts or less: Our B69 SD25 will fit in this category.

(2) The table below shows the dc voltages applied to and dc currents into the radio frequency amplifying device for normal operation over the stated power range. The table is the result of opening the clad on the RF Power Amplifier printed circuit board, SLP10001, between the Modulator circuitry and the final RF Power Amplifier. A Tekrtonix TAS 475 oscilloscope was used to verify the proper RF Power output at a 50 Ohm dummy load, a Fluke 87 digital voltmeter was used to monitor the voltage at the PA's input and a Weschler R-351 RF ammeter was used to measure the current between the Modulator and PA. The system operating frequency was 320 Khz

Watts = Calculated output power at 50 Ohm non inductive load
Pav = Voltage present at the input of the final Power Amplifier
Pai = Current present at the input of the final Power Amplifier

Watts	Pav	Pai
5	9.7	0.55
10	13.5	0.80
15	16.5	0.95
20	19.0	1.10
25	21.2	1.25

(3) Below are descriptions of all circuitry and devices provided for determining frequency, for suppression of spurious radiation, for limiting modulation, and for limiting power. Please refer to the user's manual for schematics.

Determining Frequency: See SEP10007 in the user's manual for the below discussion.

The frequency is selected by the customer through a factory supplied user interface program, but it is ultimately determined on the Controller / Monitor printed circuit Board SLP10007. On this board 32-bits are written to the Direct Digital Synthesizer (DDS) U16 on page 2 of 6 from the microprocessor U18 on page 3 of 6. U18 uses five iterative loads of an 8-bit control word to comprise the 32 bit frequency tuning word to U16. The 8-bit control word is output from U18's data port D24 – D31. The output of U16 pin 13 is a sine wave at the desired frequency and loaded into 50 Ohms. A Frequency vs. Temperature stability curve in CFR 47 part 2.1055 below establishes that the frequency changes less that 5 ppm from -30º C to +50º C.

Suppression of Spurious Radiation: See SEP10002 in the user's manual for the below discussion.

The RF Filter SLP10002 is a symmetrical 7 element 50 Ohm Butterworth Low Pass filter. Its frequency bands, chosen with jumpers, are 190-220kHz, 220-280kHz, 280-360kHz, 360-440kHz and 440-535kHz. The RF Filter accepts square wave energy from the RF Power Amplifier's impedance transformer T1 and attenuates all harmonic energy other than the fundamental frequency in one of the five bands listed above.

The second part of the spurious harmonic suppression circuit is the Auto Tuning Unit (ATU) and the radiating Antenna. As shown in CFR 47 part 2.1051 below, all harmonics are attenuated below –77 dB, when the transmitter's output is attached to a typical termination of the ATU and a 500pF capacitor in series with 10 Ohms to ground. See the system Block Diagram for the Transmitter in the user's manual on page 23 for the ATU and Antenna configuration.

Limiting Modulation: See SEP10020 and SEP10009 in the manual for the below discussion.

The Audio Board SEP10020 has a nominal voice input of –17dBm, but has minimum percent change in modulation when configured for either 600 Ohm or high impedance with an input ranging from –28dBm to +5 dBm. The audio input is fed into the balanced amplifier circuit comprised of U2A, U3A and U2B on page 1 of 2. From U2B pin 7 the Automatic Gain Control (AGC) circuit, comprised of U1C, Q3, Q4 and Q2, is utilized when jumper JP3 is made from 1 to 2. The signal from U2B is coupled through high pass filter C13, R25, C14 and Audio Input Level control R24. Q2 act as a variable resistor at the input of U1C. The resistance of Q2 is controlled by the signal level fed back from pin 8 of U1C. As the audio signal level increases, the gate voltage of Q2 decreases and the resistance decreases, thus lowering the audio input level to U1C pin 10 and holding the average audio output level from U1C pin 8 constant. This output signal is amplified and filtered by U1D and the AGC output level is adjusted by R29.

The unity gain buffer U1A on page 1 of 2, peak detector made up of CR1, C2 and R4 plus comparator U1B act together to turn switch Q1 on with the presence of an audio input greater than –28dBm. The Voice Detect signal from page 1 of 2 of the Audio PCB is fed to XA_P4 on page 6 of 6 of the Digital I/O and PWM PCB. From there it can be seen at the lower left on page 5 of 6 where, with JP1 made from 1 to 3, it acts as a squelch control for automatic code tone level reduction during simultaneous voice and code tone modulation.

The AGC output, VOICE_FLTR_IN, is fed into the audio filter made up of U4, U5A and U5B. This filter is designed to exhibit a roll off at 3000hz and exhibit 40 dB of attenuation at 4000hz. The audio filter output, VOICE_FLTR_OUT, is also fed to the Digital I/O and PWM PCB page 5 of 6 and summed with the attenuated tone signal at pin 2 of U28A. This summed output is fed to comparator U26A pin 4 and a modulation limiter circuit made up of CR1, U24A and variable resistor R5. R5 can be adjusted to limit percent modulation at any value, but it is ideally adjusted to limit over modulation caused by sudden audio peaks that would result in modulation in excess of 100 percent.

Limiting Power: See SEP10002, SEP10005 and SEP10007 in the user's manual for the below discussion.

Please refer to SEP10002, Filter/Bridge PCB. The filter circuit was explained above as a seven element Butterworth filter responsible for suppressing unwanted harmonic energy of the fundemental frequency. All RF energy leaves the filter section on page 1 of 3 at FLTR_RF and enters the RF Bridge section on page 3 of 3. The bridge, made up of C29 to C30, C33, C34, L6, L7, T2, CR2, CR3, R21 and R22, gives a calibrated output of the RF's Peak Envelope Power in both Forward (FWD) and Reverse (RFL) directions. The Bridge is factory calibrated using a non-inductive 50 Ohm dummy load and Oscilloscope in both FWD and RFL directions. Voltages proportional to FWD and RFL power leaves

L6 and L7 respectively and enters fault detection comparators (U2A, U2B) and output amplifiers U1A and U1B on page 2 of 3. A voltage proportional to the FWD and RFL leaves the board on page 3 of 3 at plugs P1A pin 16 and P1B pin 16 and routes via twisted wire pair from the RF Motherboard, SLP10004, to the Controller Motherboard SLP100012. Once on the Controller Motherboard these signals route to SLP10005, the Analog I/O board, pins 1 and 8 of P1A on sheet 5 of 5 of SLP10005. The signals are buffered through unity gain op amps (U14A, U17D) where the signal names change to sAIO1 and sAIO9 on page 3 of 5. The signals then route to page 1 of 5 to U1 and U7 pin 14. Once receiving the dd1 strobe signal, the outputs of U1, U4, U7 and U10 are placed on the first 16 bits of the microprocessor's 32 bit data buss. These bits leave the Analog I/O PCB at P1B on page 5 of 5. See the Controller Monitor PCB SEP10007 for the remaining discussion of limiting power.

The signals representing the FWD and RFL power are seen on page 6 of 6 of the Controller Monitor PCB at P6A pins 2 and 12 where their names are changed to PAD1 and PAD9 respectively. These signals route to unity gain buffers U1B and U9B on page 1 of 6 and ultimately to the twelve bit A to D converters U2 pin 41 and U10 pin 41. Thus the FWD and RFL power readings have been converted from the analog voltage measured on the Filter/Bridge PCB to a twelve bit digital word readable and acted on by the microprocessor (uP) on page 3 of 6.

During normal operation the uP monitors the FWD and RFL power to determine if the FWD power has increased over the maximum software limit. If this condition should exist, the uP would shut down the system or transfer to the secondary system. During customer setup or periodic adjustment, the customer has the ability to only adjust power up to the maximum software limit. When this limit is reached, the power level will be held at the maximum value and displayed on the Operation Panel or Personal Computer (PC) as a constant value. This same power limit is activated when an attempt to adjust over the power limit occurs from a remote PC via modem, local PC control, remote panel operation by RS485 or local control panel adjustment. For 25 Watt rated systems the maximum power limit activates at 25 percent over the rated power.

See below for an overall description and general theory of operation.

SD25,SD50, and SD100 Description and General Theory of Operation

Briefly, the SDxx system takes advantage of the powerful Motorola ColdFire® microprocessor. It is located on the Controller / Monitor PCB and is the heart of the system, generally controlling all system operation either directly or in conjunction with an Analog and Digital I/O multiplexing interface.

The following are all controlled by the embedded firmware, Direct Digital Synthesis (DDS) of RF frequency and AF tone frequency , Identifier Morse code dot, dash and space intervals., Customer IDENT sequence, the standard alarms, any additional Fault handling based on multipoint voltage, current and temperature monitoring , transfer criteria (Dual Only), power limiting and modulation limiting.
RS 232,RS422 and RS485 protocols are supported. A US Robotics Modem is furnished for using phone lines.

The RF section consists of the RF PA Power Supply, The RF PA Amplifier, The Filter /Bridge, and the Mother Board which interconnects them all. This section is interconnected with the Controller/Monitor which Dictates the Frequency of operation, power output, and modulation percentage. Operational information is also passed. A more detailed breakdown as to functionality follows on a board by board basis.

SLP10007 – Controller / Monitor

The CONTROLLER/ MONITOR employs the new Motorola MCF5206 COLDFIRE® microprocessor. It encompasses the following sections:

COLDFIRE Processor – 32-bit
ADC – 8-Channel 12-bit
DAC – 8-Channel 8-bit
DDS - Radio Frequency (190K to 1800KHz)
DDS – Tone Frequency (400 / 1020 Hz)
Flash Memory – 4Mb
DRAM – 16Mb
Programmable Logic
Digital I/O (Read/Write)
UART
Watch Timer and NV-RAM

COLDFIRE Processor section:
The LOGIC program creates 16MHz from 32MHz for the clock frequency of the microprocessor. The processor controls several peripheral functions such as memory, task timers, I/O bus lines, and RS-232 ports. For the dual system, the primary Controller / Monitor and secondary Controller / Monitor may talk to each other through Controller / Monitor Motherboard (SLP10012) by using 2 COM-PORT lines (ex: RXD & TXD). Each Controller / Monitor has one interrupt line for paying attention what other Controller / Monitor has something is important, then Controller / Monitor sets “RS-232” MUX to be enabled.

Analog-to-Digital converter (ADC) section:
The Controller / Monitor Controller PCB has two (AD7891) 12-bit ADC chips, so there are 16 analog inputs. The channel selection of input range is 0 to +5 V.

Digital-to-Analog Converter (DAC) section:
The 8-bit DAC provides eight digitally controlled dc voltage outputs. The limited of output range is 0 to +5 V. The user may adjust dc analog level or turn on/off likely digital level.

RF Direct Digital Synthesizer (DDS) section:

The 50MHz clock input is for the RF DDS. The RF DDS provides two different signal-waves (square wave and sine wave). The square wave level is 0 to +5.0 V (recommended) and the sine wave level is 0 to 1.0 V. The DDS has 8 data digitally inputs. The code may store 4 data bytes for the 32-bit RF DDS tuning word. RF is enabled by writing the desired frequency to the DDS, and disabled by writing a zero frequency to the DDS. The RF DDS goes the signal through EMI filter to generate a low jitter square wave output.

Tone Frequency Direct Digital Synthesizer section:
The 50MHz clock input is also used by the AF DDS. The AF DDS signal is sine wave only. The user may adjust AF amplitude modulation. Two methods for keying the tone are available. The first is like the RF DDS - load a frequency into the registers of the DDS chip. The second is simply "keying" (digital ON/OFF) of a reserved I/O signal. The settings for ID mode, ID code, ID rate, sequence of operation and other parameters are set by a user interface program.

Flash Memory section:
Its 4Mb of memory is organized as 512K x 8. The firmware for the E(E)PROM is written in assembly / C code. It may move data to DRAM and NV-RAM memory when the power is up. It is simple to replace when the code is updated.

DRAM section:
The PCB has two DRAM devices. It totals 1Mb x 16 x 2 (32-bit data). During initialization the EPROM moves data to the DRAM.

Programmable LOGIC (LATTICE device) section:
There are two LATTICE chips on the PCB. The Programmable Logic provides several necessary functions such as control lines, 1Hz, 16MHz, enabled / disabled lines and interrupt lines.

Digital I/O section:
There are 32 digital inputs or outputs and 4 control lines for writing. Each control has 8 data lines organized as one byte each. They are used for the status fault, frequency reading, reset, and control data.

Universal Synchronous/Asynchronous Receiver/Transmitters (UART) section:
The Controller / Monitor processor has two UARTs. They are used for RS-232 only. SAC offers four possible transmitter configurations as follows:
Single TX without a LOCAL CONTROL panel:
The Controller / Monitor serial port 1 is probably used for PC.
The Controller / Monitor serial port 2 is used for PC / Modem through Controller / Monitor Motherboard (Controller / Monitor MB – SLP10012).
Single TX with a LOCAL CONTROL panel:
The Controller / Monitor serial port 1 is used for the local operating panel.
The Controller / Monitor serial port 2 is used for PC / Modem through Controller / Monitor MB.
Dual TX without a LOCAL CONTROL panel:
Either Controller / Monitor1 or Controller / Monitor2 serial port 1 is probably used for PC.
The serial port 2 is used for PC / Modem through Controller / Monitor MB.
Dual TX with a LOCAL CONTROL panel:
Either Controller / Monitor1 or Controller / Monitor2 serial port 1 is used for local operating panel.
The serial port 2 is used for PC / Modem through Controller / Monitor MB.

Watch Timer and NV-RAM section:
The NV-RAM provides 32Kb of memory available to the user. The NV-RAM can hold data more than 10 years in the absence of power. It allows the operator to store various settings in NV memory. When the power is up, Controller / Monitor can follow the user settings in NV memory. The Watchdog timer restarts an out of control Controller / Monitor processor. The code may use the real-time clock for 255 task timers (background).

SLP10009 Digital I/O and PWM Theory

The Digital I/O and PWM PCB consists of several sub sections which accomplish the following functions:

Digital Input State Reading
Digital Output Control
Frequency Counting
Audio to PWM Conversion
AWOS Option.

The Digital Input Section receives and conditions state information from the various system modules mainly indicating the fault status of these sections but also monitoring the state of other sensors. While retaining their unique state value all of these signals are combined into one interrupt request (IRQ) line for rapid servicing of external events. A local red fault LED indicates the arrival of a fault condition. The processor take action depending on the nature of the condition.

The Digital Output Section conditions and outputs a state condition to the various system modules primarily to perform fault resets. Antenna switching is also controlled by this section.

The Frequency Counter section conditions and samples the Direct Digital Synthesizer generated frequency from the RF power amplifier. This data is relayed to the processor which monitors the output RF frequency for accuracy.

The PWM section of this board inputs audio signals from the tone generating Direct Digital Synthesizer and from an optional voice input piggybacked PCB for AWOS functionality. The composite audio signal is summed with an adjustable DC level and converted into a 75 kHz Pulse Width Modulated signal with its basic no-audio duty cycle being set at a fixed percentage. This fixed level facilitates modulation tracking irregardless of power level output. A back-up modulation limiting circuit prevents over-modulation from damaging the RF Amplifier but main over modulation protection control for Tone signals is a software function of the processor which monitors modulation at all times.

The Optional AWOS plug in PCB Contains an AGC section which prevents over-modulation by the USER audio signal. There is also a built in active Audio band-pass filter which eliminates signals outside of the 300 to 3000Hz pass band. Signals generated on this Optional PCB also alert the processor which then cuts the main tone level and temporarily ceases issuing any modulation alarms based on modulation percentage.

SLP10020 OPTIONAL AUDIO PCB (AWOS)

The Audio PCB is an OPTIONAL addition to the normal system which allows the user to broadcast AWOS announcements. The Option is implemented as a plug in piggyback board to the Digital I/O PCB and consists of four sections as follows:

Voice Amplifier
Automatic Gain Control
Chebychev Passband Filter
Voice Detector

The Voice amplifier takes the nominal -17dBm signal level and boost it to a level useable by the AGC section
It is common mode balanced and its Gain is adjustable.

The AGC circuit is responsible for modulation limiting. It is adjusted to "capture" the level at -17dBm and output a constant modulation level to the Digital I/O PWM section up to levels exceeding +10 dBm. This section prevents inadvertent over modulation of the voice signal, and is necessary since the Controller / Monitor has no control over user input.

The Chebychev Passband filter is designed for 300 to 3000 Hz. The output at 4000 Hz is down more than 45 dB ensuring any out of band audio signals from the USER will not cause adjacent channel interference.

The Voice Detector has two functions. It detects the presence of an announcement sequence and automatically attenuates the Keying tone level down to 20% modulation. The announcement level is summed with the Keying tone level and set to achieve 95% composite modulation. This action prevents over modulation and allows the announcement to be heard over the beacon Morse code IDENT tones. It also signals the Controller /Monitor which in turn temporarily suspends Modulation Alarms since the IDENT tone level is dropped below the alarm threshold.

SLP10005 Analog I/O

The Analog I/O and PWM PCB consists of several sub sections which accomplish the following functions:

Analog Signal Input
Analog Signal Output
Modulation Detection

The Analog Input Section is essentially a 40 channel low pass filtered analog MUX. These multiplexed inputs are actually an expansion scheme which adds additional analog inputs to those already available to the controller/ monitor. This allows the overall system to be expanded to control larger multi-section transmitters up to 1KW at present.
Signals such as RF Power Amplifier voltage, current and temperature, to name only a few, are sampled and read in to the Controller / Monitor via this MUX. The multiplexing process is directly controlled by the Controller Monitor.

The Analog Signal Output Section is a smaller MUX facilitating output control expansion. As an example, an analog control signal originating in the Controller / Monitor such as PWR_LEVEL (a 0.0 to 4.0 volt DC level) is sent to this Sample and Hold MUX channel 1. Via this channel the MUX outputs this particular level to the PA Power Supply which dictates the output power level of the transmitter. The Next Channel of the MUX can control yet another module requiring some level of control voltage if needed.

The Modulation Detector receives a detected sample of the RF envelope form the bridge circuit and converts it into two DC levels called Vmax and Vgref. The Controller / Monitor reads in these levels and subtracts Vgref from Vmax to derive Vmin. Vmax and Vmin are then used in the standard modulation formula to obtain modulation percentage in the same way as someone would calculate it manually using an oscilloscope. This circuit is intended to free the Controller / Monitor from having to sample large amounts of envelope data to statistically calculate the percentage thereby facilitating more of a real-time monitoring of modulation. Correction curves are embedded to resolve linearity issues arising from the detection process.

SLP10017 Low Voltage Power Supply

The LVPS Furnishes +5, +12, and -12VDC to the Controller/ Monitor Mother Board and itself plugs into the mother PCB. It is transformer driven to allow for 115/230VAC operation. 48VDC operation allows running off of emergency battery. The LVPS also passes 50VDC or 48V BATTERY to the user section to power miscellaneous circuitry.

SLP10003 PA Power Supply Theory

The PA Power Supply (PAPS)

The PA Power Supply consists of three sub-sections, namely, the Inrush Current section , the DC Controller, and the DC-DC Converter. Included with these are associated signal sense and fault circuitry. Taking them one at a time in the general structure of their usage follows.

1.) The Inrush Current Section:
After receiving the HV-ON signal from the Controller / Monitor, this section switches on HV-DC and controls the charge rate of the HV DC supply capacitors to avoid damagingly high inrush currents. It does this by limiting the charge current and monitoring the voltage build-up on the large capacitor bank until it reaches an acceptable charge level, after which unlimited current is applied. The Raw HV is sampled and fed back to the Controller / Monitor.

2.) The DC Controller
This section is a buck regulator with feedback control to reduce the Raw HV DC down to level usable by the RF Power Amplifier section. Under Controller / Monitor control, the output of this section can be varied, which in turn will vary the power output of the RF Power Amplifier. The feedback allows the DC Controller to respond to the peak power demands of the PA greatly reducing or eliminating carrier droop. This section Also isolates the PA from input power fluctuations and or "brown-outs", and maintains a steady power output over widely varying conditions. Since the DC Controller controls the RF power output and the PA sections modulator can run a constant carrier level duty cycle, power can be changed with out resetting the modulation percentage. The DC Controllers Voltage and Current output is sampled and fed back to the Controller / Monitor for monitoring. Fault conditions for current and voltage will automatically shut down the section and report to the Controller / Monitor which can attempt to bring the unit back on line if the problem was transitory or perhaps switch transmitters if the system is a dual configuration.

3.) The DC-DC Converter
The converter will take an optional 48VDC battery back-up source and produce HV which is combined with the normal AC HVDC to provide a seamless transition from AC to DC operation in the event of a Brownout or AC power failure. It is purposely set lower than the nominal AC HVDC to allow for simple diode combining and to preserve battery life while outputting a legal signal. It is NOT regulated but rather will slowly output less HV as the batteries drain. If regulated it would draw more and more current as the batteries became weaker. Since the system is computer controlled decisions can be made to stay on the air at reduced power levels in emergency situations allowing battery conservation . The Converter is a basic Chopped DC-DC converter with over-current sensing and local fault shutdown latches. The fault condition is also reported to the Controller / Monitor. A Reset of all latched fault logic states can be is performed by the Controller / Monitor as necessary. A dual low voltage +12VDC supply 12VA and 12VB is fed by +50VDC derived from the AC line or 48VDC supplied by the battery backup ensuring continuous operation of the low level stages after the initial power on. The separated 12V feeds ensures minimal cross-talk between the DC-DC Controller and the DC Controller. As an aside the 50VDC supply (located elsewhere depending on the system) is also monitored by the Controller / Monitor along with 48VDC Battery current and voltage for diagnostic information.

SLP10001 RF Power Amplifier

The RF Power Amplifier PCB is a Pulse Width Modulator and RF power amplifier in one package. The Pulse width Modulator section is commonly called the Modulator and the RF Power Amplifier is commonly called the PA. These terms will be used for the rest of this discussion.

The PA section is comprised of a broadband pre-amplifier and Class "D" RF power amplifier. It inputs either the Controller / Monitor controlled Direct Digital Synthesized RF drive signal or a customer furnished signal. Its output power is controlled by the Modulator.

The Modulator is basically a 75 kHz buck converter. It inputs D.C. High Voltage from the PA Power supply Section and uses a 75 kHz square-wave input from the Controller / Monitor-I/O section to chop, filter and reduce the DC-HV to a level usable by the PA. The Voltage the Modulator outputs to the PA is a function of both the input HV and the duty cycle of the 75 Khz square-wave. The 75 kHz Duty cycle of is set to 45% and not used to change the overall RF Power output level. The power output level of the PA is set by changing the input DC-HV and this is done under Controller / Monitor control. To Modulate the PA, audio frequency information in the form of a Morse Code Station ID tone sequence or an AWOS voice announcement, pulse width modulates the 75 kHz signal controlling the Modulator section thus varying its output voltage at the audio rate. This varies the instantaneous voltage applied to the PA, modulating its output Power.

Critical parameters such as PA Voltage , Current , and Temperature are sensed and monitored continuously by the Controller / Monitor. Local (on board automatic) over-current protection is built in. The protection scheme also provides interrupt driven fault reporting to the Controller / Monitor.

SLP10002 Filter/Bridge PCB Theory

The Filter/Bridge includes a broadband toroidal impedance transformer, a seven pole Butterworth low pass filter, a broadband RF power bridge, modulation envelope detector and associated level sampling and fault latching circuitry.

The Impedance transformer receives as input the RF Power Amplifiers Class D output and impedance matches it to the 50Ohm Butterworth Low Pass Filter, which is configured for optimum characteristics via simple jumpers for the frequency band in use. The sinusoidal 50Ohm output of the Filter is Fed then fed through the RF power bridge which reports readings of Forward and Reflected RF Power to the Controller / Monitor. The Controller / Monitor then normalizes and calibrates the power curve and calculates SWR. Fault latches are also set up to report High reflected power or RF over-current conditions for immediate action via a fault interrupt structure. A sample of the final RF output envelope is detected and sent back to the Controller / Monitor where other circuitry derives Vmax/Vmin information for modulation percentage calculation via Controller / Monitor firmware.

SLP10016 – OPTIONAL Local / Remote Control

The Optional Local Control can be used as either a local or remote operating panel. The Local Control is a microprocessor-based (Motorola M68HC11) unit offering partial control over the controller / monitor and thereby the system. It offers similar functionality to a standard front panel on older equipment.

Pushbuttons allow the user to select and or control the following:
Primary Transmitter Select (1 or 2)
Mode Select (ID, CONT or CARR)
Transmitter Displayed (1 or 2)

And view readings of: readings for:
PA Voltage

PA Current
PA Temperature
Forward Power
Reflected Power
Modulation%
Audio Frequency (tone)
RF Frequency

The user can adjust or set the:
Modulation Percentage
RF Power output level
RF ON/OFF
Enable/Disable Alarms
Select Local/Remote Control

When one of any pushbuttons is pressed except RESET, the 6811 processor sends a data command to the Controller / Monitor through the serial communication port.
RESET forces Local Panel re-initialization.

The 7 segment led display update comes from the Controller / Monitor The displays provide the 3 following groups for reading:
RF Power:
Up to 4 digits display the Modulation%, forward power and reflected power.
Power Amplifier (P.A.):
Up to 3 digits Display the voltage, current and temperature.
Frequency:
Up to 5 digits display the tone frequency (set) and RF frequency (measured).

The LED indicators simply display the system status. The Local Control receives a command string from the Controller / Monitor and uses this to set the status indicators.
The complex logic needed to for pushbutton control and display is accomplished using programmable gate-array logic.
The Local Control provides two serial communication ports (RS-232 / RS-485). The RS-232 port is used locally for the Controller / Monitor serial port 1. The RS-485 port is connected remotely to the Controller / Monitor port 1.