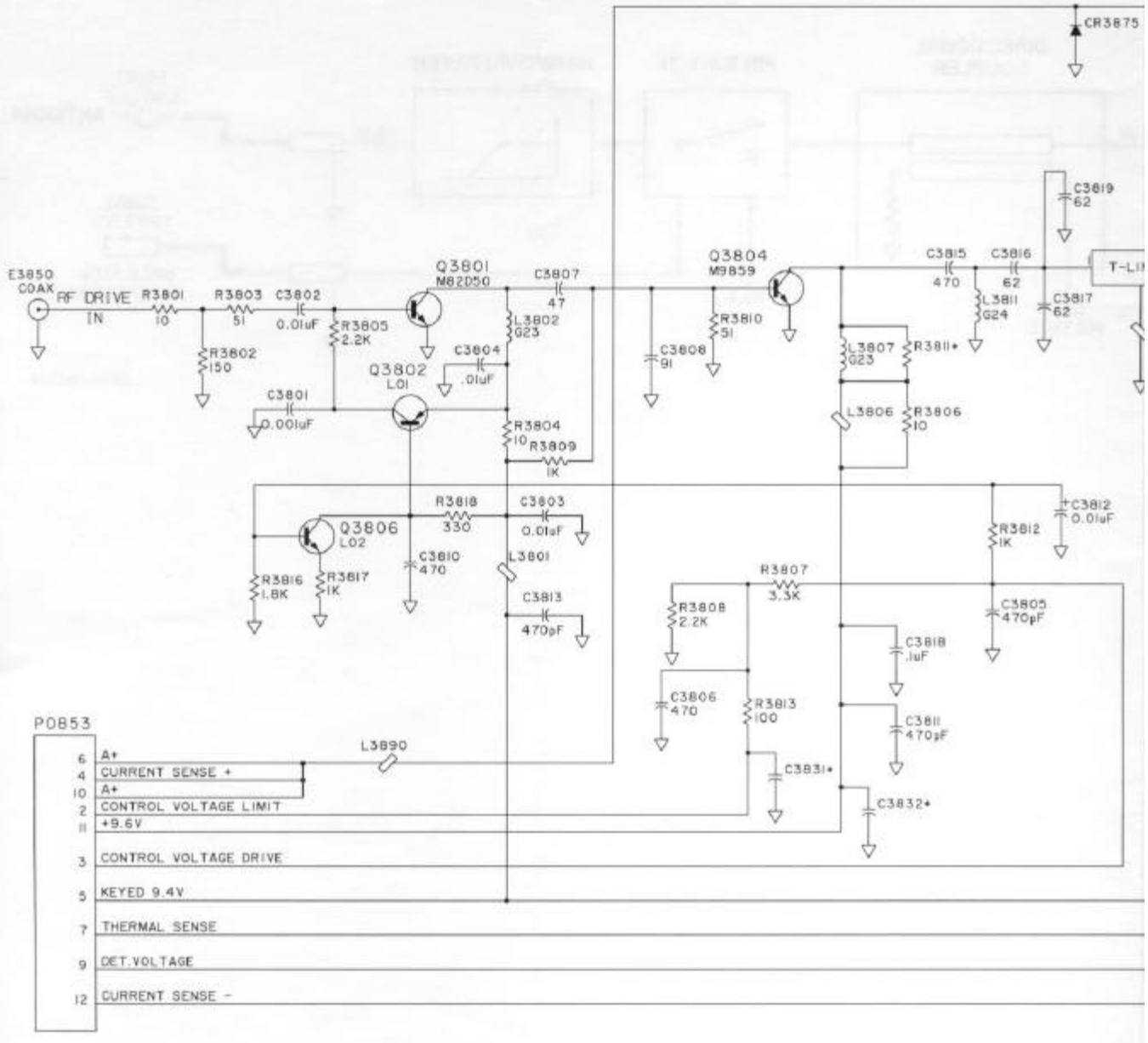
CIRCUIT SCHEMATICS

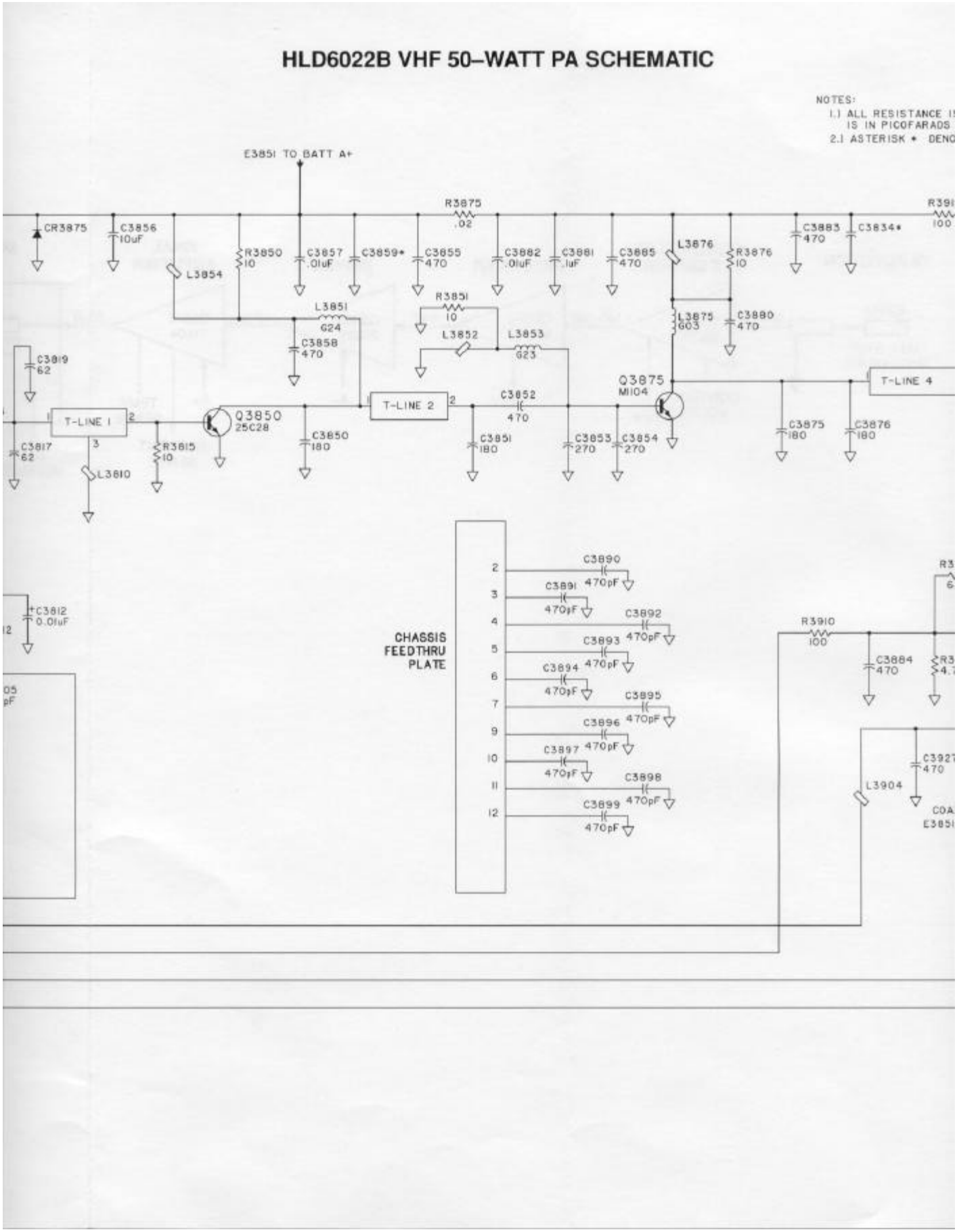
Pursuant to 47CFR 2.1033(c)10

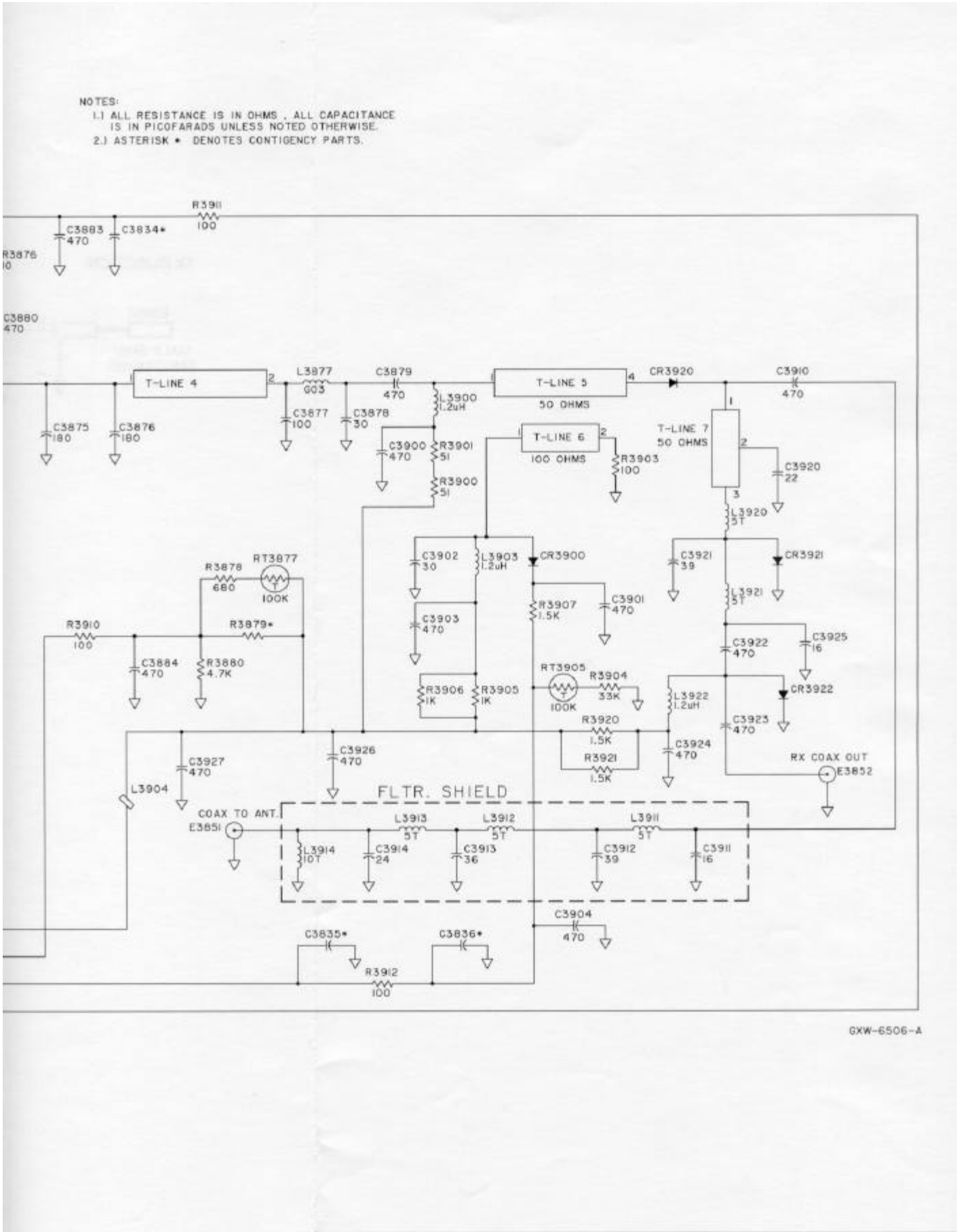
EXHIBIT	DESCRIPTION
5A	RF POWER AMPLIFIER/HARMONIC FILTER
5B	EXCITER



Schematic, Circuit Board Diagrams, and Parts List
for HLD6022B *Spectra* VHF 50–Watt PA
PW–6505–A
(Sheet 1 of 2)
3/30/90

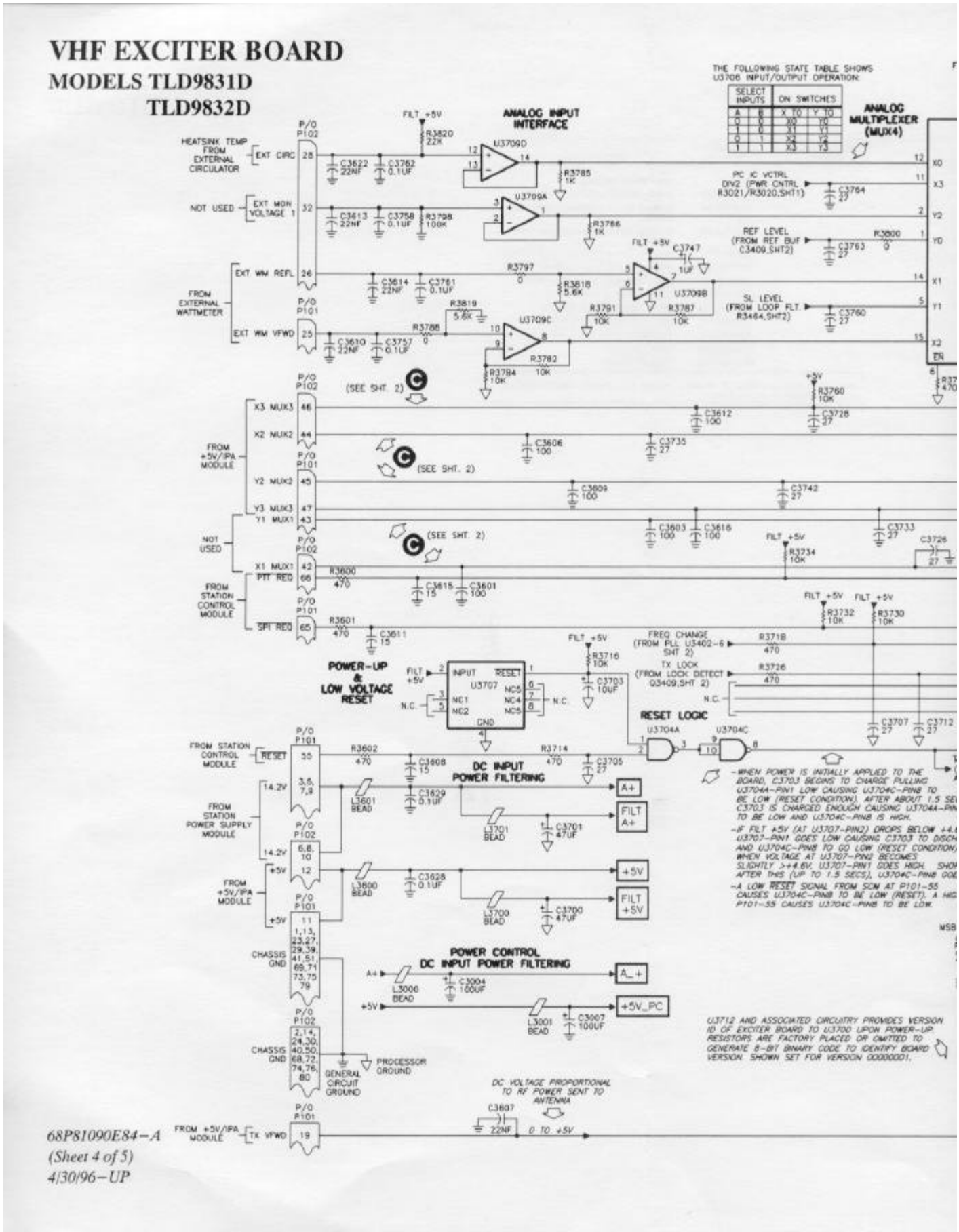
HLD6022B VHF 50–WATT PA SCHEMATIC

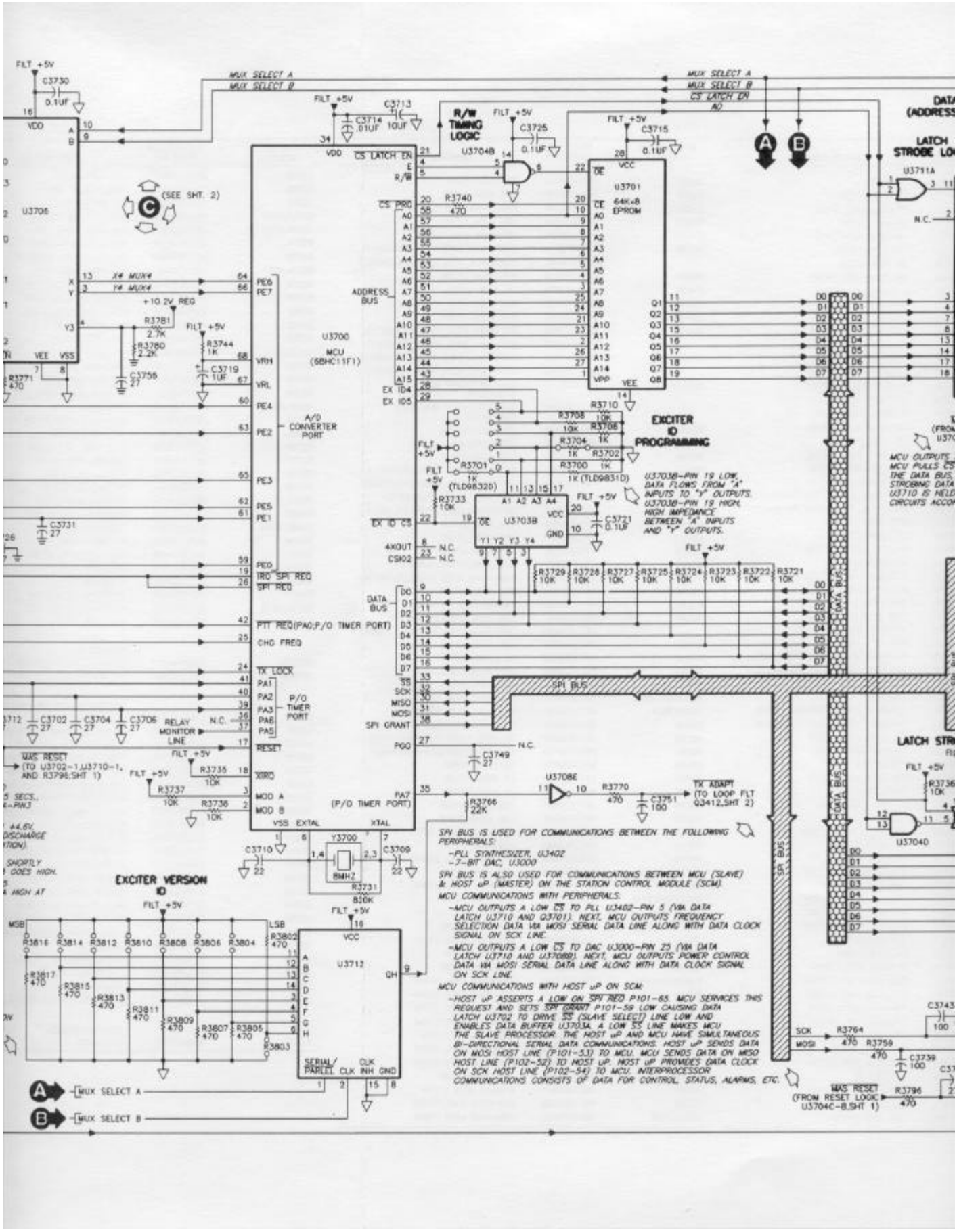


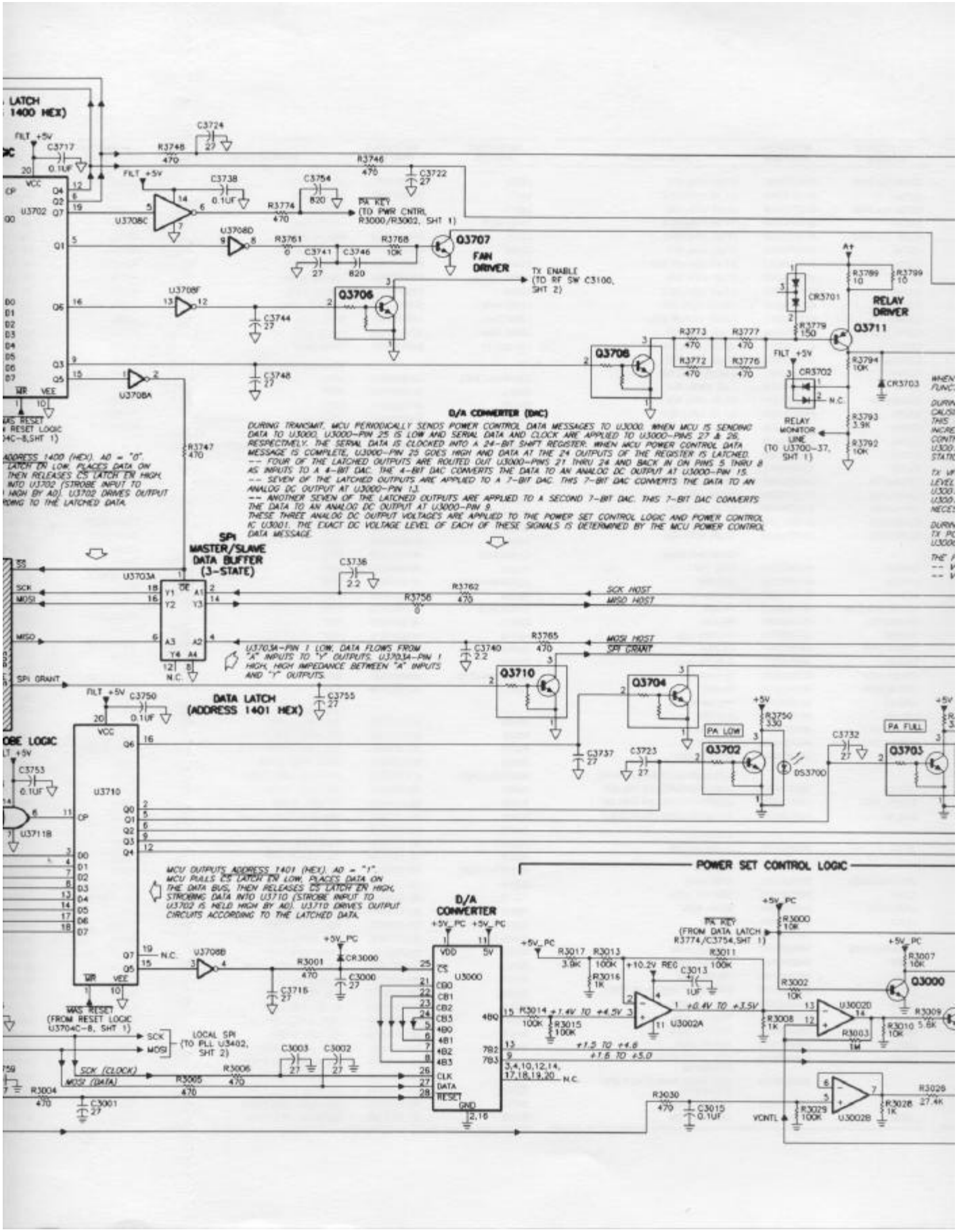

NOTES:
1.) ALL RESISTANCE IS IN OHMS . ALL CAPACITANCE IS IN PICOFARADS UNLESS NOTED OTHERWISE.
2.) ASTERISK * DENOTES CONTIGENCY PARTS.
R3911
100
C3883
470
C3834*
R3876
C3880
470
T-LINE 4
L3877
G03
C3879
470
C3877
100
C3878
30
C3875
180
C3876
180
L3900
1.2uH
C3900
470
R3901
51
R3900
51
T-LINE 5
50 OHMS
CR3920
C3910
470
T-LINE 6
100 OHMS
R3903
100
T-LINE 7
50 OHMS
C3920
22
L3920
5T
C3902
30
L3903
1.2uH
CR3900
R3907
1.5K
C3901
470
C3903
470
C3921
39
CR3921
L3921
5T
R3878
680
RT3877
100K
R3910
100
R3879*
C3884
470
R3880
4.7K
C3922
470
C3925
16
RT3905
100K
R3904
33K
R3906
1K
R3905
1K
L3922
1.2uH
CR3922
C3923
470
R3920
1.5K
R3921
1.5K
C3924
470
C3926
470
C3927
470
L3904
RX COAX OUT
E3852
FLTR. SHIELD
COAX TO ANT.
E3851
L3913
5T
L3912
5T
L3911
5T
L3914
10T
C3914
24
C3913
36
C3912
39
C3911
16
C3904
470
C3835*
C3836*
R3912
100
GXW-6506-A

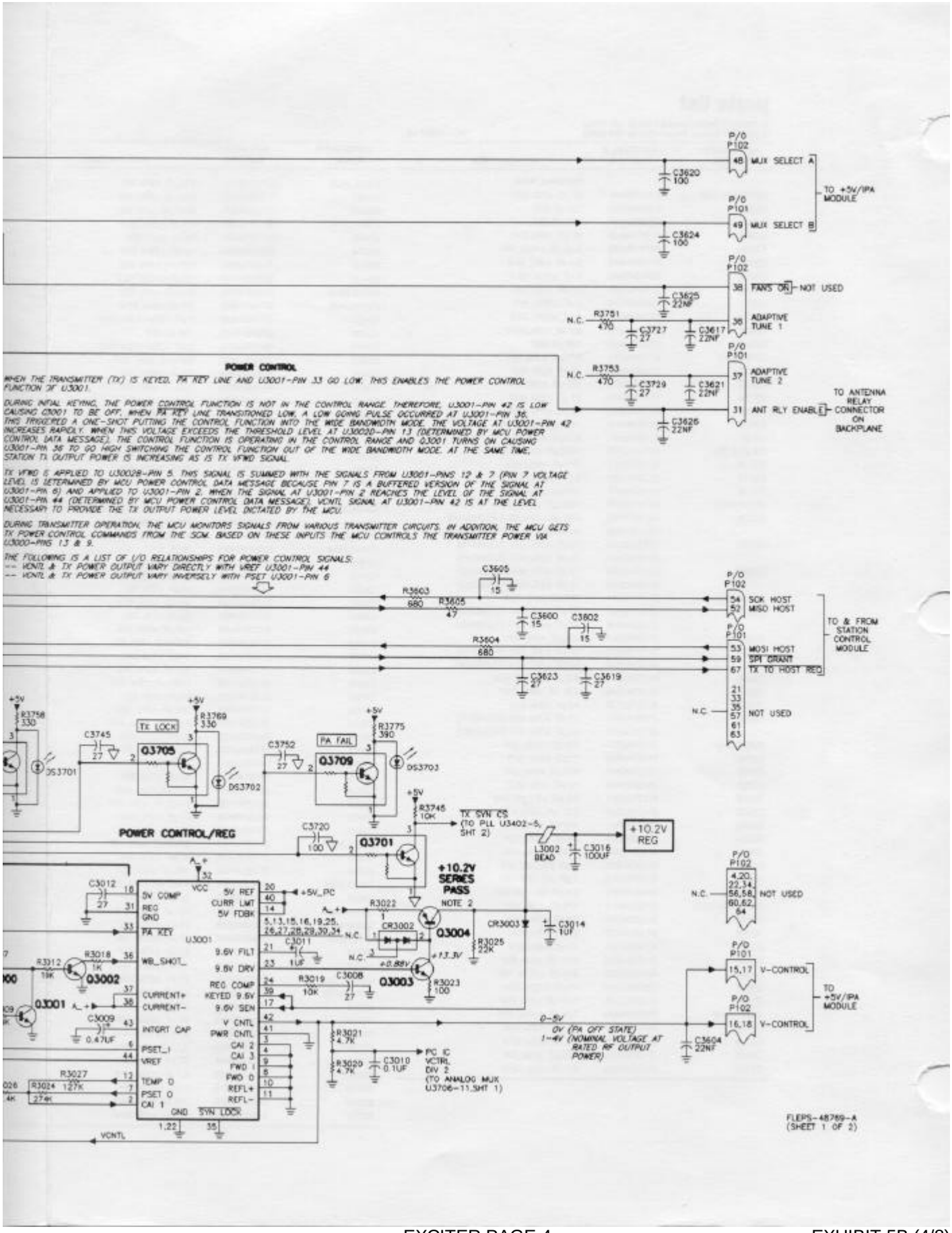
VHF EXCITER BOARD

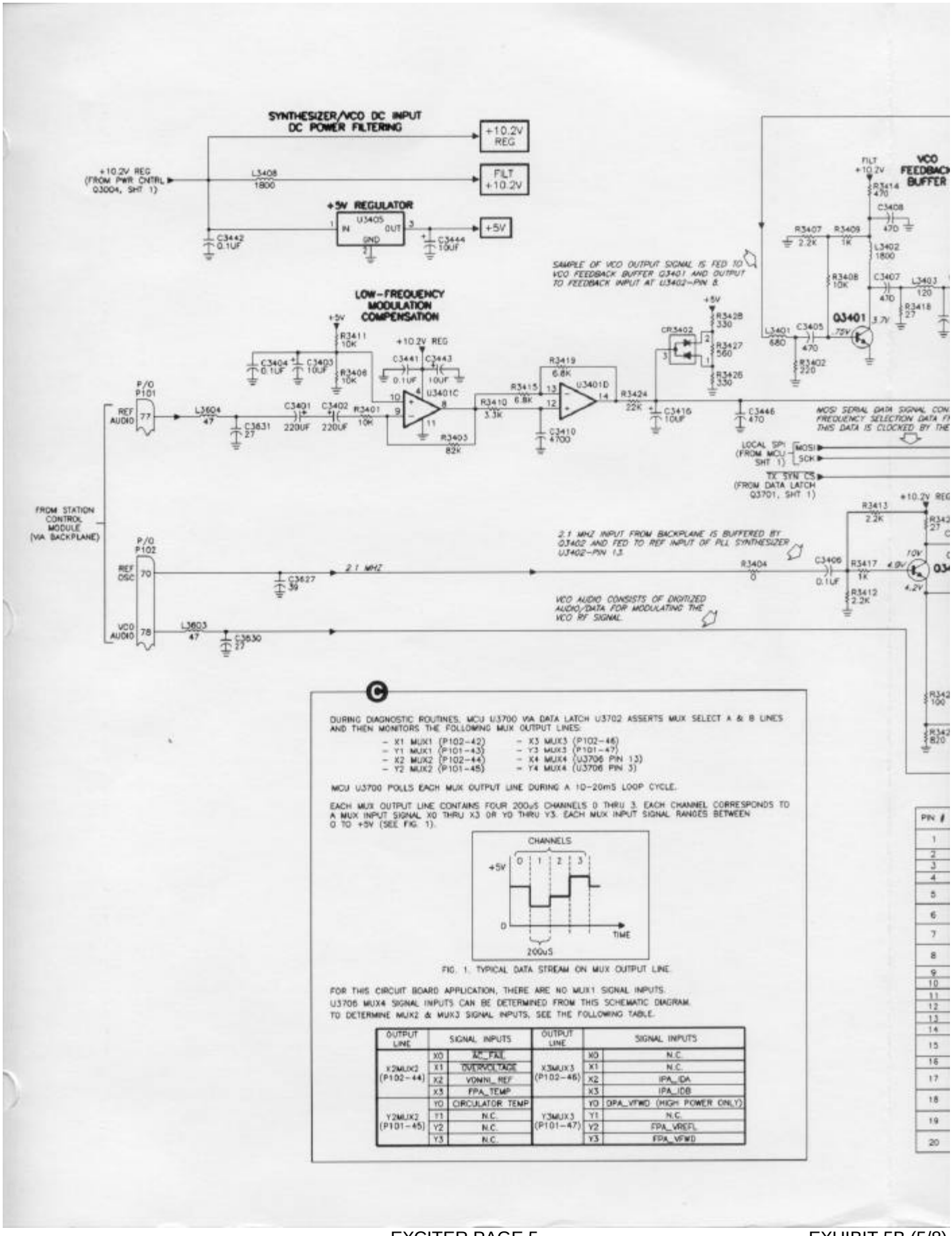
MODELS TLD9831D
TLD9832D

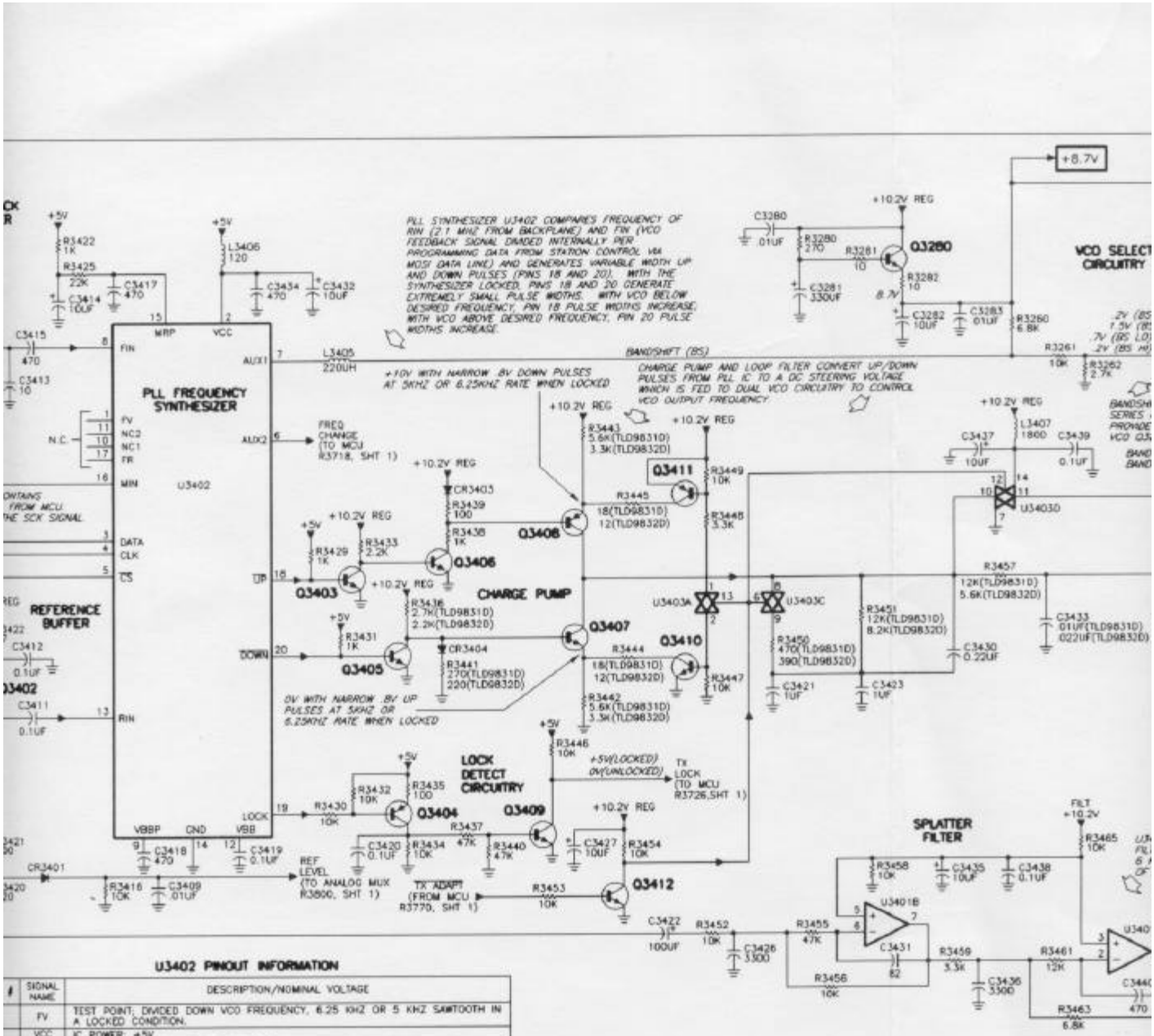



MUX SELECT A
MUX SELECT B
CS LATCH EN
A0
R/W TIMING LOGIC
U3704B
U3701
64K x 8 EPROM
U3700
MCU (68HC11F1)
A/D CONVERTER PORT
P/O TIMER PORT
EXCITER ID PROGRAMMING
U3703B
U3708A
U3708B
U3712
Y3700
8MHZ
SPI BUS
DATA BUS
ADDRESS BUS
EXCITER VERSION ID
SPI BUS IS USED FOR COMMUNICATIONS BETWEEN THE FOLLOWING PERIPHERALS:
-PLL SYNTHESIZER, U3402
-7-BIT DAC, U3000
SPI BUS IS ALSO USED FOR COMMUNICATIONS BETWEEN MCU (SLAVE) & HOST uP (MASTER) ON THE STATION CONTROL MODULE (SCM).
MCU COMMUNICATIONS WITH PERIPHERALS:
-MCU OUTPUTS A LOW ON CS TO PLL U3402-PIN 5 (VIA DATA LATCH U3710 AND Q3701). NEXT, MCU OUTPUTS FREQUENCY SELECTION DATA VIA MOSI SERIAL DATA LINE ALONG WITH DATA CLOCK SIGNAL ON SCK LINE.
-MCU OUTPUTS A LOW CS TO DAC U3000-PIN 23 (VIA DATA LATCH U3710 AND U3708B). NEXT, MCU OUTPUTS POWER CONTROL DATA VIA MOSI SERIAL DATA LINE ALONG WITH DATA CLOCK SIGNAL ON SCK LINE.
MCU COMMUNICATIONS WITH HOST uP ON SCM:
-HOST uP ASSERTS A LOW ON SPI REQ P101-65. MCU SERVICES THIS REQUEST AND SETS SPI GRANT P101-59 LOW CAUSING DATA LATCH U3702 TO DRIVE SS (SLAVE SELECT) LINE LOW AND ENABLES DATA BUFFER U3703A. A LOW SS LINE MAKES MCU THE SLAVE PROCESSOR. THE HOST uP AND MCU HAVE SIMULTANEOUS BI-DIRECTIONAL SERIAL DATA COMMUNICATIONS. HOST uP SENDS DATA ON MOSI HOST LINE (P101-53) TO MCU. MCU SENDS DATA ON MISO HOST LINE (P102-52) TO HOST uP. HOST uP PROVIDES DATA CLOCK ON SCK HOST LINE (P102-54) TO MCU. INTERPROCESSOR COMMUNICATIONS CONSISTS OF DATA FOR CONTROL, STATUS, ALARMS, ETC.
MAS RESET
(FROM RESET LOGIC U3704C-8,SHT 1)
TX ADAPT
(TO LOOP FLT Q3412,SHT 2)
(SEE SHT. 2)


LATCH
1400 HEX)
U3702
U3708C
U3708D
Q3707
FAN
DRIVER
TX ENABLE
(TO RF SW C3100,
SHT 2)
U3708F
Q3706
U3708A
Q3708
RELAY
DRIVER
Q3711
CR3701
CR3702
CR3703
RELAY
MONITOR
LINE
(TO U3700-37,
SHT 1)
D/A CONVERTER (DAC)
DURING TRANSMIT, MCU PERIODICALLY SENDS POWER CONTROL DATA MESSAGES TO U3000. WHEN MCU IS SENDING DATA TO U3000, U3000-PIN 25 IS LOW AND SERIAL DATA AND CLOCK ARE APPLIED TO U3000-PINS 27 & 26, RESPECTIVELY. THE SERIAL DATA IS CLOCKED INTO A 24-BIT SHIFT REGISTER. WHEN MCU POWER CONTROL DATA MESSAGE IS COMPLETE, U3000-PIN 25 GOES HIGH AND DATA AT THE 24 OUTPUTS OF THE REGISTER IS LATCHED.
-- FOUR OF THE LATCHED OUTPUTS ARE ROUTED OUT U3000-PINS 21 THRU 24 AND BACK IN ON PINS 5 THRU 8 AS INPUTS TO A 4-BIT DAC. THE 4-BIT DAC CONVERTS THE DATA TO AN ANALOG DC OUTPUT AT U3000-PIN 15.
-- SEVEN OF THE LATCHED OUTPUTS ARE APPLIED TO A 7-BIT DAC. THIS 7-BIT DAC CONVERTS THE DATA TO AN ANALOG DC OUTPUT AT U3000-PIN 13.
-- ANOTHER SEVEN OF THE LATCHED OUTPUTS ARE APPLIED TO A SECOND 7-BIT DAC. THIS 7-BIT DAC CONVERTS THE DATA TO AN ANALOG DC OUTPUT AT U3000-PIN 9.
THESE THREE ANALOG DC OUTPUT VOLTAGES ARE APPLIED TO THE POWER SET CONTROL LOGIC AND POWER CONTROL IC U3001. THE EXACT DC VOLTAGE LEVEL OF EACH OF THESE SIGNALS IS DETERMINED BY THE MCU POWER CONTROL DATA MESSAGE.
SPI
MASTER/SLAVE
DATA BUFFER
(3-STATE)
U3703A
SCK HOST
MOSI HOST
MISO HOST
MOSI HOST
SPI GRANT
U3703A-PIN 1 LOW, DATA FLOWS FROM "A" INPUTS TO "Y" OUTPUTS. U3703A-PIN 1 HIGH, HIGH IMPEDANCE BETWEEN "A" INPUTS AND "Y" OUTPUTS.
DATA LATCH
(ADDRESS 1401 HEX)
U3710
Q3710
Q3704
Q3702
Q3703
PA LOW
PA FULL
DS3700
POWER SET CONTROL LOGIC
D/A
CONVERTER
U3000
MCU OUTPUTS ADDRESS 1401 (HEX), A0 = "1". MCU PULLS CS LATCH EN LOW, PLACES DATA ON THE DATA BUS, THEN RELEASES CS LATCH EN HIGH, STROBING DATA INTO U3710 (STROBE INPUT TO U3702 IS HELD HIGH BY A0). U3710 DRIVES OUTPUT CIRCUITS ACCORDING TO THE LATCHED DATA.
MAS RESET
(FROM RESET LOGIC
U3704C-8, SHT 1)
LOCAL SPI
(TO PLL U3402,
SHT 2)
SCK (CLOCK)
MOSI (DATA)
PA KEY
(TO PWR CNTRL
R3000/R3002, SHT 1)
PA KEY
(FROM DATA LATCH
R3774/C3754, SHT 1)
+10.2V REG
+1.4V TO +4.5V
+0.4V TO +3.5V
+1.5 TO +4.6
+1.5 TO +5.0
U3002A
U3002B
VCONTL


POWER CONTROL
WHEN THE TRANSMITTER (TX) IS KEYED, PA KEY LINE AND U3001-PIN 33 GO LOW. THIS ENABLES THE POWER CONTROL FUNCTION OF U3001.
DURING INITIAL KEYING, THE POWER CONTROL FUNCTION IS NOT IN THE CONTROL RANGE. THEREFORE, U3001-PIN 42 IS LOW CAUSING Q3001 TO BE OFF. WHEN PA KEY LINE TRANSITIONED LOW, A LOW GOING PULSE OCCURRED AT U3001-PIN 36. THIS TRIGGERED A ONE-SHOT PUTTING THE CONTROL FUNCTION INTO THE WIDE BANDWIDTH MODE. THE VOLTAGE AT U3001-PIN 42 INCREASES RAPIDLY. WHEN THIS VOLTAGE EXCEEDS THE THRESHOLD LEVEL AT U3002D-PIN 13 (DETERMINED BY MCU POWER CONTROL DATA MESSAGE), THE CONTROL FUNCTION IS OPERATING IN THE CONTROL RANGE AND Q3001 TURNS ON CAUSING U3001-PIN 36 TO GO HIGH SWITCHING THE CONTROL FUNCTION OUT OF THE WIDE BANDWIDTH MODE. AT THE SAME TIME, STATION TX OUTPUT POWER IS INCREASING AS IS TX VFWD SIGNAL.
TX VFWD IS APPLIED TO U3002B-PIN 5. THIS SIGNAL IS SUMMED WITH THE SIGNALS FROM U3001-PINS 12 & 7 (PIN 7 VOLTAGE LEVEL IS DETERMINED BY MCU POWER CONTROL DATA MESSAGE BECAUSE PIN 7 IS A BUFFERED VERSION OF THE SIGNAL AT U3001-PIN 6) AND APPLIED TO U3001-PIN 2. WHEN THE SIGNAL AT U3001-PIN 2 REACHES THE LEVEL OF THE SIGNAL AT U3001-PIN 44 (DETERMINED BY MCU POWER CONTROL DATA MESSAGE), VCNTL SIGNAL AT U3001-PIN 42 IS AT THE LEVEL NECESSARY TO PROVIDE THE TX OUTPUT POWER LEVEL DICTATED BY THE MCU.
DURING TRANSMITTER OPERATION, THE MCU MONITORS SIGNALS FROM VARIOUS TRANSMITTER CIRCUITS. IN ADDITION, THE MCU GETS TX POWER CONTROL COMMANDS FROM THE SCM. BASED ON THESE INPUTS THE MCU CONTROLS THE TRANSMITTER POWER VIA U3000-PINS 13 & 9.
THE FOLLOWING IS A LIST OF I/O RELATIONSHIPS FOR POWER CONTROL SIGNALS:
-- VCNTL & TX POWER OUTPUT VARY DIRECTLY WITH VREF U3001-PIN 44
-- VCNTL & TX POWER OUTPUT VARY INVERSELY WITH PSET U3001-PIN 6
P/O P102
48 MUX SELECT A
C3620 100
TO +5V/IPA MODULE
P/O P101
49 MUX SELECT B
C3624 100
P/O P102
38 FANS ON
NOT USED
C3625 22NF
N.C. R3751 470
C3727 27
C3617 22NF
36 ADAPTIVE TUNE 1
P/O P101
N.C. R3753 470
C3729 27
C3621 22NF
37 ADAPTIVE TUNE 2
31 ANT RLY ENABLE
TO ANTENNA RELAY CONNECTOR ON BACKPLANE
C3626 22NF
C3605 15
R3603 680
R3605 47
C3600 15
C3602 15
R3604 680
C3623 27
C3619 27
P/O P102
54 SCK HOST
52 MISO HOST
P/O P101
53 MOSI HOST
59 SPI GRANT
67 TX TO HOST REQ
TO & FROM STATION CONTROL MODULE
21, 33, 35, 57, 61, 63 N.C. NOT USED
+5V
R3758 330
TX LOCK
R3769 330
C3745 27
Q3705
DS3701
DS3702
C3752 27
PA FAIL
R3775 390
Q3709
DS3703
R3746 10K
TX SYN CS (TO PLL U3402-5, SHT 2)
POWER CONTROL/REG
C3720 100
Q3701
+10.2V SERIES PASS
NOTE 2
L3002 BEAD
C3016 100UF
+10.2V REG
U3001
VCC
5V COMP
REG GND
PA KEY
WB_SHOT_
CURRENT+
CURRENT-
INTGRT CAP
PSET_I
VREF
TEMP D
PSET Q
CAI 1
5V REF
CURR LMT
5V FDBK
9.6V FILT
9.6V DRV
REG COMP
KEYED 9.6V
9.6V SEN
V CNTL
PWR CNTL
CAI 2
CAI 3
FWD I
FWD Q
REFL+
REFL-
GND
SYN LOCK
+5V_PC
5,13,15,16,19,25,26,27,28,29,30,34 N.C.
C3011 1UF
R3022
CR3002
Q3004
CR3003
C3014 1UF
R3025 22K
+13.3V
+0.88V
R3019 10K
C3008 27
Q3003
R3023 100
R3018 1K
Q3002
R3012 19K
Q3001
C3009 0.47UF
C3012 27
R3027
R3024 127K
274K
R3021 4.7K
R3020 4.7K
C3010 0.1UF
I²C IC VCTRL DIV 2 (TO ANALOG MUX U3706-11, SHT 1)
0-5V
0V (PA OFF STATE)
1-4V (NOMINAL VOLTAGE AT RATED RF OUTPUT POWER)
C3604 22NF
P/O P102
4,20,22,34,56,58,60,62,64 N.C. NOT USED
P/O P101
15,17 V-CONTROL
P/O P102
16,18 V-CONTROL
TO +5V/IPA MODULE
VCNTL
FLEPS-48769-A (SHEET 1 OF 2)


SYNTHESIZER/VCO DC INPUT
DC POWER FILTERING
+10.2V REG
FILT +10.2V
+5V REGULATOR
+5V
LOW-FREQUENCY MODULATION COMPENSATION
SAMPLE OF VCO OUTPUT SIGNAL IS FED TO VCO FEEDBACK BUFFER Q3401 AND OUTPUT TO FEEDBACK INPUT AT U3402-PIN 8.
Q3401
FROM STATION CONTROL MODULE (VIA BACKPLANE)
2.1 MHZ INPUT FROM BACKPLANE IS BUFFERED BY Q3402 AND FED TO REF INPUT OF PLL SYNTHESIZER U3402-PIN 13.
2.1 MHZ
VCO AUDIO CONSISTS OF DIGITIZED AUDIO/DATA FOR MODULATING THE VCO RF SIGNAL.
LOCAL SPI (FROM MCU SHT 1)
MOSI
SCK
TX SYN CS (FROM DATA LATCH Q3701, SHT 1)
C
DURING DIAGNOSTIC ROUTINES, MCU U3700 VIA DATA LATCH U3702 ASSERTS MUX SELECT A & B LINES AND THEN MONITORS THE FOLLOWING MUX OUTPUT LINES:
- X1 MUX1 (P102-42)
- Y1 MUX1 (P101-43)
- X2 MUX2 (P102-44)
- Y2 MUX2 (P101-45)
- X3 MUX3 (P102-46)
- Y3 MUX3 (P101-47)
- X4 MUX4 (U3706 PIN 13)
- Y4 MUX4 (U3706 PIN 3)
MCU U3700 POLLS EACH MUX OUTPUT LINE DURING A 10-20mS LOOP CYCLE.
EACH MUX OUTPUT LINE CONTAINS FOUR 200uS CHANNELS 0 THRU 3. EACH CHANNEL CORRESPONDS TO A MUX INPUT SIGNAL X0 THRU X3 OR Y0 THRU Y3. EACH MUX INPUT SIGNAL RANGES BETWEEN 0 TO +5V (SEE FIG. 1).
CHANNELS
+5V
0
TIME
200uS
FIG. 1. TYPICAL DATA STREAM ON MUX OUTPUT LINE.
FOR THIS CIRCUIT BOARD APPLICATION, THERE ARE NO MUX1 SIGNAL INPUTS.
U3706 MUX4 SIGNAL INPUTS CAN BE DETERMINED FROM THIS SCHEMATIC DIAGRAM.
TO DETERMINE MUX2 & MUX3 SIGNAL INPUTS, SEE THE FOLLOWING TABLE.
OUTPUT LINE
SIGNAL INPUTS
X2MUX2 (P102-44)
X0 AC_FAIL
X1 OVERVOLTAGE
X2 VONNL_REF
X3 FPA_TEMP
Y2MUX2 (P101-45)
Y0 CIRCULATOR TEMP
Y1 N.C.
Y2 N.C.
Y3 N.C.
X3MUX3 (P102-46)
X0 N.C.
X1 N.C.
X2 IPA_IDA
X3 IPA_IDB
Y3MUX3 (P101-47)
Y0 DPA_VFWD (HIGH POWER ONLY)
Y1 N.C.
Y2 FPA_VREFL
Y3 FPA_VFWD
PIN #



U3402 PINOUT INFORMATION

#	SIGNAL NAME	DESCRIPTION/NOMINAL VOLTAGE
	FV	TEST POINT; DIVIDED DOWN VCO FREQUENCY, 6.25 KHZ OR 5 KHZ SAWTOOTH IN A LOCKED CONDITION.
	VCC	IC POWER; +5V
	DATA	SERIAL DATA INPUT; 0-5V LOGIC LEVEL
	CLK	CLOCK FOR SERIAL DATA PROGRAMMING; 0-5V LOGIC LEVEL
	$\overline{CS}$	CHIP SELECT; LOW WHEN PROGRAMMING, HIGH WHEN NOT PROGRAMMING (0-5V LOGIC LEVEL)
	AUX2	CHANGE FREQUENCY; TOGGLES BETWEEN LOGIC LOW AND HIGH WITH EVERY FREQUENCY CHANGE
	AUX1	BANDSHIFT; HIGH SELECTS LOW FREQUENCY VCO (Q3200/Q3201), LOW SELECTS HIGH FREQUENCY VCO (Q3230/Q3231)
	FIN	FEEDBACK RF INPUT; 132 MHZ TO 154 MHZ (TLD9831C) OR 150 MHZ TO 174 MHZ (TLD9832C) RIDING ON 1.4V DC
	VBBP	DC BIAS FOR PRESCALER INPUT; 1.4V DC
	NC1	NOT USED
	NC2	NOT USED
	VBB	DC BIAS FOR REFERENCE DIVIDER INPUT; 1.4V DC
	RIN	REFERENCE DIVIDER INPUT; 5V P-P, 2.1 MHZ SQUARE WAVE RIDING ON 1.4V DC
	GND	IC GROUND; 0V
	MRP	CONNECTION TO EXTERNAL RAMP CIRCUIT FOR PHASE MODULATOR; STEEPLY SLOPED RAMP, RAMPING BETWEEN 0 AND 5V @ 6.25 KHZ OR 5 KHZ RATE.
	MIN	MODULATION INPUT TO PHASE MODULATOR; +2.5V DC BIAS
	FR	TEST POINT; DIVIDED DOWN 2.1 MHZ REFERENCE @ 6.25 KHZ OR 5 KHZ IN A LOCKED CONDITION.
	$\overline{DP}$	WHEN LOCKED, NARROW (<1US) DOWN PULSES AT 6.25 KHZ OR 5 KHZ RIDING ON .7V DC
	LOCK	LOOP LOCKED; WHEN LOCKED, NARROW (<1US) DOWN PULSES AT 6.25 KHZ OR 5 KHZ RIDING ON 5V DC
	$\overline{DOWN}$	WHEN LOCKED, NARROW (<1US) DOWN PULSES AT 6.25 KHZ OR 5 KHZ RIDING ON .7V DC

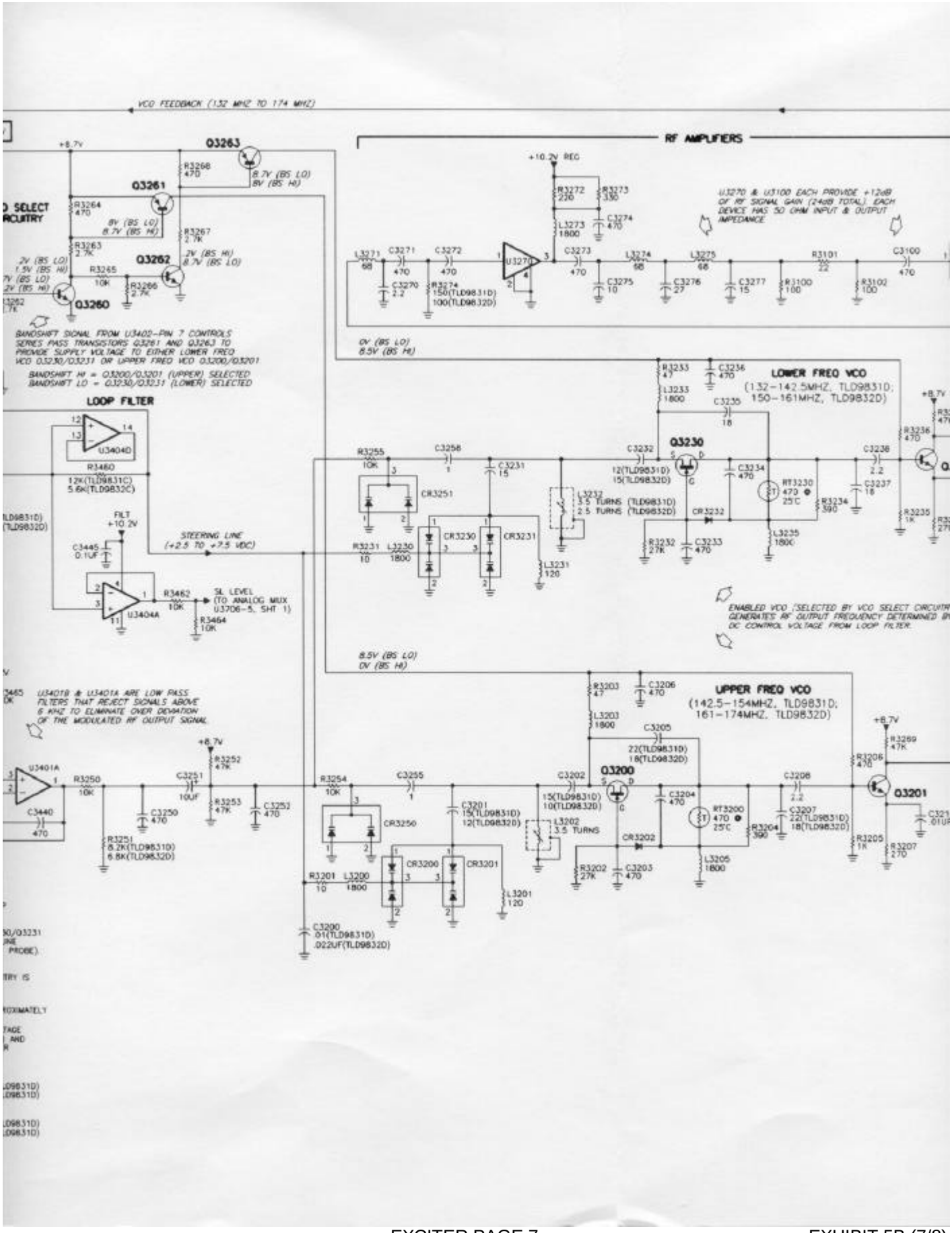
VCO TROUBLESHOOTING

1) Q3280 AND ASSOCIATED CIRCUITRY COMPRISE +8.7V SUPERFILTER. MEASURE VOLTAGE DROP ACROSS R3282 AND CALCULATE CURRENT (SHOULD BE APPROXIMATELY 60 MA).

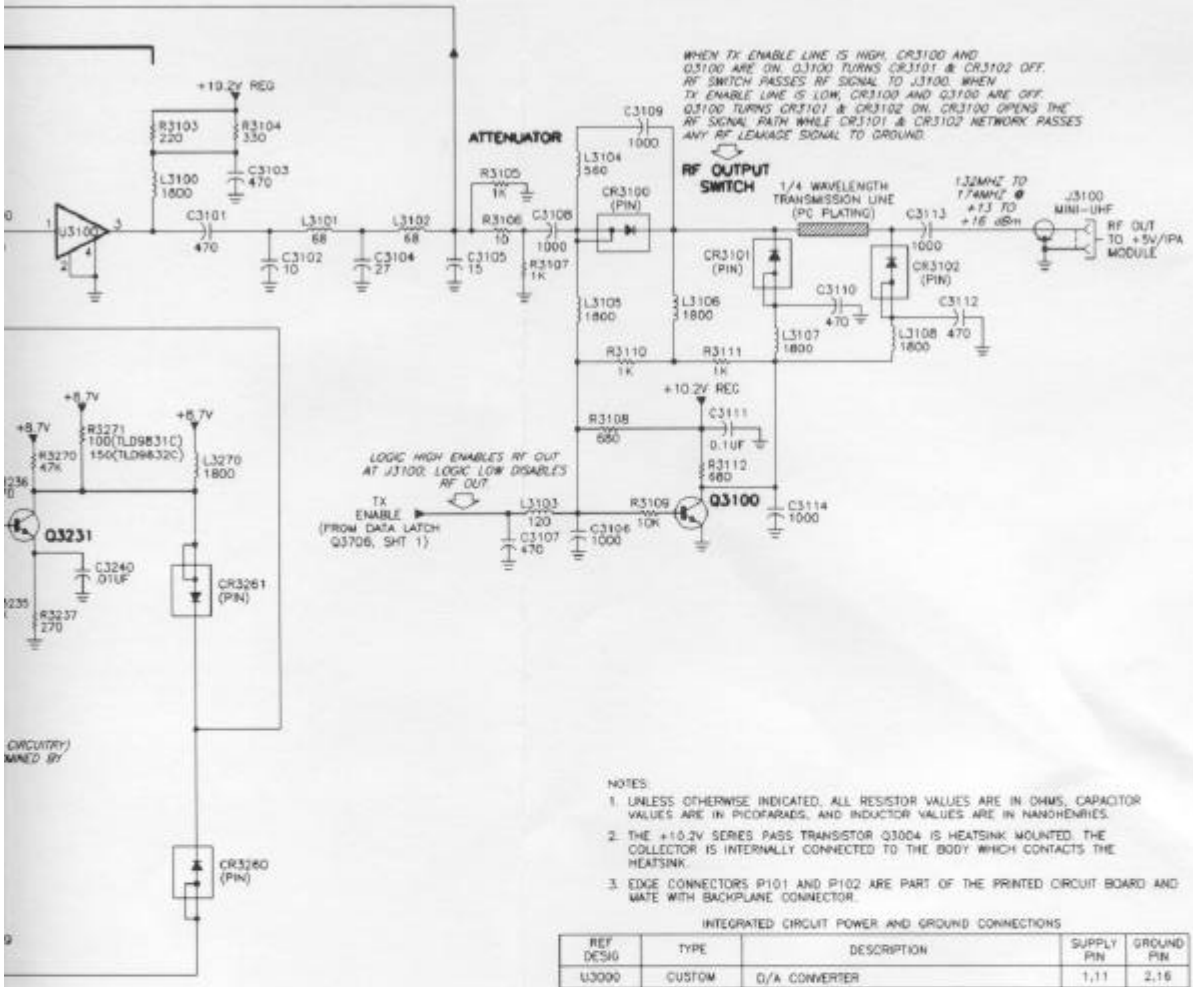
2) Q3260 THRU Q3263 COMPRISE BANDSHIFT CIRCUITRY WHICH SWITCHES DC POWER TO Q3230/Q3231 (LOWER PORTION OF BAND) OR TO Q3200/Q3201 (UPPER PORTION OF BAND). STEERING LINE SENSITIVITY IS APPROXIMATELY 3 MHZ/VOLT (STEERING LINE EXTREMELY SENSITIVE; DO NOT PROBE). POWER AT CR3260/CR3261 OUTPUT SHOULD BE APPROXIMATELY +10DBM INTO 50 OHMS.

3) IF BOARD IS NOT LOCKED, PERFORM FOLLOWING PROCEDURE TO DETERMINE IF VCO CIRCUITRY IS AT FAULT:
   A) VERIFY DC VOLTAGES AS SHOWN ON SCHEMATIC
   B) MEASURE POWER AND FREQUENCY AT OUTPUT OF CR3260/CR3261. SHOULD BE APPROXIMATELY +10 DBM INTO 50 OHMS; FREQUENCY SHOULD BE WITHIN LOWER OR UPPER RANGE.
   C) MEASURE STEERING LINE VOLTAGE AT U3404A-PIN 1. IF BOARD IS NOT LOCKED, VOLTAGE WILL BE EITHER .85V OR +9.15V. DETERMINE WHICH VCO IS ENABLED (U3402-PIN 7) AND VERIFY VCO OUTPUT FREQUENCY BASED ON MEASURED STEERING LINE VOLTAGE. REFER TO DATA BELOW.

Q3200/Q3201 ENABLED			
STEERING LINE VOLTAGE .85V	APPROX. 145 MHZ (TLD98320)	126 MHZ (TLD9831D)	
STEERING LINE VOLTAGE +9.15V	APPROX. 170 MHZ (TLD98320)	154 MHZ (TLD9831D)	
Q3230/Q3231 ENABLED			
STEERING LINE VOLTAGE .85V	APPROX. 154 MHZ (TLD98320)	135 MHZ (TLD9831D)	
STEERING LINE VOLTAGE +9.15V	APPROX. 185 MHZ (TLD98320)	158 MHZ (TLD9831D)	


VCO FEEDBACK (132 MHZ TO 174 MHZ)
RF AMPLIFIERS
+10.2V REG
Q3263
Q3261
Q3262
Q3260
Q3230
Q3200
Q3201
U3270 & U3100 EACH PROVIDE +12dB OF RF SIGNAL GAIN (24dB TOTAL). EACH DEVICE HAS 50 OHM INPUT & OUTPUT IMPEDANCE
BANDSHIFT SIGNAL FROM U3402-PIN 7 CONTROLS SERIES PASS TRANSISTORS Q3261 AND Q3263 TO PROVIDE SUPPLY VOLTAGE TO EITHER LOWER FREQ VCO Q3230/Q3231 OR UPPER FREQ VCO Q3200/Q3201
BANDSHIFT HI = Q3200/Q3201 (UPPER) SELECTED
BANDSHIFT LO = Q3230/Q3231 (LOWER) SELECTED
LOOP FILTER
LOWER FREQ VCO
(132-142.5MHZ, TLD9831D; 150-161MHZ, TLD9832D)
UPPER FREQ VCO
(142.5-154MHZ, TLD9831D; 161-174MHZ, TLD9832D)
STEERING LINE (+2.5 TO +7.5 VDC)
SL LEVEL (TO ANALOG MUX U3706-5, SHT 1)
ENABLED VCO (SELECTED BY VCO SELECT CIRCUITRY) GENERATES RF OUTPUT FREQUENCY DETERMINED BY DC CONTROL VOLTAGE FROM LOOP FILTER.
U3401B & U3401A ARE LOW PASS FILTERS THAT REJECT SIGNALS ABOVE 6 KHZ TO ELIMINATE OVER DEVIATION OF THE MODULATED RF OUTPUT SIGNAL
8.7V (BS LO) 8V (BS HI)
8V (BS LO) 8.7V (BS HI)
2V (BS LO) 8.7V (BS HI)
0V (BS LO) 8.5V (BS HI)
8.5V (BS LO) 0V (BS HI)

VHF EXCITER BOARD
MODELS TLD9831D
TLD9832D

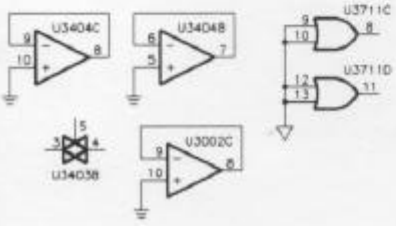


NOTES:
1. UNLESS OTHERWISE INDICATED, ALL RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS, AND INDUCTOR VALUES ARE IN NANOHENRIES.
2. THE +10.2V SERIES PASS TRANSISTOR Q3004 IS HEATSINK MOUNTED. THE COLLECTOR IS INTERNALLY CONNECTED TO THE BODY WHICH CONTACTS THE HEATSINK.
3. EDGE CONNECTORS P101 AND P102 ARE PART OF THE PRINTED CIRCUIT BOARD AND MATE WITH BACKPLANE CONNECTOR.

INTEGRATED CIRCUIT POWER AND GROUND CONNECTIONS

REF DESIG	TYPE	DESCRIPTION	SUPPLY PIN	GROUND PIN
U3000	CUSTOM	D/A CONVERTER	1,11	2,16
U3001	CUSTOM	REGULATOR/POWER CONTROL	32	1,31
U3002	MC3303DR2	QUAD DIFFERENTIAL-INPUT OPERATIONAL AMPLIFIER	4	11
U3100 & U3270	MSA0386	MICROWAVE AMPLIFIER, 50-OHM INPUT & OUTPUT IMPEDANCE (MMIC)	3	2,4
U3401	MC33074D	QUAD DIFFERENTIAL-INPUT OPERATIONAL AMPLIFIER	4	11
U3402	CUSTOM	PHASE LOCKED LOOP SYNTHESIZER	2	14
U3403	MC74HC4066	QUAD ANALOG MULTIPLEXER/DEMULTIPLEXER	14	7
U3404	MC33184	LOW POWER QUAD OPERATIONAL AMPLIFIER	4	11
U3405	MC7805	+5V VOLTAGE REGULATOR	1	2
U3700	M68HC11F1	MICROCONTROLLER (MCU) W/SCI, SPI (NON-MULTIPLEXED ADDRESS/DATA BUS)	34	1
U3701	27C512	64K X 8-BIT EPROM, PROGRAMMED	28	14
U3702	MC74AC273	OCTAL D-TYPE FLIP-FLOP	20	10
U3703	MC74AC244	OCTAL BUFFER/LINE DRIVER, WITH 3-STATE OUTPUTS	20	10
U3704	MC74AC00	QUAD 2-INPUT NAND GATE	14	7
U3706	74HC4052	ANALOG MULTIPLEXER/DEMULTIPLEXER	16	7,8
U3707	MC33064	UNDERVOLTAGE SENSING CIRCUIT	2	4
U3708	MC74AC04	HEX INVERTER	14	7
U3709	MC3303DR2	QUAD DIFFERENTIAL-INPUT OPERATIONAL AMPLIFIER	4	11
U3710	MC74AC273	OCTAL D-TYPE FLIP-FLOP	20	10
U3711	MC74AC32	QUAD 2-INPUT OR GATE	14	7
U3712	MC74HC165	8-BIT SERIAL OR PARALLEL INPUT SHIFT REGISTER	16	8

UNUSED GATES



FLEPS-48769-A (SHEET 2 OF 2)

68P81090E84-A
(Sheet 5 of 5)
4/30/96-UP