CIRCUIT DESCRIPTIONS

EXHIBIT 5A – MEANS FOR FREQUENCY STABILIZATION

Frequency stability is maintained by a reference oscillator/programmable temperature compensation circuit located in the frequency synthesizer IC U3201. The oscillator is a Colpitts design with an amplifier in the IC. The 16.8 MHz crystal Y3261, varactor D3261, and feedback capacitors are external circuitry. A control voltage applied to the varactor via the programmable compensation circuit within U3201maintains the frequency stability to within +/-2.5 ppm over the specified operating temperature range. Frequency tuning, also from the programmable compensation circuit, has 128 steps of resolution.

Each 16.8 MHz crystal is numerically coded providing its unique characteristic over the operating temperature range. With the crystal temperature characteristic known, a computed compensation characteristic is programmed into the compensation algorithm.

EXHIBIT 5B – MEANS FOR LIMITING MODULATION

Modulation limiting is accomplished within the custom IC, U0221. The limiting action itself occurs at the rails (i.e., 5V and ground). Using an opamp with feedback, very hard limiting is obtained. The limited modulation signal is then applied to a low-pass splatter filter, and then to an electronic attenuator within U0221 in order to adjust for variations in modulation sensitivities of the frequency synthesizer.

The electronic attenuator is controlled by the radio's microprocessor, U0101. To keep the deviation constant over the RF frequency range & channel bandwidth, the microcomputer adds the proper correction factor to the attenuator.

EXHIBIT 5C – MEANS FOR ATTENUATION OF HIGHER AUDIO FREQUENCIES

The output of the limiter is applied to a low-pass splatter filter. This filter is a fifth-order switched capacitor filter with the roll-off corner located at 3000 Hz. The output of the low-pass filter is applied to the electronic attenuator before being routed to the modulator.

EXHIBIT 5D – MEANS FOR ATTENUATION OF SPURIOUS EMISSIONS

The final stage of the RF power amplifier circuit feeds a low-pass filter in order to attenuate harmonics of the carrier frequency as well as any spurious signals. The filter is a seven-pole Chebychev design using LC lumped elements.

The cast metal chassis forms a compartmentalized shielded enclosure upon which the main circuit board is mounted. A second cast metal compartmentalized shielded enclosure is placed over the main circuit board and secured to the chassis with screws. A conductive elastomeric coating is bonded to the edges of the metal chassis and shield enclosure walls, which come in contact with gold-plated areas of the circuit board when the circuit board and shield are assembled to the chassis. This technique provides very effective and reliable shielding of the various circuits on the main board from each other and from the external environment, minimizing spurious RF radiated emissions.

EXHIBIT 5E – MEANS FOR LIMITING OUTPUT POWER

Output power is regulated through the use of a forward power detection ALC loop. A directional coupler samples a portion of the forward RF power. The sampled RF is rectified by diode D3451, and the resulting dc voltage is routed to the Power Control IC U3501. This signal is then compared to the preprogrammed reference and the error signal is amplified and used to generate a control voltage to control the bias of the first transmitter stage, U3401.

EXHIBIT 5F – MODULATION TECHNIQUES

The transmitter is capable of the following types of modulation:

i) Modulation of PL (Private Line) - Direct FM tone modulation of 67 Hz to 250.3 Hz at 15% of full system deviation.
ii) Modulation of DPL (Digital Private Line) - Direct FM modulation at 134 BPS at 15% of full system deviation.
iii) Modulation of DTMF tones at nominally 60% of full system deviation.

The Carson's Rule calculations for necessary bandwidth, Bn = 2M + 2DK, where M = maximum modulating frequency in Hz, D = peak deviation in Hz, and K = 1, are as follows:

For 25 kHz Channel Spacing, Bn = 2(3000) + 2(5000)(1) = 16000 Hz (16K0 designator).
For 12.5 kHz Channel Spacing, Bn = 2(3000) + 2(2500)(1) = 11000 Hz (11K0 designator).

Direct FM of PL or DPL is generated by a 6-bit D/A converter contained within U0221. The frequency-determining clock signal is generated by the radio microcomputer. The modulation signal is processed through a five pole switched capacitor filter. The output of the filter is input to the electronic attenuator circuit.

The microcomputer adjusts the attenuator to compensate for modulation sensitivity variations of the synthesizer & channel bandwidth ensuring 15% of full system deviation for PL and DPL. DTMF tones are generated by the audio processing IC, U0221. The tones are routed and processed in the same manner as the voice signals.

EXHIBIT 5G – MEANS FOR CONTROLLING TRANSIENT FREQUENCY BEHAVIOR

The effects of VCO frequency shifts due to transmitter key-up and de-key impedance variations are minimized through the use of a multiple-stage transmitter lineup with resistive isolation pads between various stages, including a pad between the output of the VCO/buffer IC and the input of the transmitter circuit.

Additionally, the value of the DAC which controls output power is gradually raised during transmitter key-up and lowered during de-key, shaping the transmitter attack and decay characteristics by gradually changing the power control voltage.

Finally, a pre-bias voltage is applied to the RF detector diode in the directional coupler so that the power control circuit does not react to a zero-power condition at transmitter key-up by attempting to increase the power output instantaneously to a high level.