FUNCTION OF RF SEMICONDUCTORS AND OTHER ACTIVE DEVICES

Reference Designator	Motorola Part no.	Description	Circuit Application	Operating Frequency	Radio Circuit
CR201	'4802233J09	IMN10	Synthesizer Circuit	16.8Mhz	FRACN
CR202	'4802233J09	IMN10	Synthesizer Circuit	16.8Mhz	FRACN
U201	'5185963A27	63A27	FGU	16.8Mhz	FRACN
Y200	'4802245J68	CRYSTAL	Reference frequency	16.8Mhz	FRACN
U202	'5105739X05	ADP3300	5V voltage regulator	DC	FRACN
U203	'5102463J58	LP2980	3V voltage regulator	DC	FRACN
Q201	'4802245J50	TRANSISTOR	DC switch	DC	FRACN
Q202	'4802245J50	TRANSISTOR	DC switch	DC	FRACN
CR251	4862824C01	1SV229	VARACTOR	896-941MHz	VCO
CR252	4862824C01	1SV229	VARACTOR	896-941MHz	VCO
CR253	4862824C01	1SV229	VARACTOR	896-941MHz	VCO
Q251	4805218N63	BFQ67W	RF Transistor	896-941MHz	VCO
Q252	4802245J50	UMC5N	DC Switch	DC	VCO
U250	5105750U54	50U54	Buffer IC	896-941Mhz	VCO
U101	'5185130C65	ANALOG IC	PA DRIVER IC	896-941MHZ	PA
U102	5185765B01	H99S-4	Power Control	DC	PA
U103	5185963A15	LM50	Temperature sensing	DC	PA
CR101	4880973Z02	MA4PH261	Diode Switch	896-941MHZ	PA
CR102	4880973Z02	MA4PH261	Diode Switch	896-941MHZ	PA
Q101	4813828A09	MRF1517T1	PA device	896-941MHZ	PA
CR440	4813833C02	MMBD6100	Current Protection	DC	CONTRL
Q400	'4809579E18	TP0101T	DC Switch	DC	CONTRL
Q403	4880214G02	MMBT3904	DC Switch	DC	CONTRL
Q405	4802245J54	UMG5	DC Switch	DC	CONTRL
Q410	4802245J54	UMG5	DC Switch	DC	CONTRL
Q416	'4809579E18	TP0101T	DC Switch	DC	CONTRL
VR432	4805656W08	MMQA5V6T1	ESD Protection Diode	AUDIO	CONTRL
VR433	4805656W08	MMQA5V6T1	ESD Protection Diode	AUDIO	CONTRL
U410	5102463J57	ILC7062CM-33	Voltage Regulator	DC	CONTRL
U420	5102463J44	TDA8547	Audio Amplifier	AUDIO	CONTRL
U400	'5102463J40	LP2951ACMM-3.3	3.3V regulator	DC	CONTRL
U409	'5102226J56	MC68HC11FL0PU1	MICROPROCESSOR	1.83MHz	CONTRL
U405	'5102463J36	MEMORY	RAM	DC	CONTRL
U406	'5102463J60	AT49LV040-90T1	Flash ROM	DC	CONTRL
VR434	'4802245J73	UDZSTE17	Audio power	DC	CONTRL
VR445	'4802245J74	UDZSTE17	Audio power	DC	CONTRL
VR446	'4802245J74	UDZSTE17	Audio power	DC	CONTRL
VR447	'4802245J74	UDZSTE17	Audio power	DC	CONTRL
VR448	'4802245J74	UDZSTE17	Audio power	DC	CONTRL
VR449	'4802245J74	UDZSTE17	Audio power	DC	CONTRL

TUNING PROCEDURE

Table for tuning frequencies.

Test/Tune Freq.	900 MHz
F1	895.975
F2	899.525
F3	902.025
F4	918.525
F5	934.975
F6	938.525
F7	941.025

TABLE 1

1.0 Reference oscillator warping (Final warp)

a) Use SBEP command to adjust warp DAC setting to get frequency F7 of table 1.
b) Use SBEP command to save warp DAC setting in code plug

DAC sensitivity measurement

a) Program radio to RX/TX mode, freq. = MHz, DAC setting=127
b) Measure if radio lock, Vctrl
c) Measure frequency and DAC voltage
d) Program DAC=97 measure freq. and DAC voltage
e) Program DAC=157 measure freq. and DAC voltage

2.0 TRANSMITTER POWER ADJUSTMENT

2.1 General description of PA bias adjustment.

Tuning of the PA Bias is required to compensate for FET device tolerances due to lot to lot variation during the FET die fabrication process. To obtain optimum power and efficiency, the bias should be tuned in the factory after it is built or after a repair.

a) Program the FRACN to switch off the RF signal by setting VCO IC to battery saver mode. If this is not possible for hardware reasons, set the VCO to RX mode. Setting the bias-tuning environment should perform this step.
b) If the VCO IC can't be set to battery saver mode, set the receive frequency to F1. This should be done automatically by the radio when entering the bias tuning environment. Previous radios required frequency setting by the tuning system.
c) Initialize the PCIC for bias tuning by setting the following parameter TX mode switch on the PIN diodes (RX to low, ANO on)
   set power D2A (D2A#1) to maximum
   set voltage limit D2A (D2A#2) to minimum
   set PA bias D2A (D2A#3) to minimum
This allows controlling the power control voltage by the voltage limit D2A. The PIN diodes should be on to avoid instabilities. For the same reason the antenna output must be terminated with 50-ohm termination. In case of PA Oscillation a RF induced additional current would lead to tuning inaccuracies.
d) Measure the dc current the radio draws from the voltage supply. Note the measured value as VL0 B0 CURRENT.
e) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the "VL0 B0 CURRENT" as specified in Table 2 "VL CURRENT". Note the measured value as "VL B0 CURRENT". The additional current is drawn by the driver.

f) Increase the PA bias D2A (D2A#3) until the dc current exceeds the "VL B0 CURRENT" as specified in table 2 " B CURRENT ". The FET draws the additional current. After this step, a balance between the FET current (Gain) and the driver current (gain) have been achieved. The balance is maintained when the RF output power is altered.

g) Store the PA bias D2A value in the PA bias softpot.

2.2 **Transmitter PA bias adjustment procedure for 900MHz High Power**

2.2.1

a) Set radio environment for PA bias-tuning. This relates to step (a) - (c) of section 2.1
b) Measure the radio dc current and note the value as "VL0 B0 CURRENT". This relates to step (d) of section of 2.1
c) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the "VL0 B0 CURRENT" by the value of "VL CURRENT" as specified in table 2 for 900 (primary). ("VL0 B0 CURRENT" + "VL CURRENT" = "VL B0 CURRENT")
Note the measured current as "VL B0 CURRENT" This relates to steps (e) of section 2.1
IF FAIL THEN USE the procedure outlined in section 2.2.2
Increase the PA bias D2A (D2A#3) until the dc current exceeds the "VL B0 CURRENT" by the value of "B CURRENT" as specified in table 2 for 900 (primary). This relates to step (f) of section 2.1

IF FAIL THEN USE the procedure outlined in section 2.2.2
e) Store the PA bias D2A value in the PA bias softpot for the tuned power level.

2.2.2
a) Set radio environment for PA bias- tuning. This relates to step (a) - (c) of section 2.1
b) Measure the radio dc current and note the value as "VL0 B0 CURRENT". This relates to step (d) of section of 2.1
c) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the "VL0 B0 CURRENT" by the value of "VL CURRENT" as specified in table 2 for 900 (secondary). ("VL0 B0 CURRENT" + "VL CURRENT" = "VL B0 CURRENT")
Note the measured current as "VL B0 CURRENT" This relates to steps (e) of section 2.1
IF FAIL THEN USE the procedure outlined in section 2.3.3

Increase the PA bias D2A (D2A#3) until the dc current exceeds the "VL B0 CURRENT" by the value of "B CURRENT" as specified in table 2 for 900 (secondary). This relates to step (f) of section 2.1

IF FAIL THEN USE the procedure outlined in section 2.3.3

Store the PA bias D2A value in the PA bias softpot for the tuned power level.

2.2.3

For each step, if the SPV Limit falls into 63/64 trapping, dump default DAC of 48 (decimal) into SP PA Bias. No default is to be dumped into SP V limit. Proceed to section 2.3

Band	VL Current	B Current
900 (primary)	7mA –12mA	40mA-70mA
900 (secondary)	40mA-80mA	180mA-220mA

Table 2

2.3 **Transmitter Power Adjustment**

(Important: Section 2.2 must be completed before power adjustment can be carried out)
The Waris radio power-level tuning is across the band at 7 discrete test frequencies, each at 2 discrete power levels. In addition, there is 2 nominal power setting.

(Important: Section 8.2.1.2 must be completed before power adjustment can be carried out). The Waris radio power level tuning is across the band at 7 discrete test frequencies, each at 2 discrete

power levels. In addition, there is 2 nominal power setting.
a) Set the radio to first tuning frequency
b) Key up the radio and measure power
c) Adjust the high power level and store the data.
d) Repeat for each tuning frequency F1-F7.
c) Repeat a) through d) for low power level.
900Mhz Power-Tuning Specification: 896-902Mhz and 935-941Mhz.
Hi power: 2.65-2.85W
Low Power: 1.1-1.3W

3.0 BALANCING/LIMITING LOW AND HIGH PORT Modulation of the Synthesizer

3.1 Modulation Balancing (MOD ATTN)

a) Program the radio for low power using the settings obtained in procedure 2.3 above.
b) Program the ASFICCMP to mute the microphone .Set ASFICcmp for FLAT_TX_RTN mode (Flat audio Response), and default attenuation settings (Note 1).
c) Program the synthesizer to the lowest transmit tune frequency as in table 1 and set the ADC bits 12-11 = “10”. These bits set the fractional-N low port sensitivity to a max. of 5.0 kHz. Set the Mod Attenuator enable bit to"1" to enable the high port modulation.
d) Apply an 80 Hz tone, 100mV rms. at the external test box "Audio In " input.
e) Measure deviation (D1)
f) Change the input tone to 3kHz, 100mVrms and measure deviation (D2)
g) Find the ratio in dB using 20log[D1/D2]
h) Remove the audio signal by disabling the external TX audio path
i) Program the Mod attenuation setting of the fractional-N using the equation below:
Modulation attenuator setting = (current setting at step i) + -(5 x (dB value of step i))
j) Re-enable the External TX audio path.
k) Repeat steps (f) - (i) until the ratio in dB of step (i) is <±0.20dB, store modulation attenuator setting to EEPROM.

NOTE: The attenuation settings of the ASFICcmp are defaulted for minimum attenuation (MOD6 - MOD0 = $FF) Before start of balancing. The fractional-N modulation attenuator should be set to 6.4dB, i.e. $20 (32 decimal).

3.2 Modulation Limiting

a) Disable the FLAT_TX_RTN mode. Select the Ext. Mic and unmute it.
b) Inject at the Ext. Mix Input a 1khz tone, 80mVrms with the preemphasis enabled
And adjust the Mod attenuator of the ASFICcmp to obtain the deviation in Table 3
c)Dekey the radio
d) Store the attenuator setting in the codeplug.
e) Repeat the step (a) to (d) for other frequencies as per the tuning matrix.

Reference Voice Deviation

Channel Spacing	Deviation (kHz)
25	4.30 - 4.60
20	3.40 - 3.60
12.5	2.20 - 2.30

Table 3

NOTE Program the synthesizer ADC bit 12.11 to 11(reduce deviation sensitivity of the synthesizer). Verify the deviation reduces to the range of 2.2 to 2.32kHz.if tuning is required, adjust only the mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency.