Exhibit 4. Circuit Description ----- 47 CFR 2.1033(c)(10)

This section provides the description of circuits required by 47 CFR 2.1033(c)(10).

The following are included:

4.1) Carrier Frequency Generation and Stabilization

4.2) Digital Modulation Technique

4.3) Modulation Limiting and Post Limiter Filter

4.4) Means for Output Power Limiting

4.5) Spurious and Harmonic Emissions Suppression

4.1. Carrier Frequency Generation and Stabilization

The synthesizer reference oscillator employs a crystal controlled Colpitts oscillator running at a frequency of 16.8Mhz. The oscillator transistor, start-up circuit, and temperature compensation circuit are located in the U301 while the oscillator feedback capacitors, crystal, and tuning varactor are external. This oscillator is temperature compensated to an accuracy of +/-2.5PPM from -25 to 60 degrees C.

The method of temperature compensation is to apply an inverse Bechmann voltage curve which matches the crystal's Bechmann curve to a varactor which constantly shifts the oscillator back on frequency. The crystal vendor characterizes the crystal over a specified temperature range and codes this information into an eight-digit code which is printed on the crystal package in a bar code.

In production this crystal code is read via a 3-dimensional bar code reader into a custom temperature compensation tuning algorithm. This tuning algorithm decodes the crystal information and takes voltage and temperature measurements on the oscillator then programs U301's temperature compensation registers to provide the specified frequency error vs. temperature performance.

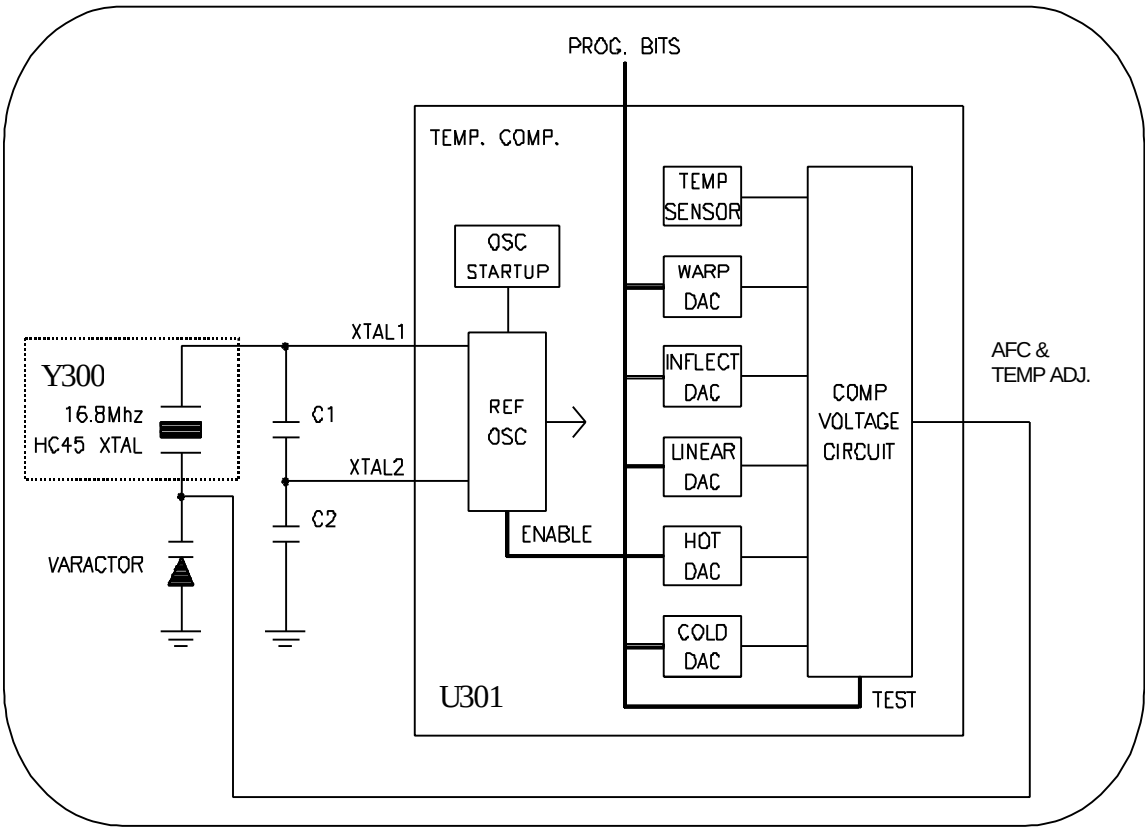

Figure 4-1: 16.8 MHz Reference Oscillator

The reference oscillator runs at 16.8 MHz. The signal from this reference oscillator is routed to the synthesizer IC (U301) and is used to control the stability of the main Voltage Controlled Oscillator (VCO) which oscillates at a frequency between *956.9-971.9* MHz (see figure 4-2). The synthesizer also buffers the 16.8 MHz signal and provides it as a clock signal to U401 (A/D and D/A IC), U501 (TX Quadrature Modulation and Linearization IC), U601 (Quadrature Receiver IC), U001 (DC Power and Audio IC) and U801 (Controller and DSP IC). The PLL inside the U601 uses the 16.8 MHz clock as the reference for the TX Offset VCO and RX 2nd LO VCO. The frequency of the TX Offset VCO is *301.8* MHz which is divided by two in U501 and mixed with the main VCO to generate the transmit frequency. The frequency of the RX 2nd LO VCO is 219.3 MHz which is divided by two in U601 and mixed with the received Intermediate Frequency (IF) signal to generate the baseband data for the DSP. The frequency control for each VCO is accomplished by a PLL inside U601 which compares the VCO frequency (after a frequency divider) to the reference frequency thus phase-locking each VCO to the reference oscillator.

The transmitter frequency is programmed to a single frequency between 806-821 MHz composed by subtracting half of the TX offset VCO frequency (*301.8* MHz) from the main VCO frequency *956.9-971.9* MHz. The subtraction is done by a mixer in U501, followed by a band pass filter (FL501) which selects the transmitter frequency of 806 - 821 MHz from the other mixing products and rejects spurious signals.

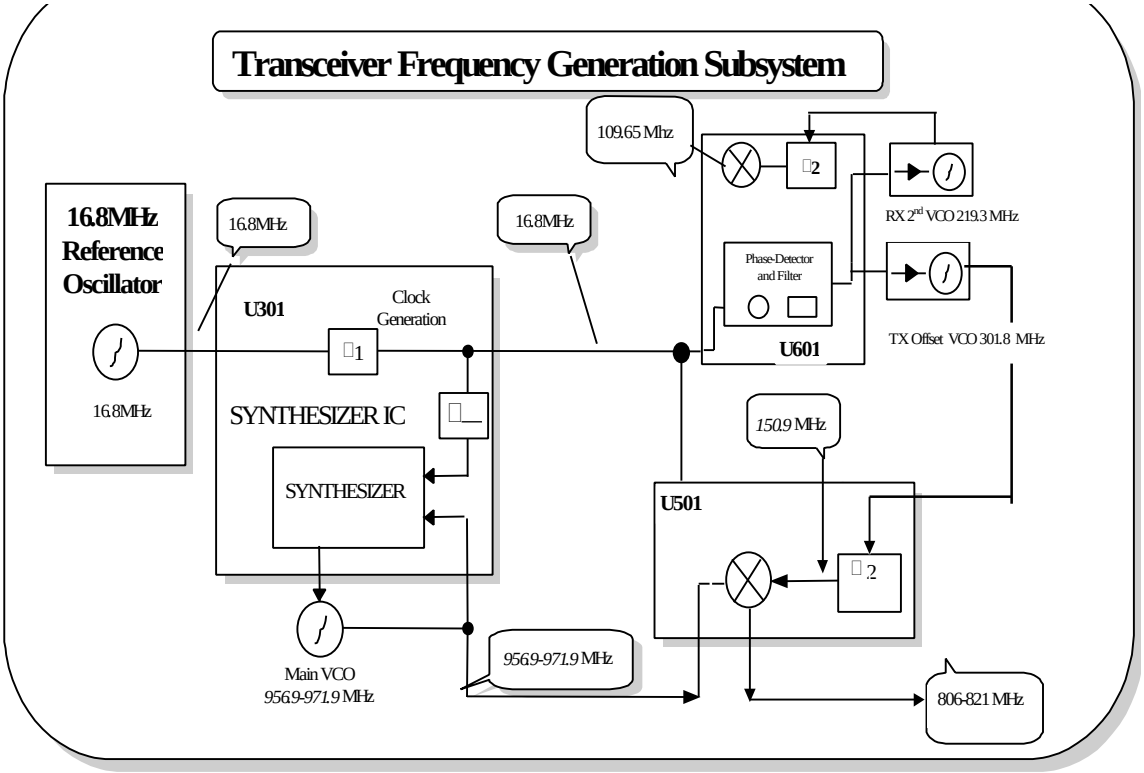

Figure 4-2 : Transceiver Frequency Generation Subsystem

4.2. Digital Modulation Techniques

The subject radio makes use of 3 different modulation techniques termed Quad-16QAM, Quad-64QAM, and Quad-QPSK. In voice mode, the radio will function in Quad-16QAM mode only. In data mode, the radio will use any one of the three different modulation techniques (Quad-16QAM, Quad-64QAM, and Quad-QPSK) in a given slot. The following describes each of the modulation techniques:

The modulation technique termed Quad-QPSK is a linear digital modulation of a multi-channel variant of Quadrature Phase Shift Keying (QPSK). Data bits to be transmitted are split into four parallel lower rate streams, each of which is QPSK modulated to its own sub carrier frequency. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite M-QPSK signal. This spectrally efficient linear modulation can achieve transmission at 32K Bits per Second in a 25 kHz channel. The transmitter is configured using TDMA time slotting so that up to 6 radio users can simultaneously share the 25 kHz channel.

The modulation technique termed Quad-16QAM is a linear digital modulation of a multi-channel variant of a 16-state Quadrature Amplitude Modulation. Data bits to be transmitted are split into four parallel lower rate streams, each of which is 16QAM modulated to its own sub carrier frequency. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite M-16QAM signal. This spectrally efficient linear modulation can achieve transmission at 64K Bits per Second in a 25 kHz channel. The transmitter is configured using TDMA time slotting so that up to 6 radio users can simultaneously share the 25 kHz channel.

The modulation technique termed Quad-64QAM is a linear digital modulation of a multi-channel variant of a 64-state Quadrature Amplitude Modulation. Data bits to be transmitted are split into four parallel lower rate streams, each of which is 64QAM modulated to its own sub carrier frequency. The four resulting sub channel signals are then combined in frequency division multiplex fashion to produce the composite M-64QAM signal. This spectrally efficient linear modulation can achieve transmission at 96K Bits per Second in a 25 kHz channel. The transmitter is configured using TDMA time slotting so that up to 6 radio users can simultaneously share the 25 kHz channel.

4.3. Modulation Limiting and Post Limiter Filter

The transmitted data or audio is processed using three software algorithms in a Digital signal Processor (DSP), which automatically prevents modulation in excess of 100 percent. The software algorithms consist of a speech encoder, a Quadruple-QPSK digital modulator, Quadruple-16QAM digital modulator, Quadruple-64QAM digital modulator, and a baseband filter as shown in Figure 4-3 below.

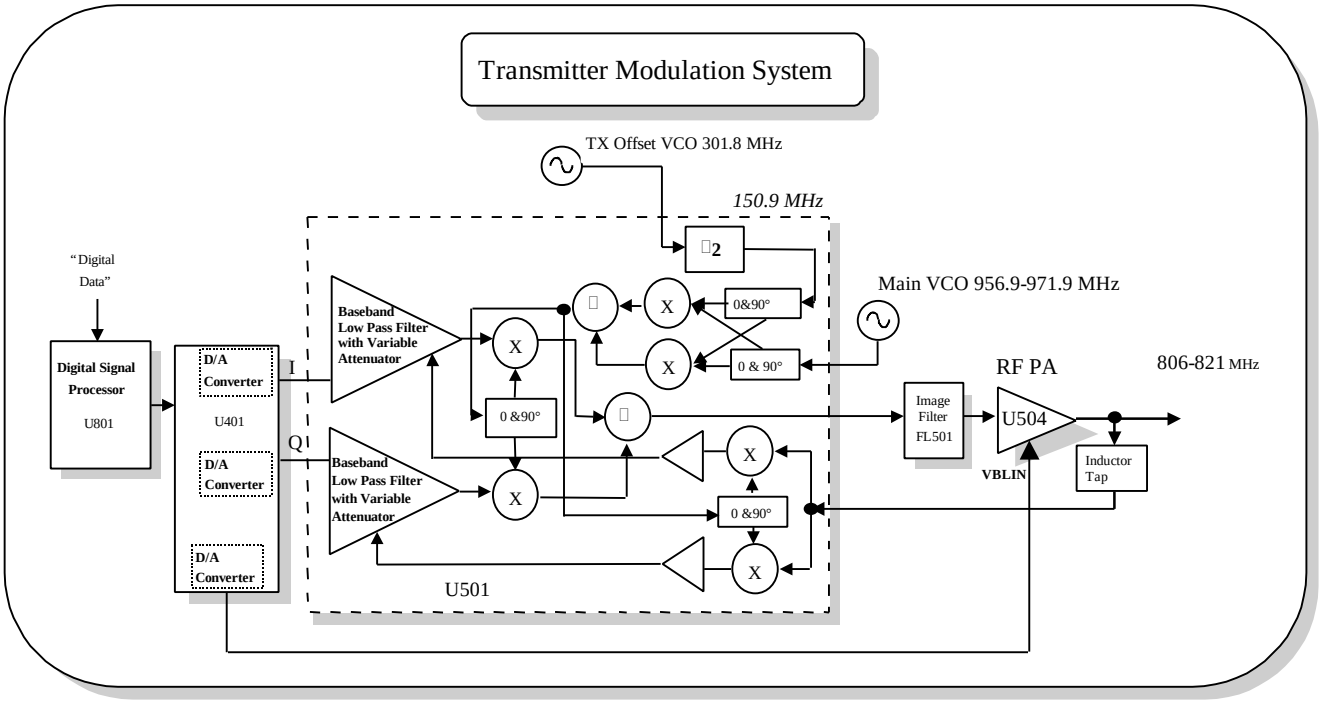

Figure 4-3: Transmitter Modulation System

4.4. Means for Output Power Limiting

The transmitter power calibration is done in two parts. The first part sets the gain of the PA and the second part sets the baseband attenuator that controls the level of baseband input into U501.

In PA gain setting, the gain of the PA is factory adjusted to a predetermined value based on the transmitter gain line-up requirements. This is accomplished by configuring the transmitter to transmit in open loop mode while the gain of the PA is adjusted by sending a digital word to U401. This digital word is converted to a corresponding control voltage (VBLIN) to bias the first stage of the PA (U504). Once the gain of the PA is set, the digital word that corresponds to the proper control voltage is then stored into the Flash Memory (U802).

After the gain of the PA is properly adjusted, the output power is then set by varying the level of baseband input into U501 which in effect changes the RF input to the PA (U504). This procedure begins by setting the baseband attenuation to zero and configure the transmitter to transmit in full power and automatic level train mode. During automatic level training, U501 will set the lowest allowable baseband attenuation that results in a maximum power out of the radio without clipping the PA. This power is typically higher than the targeted power setting. To lower the output power, the level of baseband attenuation is increased until it is within the target window. This is accomplished by reading the level train result from U501, using it as

the starting point and iteratively increasing it until the output power is within the target window. Then the digital word that corresponds to that particular attenuator setting is then stored into the Flash Memory (U802). If automatic level training resulted in a power lower than the target power, the baseband attenuator will not be decreased since doing so will clip the RF PA (U504) and increase potential adjacent channel power. This calibration is performed at five frequencies across the band and is maintained over various conditions as follows:

- An interpolation algorithm is used to calculate the settings in-between the calibration frequencies.
- Two temperature points: One for 3dB cutback (at 80°C) and the other total thermal shutdown (at 100°C). The temperature is monitored by the microprocessor via an on board thermistor located near the RF PA.

4.5. Spurious and Harmonic Emissions Suppression

Refer to Figure 4-4 below for the following description. One SAW filter, FL501, providing a minimum of 42 dB of rejection at the image frequency, is placed before the Power Amplifier (U504) to insure that a spectrally pure transmitter frequency is delivered to the Power Amplifier input. The power amplifier output is isolated from mismatched loads in the antenna connector by an isolator. The isolator ensures that the power amplifier will see a stable load for any load variations applied to the antenna connector. A trap filter, providing a approximately 20 dB of rejection at the fourth harmonic frequency, is placed after the isolator to insure that a spectrally pure transmitted signal is delivered to the antenna switch.

The bandpass SAW filter, the isolator and the trap filter attenuate spurious and harmonic signals that are generated in the transmitter section. Proper shielding within the transceiver also attenuates radiated spurious emissions and harmonics.

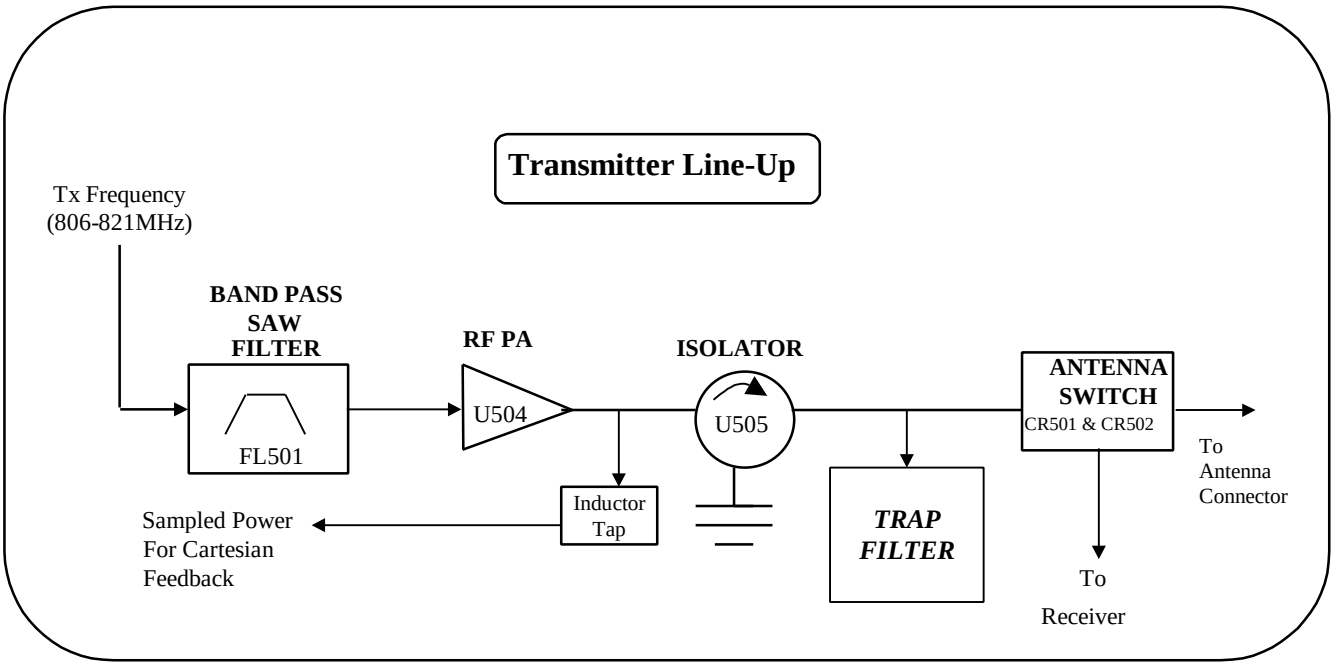

Figure 4-4: Transmitter Line-Up