FUNCTION OF RF SEMICONDUCTORS AND OTHER ACTIVE DEVICES

Reference Designator	Motorola Part no.	Description	Circuit Application	Operating Frequency	Radio Circuit
CR203	4862824C03	1SV232	TX VCO FREQ	806-870MHz	FRACN
D201	4802233J09	IMN10	Synthesizer Circuit	16.8MHz	FRACN
D202	4802233J09	IMN10	Synthesizer Circuit	16.8MHz	FRACN
Q200	4802245J50	UMC5N	DC Switch	DC	FRACN
Q210	4802245J50	UMC5N	DC Switch	DC	FRACN
U201	5185963A27	63A27	FGU	16.8MHz	FRACN
U247	5105739X05	ADP3300	5V Voltage Regulator	DC	FRACN
U248	5102463J58	LP2980	3.3 Voltage Regulator	DC	FRACN
CR251	4862824C01	1SV229	VARACTOR	806-870MHz	VCO
CR252	4862824C01	1SV229	VARACTOR	806-870MHz	VCO
CR253	4862824C01	1SV229	VARACTOR	806-870MHz	VCO
Q251	4805218N63	BFQ67W	RF Transistor	806-870MHz	VCO
Q252	4802245J50	UMC5N	DC Switch	DC	VCO
U205	4802245J58	RESONATOR	Resonator	900 MHz	VCO
U206	4802245J57	RESONATOR	Resonator	1.2GHz	VCO
U250	5105750U54	50U54	Buffer IC	740-870MHz	VCO
CR101	4880973Z02	MA4PH261	Diode Switch	806-870MHz	PA
CR102	4880973Z02	MA4PH261	Diode Switch	806-870MHz	PA
Q101	5105385Y73	85Y73	PA DEVICE	806-870MHz	PA
U101	5102463J66	RF2103	PA DRIVER IC	806-870MHz	PA
U102	5185765B01	H99S-4	Power Control	DC	PA
U103	5185963A15	LM50	Temperature sensing	DC	PA
CR440	4813833C02	MMBD6100	Reverse Current Protection	DC	CONTRL
Q400	4809579E18	TP0101T	DC Switch	DC	CONTRL
Q403	4880214G02	MMBT3904	DC Switch	DC	CONTRL
Q405	4802245J54	UMG5	DC Switch	DC	CONTRL
Q410	4802245J54	UMG5	DC Switch	DC	CONTRL
Q411	4802245J54	UMG5	DC Switch	DC	CONTRL
Q416	4809579E18	TP0101T	DC Switch	DC	CONTRL
U400	5102463J40	LP2951ACMM-3.3	3.3 Voltage Regulator	DC	CONTRL
U409	5102226J55	MC68HC11FL0	Micro Processor	1.83MHz	CONTRL
U410	5102463J57	ILC7062CM-33	Voltage Regulator	DC	CONTRL
U420	5102463J44	TDA8547	Audio Amplifier	AUDIO	CONTRL
VR432	4805656W08	MMQA5V6T1	ESD Protection Diode	AUDIO	CONTRL
VR433	4805656W08	MMQA5V6T1	ESD Protection Diode	AUDIO	CONTRL
VR434	4802245J51	BZX284	ESD Protection Diode	DC	CONTRL
VR445	4802245J53	BZX284	ESD Protection Diode	DC	CONTRL
VR446	4802245J53	BZX284	ESD Protection Diode	DC	CONTRL
VR447	4802245J53	BZX284	ESD Protection Diode	DC	CONTRL

TUNING PROCEDURE

Table for tuning frequencies.

Test/Tune Freq	800 MHz
F1	805.975
F2	815.525
F3	825.025
F4	838.025
F5	850.075
F6	860.525
F7	870.025

TABLE 1

1.0 CRYSTAL CODE EXTRACTION

a) Scan the 2D barcode of the Reference xtal

b) Decode the crystal code to get crystal maximum ppm, crystal inflection temperature (xtal_infl_temp) and crystal curve ppm(t)(crystal ppm at given temperature) and store them in xtal_max_ppm, xtal_infl_temp and xtal_curve_ppm(t). The following equations are used to calculate the above parameters

q1=(dig1*10)+dig2
q2=(dig3*100)+(dig4*10)+dig5
q3=(dig6*10)+dig7
xtal_infl_temp=q1/10+22
a1=-q2/1000
a2=(q3+0.1*q2+410)/(5*10^6)
delta_temp=temps(t)-ref_temp
xtal_curve_ppm(t) =a1*delta_temp+a3*delta_temp^3

where

q1: Digits 1 and 2 from xtal code
q2: Digits 3,4,5 from xtal code
q3: Digits 6 and 7 from xtal code ref_temp:
temps(t): Array of temperature in steps of 5 deg c from -35deg C to 90deg C

1.1 Oscillator sensitivity measurement

a) Use SBEP command to program synthesizer to receive frequency F7 of table 1 and also set the INFLECTION, COLD HOT AND LINEAR dacs to maximum to turn them off (INFLECTION dac=127, COLD dac=127, HOT dac=127, LINEAR dac=127)

b) Use SBEP command to adjust warp dac to get frequency F7 within limits of table. Store warp dac value in warp_dac_center

c) Indicate the PASS/FAIL status of the warp dac value. If FAIL: “Failed set warp dac value” warp_dac_center must fall within range of 122 to 390

d) Obtain warp_dac_high and warp_dac_low using the equations below:

xtal_max_v=(xtal_max_ppm*2)/approx_sens
warp_dac_range=ABS(xtal_max_v/warp_dac_step_v)
warp_dac_high=INT(warp_dac_center+(warp_dac_range/2))
warp_dac_low=INT(warp_dac_center-(warp_dac_range/2))

where

xtal_max_v=maximum required compensation voltage
xtal_max_ppm=calculated in 1.0 (a).

constants: warp_dac_step_v=0.0065 v/step
approx._sens=20 ppm/v
e) Use SBEP command to program the radio to warp_dac_high
f) Use DMM to get voltage reading. Store it in V_H
g) Use frequency counter to get frequency reading. Store it in F_H
h) Use SBEP command to program the radio to warp_dac_low
i) Use DMM to get voltage reading. Store it in V_L
j) Use frequency counter to get frequency reading. Store it in F_L
k) Calculate the oscillator sensitivity using the equation below;

comp_range_v=V_L-V_H

ppm_range=[(F_L-F_H)/F_H]*10^6

osc_sens=ABS(ppm_range/ ppm_range_v)+osc_sens_offset

where

osc_sens=The sensitivity of the oscillator's frequency to the voltage applied to the varactor
constants: osc_sens_offset= 0

1.2 **Translate crystal's ppm curve into voltage curve**

a) Convert the crystal ppm curve vs temperature to voltage vs temperature curve as follows;
V(t)=[(xtal_curve-ppm(t)+osc_contrib(t)]/osc_sens
where

V(t)=voltage at given temperature
osc_contrib(t)=determined by hardware team
osc_sens=determined in 1.1 (m)

b) Invert the voltage vs temperature curve for compensation procedure as follows;

comp_curve_v(t)=comp_curve_vref+reg_contrib(t)-V(t)

where

comp_curve_v(t)=inverted voltage at given temperature
comp_curve_vref=1/2 of VRO
req-contrib(t)=determined by hardware team
V(t)=voltage at given temperature calculated in 1.2(a)

1.3 **Search the IC's T.C. table for best compensation curve**

a) Compare the converted crystal curve to the table of compensation of voltage curves located in the file given to the factory to find the curve which gives the minimum error over the entire temperature range. The curve fitting would give cold, hot and linear dacs values.

1.4 **Align the crystal curve to the IC's compensation curve**

a) Send SBEP command to program the LVFRACN with a warp value of warp_dac-center found in 1.1 (a) with inflection, cold hot and linear dacs off.
b) Use frequency counter to get frequency of the oscillator. Store it in ic_infl_ref
c) Send SBEP command to program the LVFRACN with inflection, cold, hot and linear dacs to settings in 1.3(a).
d) Use SBEP command to adjust inflection dac setting to get as close as possible to frequency of ic_infl_ref in 1.4 (b). Store it in ic_infl_set_amb
e) Use thermo-hunter to get the temperature at crystal. Store it in ic_temp

f) Calculation of inflection dac setting using the equation below;
infl_dac=INT(ic_infl_set_amb+(1/infl_dac_step)*(ic_temp xtal_infl_temp+infl_tmp_offset)
where

infl_dac=inflection dac value
ic_infl_set_amb=inflection dac value in 1.4 (d)
ic_temp=temperature measured in 1.4 (e)
xtal_infl_temp=temperature read from 2D code in 1.0 (a)
constants: infl_dac_step=0.33 deg/step
infl_tmp_offset=0 deg

g) Use SBEP command to save inflection, cold, hot and linear dac settings in the codeplug

1.5 **Reference oscillator warping (Final warp)**

a) Use SBEP command to adjust warp dac setting to get frquency F7 of table 1.
b) Use SBEP command to save warp dac setting in codeplug

1.6 **Dac sensitivity measurement**

a) Program radio to rx/tx mode, freq=MHz, DAC setting=127
b) Measure if radio lock, Vctrl
c) Measure frequency and DAC voltage
d) Program DAC=97, measure freq and DAC voltage
e) Program DAC=157, measure freq and DAC voltage

2.0 TRANSMITTER POWER ADJUSTMENT

2.1 **General description of PA bias adjustment.**

Tuning of the PA Bias is required to compensate for FET device tolerances due to lot to lot variation during the FET die fabrication process. To obtain optimum power and efficiency, the bias should be tuned in the factory after it is built or after a repair.

a) Program the FRACN to switch off the RF signal by setting VCO IC to battery saver mode. If this is not possible for hardware reasons, set the VCO to RX mode. This step should be performed by setting the bias tuning environment.
b) If the VCO IC can't be set to battery saver mode, set the receive frequency to F1. This should be done automatically by the radio when entering the bias tuning environment. Previous radios required frequency setting by the tuning system.
c) Initialize the PCIC for bias tuning by setting the following parameters TX mode switch on the PIN diodes (RX to low, ANO on)

set power D2A (D2A#1) to maximum
set voltage limit D2A (D2A#2) to minimum
set PA bias D2A (D2A#3) to minimum

This allows controlling the power control voltage by the voltage limit D2A. The PIN diodes should be on to avoid instabilities. For the same reason the antenna output must be terminated with 50 ohm termination. In case of PA oscillation an RF induced additional current would lead to tuning inaccuracies.
d) Measure the dc current the radio draws from the voltage supply. Note the measured value as VL0 B0 CURRENT.
e) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the "VL0 B0 CURRENT" as specified in table 2 "VL CURRENT". Note the measured value as "VL B0 CURRENT". The additional current is drawn by the driver.

f) Increase the PA bias D2A (D2A#3) until the dc current exceeds the "VL B0 CURRENT" as specified in table 2 " B CURRENT ". The additional current is drawn by the FET. After this step a balance between the FET current (gain) and the driver current (gain) has been achieved. The balance is maintained when the RF output power is altered.
g) Store the PA bias D2A value in the PA bias softpot.

2.2 **Transmitter PA bias adjustment procedure**

a) Set radio environment for PA bias tuning. This relates to steps a)-c) of section 2.1.
b) Measure the radio dc current and note the value as " VL0 B0 CURRENT". This relates to step d) of section of 2.1.
c) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the „VL0 B0 CURRENT" as specified in table 2 "VL CURRENT" . Note the measured current as " VL B0 CURRENT". This relates to steps e) of section 2.1.
d) Increase the PA bias D2A (D2A#3) until the dc current exceeds the „VL B0 CURRENT" as specified in table 2

" B CURRENT". This relates to steps f) of section 2.1.
e) Store the PA bias D2A value in the PA bias softpot.

Frequency Band	VL Current	B Current
800	60mA +/- 10%	280mA +/- 10%

Table 2.

2.3 **Transmitter Power Adjustment**

(Important: Section 2.2 must be completed before power adjustment can be carried out)
The Waris radio power-level tuning is across the band at 7 discrete test frequencies, each at 2 discrete power levels. In addition, there are 2 power setting.

a) Program radio to Test Mode Carrier Squelch Environment to appropriate power level
b) Set radio to the correct transmitter frequency
c) Key up the radio
d) Set PA control Voltage Limit softport to $3F without codeplug update
e) Set Transmit Power Softpot to DAC1 value and measure output power P1
f) Set Transmit Power Softpot to DAC2 value and measure the output power P2
g) Dekey the radio and calculate the Mcp & Kcp

M =(SQRT(P1)-SQRT(P2))/(DAC1-DAC2)
Mcp = -1000*M
Kcp = 20*(SQRT(P1)-(M*DAC1))

h) Repeat for other test point frequencies that require tuning, value for untuned frequencies are to be interpolated by the test controller and programmed into codeplug

DAC_PWR_SET = 50*(Kcp-Pcp)/Mcp
Pcp = 20*SQRT(desired power)

Power is tuned to the window specified below:

800MHz:	805.975-825.025MHz	838.025-870.025MHZ
Hi Power	2.5 W	2.1-2.3W
Low Power	1.1-1.3W	1.1-1.3W

3.0 BALANCING/LIMITING LOW AND HIGH PORT Modulation of the Synthesizer

3.1 Modulation Balancing (MOD ATTN)

a) Program the radio for low power using the settings obtained in procedure 2.3 above.
b) Program the ASFICCMP to mute the microphone .Set ASFICcmp for FLAT_TX_RTN mode (Flat audio response) and default attenuator settings (Note 1).
c) Program the synthesizer to the lowest transmit tune frequency as in table 1 and set the ADC bits 12-11 = "10" . These bits set the fractional-N low port sensitivity to a max of 5.0 kHz. Set the Mod Attenuator enable bit to"1" to enable the high port modulation.
d) Apply an 80 Hz tone, 100 mVrms (140mV for 800MPT)at the external test box "Audio In " input.
e) Measure deviation (D1)
f) Change the input tone to 3kHz, 100mVrms (7mV for 800MPT)and measure deviation (D2)
g) Find the ratio in dB using 20log[D1/D2]
h) Remove the audio signal by disabling the external Tx audio path
i) Program the Mod attenuator setting of the fractional-N using the equation below:
Modulation attenuator setting = (current setting at step i) + -(5 x (dB value of step i))
j) Re-enable the External Tx audio path.
k) Repeat steps (f) - (i) until the ratio in dB of step (i) is <±0.20dB, store modulation attenuator setting to EEPROM.

NOTE : The attenuator settings of the ASFICcmp are defaulted for minimum attenuation (MOD6 - MOD0 = $FF) before start of balancing. The fractional-N modulation attenuator should be set to 6.4dB, ie $20 (32 decimal).

3.2 **Modulation Limiting**

a) Disable the FLAT_TX_RTN mode. Select the Ext Mic and unmute it.
b) Inject at the Ext Mix Input a 1khz tone,80mVrms with the preemphasis enabled and adjust the Mod attenuator of the ASFICcmp to obtain the deviation in Table 3
c)Dekey the radio
d) Store the attenuator setting in the codeplug.
e) Repeat the steps (f) to (p) for other frequencies as per the tuning matrix.

Reference Voice Deviation

Channel Spacing	Deviation (kHz)	Table 3
25	4.30 - 4.60	
20	3.40 - 3.60	

NOTE 2 :For 20khz channel spacing, increase the Mod attenuator of ASFICcmp by 1.95db. Verify the deviation reduces to the range of 3.4 to 3.6khz. If tuning is required, adjust only the Mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency