CIRCUIT DESCRIPTION/BLOCK DIAGRAMS

A general description of the overall circuit is not covered in an instruction manual. This section provides the description of circuits required by subpart 2.983 of the Commissions' rules. Circuits not described in the manual are covered in this exhibit.

The following are included:

1. Means for Frequency Stabilization*	4A
2. Means for Modulation Limiting and Low Pass Filter*	4B
3. Means for Harmonic Suppression	4C
4. Means for Limiting Power*	4D

* From currently Type Accepted Transmitter FCC ID: AZ489FT4818.

CARRIER FREQUENCY GENERATION AND STABILIZATION

BLOCK DIAGRAMS:

The carrier frequency is generated using a fractional-N frequency synthesizer inside the DFP99(U501). This consists of a phase-locked loop circuit with a voltage controlled oscillator (VCO) whose output is fed back to a programmable divider chain. The divide ratios are determined from information stored in the microcomputer and bussed to the synthesizer via a microcomputer. The microcomputer extracts the data for the division ratios as determined by the system select switch or by loading data stored in the memory ICs. Using a time averaged algorithm a combination of divide ratios are used so that the reference frequency can be a much higher value than the value of the frequency resolution. Modulation occurs by a combination of directly coupling the modulation signal to the low pass filter in the loop and by processing the digitized analog modulation signal to alter the divider values. A temperature compensated crystal oscillator at 16.8 MHz and stable to 2.5 parts per million over temperature extremes is used for the frequency reference. The 16.8 MHz reference is further divided into one of three reference frequencies which is compared to the divided down VCO output in a phase detector which in turn provides a DC steering voltage back to the VCO.

MODULATION LIMITING AND LOW PASS FILTER

BLOCK DIAGRAMS:

The pre-emphasis modulation limiting and low pass filtering of this transmitter are in integrated circuit form on the Audio/Signaling Filter section of the AFP99 (U401). Audio from the microphone initially enters the AFP99 (U401) where it is amplified, filter and pre-emphasized. The limited, filtered audio is then fed through digitally programmable attenuators to the modulation port on the synthesizer module into the DFP99 (U501). There is no access to the post limiter in the DPP99 (U501).

HARMONIC SUPPRESSION CIRCUIT

CIRCUIT DESCRIPTION:

Attenuation for harmonics is provided by a low pass filter before the RF Power Amplifier and one after it, as well as, the Harmonic Filter after the Antenna Switch. The low pass filter in the RF PA is composed of C208, C215and L208 on the output . The Harmonic Filter is a fifth order Low Pass Chebyshev with 0.1 dB of ripple composed of C101, C102 and C103, C104, C105, L101, L102, L105.

For Circuit Diagram refer to the Schematics in Exhibit 5.

MEANS FOR LIMITING POWER

CIRCUIT DESCRIPTION

The transmit power Amplifier is a two stage design. The PA is a Temic PA RF power amplifier IC chip with an input level of 3 dBm(2 mW)., and 25-30 dB gain. The PA has a specified maximum output of 1.0 Watt. The antenna switch controls the RF signal flow. In transmit mode, the RF signal flow is directed to the Harmonic filter. The output of the harmonic filter is connected to the antenna.

For Circuit Diagram refer to the Schematics in Exhibit 5.