FUNCTION OF RF SEMICONDUCTORS AND OTHER ACTIVE DEVICES

SCHEMATIC KEY	PART NUMBER	CIRCUIT APPLICATION	OPERATING FREQUENCY	INDUSTRY EQUIVALENT
CR101	48-80973Z02	ANTENNA SWITCH	450-512 MHz	MA4PH261
CR102	48-02245J41	ANTENNA SWITCH	450-512 MHz	HSMP3820
CR105	51-85963A15	POWER AMPLIFIER	450-512 MHz	LM50
CR201	48-02233J09	SYNTHESIZER	16.8 MHz	IMN10
CR203	48-62824C03	TX VCO FREQ	430-470 MHz	1SV232
CR241	48-05649Q13	RX. VCO	355-425 MHz	1SV228
CR242 & CR243	48-62824C01	RX. VCO	355-425 MHz	1SV229
CR251	48-62824C01	TX. VCO	450-512 MHz	1SV229
CR301 & CR302	48-62824C01	RX. SYSTEM	450-512 MHz	1SV229
CR303	48-80154K03	ESD PROTECTION	DC	MMBD353
CR304 & CR305	48-62824C01	RX. SYSTEM	450-512 MHz	1SV229
CR306	48-02245J42	MIXER	DC	HSMP3820
CR310	48-62824C01	2ND OSCILLATOR	90.2 MHz	1SV229
CR414, CR412 & CR413	48-02245J47	REVERSE CURRENT PROTECTION	DC	RB471E
CR440	48-13833C02	REVERSE CURRENT PROTECTION	DC	MMBD6100
CR501	48-80107R01	REVERSE CURRENT PROTECTION	DC	BYD17D
CR503	48-05729G49	LED	DC	BRPY1204W
Q110	48-02245J55	POWER AMPLIFIER	450-512 MHz	PRF1507
Q111, Q210, Q260, Q261 & Q417, Q418, Q506	48-02245J50	DC SWITCH	DC	UMC5N
Q241	48-05218N63	VCO OSCILLATOR	450-512 MHz	BFQ67W
Q301	48-02245J44	RF AMPLIFIER	450-512 MHz	HP415
Q302	48-02245J44	IF AMPLIFIER	45.1 MHz	HP415
Q315, Q421 & Q505	48-80214G02	DC SWITCH	DC	MMBT3904
Q320	48-05218N63	2ND OSCILLATOR	90.2 MHz	BFQ67W
Q400	48-09579E18	DC SWITCH	DC	TP0101T
Q403, Q433	48-80214G02	DC SWITCH	DC	MMBT3904
Q405 & Q410	48-02245J54	DC SWITCH	DC	UMG5
Q420	48-05128M67	AMPLIFIER	DC	MMBT3906
Q418				
Q419, Q431 & Q502	51-80159R01	DC SWITCH	DC	LM50
U101	51-055109Z67	TRANSMITTER SYSTEM	450-512 MHz	CUSTOM
U102	51-85765B01	TRANSMITTER SYSTEM	450-512 MHz	CUSTOM
U201	51-85963A27	FGU	16.8 MHz	CUSTOM
U211	51-02463J61	FGU	DC	TC7SET04FU
U241	51-05750U54	FGU	450-512 MHz	CUSTOM
U247	51-05739X05	5V VOLTAGE REGULATOR	DC	ADP3300
U248	51-02463J58	3.3V VOLTAGE REGULATOR	DC	LP2980
U301	51-09632D83	RX. SYSTEM		CUSTOM
U400	51-02463J40	3.3V VOLTAGE REGULATOR	DC	AT49BV020
U404	51-85963A53	AUDIO SYSTEM	AUDIO	CUSTOM
U406	51-02463J59	CONTROLLER SYSTEM	1.83 MHz	AT49HLV010
U409	51-02463J56	CONTROLLER SYSTEM	1.83 MHz	MC74HC4066
U410	51-02463J57	3.3V VOLTAGE REGULATOR	DC	TDA8547
U420	51-02463J44	AUDIO AMPLIFIER	AUDIO	TC7SET04FU
VR440-VR444, VR431 & VR506	48-02245J51	ESD PROTECTION DIODE	DC	BZX284_6V8
VR450 & VR451	48-02245J53	ESD PROTECTION DIODE	DC	BZX284_C10
VR439, VR432, VR433	48-80140L15	ESD PROTECTION DIODE	DC	MMBZ5240B
VR501	48-13830A18	ESD PROTECTION DIODE	DC	MMBZ5235B
U602	51-02463J49	KEYPAD BOARD		LMC7211

TUNING PROCEDURES

1. Tuning frequencies

These frequencies should be used for transmitter tuning. To avoid interference, the factory should use a frequency offset of 100KHz from these frequencies for an receiver tuning or testing.

Test/Tune Freq	UHF Band 2
F1	450.025
F2	462.850
F3	475.675
F4	488.500
F5	501.325
F6	514.150
F7	526.975

Table 1.1

This procedure was written in the sequence that the radio is to be tuned. The following points should be noted:

1) Radio controller refers to the microprocessor in the radio.
2) Tester/test controller refers to external test system (hardware as well as software).
3) Values in tables may change to improve yield.
4) Disable LLE for all tuning and testing.

2. PRO -SCANNING PROGRAMMING

2.1 Flashing

2.2 Download default codeplug

2.3 Scan the 2D barcode of the Reference xtal

2.3.1 Decode of the barcode

a) Decode the crystal code to get crystal maximum ppm, crystal inflection temperature (xtal_infl_temp) and crystal curve ppm(t)(crystal ppm at given temperature) and store them in xtal_max_ppm, xtal_infl_temp and xtal_curve_ppm(t). The following equations are used to calculate the above parameters

q1=(dig1*10)+dig2
q2=(dig3*100)+(dig4*10)+dig5
q3=(dig6*10)+dig7
xtal_infl_temp=q1/10+22
a1=-q2/1000
a2=(q3+0.1*q2+410)/(5*10^6)
delta_temp=temps(t)-ref_temp
xtal_curve_ppm(t) =a1*delta_temp+a3*delta_temp^3

where

q1: Digits 1 and 2 from xtal code
q2: Digits 3,4,5 from xtal code
q3: Digits 6 and 7 from xtal code
ref_temp:
temps(t): Array of temperature in steps of 5 deg c from -35deg C to 90 deg C

2.4 Temperature compensation tuning

2.4.1 **Oscillator sensitivity measurement**

a) Use SBEP command to program synthesizer to receive frequency F7 of table 1.1 and also set the INFLECTION, COLD HOT AND LINEAR dacs to maximum to turn them off (INFLECTION dac=**63**, COLD dac=127, HOT dac=127, LINEAR dac=**63**)

b) Use SBEP command to adjust warp dac to get frequency F7 within +/- 0.2 ppm
Store warp dac value in warp_dac_center

c) Indicate the PASS/FAIL status of the warp dac value
If FAIL: ÏFailed set warp dac valueÓ
warp_dac_center must fall within range of 122 to 390

d) Obtain warp_dac_high and warp_dac_low using the equations below:
xtal_max_v=(xtal_max_ppm*2)/approx_sens
warp_dac_range=ABS(xtal_max_v/warp_dac_step_v)
warp_dac_high=INT(warp_dac_center+(warp_dac_range/2))
warp_dac_low=INT(warp_dac_center-(warp_dac_range/2))

where
xtal_max_v=maximum required compensation voltage
xtal_max_ppm=calculated in 2.3.1a
constants: warp_dac_step_v=0.0065 v/step
approx_sens=20 ppm/v

e) Use SBEP command to program the radio to warp_dac_high

f) Use DMM to get voltage reading. Store it in V_H

g) Use frequency counter to get frequency reading. Store it in F_H

h) Use SBEP command to program the radio to warp_dac_low

i) Use DMM to get voltage reading. Store it in V_L

j) Use frequency counter to get frequency reading. Store it in F_L

k) Calculate the oscillator sensitivity using the equation below;
comp_range_v=V_L-V_H
ppm_range=[(F_L-F_H)/F_H]*10^6
osc_sens=ABS(ppm_range/ **comp_range_v**)+osc_sens_offset where
osc_sens=The sensitivity of the oscillatorÌs frequency to the voltage applied to the varactor constants: osc_sens_offset= 0

2.4.2 **Translate crystal's ppm curve into voltage curve**

a) Convert the crystal ppm curve vs temperature to voltage vs temperature curve as follows;
V(t)=[(xtal_curve-ppm(t)+osc_contrib(t)]/osc_sens where
V(t)=voltage at given temperature
osc_contrib(t)=determined by hardware team ! **Currently equal to zero**
osc_sens=determined in m

b) Invert the voltage vs temperature curve for compensation procedure as follows;
comp_curve_v(t)=comp_curve_vref+reg_contrib(t)-V(t) where
comp_curve_v(t)=inverted voltage at given temperature
comp_curve_vref=1/2 of VRO=**2.500V**
req-contrib(t)=determined by hardware team
V(t)=voltage at given temperature calculated in 2.4.2 (a)

2.4.3 **Search the IC's T.C. table for best compensation curve**

a) Compare the converted crystal curve to the table of compensation of voltage curves located in the file given to the factory to find the curve which gives the minimum error over the entire temperature range. The curve fitting would give cold, hot and linear dacs values

2.4.4 **Align the crystal curve to the IC's compensation curve**

a) Send SBEP command to program the LVFRACN with a warp value of warp_dac-center found in 2.4.1(a) with inflection, cold hot and linear dacs are off

b) **Measure the voltage on the IC's WARP pin** . Store it in ic_infl_ref

c) Send SBEP command to program the LVFRACN with inflection, cold, hot and linear dacs to settings in 2.4.3 (a)

d) Use SBEP command to adjust inflection dac setting to get the **WARP voltage as close to the ic_infl_ref in 2.4.4 (c**). Store it in ic_infl_set_amb

e) Use thermo-hunter to get the temperature at crystal. Store it in ic_temp

f) Calculation of inflection dac setting using the equation below;
infl_dac=INT(ic_infl_set_amb+(1/infl_dac_step)*(ic_temp-xtal_infl_temp+infl_tmp_offset)
where
infl_dac=inflection dac value
ic_infl_set_amb=inflection dac value in 2.4.4d)
ic_temp=temperature measured in 2.4.4e)
xtal_infl_temp=temperature read from 2D code in 2.3.1a)
constants: infl_dac_step=0.33 deg/step
infl_tmp_offset=0 deg

g) Use SBEP command to save inflection, cold, hot and linear dac settings in the codeplug

2.4.5 **Reference oscillator warping (Final warp)**

a) Use SBEP command to adjust warp dac setting to get frquency F7 of table 1.1.

b) Use SBEP command to save warp dac setting in codeplug

3. TRANSMITTER POWER ADJUSTMENT

3.1 General description of PA bias adjustment.

Tuning of the PA Bias is required to compensate for FET device tolerances due to lot to lot variation during the FET die fabrication process. To obtain optimum power and efficiency, the bias should be tuned in the factory after it is built or after a repair.

a) Program the FRACN to switch off the RF signal by setting VCO IC to battery saver mode. If this is not possible for hardware reasons set the VCO to RX mode. This step should be performed by setting the bias tuning environment.

b) If the VCO IC cannot be set to battery saver mode, set the receive frequency to the following frequency :

Frequency Band	Test Frequency
UHF Band 2	F7

Table 1.2

This should be done automatically by the radio when entering the bias tuning environment. Previous radios required frequency setting by the tuning system.

c) Initialize the PCIC for bias tuning by setting the following parameters
TX mode
switch on the PIN diodes (RX to low, ANO on)
set power D2A (D2A#1) to maximum
set voltage limit D2A (D2A#2) to minimum
set PA bias D2A (D2A#3) to minimum

This allows controlling the power control voltage by the voltage limit D2A. The PIN diodes should be on to avoid instabilities. For the same reason the antenna output must be terminated with 50 Ω. In case of PA oscillation an RF induced additional current would lead to tuning inaccuracies.

d) Measure the dc current the radio draws from the voltage supply. Note the measured value as “VL0 B0 CURRENT”.
e) Increase the voltage limit D2A (D2A#2) until the dc current is within the limits of the “VL0 B0 CURRENT“ as specified in table 1.3 “VL CURRENT“. Note the measured value as “VL B0 CURRENT“. The additional current is drawn by the driver.
f) Increase the PA bias D2A (D2A#3) until the dc current exceeds the “VL B0 CURRENT“ as specified in table 1.3 “ B CURRENT “ . The additional current is drawn by the FET. After this step a balance between the FET current (gain) and the driver current (gain) has been achieved. The balance is maintained when the RF output power is altered.
g) Store the PA bias D2A value in the PA bias softpot.

3.2 Transmitter PA bias adjustment procedure

a) Set radio environment for PA bias tuning. This relates to steps (a)-(c) of section 3.1
b) Measure the radio dc current and note the value as “VL0 B0 CURRENT“. This relates to steps (d) of section of 3.1
c) Increase the voltage limit D2A (D2A#2) until the dc current is within the limits of the “VL0 B0 CURRENT“ as specified in table 1.3 “VL CURRENT’ . Note the measured current as “VL B0 CURRENT“. This relates to steps (e) of section 3.1
d) Increase the PA bias D2A (D2A#3) until the dc current exceeds the “VL B0 CURRENT“ as specified in table 1.3 “B CURRENT”. This relates to steps (f) of section 3.1
e) Store the PA bias D2A value in the PA bias softpot.

Frequency	**VL Current**	**B Current**
UHF Band 2	peak 10mA-17mA	peak 400mA-440mA

Table 1.3

3.2 Transmitter Power Adjustment

(Important: Section 3.2 must be completed before power adjustment can be carried out)

The radio power-level tuning is across the band at 7 discrete test frequencies, each at 2 discrete power levels. In addition, there are 2 nominal power settings.

a) Set the radio to first tuning frequency
b) Key up the radio and measure power.
c) Adjust the high power level (4W) and store the data.
d) Repeat for all other tuning frequency points.
e) Repeat a) through d) for low power level (1W).

Power Tuning Level Specification at each test point in table 1.1:

	UHF BAND 2
	(450-512MHz)
Hi Power	4.2-4.5W
Lo Power	1.1-1.3W

Table 1.4

4. BALANCING/LIMITING LOW AND HIGH PORT Modulation of the Synthesizer

4.1 Modulation Balancing (MOD ATTN):

a) Program the radio for low power using the settings obtained in procedure 3.3 above.
b) Program the ASFICCMP to mute the microphone .Set ASFICcmp for FLAT_TX_RTN mode (Flat audio response) and default attenuator settings (Note 1).
c) Program the synthesizer to the lowest transmit tune frequency as in table 1.1 and set the ADC bits 12-11 = „10„ . These bits set the fractional-N low port sensitivity to a max of 5.0 KHz. Set the Mod Attenuator enable bit to"1" to enable the high port modulation.
d) Apply an 80 Hz tone, 100 mVrms at the external test box "Audio In " input.
e) Measure deviation (D1).
f) Change the input tone to 3KHz, 91mVrms and measure deviation (D2).
g) Find the ratio in dB using 20log[D1/D2].
h) Remove the audio signal by disabling the external Tx audio path.
i) Program the Mod attenuator setting of the fractional-N using the equation below:
Modulation attenuator setting = (current setting at step i) + -(5 x (dB value of step i))
j) Re-enable the External Tx audio path .
k) Repeat steps f) - l) until the ratio in dB of step i) is <±0.20dB, store modulation attenuator setting to EEPROM.

(NOTE 1: The attenuator settings of the ASFICcmp are defaulted for minimum attenuation (MOD6 - MOD0 = $FF) before start of balancing. The fractional-N modulation attenuator should be set to 6.4dB, ie $20 (32 decimal)).

5. MODULATION LIMITING

a) Disable the FLAT_TX_RTN mode. Select the Ext Mic and unmute it.

b) Inject at the Ext Mix Input a 1KHz tone, 80mVrms with the pre-emphasis enabled and adjust the Mod attenuator of the ASFICcmp to obtain the deviation in table 1.5.

c) Dekey the radio

d) Store the attenuator setting in the codeplug.

e) Repeat the steps (a) to (d) for other frequencies as per the tuning matrix.

(Note 2: For 20kHz channel spacing, increase the Mod attenuator of ASFICcmp by 1.95db. Verify the deviation reduces to the range of 3.4 to 3.6kHz. If tuning is required, adjust only the Mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency.)

12.5kHz Channel spacing.

Program the synthesizer ADC bit 12..11 to 11(Reduce deviation sensitivity of the synthesizer).
Verify the deviation reduces to the range of 2.2 to 2.3 kHz. If tuning is required, adjust only the Mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency.

5.1 DTMF DEVIATION

a) Set radio to the first tuning frequency.
b) Key up the radio.
c) Program the PCIC for Low Power.
d) Program the Mod Attenuator of the ASFICcmp and the Mod Attenuator of the synthesizer to the values determined for balancing/limiting.
e) Set the ADC bits 12-11 of the synthesizer to „10„ . These bits set the fractional-N low port sensitivity to a max of 5.0 KHz. Set the Mod Attenuator enable bit to"1" to enable the high port modulation.
f) Enable DTMF pre-emphasis in ASFICcmp and generate DTMF # digit.
g) Program the ASFICcmp TX High Speed Attenuator with default value (from default codeplug).
h) Adjust the ASFICcmp TX High Speed Attenuator if necessary to obtain deviation per table 1.6.
i) Dekey the radio
j) Store the attenuator setting in the codeplug.

Reference Voice Deviation

Channel Spacing (kHz)	Deviation (kHz)
25	4.30 - 4.60
20	3.40 – 3.60
12.5	2.20 – 2.30

Table 1.5

PL & DPL Reference Deviation

Channel Spacing (kHz)	Deviation (kHz)
25	0.50 – 1.00
20	0.40 – 0.80
12.5	0.25 – 0.50

Table 1.6