BLOCK DIAGRAMS

A general description of the overall circuit is not covered in an instruction manual. This section provides the description of circuits required by subpart 2.983 of the Commissions' rules. Circuits not described in the manual are covered in this exhibit.

The following are included:

1. Means for Frequency Stabilization	4A
2. Means for Modulation Limiting and Low Pass Filter	4B
3. Means for Harmonic Suppression	4C
4. Means for Limiting Power	4D

CARRIER FREQUENCY GENERATION AND STABILIZATION

CIRCUIT DESCRIPTION:

The carrier frequency is generated using frequency synthesizer IC102 with an external voltage controlled oscillator (VCO) composed of active element Q103, tunable inductor L106 and varactor D102 and associated bias and filtering components. The reference frequency for the synthesizer is set at 12.8 MHz by X-OSC01 a 2.5 ppm temperature compensated crystal oscillator. The oscillator operates off a regulated voltage to minimize frequency variations with battery voltage. Transistor Q106 and PIN diode D103 is used to range shift the VCO between transmit and receive frequencies. The VCO operates at one half the desired frequency and discrete components are used select the second harmonic for the transmit power amplifier and the receiver local oscillator. Transmitter modulation is applied to PIN diode D103 through variable resistor VR102.

For circuit diagram refer to the schematic in Exhibit 5.

MODULATION LIMITING AND LOW PASS FILTER

BLOCK DIAGRAMS:

Microphone audio is generated in audio transducer MIC101 or applied from an external audio accessory through accessory jack CN101. This signal is then high pass filtered using IC104A and discrete components. This filtered signal is then compressed by compander IC103 and pre-emphasized and limited by IC104B and associated discrete components. Q109 and associated discrete components provide a 3 pole low pass filter with a corner frequency of 3 kHz to filter the limiter output. Variable resistor VR102 is used to set the maximum deviation to 2.4 kHz. PIN diode D103 is used to couple the modulation signal into the VCO.

For circuit diagram refer to the schematic in Exhibit 5.

HARMONIC SUPPRESSION CIRCUIT

CIRCUIT DESCRIPTION:

. The output of the transmit power amplifier is followed by a combination matching network and low pass filter to attenuate harmonics from the amplifier and PIN diode based antenna switch. The matching and low pass filter is composed of C148, L111, C149, C150, C151, L112, C152 and C153. Bias for the PIN diode antenna switch (D104 and D101) is provided by L110 and R127.

For circuit diagram refer to the schematic in Exhibit 5.

MEANS FOR LIMITING POWER

CIRCUIT DESCRIPTION

The transmit power amplifier is a two stage discrete design. The driver stage uses a Toshiba 2SC5087 bipolar transistor (Q104) with an input drive of about 0 dBm and an output power of about 18 dBm. The output stage uses a Toshiba 2SK3078 FET (Q105) with an output power of about 27 dBm. The output stage is followed by a low pass filter, a PIN diode antenna switch and a permanently attached antenna. The output power is not adjustable and is set by discrete components in the power amplifier.

For circuit diagram refer to the schematic in Exhibit 5.