LIST OF EXHIBITS

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lII.	General Information	3	
	1. Production Plans		2.981-(c)
	2. Application References		2.1061
	3. Data Submittal Procedures		
	4. Similar Applications		
lV.	Description	4	
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V.	Function of Semiconductor or other Active Devices	5	2.983-(d)-6
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Xll.	User Manual (Basic Operation)	12	
	1. GP328		
	2. GP338		

STATEMENT OF CERTIFICATION

The technical data supplied with this application, having been taken under my supervision is hereby duly certified. The following is a statement of my qualifications:

I have received a Beng (Hons) degree from Brighton Polytechnic, Brighton, UK.

I have more tan 10 years of Design and Development experience in the field of two-way radio communication.

NAME: Ang Eng Teong

SIGNATURE: ET Ang

DATE: 5th. June 1998

POSITION: Engineering Group Leader

I hereby certify that the above application was prepared under my direction and that to the best of my knowledge and belief, the facts set forth in the application and accompanying technical data are true and correct:

NAME : Ong Kheok Chin

SIGNATURE : KC Ong

DATE : 5th. June 1998

POSITION : Engineering Manager

IDENTIFICATION LABEL

LOCATION

__X____ See The Attached Photograph or Sketch
________ Back Of Radio
________ Back Of Radio Under Belt Clip

TYPE

________ The label is a paper polyester firm laminate with a pressure sensitive adhesive backing. The adhesive is a permanent type acrylic with a minimum peel strength of 40 inches/oz.

MARKINGS (TEXT)

________ See The Attached Photograph
__X____ Refer to Exhibit 10
________ See Attached Drawing

GENERAL INFORMATION

l. Production Plans -- Pursuant 2.981

Quantity production is planned

ll. Application References -- Pursuant 2.1061

Reference is made to the following Motorola
“Application References”

1. Portable Products and their application
2. Portable Products Transmitter Modulations Methods
3. Motorola Penang Open Area Test Site

lll. Data Submittal Procedure:

Data is supplied in accordance with Part 2, Sub-part J of the Commissions’ Rules.

lV Similar, currently Type Accepted Transmitter, **FCC ID: AZ489FT4826**

DESCRIPTION

l. **Transmitter Technical Characteristics -- Pursuant 2.983 (d)**

a. RF Power Output :	1- 4 Watt Variable Power
b. Transmit Frequency Range :	403 - 470 MHz
c. Receive Frequency Range :	403 - 470 MHz
d. Frequency Stability :	2.5 PPM
e. Emissions	16K0F3E & 11K0F3E
f. Spurious Emissions	25 uW
g. DC Voltage and Current into	7.5 VDC
the final RF amplifier stage/stages	1.5 A

2. **Transmitter Application**

This transmitter is primarily intended for use in a portable environment. It is characterized by the following features, options, and accessories.

a. Power Supply Available :
- i. NiCd Rechargeable Low Capacity Battery
- ii. NiCd Rechargeable High Capacity Battery
- iii. Alkaline Battery
- iv. NiMH Rechargeable Ultra High Battery
- v. Lithium Ion Battery

b. Antenna Available :
- i. Helical Antenna
- ii. Whip antenna

c. Squelch Type Available :
- i. Carrier Squelch
- ii. Tone “Private Line”
- iii. Digital “Private Line”
- iv. DTMF
- v. MDC
- vi. Quick Call II

d. Microphone - Control :
- I. Handset/Palm Microphone

e. Maximum Transmit Channel Capability :
- i. 16 Channel (GP328 model)
- ii. 128 Channel (GP338 model)

f. Housing :
- i. The transmitter will be housed in the housing shown in the accompanying photographs

g. Other Options :
- i. Time out Timer

h. The minimum voltage for the micro-P to operate is 3.3V.

FUNCTION OF RF SEMICONDUCTORS AND OTHER ACTIVE DEVICES

SCHEMATIC KEY	PART NUMBER	CIRCUIT APPLICATION	OPERATING FREQUENCY	INDUSTRY EQUIVALENT
CR101	48-80973Z02	ANTENNA SWITCH	403-470 Mhz	MA4PH261
CR102	48-02245J41	ANTENNA SWITCH	403-470 Mhz	HSMP3820
CR105	51-85963A15	POWER AMPLIFIER	403-470 Mhz	LM50
CR201	48-02233J09	SYNTHESIZER	16.8 Mhz	IMN10
CR203	48-62824C03	TX VCO FREQ	430-470 Mhz	1SV232
CR241	48-05649Q13	RX. VCO	355-425 Mhz	1SV228
CR242 & CR243	48-62824C01	RX. VCO	355-425 Mhz	1SV229
CR251	48-02245J22	TX. VCO	403-470 Mhz	1T363
CR301 & CR302	48-62824C01	RX. SYSTEM	403-470 Mhz	1SV229
CR303	48-80154K03	ESD PROTECTION	DC	MMBD353
CR304 & CR305	48-62824C01	RX. SYSTEM	403-470 Mhz	1SV229
CR306	48-02245J42	MIXER	403-470 Mhz	HPSM2827
CR308	48-02245J41	AGC	DC	HSMP3820
CR310	48-62824C01	2ND OSCILLATOR	90.2 Mhz	1SV229
CR411,CR412 & CR413	48-02245J47	REVERSE CURRENT PROTECTION	DC	RB471E
CR440	48-13833C02	REVERSE CURRENT PROTECTION	DC	MMBD6100
CR501	48-80107R01	REVERSE CURRENT PROTECTION	DC	BYD17D
CR503	48-05729G49	LED	DC	BRPY1204W
D300	48-13833C02	REVERSE CURRENT PROTECTION	DC	MMBD6100
Q110	48-02245J55	POWER AMPLIFIER	403-470 Mhz	PRF1507
Q111,Q210,Q260,Q261 & Q417	48-02245J50	DC SWITCH	DC	UMC5N
Q241	48-05218N63	VCO OSCILLATOR	403-470 Mhz	BFQ67W
Q301	48-02245J44	RF AMPLIFIER	403-470 Mhz	HP415
Q302	48-02245J44	IF AMPLIFIER	45.1 Mhz	HP415
Q310	48-13827A07	BUFFER AMPLIFIER	403-470 Mhz	MMBR941
Q311	48-02245J04	DC SWITCH	DC	BCX71K
Q315,Q505 & Q316	48-80214G02	DC SWITCH	DC	MMBT3904
Q320	48-05218N63	2ND OSCILLATOR	90.2 Mhz	BFQ67W
Q400 & Q416	48-09579E18	DC SWITCH	DC	TP0101T
Q403	48-80214G02	DC SWITCH	DC	MMBT3904
Q405 & Q410	48-02245J54	DC SWITCH	DC	UMG5
Q502	58-80159R01	DC SWITCH	DC	LM50
U101	51-055109Z67	TRANSMITTER SYSTEM	403-470 Mhz	CUSTOM
U102	51-05835U97	TRANSMITTER SYSTEM	403-470 Mhz	CUSTOM
U201	51-85963A27	FGU	16.8 Mhz	CUSTOM
U211	51-02463J45	FGU	DC	TC7SET04FU
U241	51-05750U54	FGU	403-470 Mhz	CUSTOM
U247	51-05739X05	5V VOLTAGE REGULATOR	DC	ADP3300
U248	51-02463J58	3.3V VOLTAGE REGULATOR	DC	LP2980
U301	51-09632D83	RX. SYSTEM		CUSTOM
U400	51-02463J40	3.3V VOLTAGE REGULATOR	DC	AT49BV020
U404	51-05109Z41	AUDIO SYSTEM	AUDIO	CUSTOM
U405	51-02463J36	CONTROLLER SYSTEM	1.83 Mhz	LP2951ACMM-3.3
U406	51-02463J42	CONTROLLER SYSTEM	1.83 Mhz	TK113
U409	51-02226J55	CONTROLLER SYSTEM	1.83 Mhz	MC74HC4066
U410	51-02463J57	3.3V VOLTAGE REGULATOR	DC	TDA8547
U420	51-02463J44	AUDIO AMPLIFIER	AUDIO	TC7SET04FU
VR432 & VR433	48-05656W08	ESD PROTECTION DIODE	DC	MMQA5V6T1
VR434,VR440-VR444 & VR506	48-02245J51	ESD PROTECTION DIODE	DC	BZX284_6V8
VR439	48-80140L15	ESD PROTECTION DIODE	DC	MMBZ5240B
VR445-VR449	48-02245J53	ESD PROTECTION DIODE	DC	BZX284_10V
VR501	48-13830A18	ESD PROTECTION DIODE	DC	MMBZ5235B
D601-D606	48-80479U01	KEYPAD BACKLIGHTING	DC	PY1111C
Q601	48-05128M67	AMPLIFIER	DC	MMBT3906
Q602 & Q603	48-80214G02	DC SWITCH	DC	MMBT3904
U602	51-02463J49	KEYPAD BOARD		LMC7211

COMMENTS: The Motorola designators are special code numbers for active devices used in Motorola radios. These devices are either identical or derived from the device family listed under Source, by the manufacturer or are proprietary to Motorola. Service people do not have access to any cross-references or given any information on proprietary devices and are prevented from making unauthorized substitution.

SCHEMATIC DIAGRAMS

The schematic diagrams are as follows:

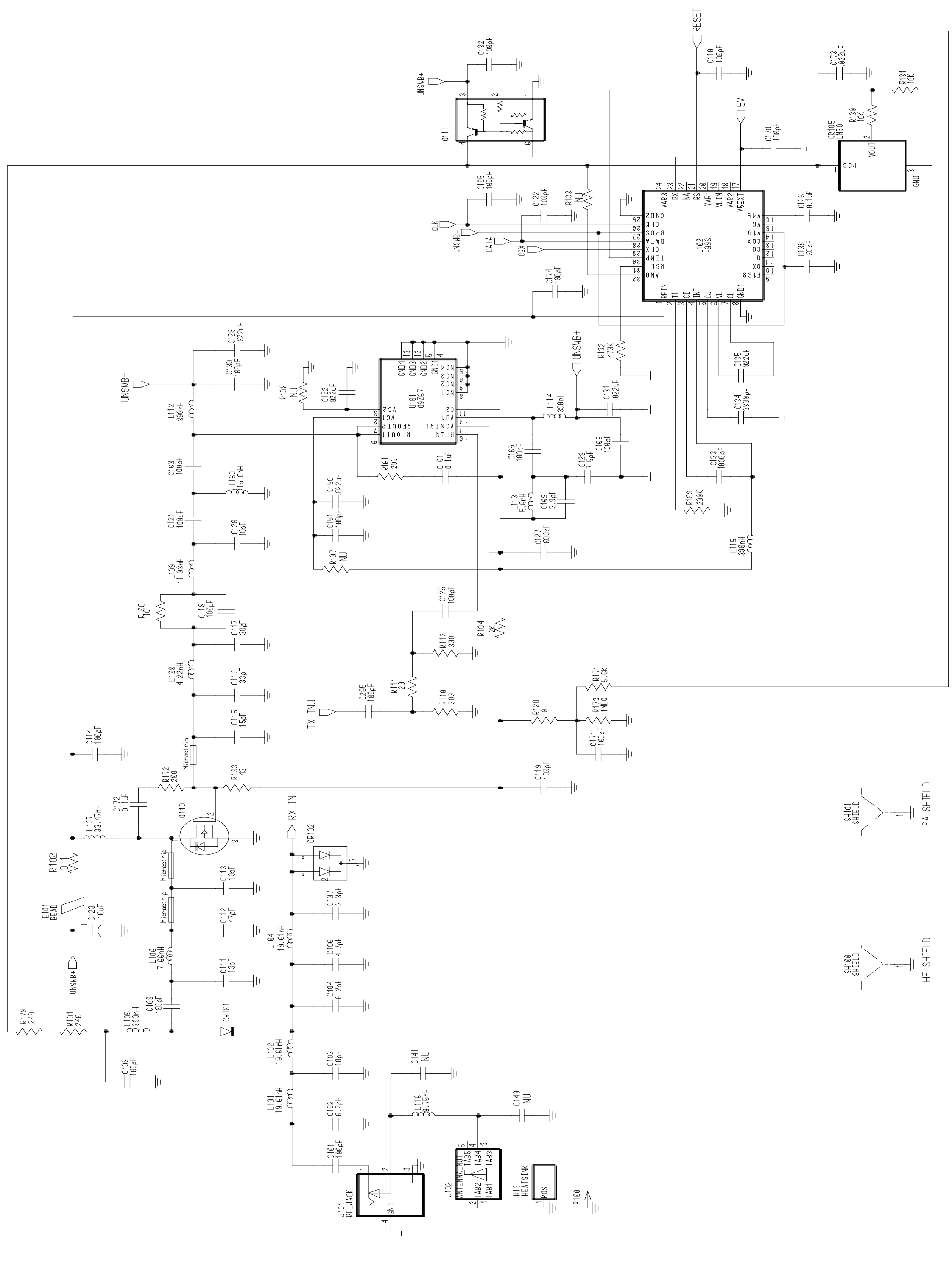
1 Basic Transmitter

2 Power Control IC

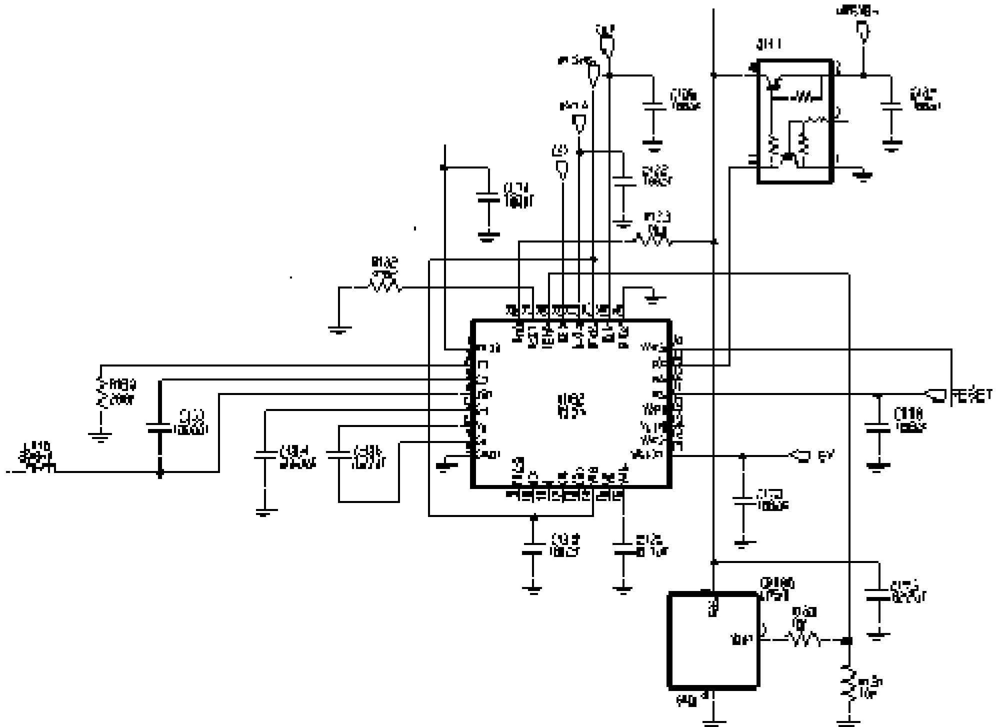
3 Driver

4 Power Amplifier/Harmonic Filter

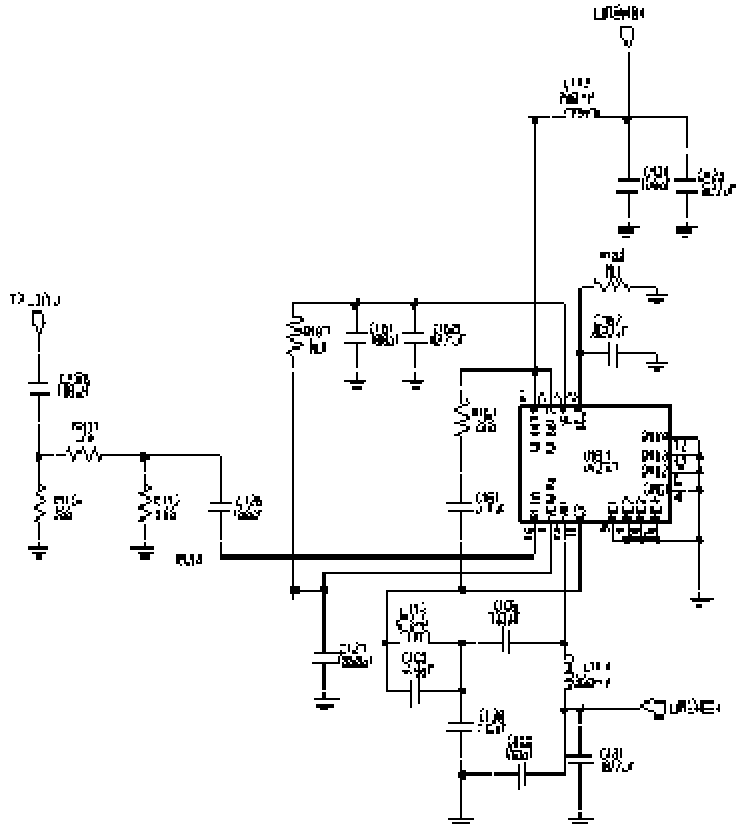
BASIC TRANSMITTER



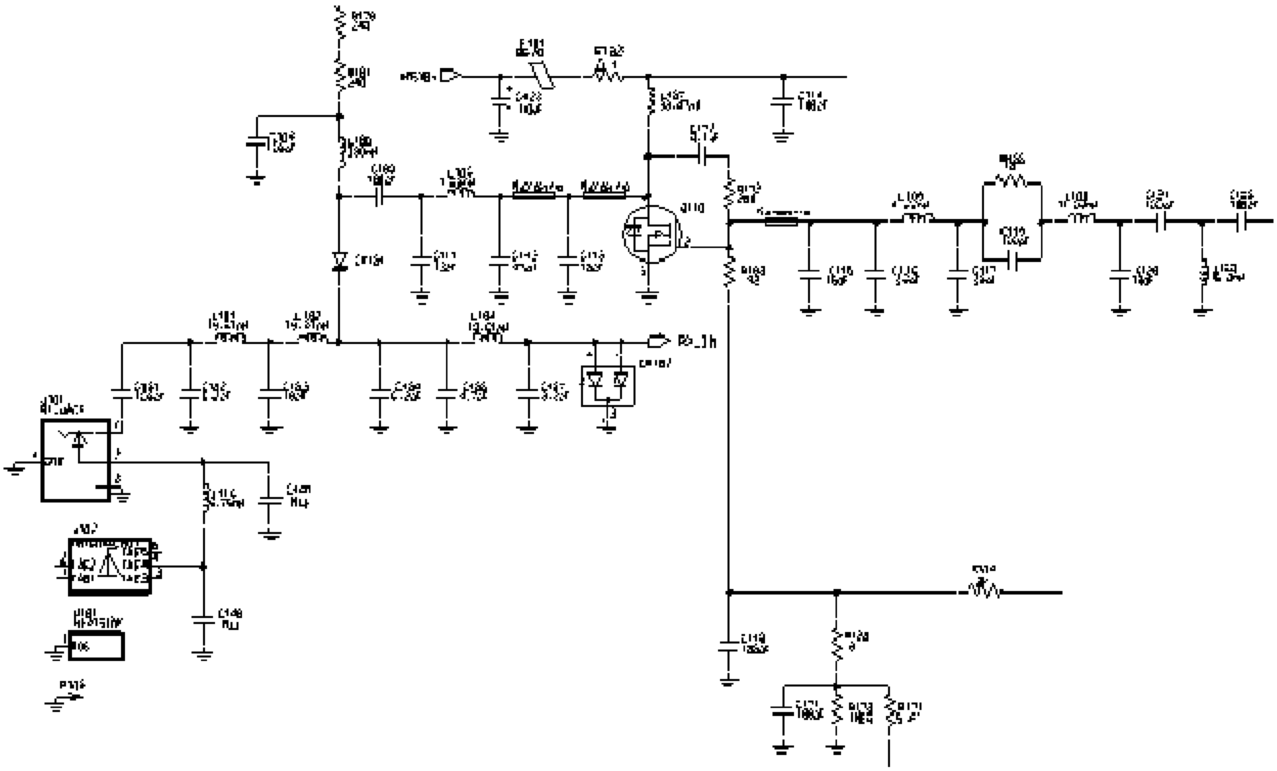
POWER CONTROL IC



DRIVER



POWER AMPLIFIER/ HARMONIC FILTER



TUNING PROCEDURE

Table for tuning frequencies.

	UHF Band1
Test/Tune Freq	403-470
F1	403.025
F2	413.025
F3	425.025
F4	437.025
F5	449.025
F6	460.025
F7	469.975

TABLE 1

1.0 CRYSTAL CODE EXTRACTION

a) Scan the 2D barcode of the Reference xtal

b) Decode the crystal code to get crystal maximum ppm, crystal inflection temperature (xtal_infl_temp) and crystal curve ppm(t)(crystal ppm at given temperature) and store them in xtal_max_ppm, xtal_infl_temp and xtal_curve_ppm(t). The following equations are used to calculate the above parameters

q1=(dig1*10)+dig2
q2=(dig3*100)+(dig4*10)+dig5
q3=(dig6*10)+dig7
xtal_infl_temp=q1/10+22
a1=-q2/1000
a2=(q3+0.1*q2+410)/(5*10^6)
delta_temp=temps(t)-ref_temp
xtal_curve_ppm(t) =a1*delta_temp+a3*delta_temp^3

where

q1: Digits 1 and 2 from xtal code
q2: Digits 3,4,5 from xtal code
q3: Digits 6 and 7 from xtal code ref_temp:
temps(t): Array of temperature in steps of 5 deg c from -35deg C to 90deg C

1.1 Oscillator sensitivity measurement

a) Use SBEP command to program synthesizer to receive frequency F7 of table 1 and also set the INFLECTION, COLD HOT AND LINEAR dacs to maximum to turn them off (INFLECTION dac=127, COLD dac=127, HOT dac=127, LINEAR dac=127)

b) Use SBEP command to adjust warp dac to get frequency F7 within limits of table. Store warp dac value in warp_dac_center

c) Indicate the PASS/FAIL status of the warp dac value. If FAIL: “Failed set warp dac value” warp_dac_center must fall within range of 122 to 390

d) Obtain warp_dac_high and warp_dac_low using the equations below:

xtal_max_v=(xtal_max_ppm*2)/approx_sens
warp_dac_range=ABS(xtal_max_v/warp_dac_step_v)
warp_dac_high=INT(warp_dac_center+(warp_dac_range/2))
warp_dac_low=INT(warp_dac_center-(warp_dac_range/2))

where

xtal_max_v=maximum required compensation voltage
xtal_max_ppm=calculated in 1.0 (a).
constants: warp_dac_step_v=0.0065 v/step
approx_sens=20 ppm/v

e) Use SBEP command to program the radio to warp_dac_high
f) Use DMM to get voltage reading. Store it in V_H
g) Use frequency counter to get frequency reading. Store it in F_H
h) Use SBEP command to program the radio to warp_dac_low
i) Use DMM to get voltage reading. Store it in V_L
j) Use frequency counter to get frequency reading. Store it in F_L
k) Calculate the oscillator sensitivity using the equation below;

comp_range_v=V_L-V_H
ppm_range=[(F_L-F_H)/F_H]*10^6
osc_sens=ABS(ppm_range/ ppm_range_v)+osc_sens_offset

where

osc_sens=The sensitivity of the oscillator's frequency to the voltage applied to the varactor
constants: osc_sens_offset= 0

1.2 **Translate crystal's ppm curve into voltage curve**

a) Convert the crystal ppm curve vs temperature to voltage vs temperature curve as follows;

V(t)=[(xtal_curve-ppm(t)+osc_contrib(t)]/osc_sens

where

V(t)=voltage at given temperature
osc_contrib(t)=determined by hardware team
osc_sens=determined in 1.1 (m)

b) Invert the voltage vs temperature curve for compensation procedure as follows;

comp_curve_v(t)=comp_curve_vref+reg_contrib(t)-V(t)

where

comp_curve_v(t)=inverted voltage at given temperature
comp_curve_vref=1/2 of VRO
req-contrib(t)=determined by hardware team
V(t)=voltage at given temperature calculated in 1.2(a)

1.3 **Search the IC's T.C. table for best compensation curve**

a) Compare the converted crystal curve to the table of compensation of voltage curves located in the file given to the factory to find the curve which gives the minimum error over the entire temperature range. The curve fitting would give cold, hot and linear dacs values.

1.4 **Align the crystal curve to the IC's compensation curve**

a) Send SBEP command to program the LVFRACN with a warp value of warp_dac-center found in 1.1 (a) with inflection, cold hot and linear dacs off.
b) Use frequency counter to get frequency of the oscillator. Store it in ic_infl_ref
c) Send SBEP command to program the LVFRACN with inflection, cold, hot and linear dacs to settings in 1.3(a).
d) Use SBEP command to adjust inflection dac setting to get as close as possible to frequency of ic_infl_ref in 1.4(b). Store it in ic_infl_set_amb
e) Use thermo-hunter to get the temperature at crystal. Store it in ic_temp

f) Calculation of inflection dac setting using the equation below;

infl_dac=INT(ic_infl_set_amb+(1/infl_dac_step)*(ic_temp xtal_infl_temp+infl_tmp_offset)

where

infl_dac=inflection dac value
ic_infl_set_amb=inflection dac value in 1.4 (d)
ic_temp=temperature measured in 1.4 (e)
xtal_infl_temp=temperature read from 2D code in 1.0 (a)
constants: infl_dac_step=0.33 deg/step
infl_tmp_offset=0 deg

g) Use SBEP command to save inflection,cold, hot and linear dac settings in the codeplug

1.5 Reference oscillator warping (Final warp)

a) Use SBEP command to adjust warp dac setting to get frequency F7 of table 1.
b) Use SBEP command to save warp dac setting in codeplug

1.6 Dac sensitivity measurement

a) Program radio to rx/tx mode, freq=MHz, DAC setting=127
b) Measure if radio lock, Vctrl
c) Measure frequency and DAC voltage
d) Program DAC=97, measure freq and DAC voltage
e) Program DAC=157, measure freq and DAC voltage

2.0 TRANSMITTER POWER ADJUSTMENT

2.1 General description of PA bias adjustment.

Tuning of the PA Bias is required to compensate for FET device tolerances due to lot to lot variation during the FET die fabrication process. To obtain optimum power and efficiency, the bias should be tuned in the factory after it is built or after a repair.

a) Program the FRACN to switch off the RF signal by setting VCO IC to battery saver mode. If this is not possible for hardware reasons, set the VCO to RX mode. This step should be performed by setting the bias tuning environment.
b) If the VCO IC can't be set to battery saver mode, set the receive frequency to F1. This should be done automatically by the radio when entering the bias tuning environment. Previous radios required frequency setting by the tuning system.
c) Initialize the PCIC for bias tuning by setting the following parameters TX mode switch on the PIN diodes (RX to low, ANO on)

set power D2A (D2A#1) to maximum
set voltage limit D2A (D2A#2) to minimum
set PA bias D2A (D2A#3) to minimum

This allows controlling the power control voltage by the voltage limit D2A. The PIN diodes should be on to avoid instabilities. For the same reason the antenna output must be terminated with 50 ?. In case of PA oscillation an RF induced additional current would lead to tuning inaccuracies.

d) Measure the dc current the radio draws from the voltage supply. Note the measured value as VL0 B0 CURRENT.
e) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the “VL0 B0 CURRENT“ as specified in table 2 “VL CURRENT“. Note the measured value as “VL B0 CURRENT“. The additional current is drawn by the driver.

f) Increase the PA bias D2A (D2A#3) until the dc current exceeds the “VL B0 CURRENT“ as specified in table 2 “ B CURRENT “ . The additional current is drawn by the FET. After this step a balance between the FET current (gain) and the driver current (gain) has been achieved. The balance is maintained when the RF output power is altered.
g) Store the PA bias D2A value in the PA bias softpot.

2.2 Transmitter PA bias adjustment procedure

a) Set radio environment for PA bias tuning. This relates to steps a)-c) of section 2.1.
b) Measure the radio dc current and note the value as “ VL0 B0 CURRENT“. This relates to steps d) of section of 2.1.
c) Increase the voltage limit D2A (D2A#2) until the dc current exceeds the „VL0 B0 CURRENT“ as specified in table 2 “VL CURRENT“ . Note the measured current as “ VL B0 CURRENT“. This relates to steps e) of section 2.1.
d) Increase the PA bias D2A (D2A#3) until the dc current exceeds the „VL B0 CURRENT“ as specified in table 2 “ B CURRENT“. This relates to steps f) of section 2.1.
e) Store the PA bias D2A value in the PA bias softpot.

	VL Current	B Current
403-470	100mA +/- 10%	280mA +/- 10%

Table 2.

2.3 Transmitter Power Adjustment

(Important: Section 2.2 must be completed before power adjustment can be carried out)
The Waris radio power-level tuning is across the band at 7 discrete test frequencies, each at 2 discrete power levels. In addition, there are 2 nominal power setting.

a) Program radio to Test Mode Carrier Squelch Environment to appropriate power level
b) Set radio to the correct transmitter frequency
c) Key up the radio
d) Set PA control Voltage Limit softport to $3F without codeplug update
e) Set Transmit Power Softpot to DAC1 value and measure output power P1
f) Set Transmit Power Softpot to DAC2 value and measure the output power P2
g) Dekey the radio and calculate the Mcp & Kcp

M =(SQRT(P1)-SQRT(P2))/(DAC1-DAC2)
Mcp = -1000*M
Kcp = 20*(SQRT(P1)-(M*DAC1))

h) Repeat for other test point frequencies that require tuning, value for untuned frequencies are to be interpolated by the test controller and programmed into codeplug
DAC_PWR_SET = 50*(Kcp-Pcp)/Mcp
Pcp = 20*SQRT(desired power)

Power is tuned to the window specified below:
UHF: (403-470)
Hi Power 4.4-4.6W
Lo Power 1.1-1.3W

3.0 BALANCING/LIMITING LOW AND HIGH PORT Modulation of the Synthesizer

3.1 Modulation Balancing (MOD ATTN)

a) Program the radio for low power using the settings obtained in procedure 2.3 above.
b) Program the ASFICCMP to mute the microphone .Set ASFICcmp for FLAT_TX_RTN mode (Flat audio response) and default attenuator settings (Note 1).
c) Program the synthesizer to the lowest transmit tune frequency as in table 1 and set the ADC bits 12-11 = “10“ . These bits set the fractional-N low port sensitivity to a max of 5.0 kHz. Set the Mod Attenuator enable bit to"1" to enable the high port modulation.
d) Apply an 80 Hz tone, 100 mVrms (140mV for 800MPT)at the external test box "Audio In " input.
e) Measure deviation (D1)
f) Change the input tone to 3kHz, 100mVrms (7mV for 800MPT)and measure deviation (D2)
g) Find the ratio in dB using 20log[D1/D2]
h) Remove the audio signal by disabling the external Tx audio path
i) Program the Mod attenuator setting of the fractional-N using the equation below:
Modulation attenuator setting = (current setting at step i) + -(5 x (dB value of step i))
j) Re-enable the External Tx audio path .
k) Repeat steps (f) - (i) until the ratio in dB of step (i) is <±0.20dB, store modulation attenuator setting to EEPROM.

NOTE : The attenuator settings of the ASFICcmp are defaulted for minimum attenuation (MOD6 - MOD0 = $FF) before start of balancing. The fractional-N modulation attenuator should be set to 6.4dB, ie $20 (32 decimal).

3.2 Modulation Limiting

a)Disable the FLAT_TX_RTN mode. Select the Ext Mic and unmute it.
b)Inject at the Ext Mix Input a 1khz tone,80mVrms with the pre-emphasis enabled and adjust the Mod attenuator of the ASFICcmp to obtain the deviation in Table 3
c)Dekey the radio
d) Store the attenuator setting in the codeplug.
e)Repeat the steps (f) to (p) for other frequencies as per the tuning matrix.

Reference Voice Deviation

Table 3

Channel Spacing	Deviation (kHz)
25	4.30 - 4.60
20	3.40 - 3.60
12.5 kHz	2.20 - 2.30

NOTE 2 :For 20khz channel spacing, increase the Mod attenuator of ASFICcmp by 1.95db. Verify the deviation reduces to the range of 3.4 to 3.6khz. If tuning is required, adjust only the Mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency

3.3 For 12.5Khz Channel spacing.

Program the synthesizer ADC bit 12..11 to 11(Reduce deviation sensitivity of the synthesizer). Verify the deviation reduces to the range of 2.2 to 2.3 khz. If tuning is required, adjust only the Mod attenuator of ASFICcmp to ensure the deviation is reduced within this range. This should be carried out at the highest frequency.

CIRCUIT DESCRIPTION

A general description of the overall circuit is covered in the instruction manual. This section provides the description of circuits required by subpart 2.983.of the Commissions' rules. Circuit not described in the manual are covered in this exhibit (8 to 8-2).

The following are included:

1) Means for Frequency Stabilization

2) Means for Modulation Limiting

3) Means for Attenuation Of Higher Audio Frequencies

4) Means for Attenuation Of Spurious Emissions

5) Means for Limiting Output Power

6) Means for Modulation Techniques

1) **Means For Frequency Stabilization**

Frequency stability is maintained by a reference oscillator/programmable temperature compensation circuit located in the frequency synthesizer IC U201. The oscillator is a Colpitts design with an amplifier in the IC. The 16.8 MHz crystal FL201, varactor and feedback capacitors are external circuitry. A control voltage applied to the varactor via the programmable compensation circuit maintains the frequency stability to within +/-2.5 ppm over temperature. Frequency tuning, also from the programmable compensation circuit, has 128 steps of resolution.

Each 16.8 MHz crystal is numerically coded providing its unique characteristic over the temperature range. With the crystal temperature characteristic known, a computed compensation characteristic is programmed into the compensation algorithm.

2) **Means for Limiting Modulation**

Modulation limiting is accomplished within the custom IC, U404. The limiting action itself occurs at the rails (i.e., 3.3V and ground). Using an opamp with feedback, very hard limiting is obtained. The limited modulation signal is then input through a low-pass splatter filter then to an electronic attenuator within U404 in order to adjust for variations in modulation sensitivities of the frequency synthesizer.

The electronic attenuator is controlled by the radio's micro-processor, U409. To keep the deviation constant over the RF frequency range & channel bandwidth, the microcomputer adds the proper correction factor to the attenuator.

3)**Means for Attenuation Of Higher Audio Frequencies**

The output of the limiter is applied to a low-pass splatter filter. This filter is a fifth-order switched capacitor filter with the rolloff corner located at 3000 Hz. The output of the low-pass filter is input to the electronic attenuator before routing to the modulator.

4) **Means For Attenuation Of Spurious Emissions**

The final stage of the RF power amplifier circuit feeds a low-pass filter in order to attenuate harmonics of the carrier frequency as well as any spurious signals. The filter is a seven elements Elliptic design using LC lump elements.

5) **Means For Limiting Output Power**

The radio utilize a current sense ALC IC U102 to regulate its output power. The current sensing resistor R102 provides a feedback signal to U102. This signal is then compared to the preprogrammed current reference and the error signal is amplified and used to generate a control voltage to control the bias for Driver U101 and final stage RF Power Amplifier, Q110.

6) **Means Modulation Techniques**

The transmitter is capable of the following types of modulation:

- i) Modulation of PL (Private Line) - Direct FM tone modulation of 67 Hz to 250.3 Hz at 15% of full system deviation.
- ii) Modulation of DPL (Digital Private Line) - Direct FM modulation at 134 BPS at 15% of full system deviation.
- iii) Modulation of DTMF tones at nominally 60% of full system deviation

Direct FM of PL or DPL is generated by a 6-bit D/A converter contained within U404. The frequency-determining clock signal is generated by the radio microcomputer. The modulation signal is processed through a five pole switched capacitor filter. The output of the filter is input to the electronic attenuator circuit.
The microcomputer adjusts the attenuator to compensate for modulation sensitivity variations of the synthesizer & channel bandwidth ensuring 15% of full system deviation for PL and DPL.
DTMF tones are generated by the audio processing IC, U404 . The tones are routed and processed in the same manner as the voice signals.