# WirelessUSB™ LS Theory of Operation

## WirelessUSB LS System Overview

WirelessUSB™ LS adds to the existing WirelessUSB portfolio a low-cost 2.4-GHz wireless solution that enables the wireless gaming console peripheral device market and displaces the 27-MHz solutions currently used for low-end retail PC Human Interface Device (HID) applications. A WirelessUSB LS system typically consists of a WirelessUSB LS Bridge and at least one WirelessUSB LS HID. The host PC is not aware of the wireless connection, since the interface to the host acts like a normal wired USB HID connection. Therefore, there is no special software required on the host PC in order to support WirelessUSB LS.

*Figure 1* is a block diagram of the WirelessUSB LS radio.

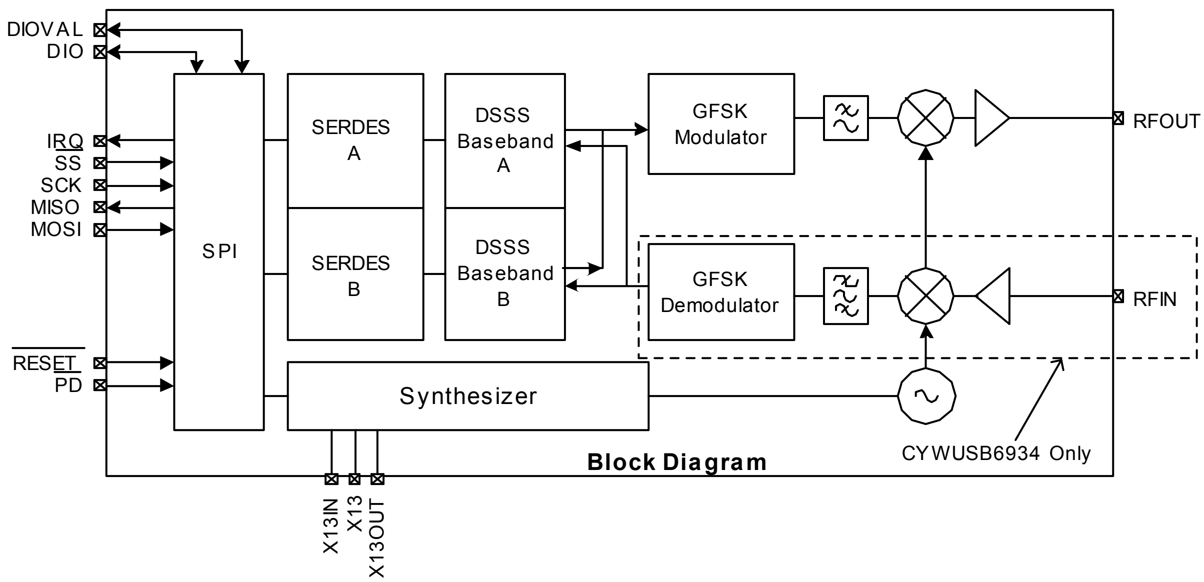


**Figure 1. WirelessUSB LS Block Diagram**

## Direct Sequence Spread Spectrum

WirelessUSB LS utilizes a 2.4-GHz direct sequence spread spectrum (DSSS) radio interface. DSSS generates a redundant bit pattern for each bit to be transmitted. This bit pattern is called a "chip" or a pseudo noise code. Notice in *Figure 2* that the pseudo noise code is a binary signal that is produced at a much higher frequency than the data that is to be transmitted. Because it has a higher frequency, it has a large bandwidth that spreads the signal in the frequency domain (i.e., it spreads its spectrum). The nature of this signal makes it appear that it is random noise.

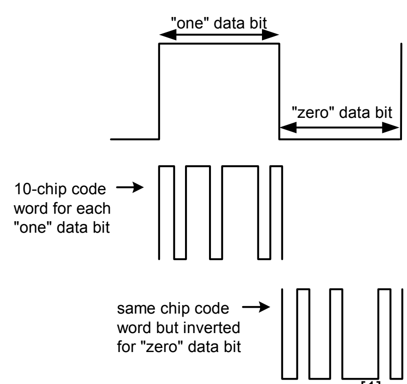


**Figure 2. Pseudo Noise Code**[1]

**Note:**

1. *Figure 2* shows the concept of PN Codes using 10 chip PN codes for illustration purposes only. The LS uses 32 chip and 64 chip PN Codes.

Contrast the spread waveform of a DSSS signal with the narrowband waveform of a traditional radio signal, both represented in *Figure 3*. The wide bandwidth provided by the pseudo noise code allows the signal power to drop below the noise threshold without losing any information. This allows DSSS signals to operate in noisy environments and reduces the interference caused by traditional narrowband signals. The longer the chip is, the greater the probability that the original data can be recovered, and, of course, the more bandwidth required. See the section below on Gold Codes for more information on the 32-bit and 64-bit pseudo noise codes used in WirelessUSB LS.

The receiver uses a locally generated replica pseudo noise code and a receiver correlator to separate only the desired coded information from all possible signals. A correlator can be thought of as a very special matched filter: it responds only to signals that are encoded with a pseudo noise code that matches its own code. Thus a correlator can be "tuned" to different codes simply by changing its local code. This correlator does not respond to man-made, natural, or artificial noise or interference. It responds only to signals with identical matched signal characteristics and encoded with the identical pseudo noise code. Even if one or more bits in the chip are damaged during transmission, statistical techniques embedded in the radio can recover the original data without the need for retransmission.

### Auto Correlation

Auto correlation is the correlation of a variable with itself over successive time intervals, in our case the pseudo noise code. Pseudo noise codes should have a high autocorrelation factor so that the receiver's correlator correctly matches the received pseudo noise code with its own code. For example, if "1010" was used as the pseudo noise code, the following sequence shows that the correlator would match the code in two separate time positions (**1010** – 0101 – **1010** – 0101). If "1001" was used instead, the correlator would only match the code in a single time position allowing the correlator to correctly process the incoming data stream (1001 – 0011 – 0110 – 1100). WirelessUSB LS uses pseudo noise codes that have a high auto correlation factor (see section on Gold Codes).

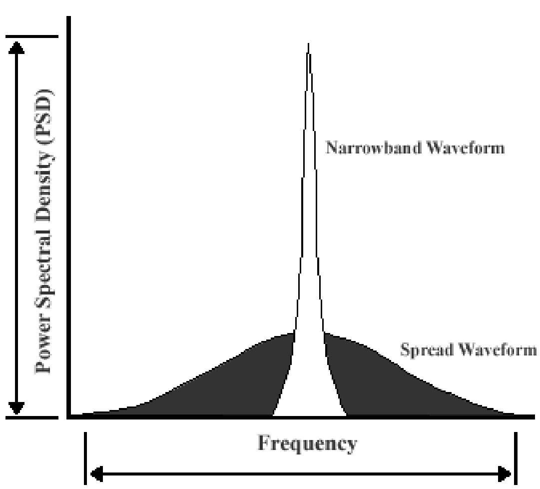


**Figure 3. Spread Signal**

### Cross Correlation

Cross correlation is the statistical correlation between two different signals as a function of relative time between the signals. In other words, cross correlation measures how unique different pseudo noise codes are. If pseudo noise codes are used that have a low cross correlation factor their signals will not interfere with each other. For example, if "1001" and "1100" are used as pseudo noise codes, if "1100" is time shifted it becomes "1001" and can be incorrectly matched to by the correlator looking for "1001" and not "1100." If "1001" and "1011" are used instead, "1011" will never be incorrectly matched by the correlator looking for "1001" because these two pseudo noise codes never match no matter how they are shifted. WirelessUSB LS uses pseudo noise codes that have a low cross correlation factor (see section on Gold Codes).

### Gold Codes

WirelessUSB LS uses sets of Gold Codes as pseudo noise codes in order to enable multiple devices to simultaneously transmit on the same frequency. Gold Codes exhibit high auto correlation and minimal, well defined, cross correlation levels with all other members of the set. Gold Codes are excellent pseudo noise codes for code division multiple access (CDMA) systems.

WirelessUSB LS can use 32-bit or 64-bit Gold Codes. There are pros and cons to each code length. 32 bit Gold Codes allow a data rate of 32-kbps, while 64-bit Gold Codes allow a data rate of 16 kbps. On the other hand, using 64-bit Gold Codes has a greater probability of recovering the data due to the longer chip length. Analysis has shown that in order to avoid more than one false correlation in one "day" of use, the maximum number or errors allowed in a 64-bit code is ten, and for 32-bit codes it is one. Tolerance to errors can be improved through the use of error correction techniques implemented in firmware. Also there are twice as many 64 bit Gold Codes as there are 32-bit Gold Codes. (There are about fifty 64-bit Gold Codes that can be used by WirelessUSB LS.)

## Frequency Division Multiple Access

WirelessUSB LS not only separates transmissions by code, it also separates transmissions by frequency. WirelessUSB LS divides the 2.4-GHz ISM band into 79 distinct frequency channels. This allows devices to transmit distinct signals by either using a unique pseudo noise code or a unique frequency. Two signals will not interfere unless they are using the same frequency channel and the same pseudo noise code. Observe that signals A and B in *Figure 4* use the same Gold Code but transmit on different frequencies, while signals C and D transmit on the same frequency but use different Gold Codes. Theoretically, hundreds of WirelessUSB LS devices could be operating in the same physical space at the same time.

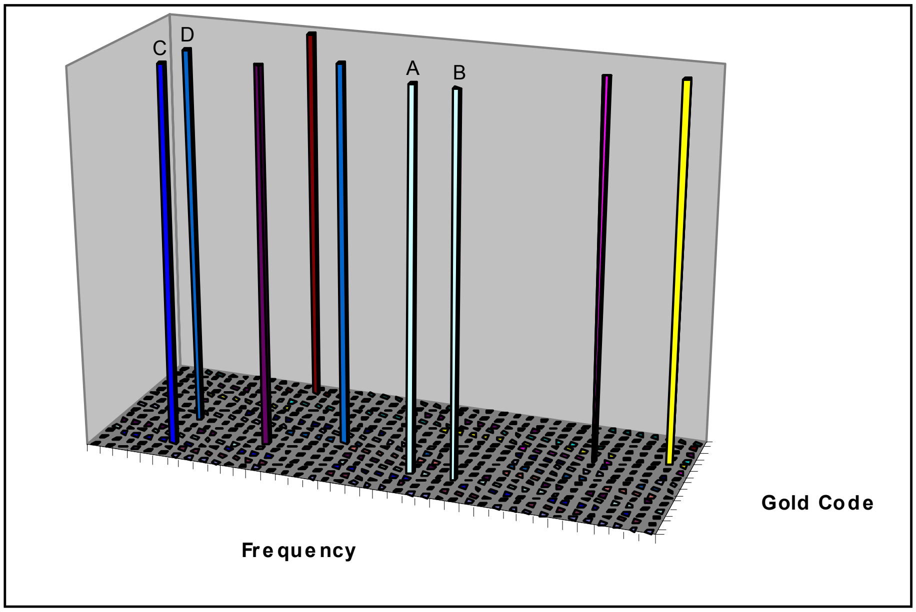


Figure 4. Frequency – Pseudo Noise Code Combination

## WirelessUSB LS Systems

There are two varieties of WirelessUSB LS devices: transmit-only devices and transceiver devices. Transmit-only HID devices are used in 1-Way WirelessUSB LS networks, while transceiver HID devices are used in 2-Way WirelessUSB LS networks. Bridge devices always use the WirelessUSB LS transceiver. The current 1-Way and 2-Way WirelessUSB LS HID protocols are targeted at 1-to-1 and 2-to-1 networks. The protocol is executed in external Microcontrollers that interface to the WirelessUSB-LS Chip. Many other applications including non-HID and N:1 HID applications can easily be implemented with WirelessUSB LS, but different protocols may be more applicable.

### WirelessUSB LS 1-Way HID Networks

WirelessUSB LS 1-Way networks utilize a communication protocol that emphasizes transmitter simplicity and is an ideal low cost, low power wireless solution for HID applications. Each HID device contains a WirelessUSB LS transmitter while bridges contain a WirelessUSB LS transceiver as shown in *Figure 5*. For more information please read *WirelessUSB LS 1-Way HID Networks*.

### WirelessUSB LS 2-Way HID Systems

WirelessUSB LS 2-Way networks contain a back channel allowing a HID to receive messages from the bridge. This back channel allows WirelessUSB LS 2-Way HIDs to establish a connection to the bridge, receive Ack/Nak messages from the bridge and receive Data messages from the bridge. All devices in WirelessUSB LS 2-Way networks contain transceivers as shown in *Figure 6*. For more information please read *WirelessUSB LS 2-Way HID Networks*.

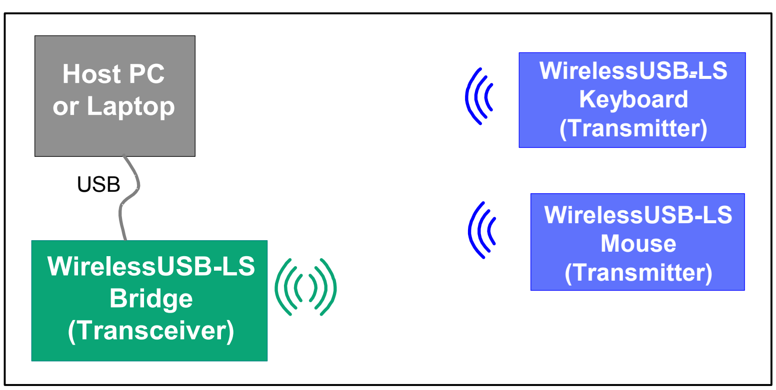


Figure 5. 1-Way WirelessUSB LS HID System

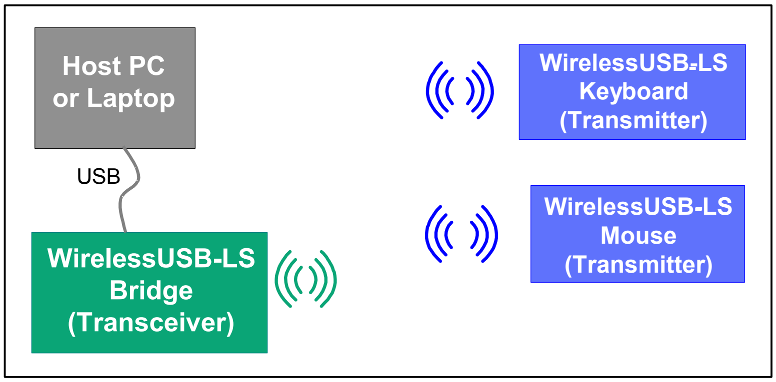


**Figure 6. 2-Way WirelessUSB LS HID System**

### Other WirelessUSB LS Non-HID Systems

- Non-HID applications may benefit from customized protocols specifically designed for each network.
- Non-HID networks could use a polling scheme to reduce the amount of overlapping HID transmissions. WirelessUSB LS is flexible and robust enough to be used in a variety of environments including barcode scanners, Point of Sale (POS) terminals, TV remotes, and wireless gamepads with rumble packs.

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Approved AN033_B 8/19/03 kkv

# WirelessUSB™ PRoC™ Flash Programmable MCU + Radio

## Features

- Microcontroller with Mixed Signal Array
  - Cypress M8C CPU
  - CPU clock up to 12 MHz
  - Internal oscillator—no crystal required
  - 8-KB Flash Program Memory with EEPROM emulation
  - 512 Bytes SRAM Data Storage
  - 4 Analog Blocks Provide:
    - 2 Comparators with DAC Refs
    - Two ADCs with
    - 10-bit resolution
  - 4 Digital Blocks Provide:
    - 8- to 32-bit Timers, Counters, and PWMs
    - CRC and PRS modules
    - Full-Duplex UART, SPI Master or Slave
    - Connectable to all GPIO pins
  - 18 GPIO lines which are individually configurable. P0 [1:0], P1[7:0], P2[7:0]
- 2.4-GHz DSSS radio transceiver
  - Operates in the unlicensed Industrial, Scientific and Medical (ISM) band (2.4 GHz –2.483 GHz)
  - –95 dBm receive sensitivity
  - Up to 0 dBm output power
  - Range of up to 50 meters or more
  - Data throughput of up to 62.5 kbits/sec
  - Highly integrated low cost, minimal number of external components required
  - DSSS baseband controller
  - 13-MHz crystal clock
  - Integrated 30-bit Manufacturing ID
- Operating voltage from 2.7V to 3.6V
- Operating temperature from 0° to 70°C
- Offered in a small footprint 48 QFN

## Applications

- Consumer/PC
  - Locator Alarms
  - Presenter Tools
  - Remote Controls
  - Toys
  - White Goods
- Building/Home Automation
  - Climate Control
  - Lighting Control
  - Smart Appliances
  - On-site Paging Systems
  - Alarm and Security
- Industrial Control
  - Inventory Management
  - Factory Automation
  - Data Acquisition
  - Automatic Meter Reading (AMR)
- Transportation
  - Diagnostics
  - Remote Keyless Entry
- Medical

## Functional Description

The CYWUSB6953 WirelessUSB™ PRoC™ (Programmable Radio System-on-Chip) device is the world's first low-cost Flash programmable microcontroller with an integrated 2.4-GHz radio transceiver.

## PRoC Block Diagram

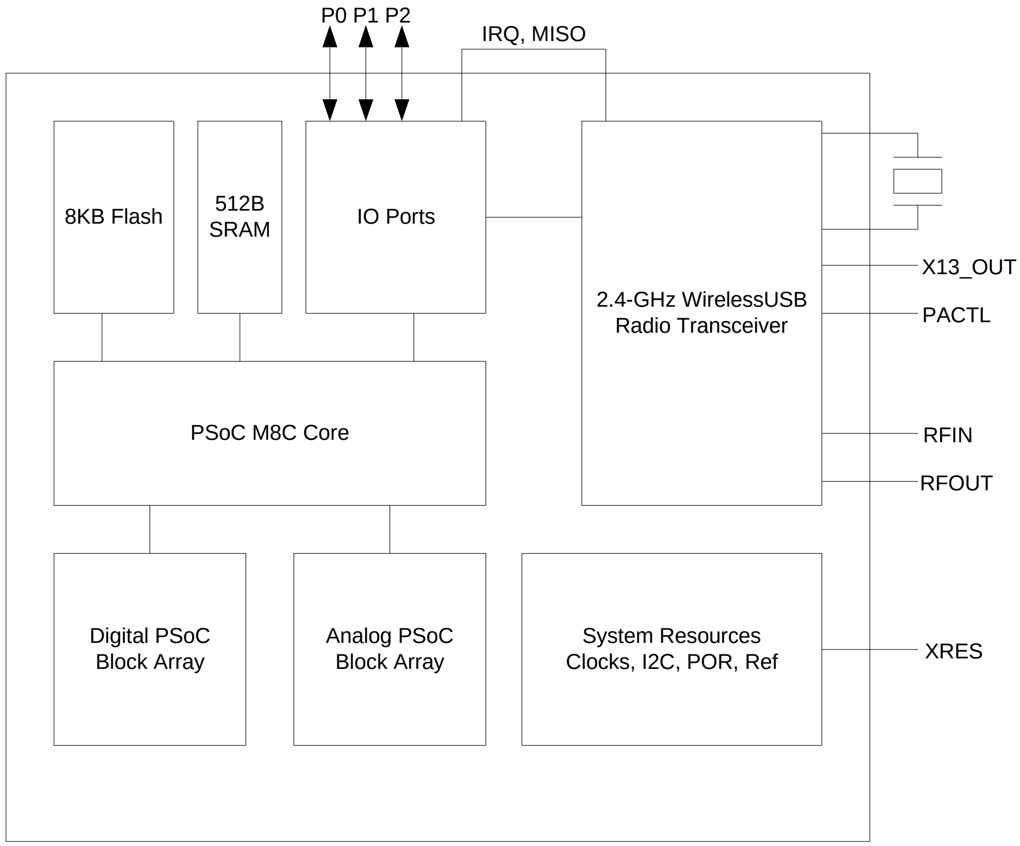



**Figure 1. PROC Block Diagram**

## Functional Overview

The CYWUSB6953 is a complete Radio System-on-Chip device, enabling many simple RF systems to be implemented with a single device and a handful of discrete components. The CYWUSB6953 is designed to implement low cost wireless systems operating in the worldwide 2.4-GHz Industrial, Scientific, and Medical (ISM) frequency band (2.400 GHz–2.4835 GHz).

The radio meets the following world-wide regulatory requirements:

- **Europe**
  - ETSI EN 301 489-1 V1.4.1
  - ETSI EN 300 328-1 V1.3.1
- **North America**
  - FCC CFR 47 Part 15
- **Japan**
  - ARIB STD-T66

The microcontroller is a powerful mixed-signal array. It has highly reconfigurable and flexible digital and analog blocks. The microcontroller core is the M8C 8-bit engine that supports a rich instruction set. It contains 512 Bytes of data SRAM and 8 Kbytes code Flash memory. Full data on the microcontroller can be found in the CY8C21534 data sheet and the PSoC™ Technical Reference Manual

The radio is a high-performance 2.4-GHz transceiver with a fully integrated DSSS baseband. The radio and baseband are both code and frequency agile. Protocols supporting frequency agile direct-spread interference avoidance algorithms such as WirelessUSB are fully compatible with this radio. Full data on the radio can be found in the CYWUSB6935 data sheet.

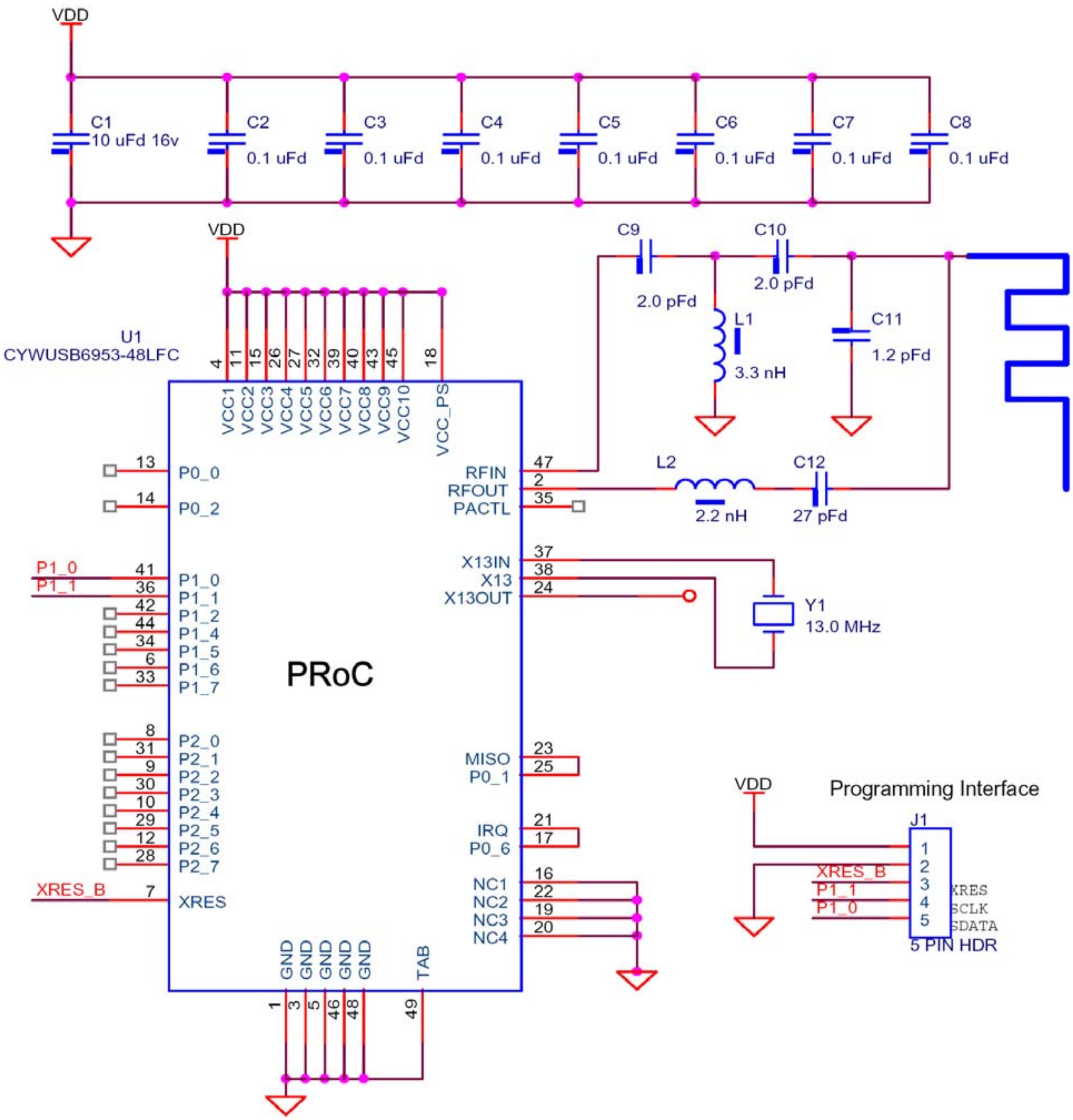
## Radio Data Rate Considerations

The PSoC Designer tool provides a software-based SPI User Module for control of the radio portion of the PRoC. Therefore, there is a direct relationship between CPU clock speed and supportable radio data rate. For operation of CPU clock rates less than 12 MHz, radio data rate must be set to 16 Kbps. Also note that for operation at $V_{CC} < 3.0V$, the CPU clock rate must be set to 3 MHz per the CY8C21534 data sheet. Therefore, at operation below 3V, the radio data rate must be set to 16 Kbps.

## Pin Descriptions

| Pin QFN | Name | Type | Die | Description |
|---|---|---|---|---|
| **Analog RF** | | | | |
| 47 | RFIN | | Radio | Modulated RF Signal Received |
| 2 | RFOUT | | Radio | Modulated RF Signal to be Transmitted |
| **Crystal/PA Control** | | | | |
| 38 | X13 | I | Radio | Crystal Input |
| 37 | X13IN | I | Radio | Crystal Input |
| 24 | X13OUT | O | Radio | Reference Clock Output |
| 35 | PACTL | IO | Radio | External Power Amplifier Control. Pull-down or make output |
| **Reserved** | | | | |
| 23, 25 | MISO | IO | Radio, MCU | Radio SPI Master In, Slave Out. Connect pins 23 and 25 on the application board |
| 17, 21 | IRQ | IO | Radio, MCU | Radio Interrupt. Connect pins 17 and 21 on the application board |
| **Microcontroller Digital/Analog** | | | | |
| 13 | P0[0] | IO/M | MCU | Analog Column Mux Input |
| 14 | P0[2] | IO/M | MCU | Analog Column Mux Input |
| 41 | P1[0] | IO/M | MCU | I2C Serial Data (SDA) |
| 36 | P1[1] | IO/M | MCU | I2C Serial Clock (SCL) |
| 42 | P1[2] | IO/M | MCU | |
| 44 | P1[4] | IO/M | MCU | Optional External Clock Input (EXT-CLK) |
| 34 | P1[5] | IO/M | MCU | I2C Serial Data (SDA) |
| 6 | P1[6] | IO/M | MCU | |
| 33 | P1[7] | IO/M | MCU | I2C Serial Clock (SCL) |
| 8 | P2[0] | IO/M | MCU | Direct Switched Capacitor Block Input |
| 31 | P2[1] | IO/M | MCU | Direct Switched Capacitor Block Input |
| 9 | P2[2] | IO/M | MCU | Direct Switched Capacitor Block Input |
| 30 | P2[3] | IO/M | MCU | Direct Switched Capacitor Block Input |
| 10 | P2[4] | IO/M | MCU | |
| 29 | P2[5] | IO/M | MCU | |
| 12 | P2[6] | IO/M | MCU | |
| 28 | P2[7] | IO/M | MCU | |
| 7 | XRES | I | MCU | Active HIGH External Reset with Internal Pull-down |
| **Power and Ground** | | | | |
| 4, 11, 15, 18, 26, 27, 32, 39, 40, 43, 45 | $V_{CC}$ | | | Supply Voltage |
| 1, 3, 5, 46, 48 | GND | | | Ground Connection |
| PADDLE | GND | | | Ground Connection |
| 19, 20 | RSVD | | | Connect to Ground |
| 16, 22, | NC | | | No Connect |

## Application Example



## PRoC Absolute Maximum Ratings

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | –55 | | 100 | °C |
| $T_A$ | Ambient Temperature with Power Applied | 0 | | 70 | °C |
| $V_{dd}$ | Supply Voltage on $V_{CC}$ Relative to VSS | –0.3 | | 3.9 | V |
| $V_{IO}$ | DC Voltage to Logic Inputs | –0.3 | | $V_{CC}$ + 0.3 | V |
| $V_{IOZ}$ | DC Voltage Applied to Outputs in High-Z State | –0.3 | | $V_{CC}$ + 0.3 | V |
| $I_{MIO}$ | Maximum Current into Any Port Pin | –25 | | 50 | mA |
| ESD | Electrostatic Discharge Voltage (Other) | | | 1600 | V |
| $I_{LU}$ | Latch-up Current | | | 200 | mA |

## PRoC Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 3 | 3.6 | V |
| TA | Ambient Temperature | 0 | 25 | 70 | °C |

## PRoC DC Electrical Characteristics

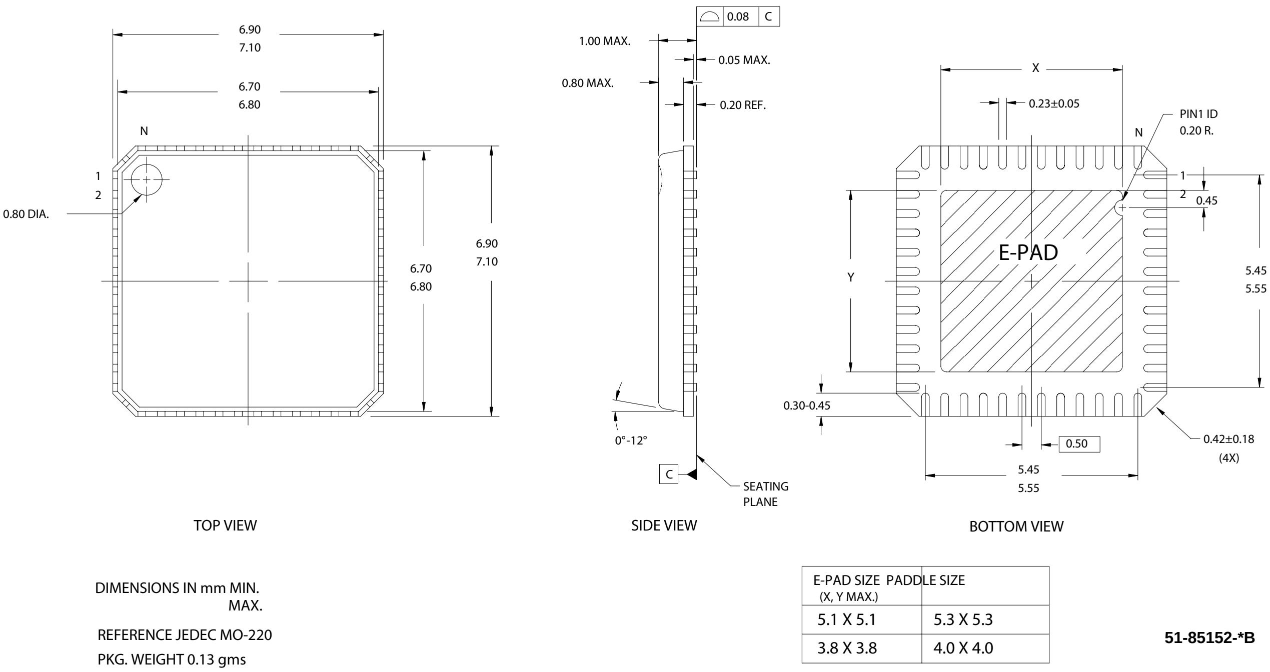
| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 3 | 3.6 | V |
| $I_{CC}$ | Supply Current (Radio in Power Down) | | 1.7 | 2 | mA |
| RX $I_{CC}$ | Supply Current Radio Receive | | 61.3 | | mA |
| TX $I_{CC}$ | Supply Current Radio Transmit | | 74.7 | | mA |
| SYNTH SETTLE $I_{CC}$ | Current Consumption with Synthesizer on, No Transmit or Receive | | 33.0 | | mA |
| IDLE $I_{CC}$ | Supply Current Radio Idle | | 5 | | mA |
| $I_{SLEEP}$ | Sleep Mode Supply Current | | 3 | 20 | µA |

## Ordering Information

| Part Number | Radio | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| CYWUSB6953-48LFXC | Transceiver | 48 QFN | Pb-Free 48 Quad Flat No Lead Package | Commercial |

## Package Diagram

### 48-Lead QFN 7 × 7 mm LF48A




| E-PAD SIZE (X, Y MAX.) | PADDLE SIZE |
|---|---|
| 5.1 X 5.1 | 5.3 X 5.3 |
| 3.8 X 3.8 | 4.0 X 4.0 |

51-85152-*B

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## Document History Page

| REV. | ECN No. | Issue Date | Orig. of Change | Description of Change |
|---|---|---|---|---|
| **Document Title: CYWUSB6953 WirelessUSB™ PRoC™ Flash Programmable MCU + Radio<br>Document Number: 38-16017** | | | | |
| ** | 329973 | See ECN | BON | New data sheet |
| *A | 337935 | See ECN | BON | In the Feature Section, changed “90 dBm receive sensitivity” to “– 90 dBm receive sensitivity”, and “13 MHz crystal clock” to “13 MHz crystal clock”<br>In the Functional Overview, changed “CYWUSB6934” to “CYWUSB6935”<br>In the Application Example, changed “ISSP” to “Programming Interface” |
| *B | 380254 | See ECN | BON | Updated the PRoC DC Electrical Characteristics. Changed “– 90 dBm receive sensitivity” to “– 95 dBm receive sensitivity” in the Feature section. Removed lead-free part offering. Changed supported CPU clock from 24 MHz to 12 MHz |
| *C | 392781 | See ECN | BON | Added the Radio Data Rate Considerations section |
| *D | 495870 | See ECN | OYR | Took off the photograph of the chip from the first page<br>Added Pb-free part numbers<br>Took off parts with lead<br>Quad flat package to QFN<br>Named Variables in Table |

## Applications

- Portable WLAN – Cell phones, PDA's
- DSSS 2.4 GHz WLAN (IEEE802.11b)
- OFDM 2.4 GHz WLAN (IEEE802.11g)

## Features

- Includes: PA, 50 ohm matching, Power detector, harmonic filter and SPDT Switch.
- 802.11g Output Power
  + 17 dBm, EVM = 3.0 %, $I_{CC}$ = 125 mA
  802.11b Output Power
  + 19 dBm, ACPR = -40 dBr, $I_{CC}$ = 150 mA
- 28 dB Gain
- Robust, selectable slope, power detector with ~1.5 dB variation over 2:1 mismatch
- Integrated power amplifier enable pin ($V_{EN}$)
- Single supply voltage: 2.7 V to 3.6 V
- Lead free and RoHs compliant
- Small, lead free package, 18 pin 4 mm x 4.5 mm x 0.6 mm QFN, MSL3

## Ordering Information

| Type | Package | Remark |
|---|---|---|
| SE2550BL | 18-QFN | Samples |
| SE2550BL-R | 18-QFN | Tape and Reel |
| SE2550BL-EK1 | Evaluation Kit | Standard |

## Product Description

The SE2550BL is a 2.4 GHz front end module designed for use in the 2.4 GHz ISM band for portable wireless LAN applications. The device offers high efficiency at the required output powers to ensure longer battery life for cellphone, PDA and other portable applications.

The SE2550BL is highly integrated, allowing for a smaller footprint and simple design. The device includes a power amplifier, digital enable control for device on/off control, T/R Switch, harmonic filter and 50 ohm matching on all I/O. With the digital enable control, the device can be directly connected to a CMOS baseband or transceiver.

The SE2550BL temperature compensated power detector has two selectable power detectors slopes, positive and negative. This allows easy use with multiple chipsets. The detector is also highly immune to mismatch at its output with less than 1.5 dB of variation with a 2:1 mismatch.

## Functional Block Diagram

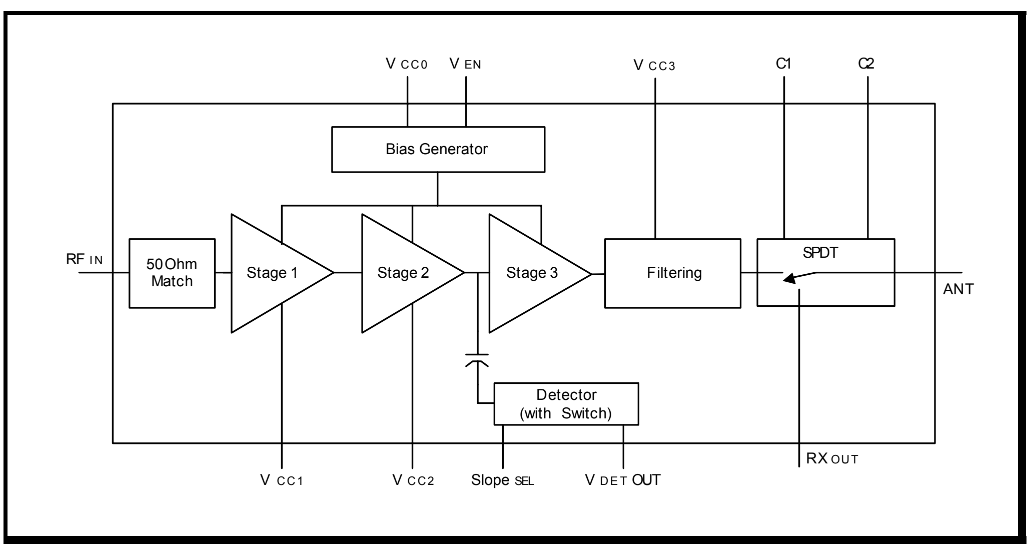



**Figure 1: SE2550BL Functional Block Diagram**

## Pin Out Diagram

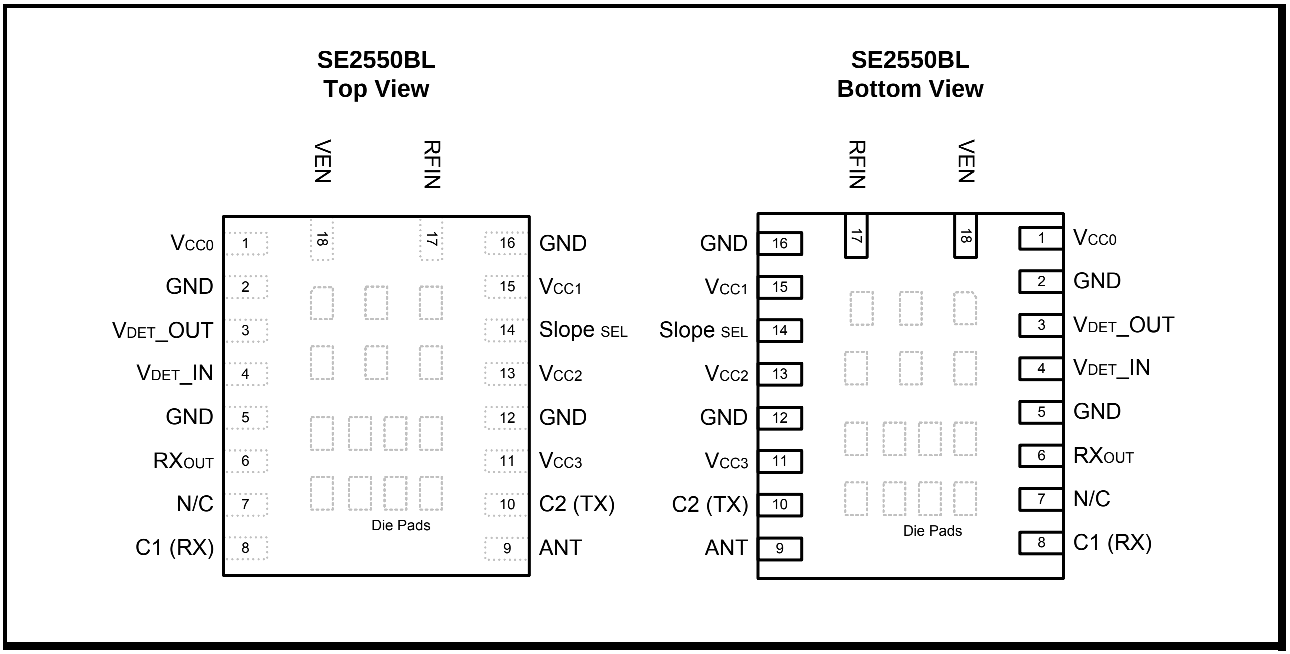



**Figure 2: SE2550BL Pin-Out Diagram**

## Pin Out Description

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{CC0}$ | Bias/Control Circuit Supply Voltage |
| 2 | GND | Ground |
| 3 | $V_{DET}$_OUT | Power Detector Output |
| 4 | $V_{DET}$_IN | Power Detector Input (Should be connected to GND to use internal coupled detector) |
| 5 | GND | Ground |
| 6 | $RX_{OUT}$ | Receive Output |
| 7 | N/C | No Connect (Do not attach to Ground) |
| 8 | C1 (RX) | Receive Switch Control |
| 9 | ANT | Antenna |
| 10 | C2 (TX) | Transmit Switch Control |
| 11 | $V_{CC3}$ | Stage 3 Collector Supply |
| 12 | GND | Ground |
| 13 | $V_{CC2}$ | Stage 2 Collector Supply |
| 14 | $Slope_{SEL}$ | Slope Select, N/C – Positive Slope, GND – Negative Slope |
| 15 | $V_{CC1}$ | Stage 1 Collector Supply |
| 16 | GND | Ground |
| 17 | $RF_{IN}$ | RF Input |
| 18 | $V_{EN}$ | Digital Pin used to power up/down the power amplifier |
| 19 - 32 | GND | Die Pads |

## Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings for a long period of time may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This device is ESD sensitive. Handling and assembly of this device should be at ESD protected workstations.

| Symbol | Definition | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage on pins $V_{CC0}$, $V_{CC1}$ $V_{CC2}$ and $V_{CC3}$ | -0.3 | 4.0 | V |
| $V_{EN}$ | Power Amplifier Enable | -0.3 | 4.0 | V |
| $RF_{IN}$ | RF Input Power | - | -4 | dBm |
| $T_{STG}$ | Storage Temperature Range | -40 | +150 | °C |

## Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage on pins $V_{CC0}$, $V_{CC1}$,$V_{CC2}$ and $V_{CC3}$ | 2.7 | 3.6 | V |
| $T_A$ | Ambient Temperature | -10 | 85 | °C |

## DC Electrical Characteristics

Conditions: $V_{CC}$ = $V_{EN}$ = 3.3 V, $T_A$ = 25 °C, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CC-802.11g}$ | Supply Current | $P_{OUT}$ = 17 dBm, 54 Mbps OFDM signal, 64 QAM | - | 125 | - | mA |
| | | $P_{OUT}$ = 15 dBm, 54 Mbps OFDM signal, 64 QAM | - | 110 | - | mA |
| $I_{CC-802.11b}$ | Supply Current | $P_{OUT}$ = 19 dBm, 11 Mbps CCK signal, BT = 0.45 | - | 150 | - | mA |
| | | $P_{OUT}$ = 17 dBm, 11 Mbps CCK signal, BT = 0.45 | - | 125 | - | mA |
| $I_{OFF}$ | Supply Current | $V_{EN}$ = 0 V | - | - | 10 | µA |
| $V_{ENH}$ | Logic High Voltage | - | 1.3 | - | $V_{CC}$ | V |
| $V_{ENL}$ | Logic Low Voltage | - | 0 | - | 0.5 | V |

## AC Electrical Characteristics

Conditions: $V_{CC} = V_{EN}$ = 3.3 V, f = 2.45 GHz, $T_A$ = 25 °C, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{L-U}$ | Frequency Range | - | 2400 | - | 2500 | MHz |
| $P_{1dB}$ | Output 1dB compression point | No modulation | - | 25 | - | dBm |
| $S_{21}$ | Small Signal Gain | $P_{IN}$ = -25 dBm | - | 28 | - | dB |
| $\Delta S_{21}$ | Gain Variation over band | $P_{IN}$ = -25 dBm, $f_{IN}$= 2400 to 2500 MHz | - | 2 | - | dB |
| 2f | Harmonic | $P_{OUT}$ = 17 dBm, 802.11b 1 Mbps CCK signal | - | - | -42 | dBm/MHz |
| 3f | | | - | - | -42 | dBm/MHz |
| EVM | Error Vector Magnitude | $P_{OUT}$ = 17 dBm, 54 Mbps OFDM signal, 64 QAM | - | 3.0 | - | % |
| ACPR | Adjacent Channel Power Ratio<br>±11 MHz offsets from carrier<br>±22 MHz offsets from carrier | $P_{OUT}$ = 19 dBm, 11 Mbps CCK signal, BT = 0.45 | - | -40<br>-60 | - | dBr |
| | | $P_{OUT}$ = 20 dBm, 11 Mbps CCK signal, BT = 0.45 | - | -38<br>-55 | - | |
| STAB | Stability | $P_{OUT}$ = 17 dBm, 54 Mbps OFDM signal, 64 QAM VSWR = 4:1 All Phases | All non-harmonically related outputs less than -50 dBc/100 kHz | | | |
| VSWR | Tolerance to output load mismatching | $P_{OUT}$ = 17 dBm, 54 Mbps OFDM signal, 64 QAM VSWR = 6:1 All Phases | No damage | | | |

## Receive Characteristics

Conditions: $V_{CC}$ = $V_{EN}$ = 3.3 V, $T_A$ = 25 °C, de-embedded data, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted. RF ports terminated with 50 Ω, $SW_{ON}$ = 2.5 V is the control voltage for each ON path, $SW_{OFF}$ = 0.0 V is the control voltage for each OFF path.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Frequency Range | - | 2400 | | 2500 | MHz |
| $RX_{IL}$ | Insertion Loss | - | - | 0.8 | 1.2 | dB |
| $RX_{RL}$ | Return Loss | - | - | -10 | - | dB |
| $RX_{ISOL}$ | TX to RX Isolation | Any 1 or 2 switches in the $SW_{ON}$ State | 13 | 18 | - | dB |

## Switch Control Logic Table

| C1 | C2 | $RX_{OUT}$ – ANT | $RF_{IN}$ – ANT |
|---|---|---|---|
| $SW_{ON}$ | $SW_{OFF}$ | ON | OFF |
| $SW_{OFF}$ | $SW_{ON}$ | OFF | ON |

## Switch Characteristics

Conditions: $V_{CC}$ = $V_{EN}$ = 3.3 V, $T_A$ = 25 °C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CTL\_ON}$ | Control Voltage (On State) | - | 2.5 | - | 3.6 | V |
| $V_{CTL\_OFF}$ | Control Voltage (OFF State) | - | 0.0 | - | 0.5 | V |
| $SW_{ON}$ | Low Loss Switch Control Voltage | High State = $V_{CTL\_ON}$ - $V_{CTL\_OFF}$ | 2.5 | - | $V_{CC}$ | V |
| $SW_{OFF}$ | High Loss Switch Control Voltage | Low State = $V_{CTL\_OFF}$ - $V_{CTL\_OFF}$ | 0 | - | 0.3 | V |
| $I_{CTL\_ON}$ | Switch Control Bias Current (RF Applied) | On pin (C1, C2) being driven high. RF Applied | - | - | 100 | µA |
| $I_{CTL\_ON}$ | Switch Control Bias Current (No RF) | On pin (C1, C2) being driven high. No RF | - | - | 30 | µA |
| $C_{CTL}$ | Control Input Capacitance | - | - | - | 100 | pF |

## Power Detector

### *Positive Slope*

Conditions: $V_{CC} = V_{EN}$ = 3.3 V, f = 2.45 GHz, $Slope_{SEL}$ = N/C, $V_{DET}$_IN = GND, $T_A$ = 25 °C, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PDR | $P_{OUT}$ detect range | - | 0 | | $P_{1dB}$ | dBm |
| VDET | Detector voltage | $P_{OUT}$ = NO RF | - | 0.35 | - | V |
| VDET | Detector voltage | $P_{OUT}$ = 17 dBm | - | 0.70 | - | V |
| VDET | Detector voltage | $P_{OUT}$ = 19 dBm | - | 0.85 | - | V |
| $PDZ_{OUT}$ | Output Impedance | - | 250 | - | 700 | Ω |
| $PDZ_{LOAD}$ | DC load impedance | - | 10 | - | - | kΩ |

### *Negative Slope*

Conditions: $V_{CC} = V_{EN}$ = 3.3 V, f = 2.45 GHz, $Slope_{SEL}$ = GND, $V_{DET}$_IN = GND, $T_A$ = 25 °C as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDET | Detector voltage | $P_{OUT}$ = NO RF | - | 0.90 | - | V |
| VDET | Detector voltage | $P_{OUT}$ = 17 dBm | - | 0.55 | - | V |
| VDET | Detector voltage | $P_{OUT}$ = 19 dBm | - | 0.45 | - | V |

Note: Please refer to Figure 9 for proper external filtering for negative slope detector with certain chipsets.

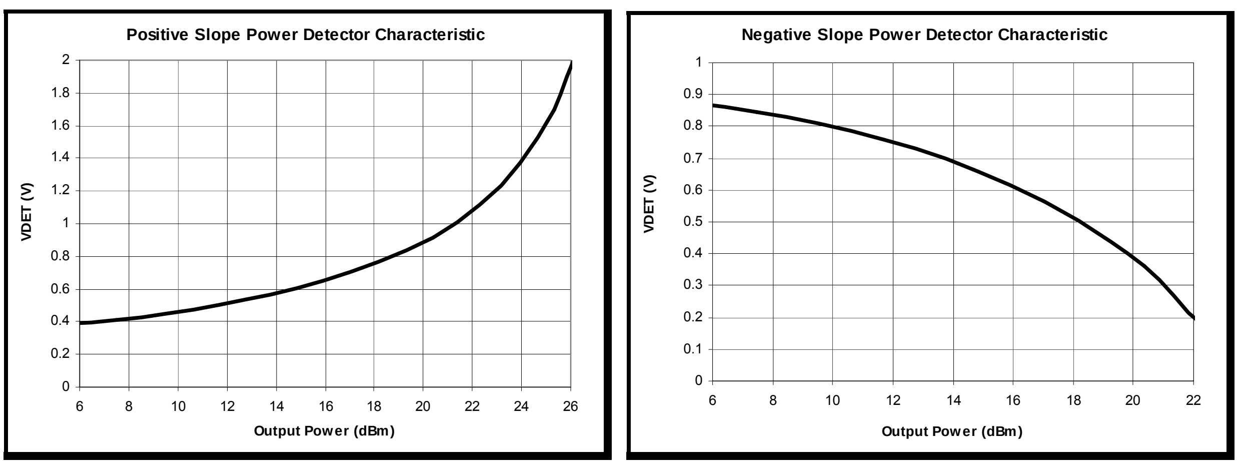



**Figure 3: SE2550BL Power Detector Characteristic**

## Detector Selection Logic

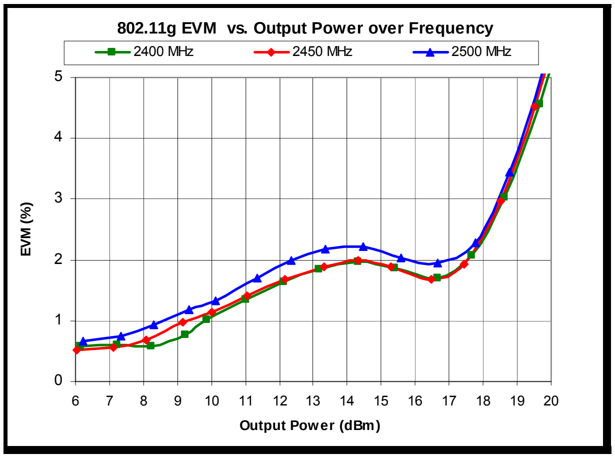
Conditions: $V_{CC} = V_{EN}$ = 3.3 V, $T_A$ = 25 °C, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board, unless otherwise noted

| $SLOPE_{SEL}$ | Detector Slope |
|---|---|
| Open Circuit | Positive |
| Ground | Negative |

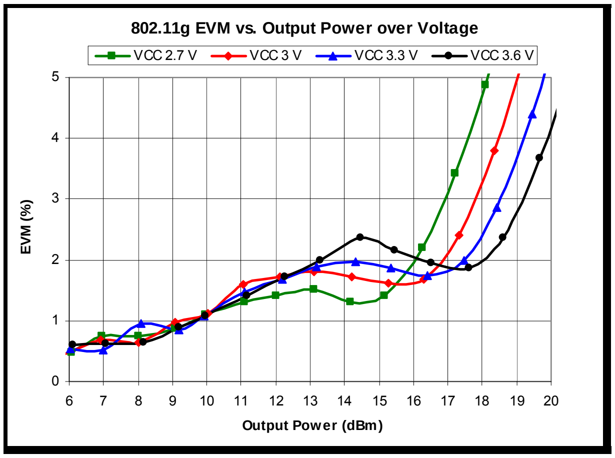
## Typical Performance

Conditions: $V_{CC} = V_{EN}$ = 3.3 V, Frequency = 2450 MHz, $T_A$ = 25 °C, as measured on SiGe Semiconductor's SE2550BL-EV1 evaluation board , all unused ports terminated with 50 ohms, unless otherwise noted.

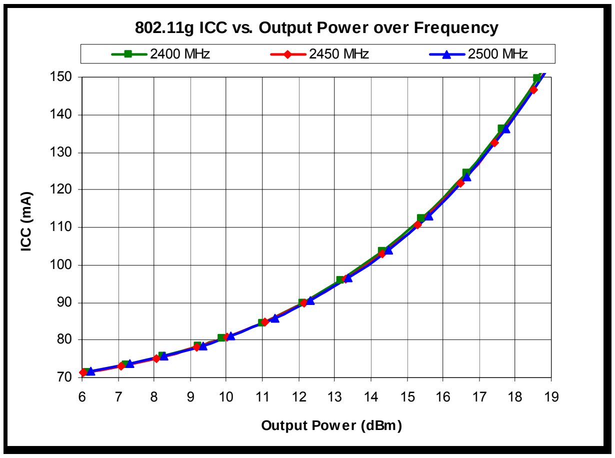
### *802.11g Typical Performance*




**(a)**



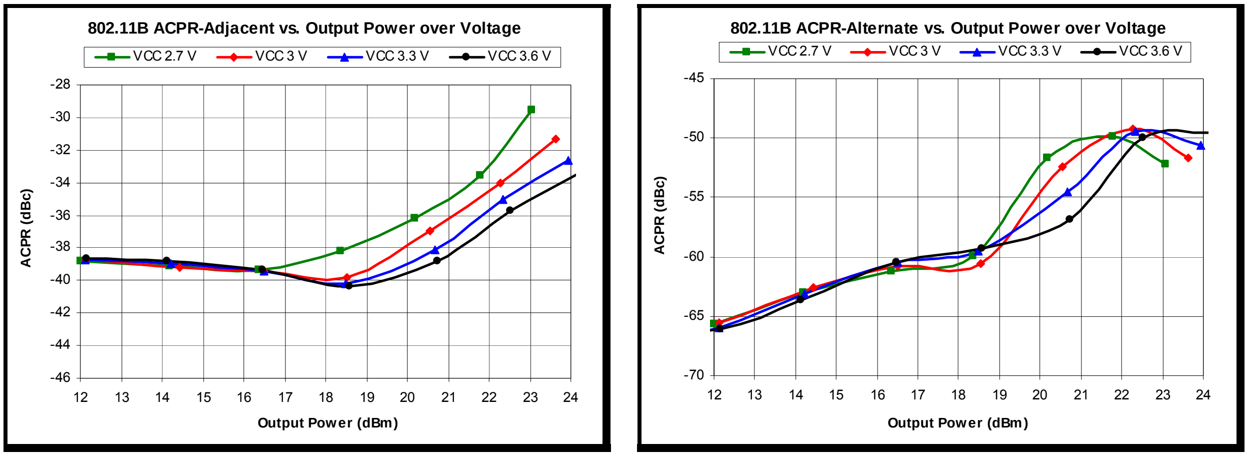

**(b)**




**(c)**

**Figure 4: Typical 802.11g Performance: (a) EVM vs. Output Power over Frequency, (b) EVM vs. Output Power over Voltage, (c) ICC vs. Output Power over Frequency**

### *802.11b Typical Performance*




**(a)** **(b)**

**Figure 5: 802.11b Typical Performance (11 Mbps, CCK): (a) Adjacent Channel (ACPR-1) vs. Pout over Voltage, (b) Alternate Channel (ACPR-2) vs. Output Power over Voltage**

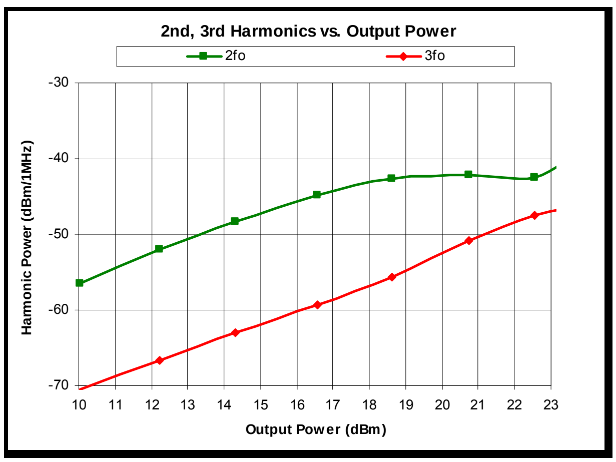



**Figure 6: Harmonic Performance (802.11b 1 Mbps, CCK signal): 2nd, 3rd Harmonic vs. Output Power**

### *Power Detector Performance*

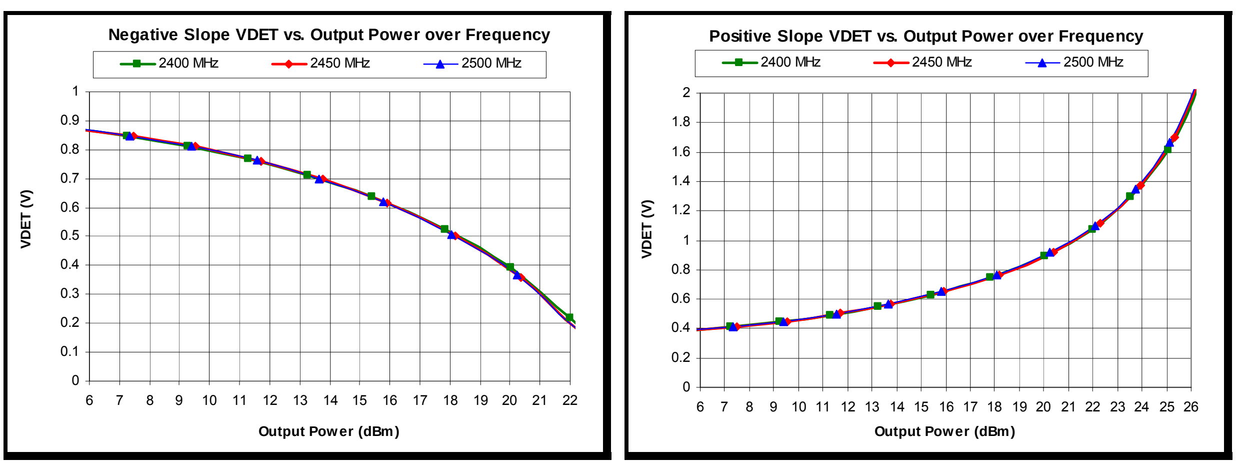
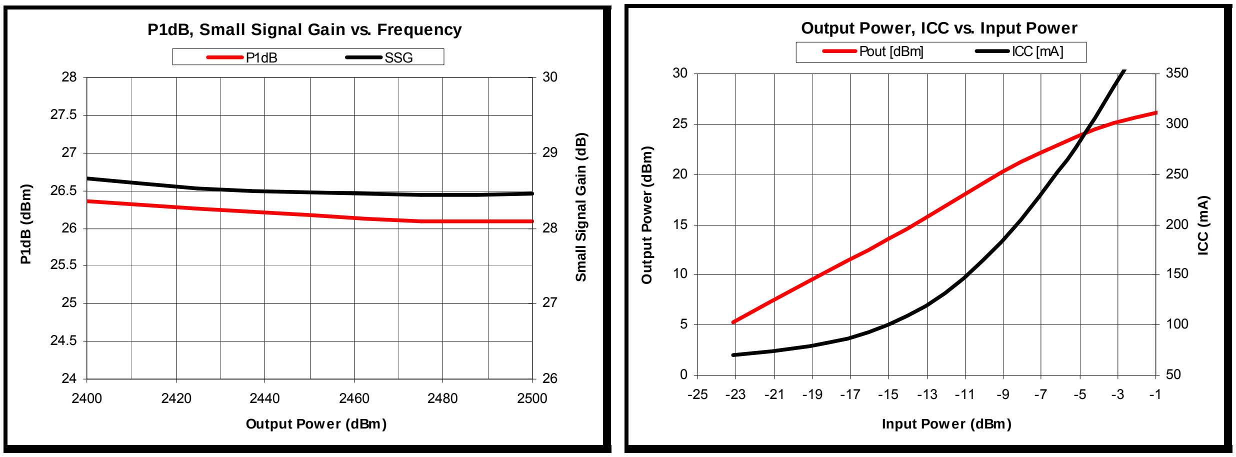



**Figure 7: Typical Power Detector Performance over Frequency (a) Negative Slope, (b) Positive Slope**

### *CW Typical Performance*




**(a)** **(b)**

**Figure 8 (a) P1dB, Small Signal Gain vs. Frequency (b) Output Power, ICC vs. Input Power**

## Application Circuit

Figure 9 shows the typical SE2550BL application circuit.

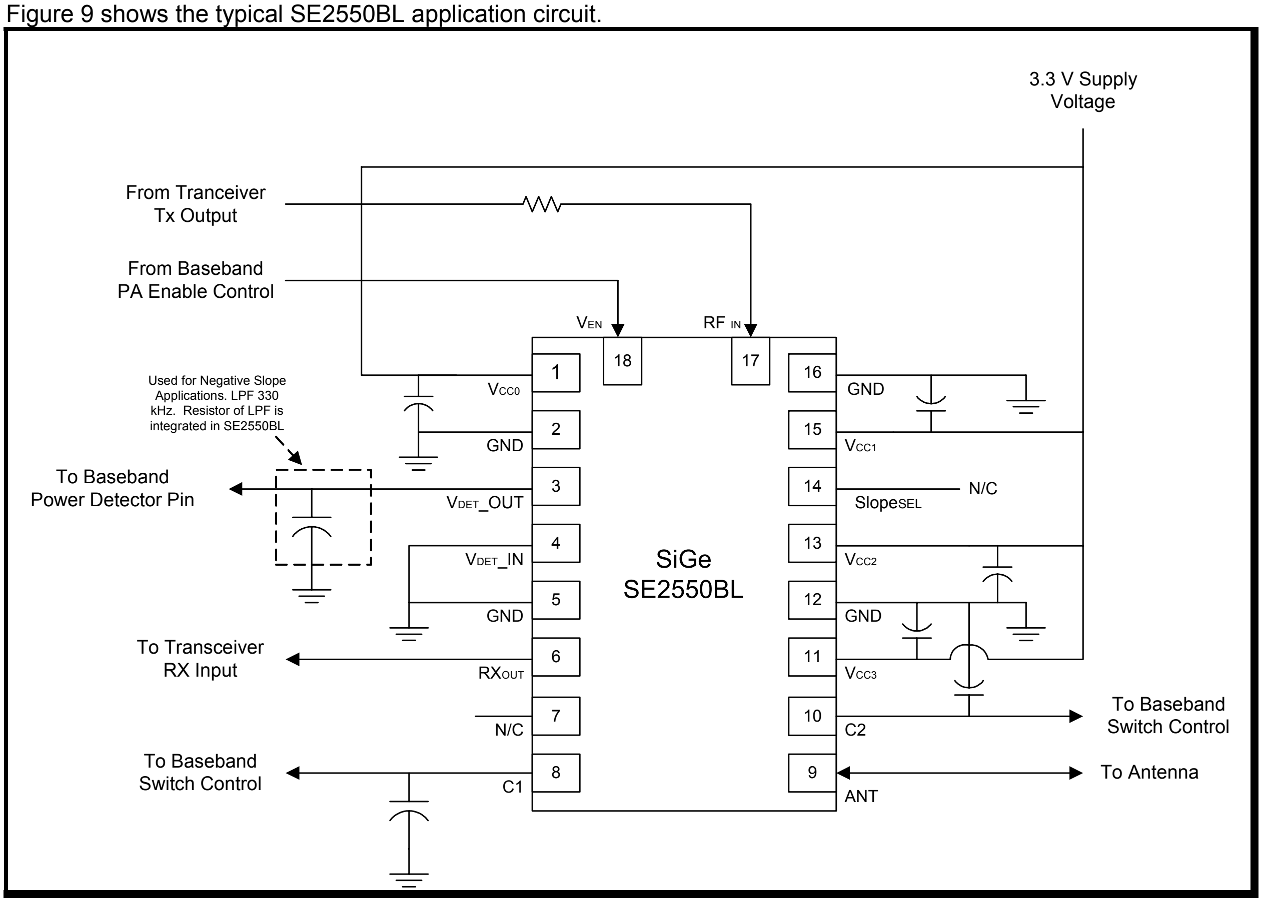
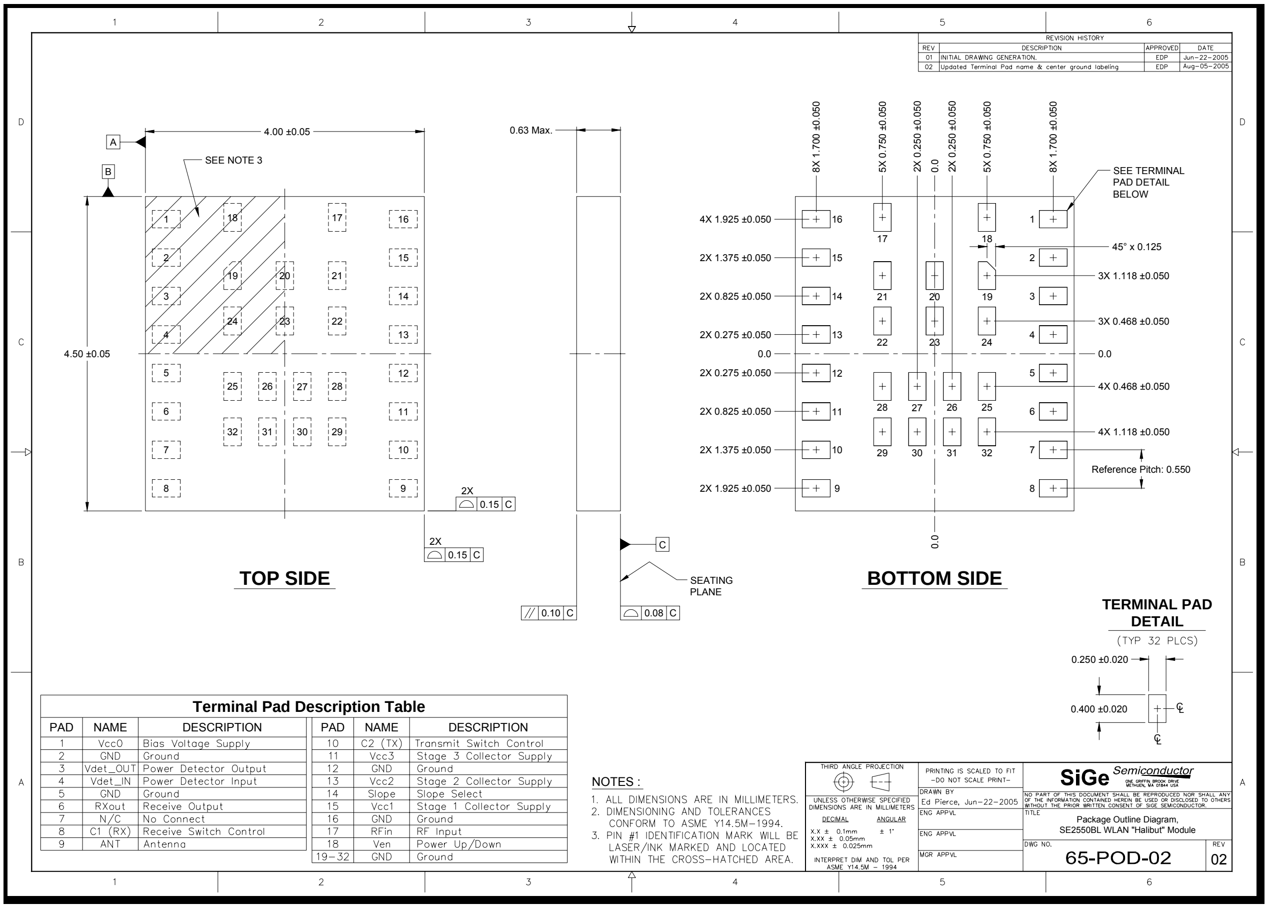



**Figure 9: SE2550BL Typical Application Circuit**

## Package Information

Figure 10 is the SE2550BL package drawing. The SE2550BL is lead free.




**Terminal Pad Description Table**

| PAD | NAME | DESCRIPTION | PAD | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | Vcc0 | Bias Voltage Supply | 10 | C2 (TX) | Transmit Switch Control |
| 2 | GND | Ground | 11 | Vcc3 | Stage 3 Collector Supply |
| 3 | Vdet_OUT | Power Detector Output | 12 | GND | Ground |
| 4 | Vdet_IN | Power Detector Input | 13 | Vcc2 | Stage 2 Collector Supply |
| 5 | GND | Ground | 14 | Slope | Slope Select |
| 6 | RXout | Receive Output | 15 | Vcc1 | Stage 1 Collector Supply |
| 7 | N/C | No Connect | 16 | GND | Ground |
| 8 | C1 (RX) | Receive Switch Control | 17 | RFin | RF Input |
| 9 | ANT | Antenna | 18 | Ven | Power Up/Down |
| | | | 19-32 | GND | Ground |

**Figure 10: SE2550BL Package Drawing**

## Branding Information

Figure 11 is the SE2550BL branding diagram.

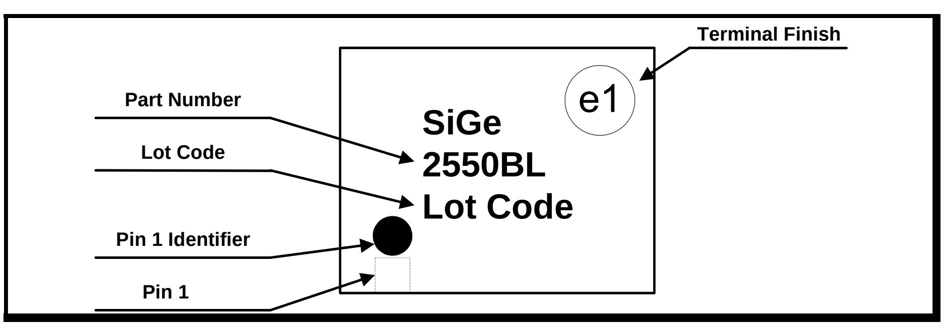



**Figure 11: SE2550BL Branding Diagram**

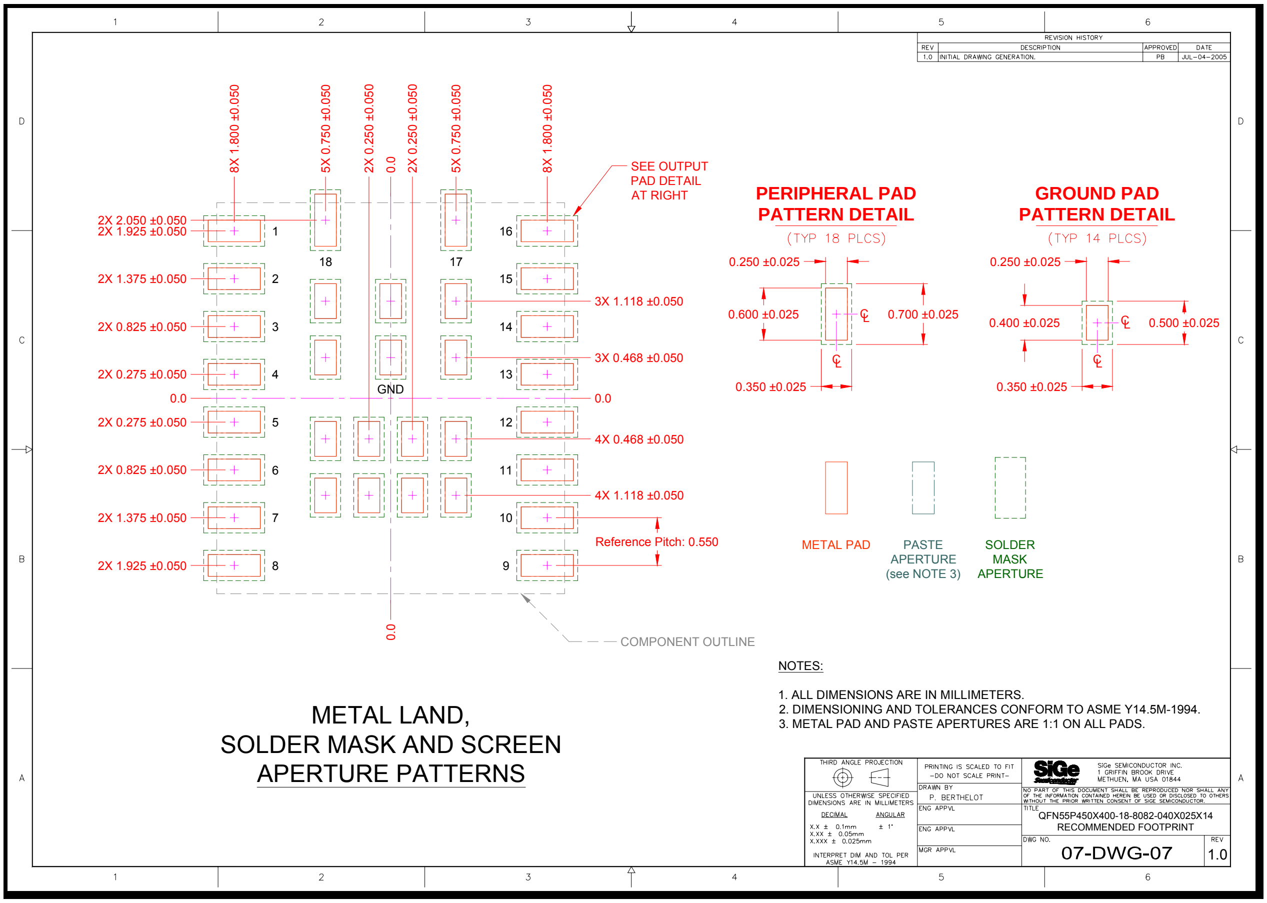



**Figure 12: SE2550BL Recommended PCB Footprint**

## Tape and Reel

Production quantities of this product are shipped in a standard tape-and-reel format. Specific tape and reel dimensions and sizing is shown in Table 1 and Figure 13.

| Parameter | Value |
|---|---|
| Devices Per Reel | 2500 |
| Reel Diameter | 13 inches |

**Table 1: Tape and Reel Dimensions**

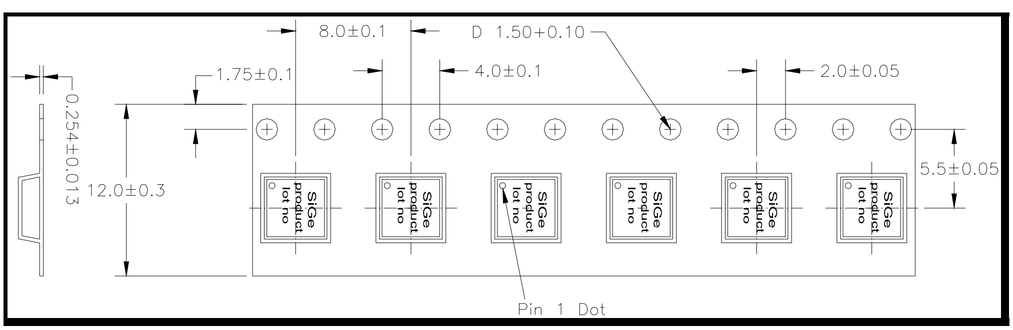



**Figure 13: SE2550BL Tape and Reel Information**

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