CIRCUIT & DEVICE DESCRIPTIONS

PARA. 2.1033 (b)(4), (c)(10)

(10) FREQUENCY STABILIZATION

A temperature compensated crystal oscillator (N1402) provides a 19.44 MHz reference frequency signal for the transmitter and receiver frequency synthesizers. This reference frequency is internally compensated to be within ±2.5 ppm over the temperature range of -30°C to +75° C. Upon power-up, the receiver searches and acquires a base station signal, and it adjusts the reference oscillator frequency to align itself to the high accuracy time base of the base station. The transmitter does not engage until after the receiver synchronizes to the base station.

(11a) ATTENUATION OF SPURIOUS EMISSIONS

The 800 MHz band transmitter frequency is obtained from mixing a phase locked VCO operating from 979.53 MHz to 1004.49 MHz with a 155.52 MHz signal. The 155.52 MHz signal is obtained by phase locking an oscillator to the VCTCXO output.

The 800 MHz band receiver frequency is obtained by dual conversion. The first conversion is obtained by mixing the incoming signal with the 979.53 MHz to 1004.49 MHz VCO to a first IF frequency of 110.52 MHz. The second conversion mixes the IF frequency with a phase locked VCO at 110.4 MHz to obtain the second IF frequency of 120 kHz. All VCO's are phase locked to the reference VCTCXO.

As a result of the above circuitry, the spurious signals are transmitter harmonics, reference oscillator 19.44 MHz harmonics, the local oscillators and the microprocessor clock.

The use of multi-layer printed circuit boards, with signal tracks between ground planes, for the radio as well as for the logic areas reduces the radiation to a minimum. Ceramic resonator bandpass filters for the duplexer attenuate conducted transmitter harmonics, reference oscillator and local oscillator signals. A bandpass filter in the receiver front end attenuates the local oscillator signal further. Additional suppression of radiation is achieved by shielding and key isolation between circuits.

(11b) LIMITING MODULATION

The modulation for the transmitter is produced inside a Digital Signal Processing integrated circuit. The modulation limiting is therefore controlled by an algorithm inside this chip. The limit is preset at the factory and cannot be changed thereafter.

ATTENUATING HIGHER AUDIO FREQUENCIES

The DSP chip provides an audio filter with a 120 log (f/3000) response, f=3K to 20KHz. Manchester encoded data signals are filtered prior to transmission by a four-pole lowpass filter providing an attenuation of 24 dB/Octave above 20 kHz.

The signal produced by the DSP chip is a differentially shifted PI/4 QPSK signal for the digital system and a FM signal for the analog cellular system. These signals are fed through a three-pole lowpass filter with a 3 dB down cut-off frequency of 25 kHz to limit the adjacent channel energy in the digital mode.

CIRCUIT & DEVICE DESCRIPTIONS

PARA. 2.1033 (b)(4)

(11c) OUTPUT POWER CONTROL

A loop circuit under supervision of the logic sets the output to any of the eleven power levels.

A digital word is transmitted to the gain control amplifier for output power adjustment.

A detector at the output of the power amplifier module senses the RF energy present and sends a corresponding DC voltage to the digital logic circuitry.

Upon receiving a command to set power level from the handset or from a base station the microprocessor sends a predetermined word to the ALC amplifier. The output detector voltage is then read by the microprocessor and compared to a preset value. If the detector voltage is outside the allowed tolerance an adjustment is made to the gain-controlled amplifier to bring the detector voltage into the proper range.

(12) DIGITAL MODULATION TECHNIQUES

The NRZ data stream is transformed to 10kbps Manchester encoded data in such a way that each NRZ binary one is transformed to a zero-to-one transition, and each NRZ binary zero is transformed to a one-to-zero transition.

The Manchester encoded data stream is filtered before being applied to the modulator. Direct binary frequency shift keying is used. A binary one into the modulator corresponds to a normal peak frequency deviation of 8kHz above the carrier frequency and a zero corresponds to a nominal peak frequency deviation 8 kHz below the carrier frequency.

(12a) DESCRIPTION OF PI/4 DQPSK

The modulation method used for the digital mode is known as PI/4 shifted differentially encoded Quadrature Phase Shift Keying. Eight distinct phase states are possible. The signal information is differentially encoded; symbols are transmitted as changes in phase rather than absolute phases. Transition of phase which would result in a zero amplitude momentarily are not allowed.

CIRCUIT & DEVICE DESCRIPTIONS

PARA. 2.1033 (b)(4)

1.0 LOGIC BOARD OPERATION

The logic board is the central controller system for the radio. It is made up of a microprocessor, DSP, codec, memory, and control logic.

1.1 ASIC CONTROL CHIP – D401

The ASIC control chip is made up of a ARM microprocessor and application specific logic circuits. The chip is the main control center for the radio and provides interfaces to the DSP's, codec, memories, keypad, display, alarms, and system interfaces.

1.2 MEMORY CHIP'S

D501 is the 1M x 8 flash memory used to store the radio's operating algorithm. This part may be field programmed to allow new revisions of the operating algorithm to be installed without opening the radio case.

D502 is the 256k x 8 static RAM used for stack, and microprocessor operation.

D503 is the 32k x 8 electrically erasable programmable read only memory. The part stores all of the users phone numbers, any system parameters that change, and the power down status of the radio.

1.3 USER INTERFACE

There is a 30 pin system connector that provides input power, control signals, and the receive and transmit audio interfaces.

1.4 AUDIO INTERFACE

D701 codec will provide the necessary audio conversions from analog to digital and digital to analog for all user interfaces. The codec will provide all necessary filters, A to D and D to A control functions for the radio.

1.5 DIGITAL SIGNAL PROCESSING

D601 is the DSP and provides all signal conversion and error correction for the incoming audio receive path and all signal conversions for the transmitted digital signal.

DESCRIPTION

Para. 2.1033 (c) (4 – 8)

This transmitter is only for use in the Domestic Public Cellular Radio telephone Communication service, Subpart H of Part 22. The frequencies are generated using a phase locked loop frequency synthesizer. The transmit audio contains a 2:1 ratio compander, 6db/Octave per-emphasis, ±12 kHz deviation limiting and a post limiter filter per para. 22.915 (d)(1). This cellular transceiver OEM module is being prepared for quantity production.

(4) Type of Emissions: AMPS 40K0FID, 40K0F8W
DAMPS 30K0DXW

(5) Frequency Range: 824-849 MHz

(6) Range of Operating Power: This transmitter is designed for cellular mobile telephone operation. The transmitter is adjusted to achieve 0.355 watts in CLASS 4 mode, measured at the antenna connector. The transmitter output is controlled by a binary data message emitted by the base station. The power level can be controlled eleven levels in CLASS 4 mode, as defined in EIA/TIA IS-137A. Each power level will be maintained to +2, -4 dB (with additional tolerances at power levels 8,9, and 10 per EIA/TIA IS-137A) over a temperature range of -40 to +70 °C and a supply voltage, measured at the radio, between 5.2 to 6.8 VDC.

(7) Maximum Power Rating: An antenna system with 2.5 dBd antenna gain and 1.5 dB cable loss, resulting in an antenna system gain of 1.0 dB is utilized in the assessment of output power and maximum power rating. The maximum power rating for CLASS 4 operation under environmental and supply voltage variations, measured at the antenna connector, is equal to 0.355 watts, plus the power level tolerance of +2, -4 dB. Therefore the maximum output power measured at the antenna connector is 0.56 watts, per EIA/TIA IS-137A. The maximum effective radiated power, which includes the 1 dBd antenna system gain, is 0.7 watts.

(8) DC Voltage and Current: The DC voltage and total input current of the entire final power amplifier module is as follows:

CLASS	PL	Po	6.0 VDC Current
4	0/2	0.355W	400 mA
4	10	0.0003W	100 mA