FRS 220A

《 CIRCUIT DESCRIPTION 》

Feb - 18 - 2002

RECEIVER SECTION

1. RF AMPLIFIER Circuit.

* The input signal received through Ant. Terminal goes through L.P.F.(L1,L2,L3,C2~7) and is Applied to RF AMP(Q9,10).

* The signal amplified by RF AMP goes through B.P.F.(F1) and is applied to 1st MIX(er) (Q11)

2. MIXER CIRCUIT.

* The signal amplified at RF AMP goes to Base of 1st MIX(Q11).
  Local signal(RX Freq – 21.7MHz) from the PLL is applied to Base of 1st MIX and is Mixed and converted to 21.7MHz.

3. IF AMPLIFIER CIRCUIT.

* The signal converted to 21.7MHz. at 1st MIX have adjacent signal removed by B.P.F. (F2) and is sent to IF AMP. (Q12).

* The signal amplified by IF AMP. goes to IC(Q13) pin 41. Signal is mixed in MIX circuit in Q13 with 2nd local signal(21.25MHz) and converted to 450KHz. and come out as output from pin 35 of Q13.

* The output signal from pin 35 is supplied to B.P.F. (F2 : LTM450GW) where adjoining signal are removed and is applied to pin 33. Signal received at pin 33 goes through 2nd IF AMP., limiter, quadrature, detector and comes out through pin 16 as detector output.

4. AUDIO AMPLIFIER SECTION.

* The detector output from goes through audio mute circuit and audio volume control circuit in Q13.
  Signal volume adjusted at Q13 goes through AF Power Amplifier(Q204).
  where the output goes through external speaker jack(J201) to operate internal speaker (E201).

5. SQUELCH CIRCUIT.

* 30Hz. - 30KHz. noise part of detector output from Q13 is amplified using the squelch amplifier in Q13.

* This signal will go to the CPU which will turn the audio signal "ON" "OFF".

6. MUTE CIRCUIT.

* With BUSY SIGNAL going to CPU mute output goes "ON" and "OFF". Pin 10 is mute output for AF power amplifier (Q204).

* When BUSY output is "LO" Pin 10 is "HI" while Pin 20 will be "HI". When in this condition, mute circuit switch(Q215) for AF Power amplifier goes "ON" and power supply for Q204 is turned "OFF". Also AF signal mute circuit(Q215) will become "OFF" condition and AF signal will go into muted condition.

* When BUSY output is "LO" the reverse operation will be done.

TRANSMITTER SECTION

1. PRE – AMP.

* Signal from PLL output amplifier goes through TX/RX switch(Q8) and to Pre-AMP (Q6, Q7) where it is amplified and supplied to Power Amplifier(Q4, Q5) as input.

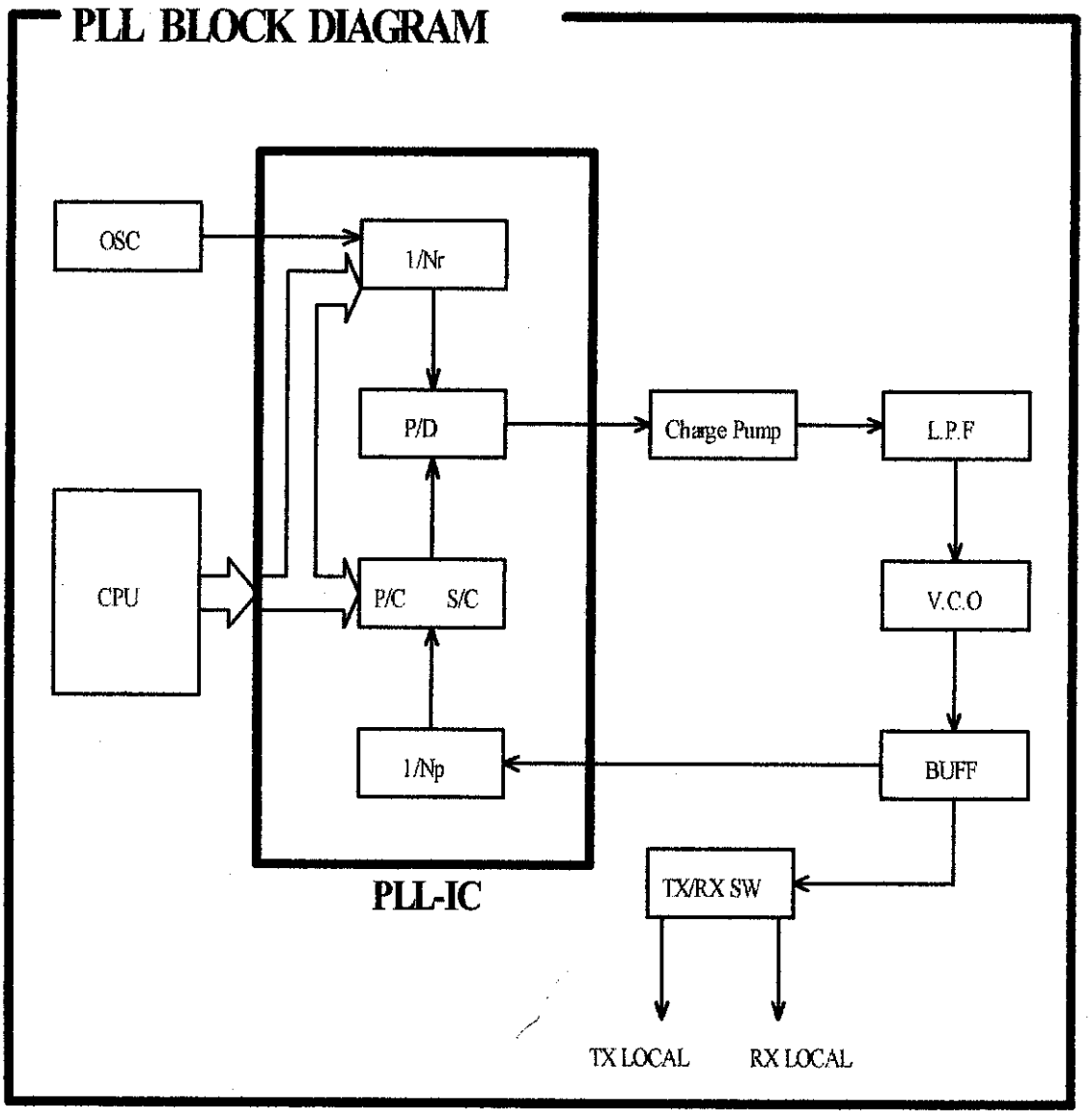
2. POWER AMP.

* Signal is amplified at Power AMP(Q4) to approximatery 0.7W. which goes through L.P.F. (L5, C13) and to ANT SW(Q1) circuit. After going through ANT SW circuit the signal goes through 2 stage of L.P.F. to reduce the high frequency harmonics and then to ANT terminal.

PLL SECTION

* PLL Block of this unit is controlled by the micro-processor which is UP DOWN channel switch which is converted to serial data.
(PLL Block is internal Q13)
* The PLL operates at the transmit frequency or the required L.O.frequency(receive-21.7MHz) according to whether it is receive or transmit mode.

* The PLL used in this circuit is a pulse swallow type and fundamental oscillator frequency divider, phase comparator, program counter, prescaler are all included internally.



1. PROGRAMMABLE COUNTER, SWALLOW COUNTER SECTION

* Frequency data goes to micro-processor(Q218) and is processed to 17 bit serial data and divider ratio is set.

* Signal from CPU is added to PLL(Q13 Internal) pin No.56(CLOCK), pin No.55(DATA), pin No.1(STROBE).
Calculation for divider ratio are set by the following;

TRANSMITTING FREQUENCY = Wanted Frequency / Step rate
RECEPTION FREQUENCY = (Wanted Frequency - 21.7MHz.) / Step rate

* The signal from V.C.O. goes into pin No.1 of PLL where the prescaler in the PLL-IC divides it by 1/64, 1/65 and goes to the program counter section.

2. PHASE DETECTION CIRCUIT SECTION, CHARGE PUMP SECTION.

* The phase difference between fundamental oscillation frequency (21.25MHz) divided to $1/N_R$ internally in Q13 and frequency from programmable counter are detected.
Detected phase difference comes out as output from pin No.46 passes through Charge Pump and is supplied to PLL loop filter.

3. PLL LOOP FILTER SECTION.

* The signal from charge pump is converted to DC voltage by loop filter consisting of CR integral circuit.
Converted DC voltage is applied to vari-cap diode(Q404) of V.C.O. to change oscillation frequency within V.C.O..

4. V.C.O. CIRCUIT.

* This is an oscillator circuit consisting of LC circuit and Q402. V.C.O. oscillating frequency is controlled by changing voltage applied to vari-cap Q404.

* The V.C.O. of this unit is made to operate wide band and TX/RX switch over circuit are not used, also the V.C.O. are made nonadjustment.

5. PLL OUTPUT CIRCUIT.

* The output of the V.C.O. goes to BUFF AMP(Q401) and is amplified to about −2dBm. This goes to TX/RX switch-over circuit(Q8) and is output to the RX LOCAL and TX LOCAL.

6. POWER SUPPLY CIRCUIT.

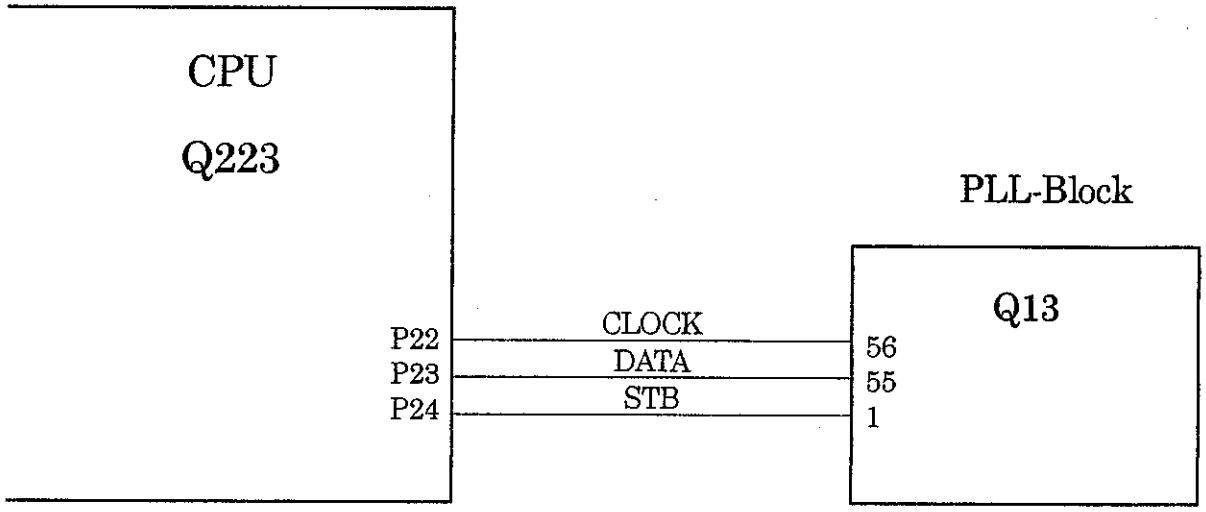
* A constant 3.3V Supply is provided by XC62FP3302(Q210). The 3.3V line is switched to each of TX SW(Q216), RX SW(Q215), IC SW(Q214).

* The switch-over of each section is done by command from CPU(Q218).

EXPLANATION OF OPERATION OF CPU

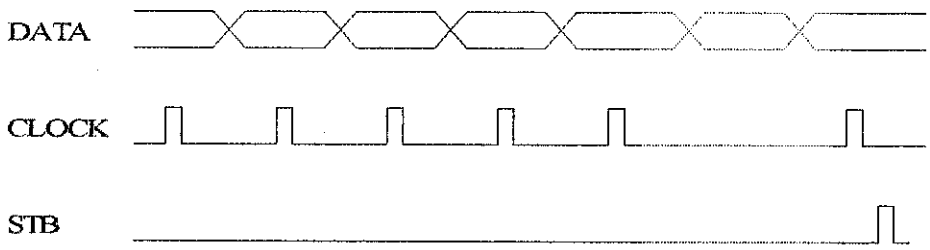
CONTROL SECTION

1. CODE OUTPUT FOR PLL-IC.



* P22(CLOCK), P23(DATA), P24(STB) of CPU(Q223) are sent out in serial form to control 12bit programmable reference divider and 17bit programmable devider.
Output data are sent out in sequence from MSB in synchronization with the CLOCK And after the LSB is sent out, one positive pulse is sent out on STB to latch the data.
In receive mode, when channel UP or DOWN, will be sent out to PLL-Block.

Sending out format is shown in drawing below:



Output data can be calculated with equation shown below:

N(RX) = (RX Frequency - 21.7 MHz) / Step rate
N(TX) = (TX Frequency) / Step rate