Product Description Sheet

The model name KY 196B is a VHF Comm Transceiver. It operates in both 25 kHz mode and 8.33 kHz mode. The FCC identifier is ASYKY196B. The technical characteristics in terms of Technical Standard Order (TSO) compliance are as follows:

Transmitter:	TSO C37c, DO-186 Class 3 TSO C37c, DO-186a Class 5
Receiver:	TSO C38c, DO-186 Class C&D TSO C38, DO-186a Class E

For more detailed information concerning the ground system and antenna refer to the enclosed Installation Manual P/N 006-10570-0000. For more detailed information concerning the circuit descriptions refer to the enclosed theory of operation.

ALLIEDSIGNAL
KY 196B
VHF COMMUNICATIONS
TRANSCEIVER

SECTION IV

THEORY OF OPERATION

4.1 GENERAL

The KY 196B, COMM Transceiver is comprised of:

A. A single conversion VHF receiver utilizing a four pole varactor tuned pre-selector, field effect transistors for RF amplifier and mixer, an 8 pole monolithic crystal IF filter and integrated circuit IF amplifier.

B. A broadband transmitter with power transistors mounted on a die-cast aluminum heat sink followed by a multi-section elliptic function low pass filter.

C. A control section utilizing a microprocessor to:

1. Increment or decrement the selected frequency.

2. Store the "USE", "STBY", 9 user programmable channels, and display brightness controls in non-volatile memory.

3. Remote Transfer the "USE" and "STBY" frequencies and remote increment the stored channels.

4. Multiplex the display with a digital gas discharge readout and automatic intensity dimming of the display.

5. Generate frequency code for the synthesizer.

6. Set bandwidth for 8.33 kHz or 25 kHz

D. A power supply made up of a discrete 9 volt regulator, a 3 terminal 5 volt regulator and switching power supply for the gas discharge display ± 90 volts.

4.2 GENERAL CIRCUIT THEORY

4.2.1 RECEIVER

A receiver block diagram is shown in figure 4-1. The received RF signal passes through: the low pass filter on the transmitter board, through the T/R diodes of the Interlock Attenuator board, through the ICAO Filter board, to the Main board preselection filter before it is amplified by the dual gate field effect transistor (FET) RF amplifier. The desired signal then proceeds to the second dual gate FET where it is mixed with the stabilized master oscillator (SMO) signal and is converted to an 11.4 MHz IF signal. It is then fed through to the top board and the selected 25 kHz or the 8.33 kHz monolithic crystal filter and back to the main board to the integrated circuit IF amplifiers followed by the AM detector. Automatic gain control (AGC) voltage is fed back to the first and second IF amplifiers and the RF amplifier to achieve more than 120 dB of dynamic range. The detected audio signal is not allowed to pass through the squelch gate until the input signal has:

A. Exceeded the noise squelch setting or,
B. Exceeded the carrier level setting.
C. Squelch has been disabled

It then proceeds through the low pass filter, which attenuates all audio frequencies above 2.5 kHz. The audio signal is then fed through the volume control to the integrated circuit audio pre-amplifier. Its output will provide more than 100 mW to a headphone, or to an external audio system.

4.2.2 TRANSMITTER/MODULATOR

The transmitter block diagram is shown in figure 4-1. In the transmit mode, the stabilized master oscillator feeds a signal to the transmitter of the frequency selected in the "USE" display window on the front panel. The signal is amplified by the broadband transmitter to the 16 watts level and fed through the elliptic function, three-section low pass filter to the antenna.

Modulation is applied to the power amplifier by series modulating the 27.5 volt line with mic audio. A small amount of mic audio is also fed to the receiver's audio amplifier for side tone.

4.2.3 STABILIZED MASTER OSCILLATOR

The stabilized master oscillator (SMO) composed of VCO, Q2407and associated components generates the RF drive for the transmitter as well as the local oscillator signal for the receiver. The SMO synthesizes frequencies that are referenced to a 8.33 kHz signal derived from a 12.8 MHz TCXO. Receive and transmit codes are fed to the synthesizer by the microprocessor (μP) and represent the frequency indicated in the "USE" window on the front panel.

4.2.4 MICROPROCESSOR AND DISPLAY

Refer to figure 4-2 Microprocessor Block Diagram. The microprocessor (μP) contains 8K bytes of permanent Read Only Memory (ROM) for program instruction. A 128 byte non-volatile memory is used externally for frequency information storage. A 3.975 MHz crystal is used in conjunction with the μP to generate the μP's clock signal

The microprocessor controls the frequency synthesizer via a three wire serial interface. The microprocessor also provides the logic that controls the analog switching circuitry that switches between the two IF filters.

The increment/decrement switches send three pulses to the μP (up, pulse, down) in a specific sequence to provide the codes and validity check for increment and decrement operations. The microprocessor also reads the CHANNEL and TRANSFER buttons.

The display is controlled by the microprocessor. The photocell is read by an analog to digital converter, which is controlled by the microprocessor. The photocell information is used to calculate the display brightness, which is controlled by pulse width modulation, and setting the current through the segments. The analog to digital converter also reads the 28 VDC or 14V DC lighting buss so that display can track the instrument panel dimming buss if desired.

4.3 DETAILED THEORY OF OPERATION

4.3.1 RECEIVER

4.3.1.1 Receiver RF Input Circuits

In the receive mode Q101 is switched on, forward biasing the T/R diodes located on the Interlock Attenuator board (09096). The desired RF signal passes through the first section of the transmitter lowpass filter (06047), then to the T/R diodes and then to the Filter (08939) board. The Filter board greatly attenuates unwanted signals in the FM broadcast band while passing the desired aircraft signal. The desired signal goes to the receiver on the main board. C102 steps up the impedance to match the first pole of the preselector.

4.3.1.2 Double Tuned Preselector

The first pole of the preselector is tuned by L101, C103 and CR101A. The signal is coupled to the second pole of the preselector by L102. The second pole of the preselector is tuned by L103, C106 and CR101B. The matched varactor diodes, CR101A and CR101B, are tuned to the desired frequency through a large resistor from the VCO's Control Voltage and a voltage scaling circuit U2103B (09501). The desired signal is coupled to gate 1 of the RF amplifier by C107.

Preselector control voltage scaling circuit. Top board (09501)
Since the VCO varactor is not matched to the four matched varactors of the preselector. A scaling circuit is necessary to match voltage vs. frequency of the two sections. R2177 is used to for alignment.

4.3.1.3 RF Amplifier

Q1501 and the associated parts make up the RF amplifier. The desired signal is applied to gate 1. The RF AGC is applied to gate 2. The RF amplifier has approximately 20 dB of gain at maximum RF AGC voltage and 30 dB of attenuation with minimum RF AGC voltage, producing a dynamic range of 50 dB. C114 couples the desired signal to the double tuned interstage.

4.3.1.4 Double Tuned Interstage Network

The first pole of the interstage network is tuned by L105, C115 and CR101C. The signal is coupled to the second pole of the interstage network by L106. The second pole of the preselector is tuned by L107, C118 and CR101D. The matched varactor diodes, CR101C and CR101D, are tuned to the desired frequency through a large resistor from the VCO's control Voltage. The desired signal is coupled to gate 1 of the mixer through L133.

4.3.1.5 Mixer

Q1502 and the associated parts make up the mixer. The local oscillator, LO, signal is fed to gate 2 at a frequency 11.4 MHz above the desired signal. The level of the local oscillator is between +4dBm and +7dBm. The desired IF signal is now at 11.4 MHz. The drain of Q103 is tuned to 11.4 MHz by T101 and matched to the 25 kHz crystal filter.

4.3.1.6 Crystal Filters

The crystal filter, FL1, provides the desired selectivity for 25 kHz spaced channels. The input and output of the filter is matched to 4100 ohms by T101 and T102 respectively. The crystal filter, FL2, provides the desired selectivity for 8.33 kHz spaced channels. The input and output of this filter is matched to 1650 ohms by L6, C66, C67 and L7, C74, C75 respectively. The bandwidth is

selected by the μP which controls the voltage applied to the diode switching circuits. The switching components are CR4, CR5, CR6, and CR7.

4.3.1.7 First IF Amplifier

The desired signal is coupled from T102 to the first IF amplifier, I101. The first IF amplifier has about 45 dB of gain with 60 dB of dynamic range. IF AGC voltage is applied to R124 in series with pin 5 of I101. R124 converts the AGC voltage to an AGC current. The output is loaded with R245 for stability. T103 is tuned for 11.4 MHz and couples the signal to the second IF amplifier.

4.3.1.8 Second IF Amplifier

I102 is the second IF amplifier. The second IF amplifier has about 45 dB gain with 60 dB of dynamic range. IF AGC voltage is applied to R126 in series with pin 5 of I102. R 126 converts the AGC voltage to an AGC current. The output is loaded with R246 for stability. T104 is tuned for 11.4 MHz and couples the signal to the detector.

4.3.1.9 Detector

Transistor Q105 and capacitor C130 makes the amplitude modulation detector. It is biased near cutoff by transistor Q104, which the emitter-base junction provides bias stability and temperature compensation. The demodulated signal is sent to a Noise amp U2103A, the IF AGC, I105A, the squelch gate, Q116 and to the demodulator buffer, Q131.

4.3.1.10 IF AGC Circuit

AGC voltage is derived from the average value of the detector's collector voltage, which is inversely proportional to the carrier level. The operational amplifier I105A filters out the audio variations and integrates to the average voltage of the detector. R159 and R160 set the maximum gain reduction at about 6.6 volts. As the detector collector voltage increases with a decrease in signal level, the AGC voltage decreases which increases the gain in the first and second IF amplifiers. The IF AGC voltage is made available at TP105 and at the rear connector pin L. The AGC voltage at pin L is reduced by one diode drop (approx. 0.6 V).

4.3.1.11 RF AGC Circuit

The RF AGC voltage is applied to the RF amplifier from I105B. The RF AGC stays at maximum voltage (max. gain of amp) until the RF signal level reaches about 12.5 μV. The level at which it attacks is set by R184. When the IF AGC voltage exceeds the reference voltage set by R184, the RF AGC voltage decreases, decreasing the gain in the RF amplifier. RF AGC is made available at TP106.

The RF AGC is gated with TX(not) through CR120A such that when the unit transmits, the RF AGC voltage goes to zero. This provides maximum attenuation in the RF amplifier during transmit.

4.3.1.12 Noise and Carrier Squelch Circuit

The carrier squelch circuit prevents the radio from squelching if an RF carrier greater than 12.5 μV has been detected. I106B compares the RF AGC voltage, which is inversely proportional to the carrier level, to the reference level set by R183 and R185. If the RF AGC voltage is greater than the reference level, then the unit is allowed to squelch; if the noise level is large enough. When the RF AGC voltage is less than the reference level, the output of I106B goes high; turning on Q140. When Q140 turns on, the input signal to the noise amp is shorted to ground, causing the noise squelch circuit to be inhibited.

The noise amp, U2103A, circuit on the top board (9501) is used compensate for different noise levels in the 25 kHz/8.33 kHz modes. It consists of a FET, Q2104, used as a switch to AC couple resistance, R2181 to ground or to provide an open circuit. Gain is unity in 25 kHz mode and adjustable in the 8 kHz mode. The noise signal is returned to the main board to drive noise amplifier, Q112.

Transistor Q112 amplifies the noise from the noise amp circuit and limits its amplitude so that impulse spikes (such as ignition noise) will not be of a higher amplitude than other noise. The output of Q112 is coupled to an 8 to 10 kHz bandpass filter, I106A. The output of the bandpass filter is fed to the comparator, I107A. The signal is compared to the reference level set by R176. When the noise signal is larger than the reference level, the comparator goes high charging C166. If C166 is charged grater than half the supply voltage, then the unit will be squelched.

CR107A will squelch the radio in transmit.

4.3.1.13 Squelch Gate

Q116, Q117 and associated parts make up the squelch gate. The audio signal comes from the detector at TP108; the detector biases Q116. When the unit is squelched the base of Q117 goes to the supply voltage and its emitter follows. Since the emitters of Q116 and Q117 are tied together, Q116 becomes reverse biased; attenuating the signal 70 dB.

4.3.1.14 Audio Low Pass Filter

Inductor L110 and its associated capacitors form a low pass elliptical filter. The filter is at least 20 dB down at 4 kHz and the notch is at least 25 dB down at 4.5 kHz. The filter does roll off below 350 Hz since the signal is A.C. coupled in and out of the filter. The low frequency roll-off helps get rid of 60 Hz hum.

4.3.1.15 Audio Compressor

The received signal is coupled through C178 to the input of the compressor amplifier, I111A. The output is fed to the volume control and to I111B. I111B will begin to discharge C179 when the amplitude to I111B exceeds the voltage across R210. Discharging C179 lowers the gate to source voltage on Q118, which reduces the drain to source resistance on Q118. As Q118 is turned on, the amplitude at C178 is reduced. This maintains a constant amplitude out of the compressor amplifier.

4.3.1.16 Audio Amplifier

The audio signal is routed through the volume control R902 to the audio amplifier, I112A. The signal is amplified approximately 30 dB and capacitively coupled through C187 to the auto-transformer, T107. The voltage and impedance are stepped up to provide a minimum of 100 mW of audio power into 500 ohm load; such as headphones or an audio panel. The sidetone, through R220, and the mic intercom, through R218, are also amplified by the audio amplifier.

4.3.2 STABILIZED MASTER OSCILLATOR (SMO) (09628)

4.3.2.1 Synthesizer

The synthesizer/VCO board (09628) is a phase locked loop (PLL) that incorporates a temperature compensated crystal oscillator (TCXO) voltage controlled oscillator (VCO) and an PLL IC. It produces the LO frequency during receive and the TX drive frequency during transmit.

The 12.8 MHz TCXO, Y2401,is stable within 2.5 PPM over temperature and set to nominal at room temperature with R2417. It produces the required reference signal at pin 1 of U24011 to which the PLL is referenced to.

The PLL: The 12.8 MHz is always divided down to 8.33 kHz to provide reference to the phase detector. The VCO frequency is divided by the variable divider set by the front panel and the μP. The output of this divider is then compared by the phase detector to the reference frequency. The IC phase detector drives the charge pump output. If the frequency is greater than 8.33 kHz, the charge pump will pulse up once every 120 μsec. If the frequency is less than 8.33 kHz the charge pump will pulse down. The greater the divided frequency from the reference frequency the wider the charge pump pulse. Output of charge pump at pin 5 is also tri-state so when no error signal is needed none is produced.

4.3.2.2 Charge pump amplifier and translator

Q2401, Q2402, Q2403, Q2404 and their associated parts make up a charge pump amplifier. It is a current limited voltage translator. The voltage translator translates from a five volt range provided by the IC charge pump to approximately 26 volt range and inverts the charge direction. Output current is limited to ± 7.5 ma. Input of the amplifier is voltage driven by pin 5 of U2401 to R2403. This resistance sets the input current delivered to the emitters of Q2402 and Q2404. The bases of Q2402 and Q2404 are biased to about 2.4 volts so that when the VCO is on frequency Q2402 and Q2404 will be turned off similar to the IC's internal charge pump. If the IC charge pump pulses low, Q2402 will turn on causing Q2403 to turn on and a 7.5 ma current pulse from a 28 Volt source is delivered to the load at TP2401. If the IC charge pump pulses high, Q2404 will turn on causing Q2402 to turn on pulling 7.5 ma out of the load at TP2401 to ground. The capacitive input Loop filter is driven from TP2401.

4.3.2.2 Loop Filter

The loop filter is a low pass filter and it sets the response time of the PLL. It is current driven into C2446 and a lead lag network. C2447, and R2409. Components R2457, C2451, R2458, C2450, R2459, C2449, R2402 and C2422 make up the rest of the low pass filter. Output voltage is connected to the VCO varactor CR2401. With this filter, the loop bandwidth is about 70 Hz, and 8.33 kHz reference pulses are more than 130 dB down. The control voltage is also fed to the receiver preselector control through R2419.

4.3.2.3 Voltage Controlled Oscillator (VCO)

Q2407 and its associate parts form a voltage controlled Collpits oscillator. The varactor CR2401 is the frequency determining element of the VCO tank circuit. C2505 determines the frequency range of the tuning voltage, the smaller the capacitor the wider the range and higher the frequency for the same voltages. R2404 and R2405 provides bias stability. The tuning range from 118.00 MHz to 148.39167 MHz has an approximate tuning voltage of 3 to 8 volts respectively. Output of the VCO drives RF OUT and the VCO buffers back to the PLL IC.

4.3.2.4 Digital Buffer

Q2408, and Q2405 and their associated parts form the digital buffers. The digital buffers are lightly coupled through C2402 and C2401 so that noise from the PLL prescaler will not get back to the VCO. Network C2432, L2403, C2434, C2433 is a low pass filter to reduce harmonic content and R2460 stabilizes U2401 pin 8 input impedance The signal is coupled to the PLL prescaler through C2540 at about 500 mV.

4.3.2.6 Lock detector and data interface to the processor

PLL IC, U2401 pin 7 produces negative going pulses when the loop is out of lock. R2455 quickly discharges C2429 through CR2402. Comparator, U2402A, output goes low indicating to the μP an out of lock condition. When locked R2420 slowly charges C2429 for positive levels (5 V) to give a slow attack and fast decay of the lock signal sent to the microprocessor. The clock, data and strobe lines are driven from the microprocessor.

4.3.2.7 VCO Buffer

Q109 and associated parts form the VCO buffer. The VCO buffer provides isolation from the transmit buffers and the receiver mixer as well as amplifying the signal to about +7dBm to the mixer.

4.3.2.8 Transmit Buffers

The transmit buffers contain two stages of amplification. The RF signal is coupled through C155 to Q110 and amplified. L134 and C157 couples the collector of Q110 to Q126 amplifies the signal to approximately 24dBm. The signal is coupled through CR117 and C228 to create the transmit drive. The drive level is adjusted for different transmitters by the resistor R1006, Q111 and Q139 are turned off during receive allowing Q110 and Q126 to be reversed biased. Q127 is also turned off during receive preventing CR117 from being turned on. During receive the RF signal is reduced by 50 dB.

4.3.3 MODULATOR

4.3.3.1 Microphone Input Compressor

The microphone is connected to pin K of the rear panel connector. Mic bias is supplied by R114 and R225. The signal passes through C191 to the Mic Gain Control. Q119 is turned on during transmit to pass the signal to the modulator compressor.

4.3.3.2 Modulator Compressor and elliptic low pass filter

The audio signal is coupled through C230 to the input of the compressor amplifier, I113A. The output is fed to the three stage elliptic low pass filter circuit consisting of U2101A&B U2102A (09501). U2101A and U2101B have notches at 4500 Hz and 3160 Hz respectively. I113B will begin to discharge C198 when the output of the modulator exceeds the voltage across R267. Discharging C198 lowers the gate to source voltage on Q120, which reduces its drain to source resistance. As Q120 is turned on the amplitude at C230 is reduced. This maintains a constant amplitude out of the compressor amplifier. R267 sets the modulation level. The bias network R257 and R267 is run off of the mod bias voltage, so that when the mod bias sags the modulation will decrease preventing distortion.

Filter circuits of U2101A&B U2102A (09501) also provide more harmonic rejection to audio signals. The resulting audio is a referenced to transmit audio detected by CR2110 andCR2109 and error corrected in op amp, U2102B. This audio then drives modulator amplifier I112A.

4.3.3.3 Modulator Amplifier

The output of the error correcting op amp U2102B is coupled to the modulator amplifier through C2231. The output is coupled to the modulator through C196 and T108.

4.3.3.4 Modulator Bias

The modulator bias (mod bias) regulates the supply voltage to just below half the supply voltage. Q123 is the regulating transistor and on the 28 volt versions Q122 is used to buffer the regulating transistor. R251, R254, and R256 set the regulated voltage, with R256 being adjustable. CR115 prevents voltage problems. CR116 and R255 determines the power set back during modulation on the KY197A. RT101, R250, and R252 set the power reduction due to a thermal overload. When RT101 becomes hot, the resistance goes up reducing the voltage at E113, causing CR114 to turn on, and thus lowers the bias on Q123.

4.3.3.4 Modulator

The audio signal is applied to the primary of T108, which has a 4 to 1 turns ratio. This steps up the voltage swing to the bases of the modulator transistors Q124 and Q130 enough to make a 1 to 24V swing on the transmitter's final and driver. This output is also fed back to the modulator compressor. The mod bias is fed to the secondary of T108 providing the bias to Q124 and Q130 with R247 being the current limit resistor.

4.3.4 TRANSMITTER 28 Volt 16 Watts KY196B (Refer to figure 4-1 and 06047 drawings)

4.3.4.1 RF Amplifier

RF is fed from the transmit buffers to the RF amp, on the transmitter board, through a 50 ohm coaxial cable. The drive level is approximately 18dBm. During receive the RF is attenuated as the TX(not) line goes high it turns on Q601 shorting the drive to ground and reverse biasing the pin diode CR604 to "OPEN" the input to Q602. During transmit, the base current is supplied through R602 and CR604. Transformer T601 is broadband tuned and steps the collector impedance down to the input impedance of the pre-driver.

4.3.4.2 Pre-Driver

RF drive is fed through C633 and C606 to the pre-driver, Q603. The pre-driver is operated class C and the collector is modulated through R606. The collector is broadband tuned and is coupled to the driver by T602.

4.3.4.3. Driver

RF drive is supplied to the base of Q604 through the coupling capacitors C610, C611, and C612. Q604 is operated class C and is modulated at the collector. The collector is broadband tuned by T603 which also matches the collector to the input of the final.

4.3.4.4 Final

Capacitor C618, C619 and C620 form the input matching network for the final power amplifier, Q605. The final is operated class C and is modulated at the collector. The low collector output impedance is stepped up to approximately 50 ohms by transformer T604.

4.3.4.5 Low Pass Filter

A three section elliptic low pass filter is placed between the final and the antenna to attenuate all harmonics which may be generated in the transmitter. During transmit the T/R diodes CR603 and CR605 are reversed biased to protect the receiver from 16 watts of power.

4.3.5 MICROPROCESSOR

4.3.5.1 Synthesizer Programming

U510, the microprocessor sends serial data from pin 35 to the synthesizer. The data is clocked by U510-36 and the synthesizer is strobed by U510-31. The lock detect line from the synthesizer is input on U510-28 and is pulled high when the synthesizer is locked.

When U510-32 is pulled low by MIC KEY(NOT), U510-25 is turned high when the synthesizer is locked to turn on the transmitter. The gate of Q501 must be low before the transmitter can be turned on. Q502 inverts the signal to TX *, the signal which turns the transmitter on.

4.3.5.2 Non-Volatile Memory

Data is sent in a serial data stream to U503-3 (non-volatile memory) from U510-35. The clock is generated by U510-36 and is read by U503-2. U510-27 drives U503-1 which selects the non-volatile memory. U503-4 is the serial data out of the non-volatile memory and is read into U510-34.

4.3.6.3 Analog to Digital Converter

Data is sent in a serial data stream to U508-17 (A/D converter) from U510-35. The clock is generated by U510-36 and is read by U508-18. U510-26 drives U508-15 which selects the A/D converter. U508-16 is the serial data out of the non-volatile memory and is read into U510-34.

The A/D (U508) uses a system clock for its conversion time. The 496.875 kHz system clock is generated from U504, a binary counter. The 3.975 MHz clock signal (the microprocessor clock) on U504-1 is divided by eight, then output on U504-9 and input on U508-19.

4.3.6.4 Microprocessor Reset Circuit

During normal operation the output on pin 13 of U505-D is 5 volts DC. The 5 volts DC on U510-44 (VDD) is produced through the 5 volt regulator I108 on the main board. On power up, the 9 volts on the input of I108 must reach 7.3 volts DC before 5 volts DC is produced on the output of I108. Therefore, on power up, the microprocessor (U510-1) is held in reset until the 9 volt DC reaches 7.9 volts DC. Pin 11 of I501-D must reach 6.2 volts DC to accomplish this. On power down, the 9 volt DC must drop to 7.5 volts DC before the microprocessor is put into reset.

4.3.6.5 Display

The display is a gas discharge type with three sections ("USE, "STBY", and "CHAN"). The "USE" frequency is the active operating frequency and is displayed in the "USE" window at all times. In reality, the display is showing a channel designator, not an actual frequency, as the actual frequency the radio is turning is not necessarily the number being displayed. A standby frequency, which can be exchanged with the "USE" frequency, is displayed in the "STBY" window when in standby entry mode. When in Channel or Program mode, the channel frequency is displayed in the "STBY" window and the channel number is displayed in the "CHAN" window. The letter "T" is displayed between the "USE" and STBY" windows during transmit.

U510 sends a 16 bit serial BCD code through pin 6 to cathode latches U501 and U502. Each bit is clocked through U510-5. At the end of the 16 bits, U510-7 latches the data into the cathode latches. This occurs for each multiplexed pair of anodes. The latched outputs of the cathode latches feed cathode drivers consisting of two transistors, one diode, and 5 resistors. The associated multiplexed anodes are then turned on through pins 8, 9, 10, 11, 12, and 30 of U510 which go to anode driver I901 on the display board. U510-24 is used to turn cathode information on and off.

The display brightness is controlled in three different ways, automatic dimming through the photo cell which acts on ambient light, dimming through the aircraft lighting bus, and max brightness all the time. The display brightness is generated by pulse width modulating the cathodes through

U510-24. The pulse width modulation signal is also fed into integrator U11-A which converts the PWM signal into a DC level (CURR_CONTROL). This signal also controls display brightness by setting current through the cathode drivers.

4.3.6.6 Bandwidth Switch Driver

U510-29 is the microprocessor output that switches the receiver between 8.33 kHz channel mode and 25 kHz channel mode. The output is high for 8.33 kHz mode and low for 25 kHz mode. U510-29 drives the differential output driver consisting of Q503, Q504, Q505, Q509 and Q510. The differential driver biases pin diodes which switch between the two IF filters in the receiver. J501-1 (8.33 KHZ) is approximately 6 VDC in 8.33 kHz mode and .7 VDC in 25 kHz mode. J501-2 (25 KHZ)is approximately 0.7 VDC in 8.33 kHz mode and 6 VDC in 25 kHz mode.

Description of Digital Information

The digital information is identified as ACARS (Aircraft Communications Addressing and Reporting System) The modulation data is further identified in ARINC 597. The modulation data signal is 16 dB above the level required for 50% modulation. A spectrum analyzer was used to observe the radio frequency spectrum with the transmitter operating in a normal mode. The modulation data was fed into the Mic Input of the KY 196B. Refer to figure 8 on page 11 of this certification submittal for spectrum data.