1 THEORY OF OPERATION

1.1 General

The KAC 1052 Antenna Coupler is a component of a KHF 1050 HF Radio Communication system. It receives 200Wpep HF signals from the KPA 1052 Power Amplifier (PA) and feed the power to an aircraft antenna efficiently. Receiving signals from an antenna is provided to the KRX 1053 Receiver/Exciter (RX/EX) via PA.

The unit is normally installed near an antenna inside of an aircraft fuselage for reducing feeder loss.

The unit is filled with dry Nitrogen and keeps it's internal pressure to prevent the RF networks from sparking caused by high voltage and low pressure.

The unit is composed of following circuit cards.

CBL-103	PS & INTERFACE
CDC-1083B	CPLR CONTROL
CCN-338	SENSOR & RLY DRV
CSC-590B	SHUNT CAP BOARD
CSC-591B	SERIES CAP BOARD
CSC-592B	COIL BOARD

CBL-103 PS & INTERFACE card is located at front panel and composed of power supply switching circuit, voltage regulators, voltage-current converter for APC, RS422 interface driver and surge protection for interface signals. The card supplies 28V, 12V and 5V DC power to all circuit cards and has all interface connectors to communicate with another LRUs.

CDC-1083B CPLR CONTROL card is located between CBL-103 PS & INTERFACE card and shield assembly and composed of CPU, CPLD, EEPROM, analog interface, RS232C interface driver, reference voltage generator, pressure sensor, temperature sensor and voltage monitor. The card administers all operations to be needed and monitoring the state of the unit.

CCN-338 SENSOR & RLY DRV card is located between shield assembly and three RF boards and composed of impedance sensor, RF power level detector, 3dB attenuator, relay driver, bridge amplifier and part of relays for RF network determination. The card detects input impedance and provides them to the CDC-1083B CPLR CONTROL, converts serial relay signals to parallel relay signals and amplifies received signals and provides to the RX/EX.

CSC-590B SHUNT CAP BOARD card is located between CSC-591B SERIES CAP BOARD and CSC-592B COIL BOARD card and composed of shunt capacitors and relays constituting the RF networks, arrestor and discharging resistor.

CSC-591B SERIES CAP BOARD card is located at right side of the unit and composed of series capacitors and relays constituting the RF networks. The capacitors are sometimes connected as shunt capacitor arm of the RF networks.

CSC-592B COIL BOARD card is located at left side of the unit and composed of inductors and relays constituting the RF networks. The inductors are connected as shunt inductor arm or series inductor arm of the RF networks.

Figure 1.1 shows overall simplified black diagram of KAC 1052 Antenna Coupler.

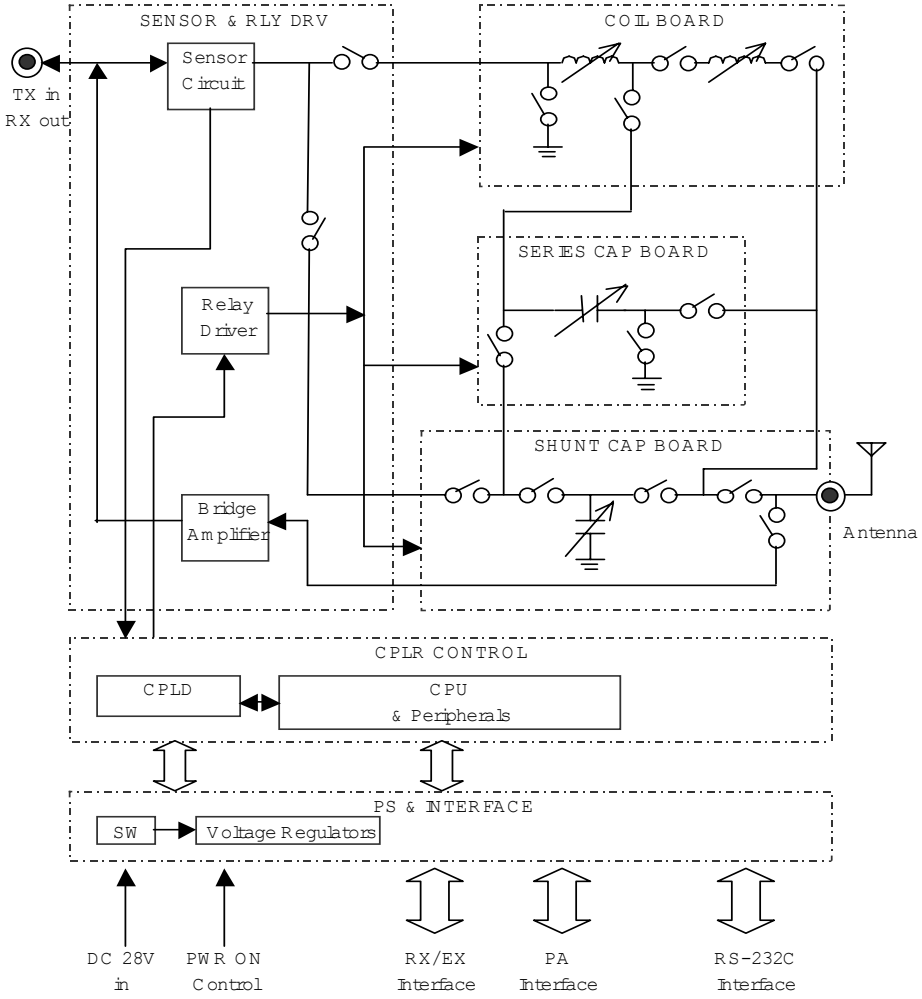


Figure 1.1 Overall Simplified Block Diagram of KAC 1052 Antenna Coupler

1.2 Construction

The mechanical configuration of the KAC 1052 Antenna Coupler is mainly composed of chassis assembly, two side plates, shield assembly, front bracket and rear bracket.

The chassis assembly is composed front panel, rear panel, top plate and bottom plate and these are welded together.

Both side plates seal chassis assembly tightly and enable to maintain internal circuit cards by removing from chassis assembly.

Shield assembly is composed of shield cap, shield plate and two support plates that isolate RF circuit and sensor circuit from digital noisy circuit such as CPU. For this purpose, the shield is located between CDC-1083B CPLR CONTROL card and CCN-338 SENSOR & RLY DRV card.

Front and rear bracket are used for fixing the unit to an aircraft fuselage with mounting tray.

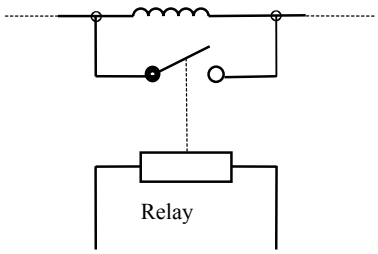
Outside of the unit has BNC connector, 37 pins sub D connector with one touch locking, 9 pins sub D connector, air valve and relief valve on the front panel and HN connector, ground terminal and vent plug on the rear panel. All these parts and side plates are airproof type to keep internal pressure level even if the unit is in low-pressure environment

The chassis assembly and side plates are designed to withstand internal high pressure of Nitrogen and severe vibrations of an aircraft.

1.3 RF Networks

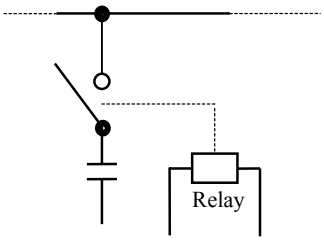
RF matching circuit of the unit is composed of three circuit arms, shunt capacitor, series capacitor and inductor circuit. Each arm is allocated for each card, CSC-590B SHUNT CAP BOARD, CSC-591B SERIES CAP BOARD and CSC-592B COIL BOARD.

Each arm is composed of 12 to 13 elements that are combination of capacitors or inductors and switching relays in order to realize both sufficient resolution at the upper limit frequency and wide coverage range at the lower limit frequency. Each capacitor or inductor is connected or disconnected by relays. Figure 1.2 shows the way of change over by relay in inductor and capacitor elements. Values of these elements are set to increase by binary system. For example, if the capacitance value of C101 is 1, the relative capacitance value of C102, C103 will be 2 and 4 in principle. Combined inductance or combined capacitance of arm is the sum of all applied elements.



When relay is OFF, inductor is applied.
When relay is ON, inductor is short circuited and does not affect circuit.

Inductance Element



When relay is ON, capacitor is applied.
When relay is OFF, capacitor is not connected and does not affect circuit.

Capacitance Element

Figure 1.2 Change over by Relay of Circuit Elements

Refer to Figure 1.3 RF Matching Network of KAC 1052 Antenna Coupler.

CSC-590B SHUNT CAP BOARD has parallel connected 13 shunt capacitor elements and three network determination relays. The maximum capacitance is approximate 5600pF.

CSC-591B SERIES CAP BOARD has parallel connected 13 series capacitor elements and three network determination relays. The maximum capacitance is approximate 1500pF.

CSC-592B COIL BOARD has series connected 12 inductor elements and three network determination relays. The maximum inductance is approximate 48uH.

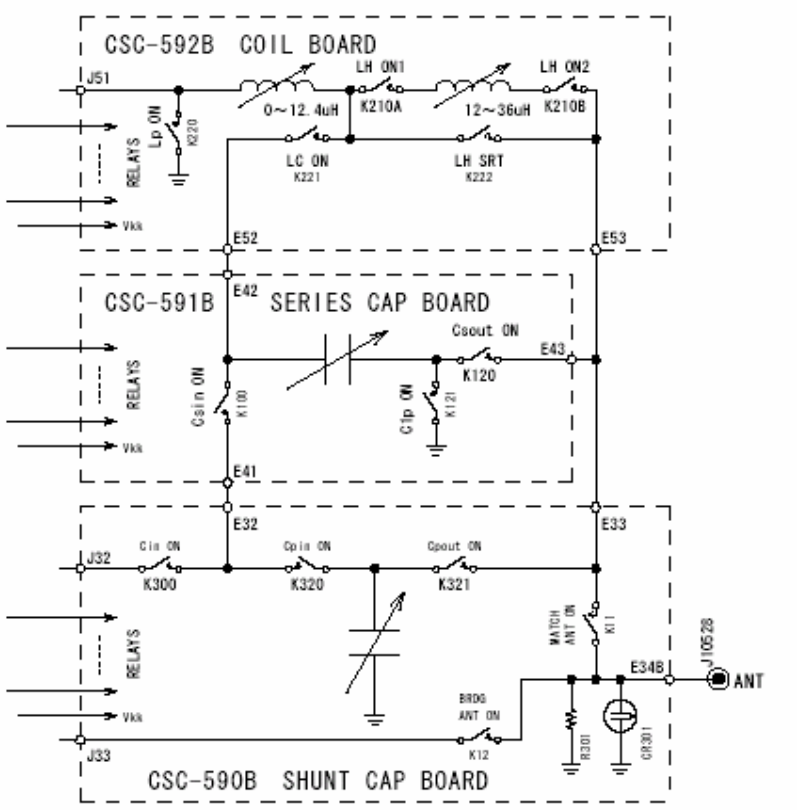
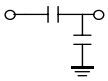
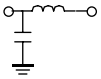
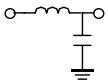
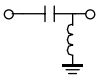
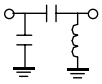
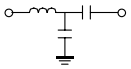
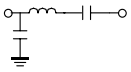
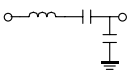
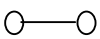


Figure 1.3 RF Matching Network of KAC 1052 Antenna Coupler

The unit has many circuit configurations that enable wide matching impedance region. Combinations of network determination relays set the circuit configuration. Available circuit configurations are listed on Table 1.1. The unit tries to set the most efficient circuit among these configurations during tuning sequence.

Table 1.1 RF Circuit Configurations of KAC 1052 Antenna Coupler

No	Circuit	Schematic	Ls on	Lp on	LC on	LH1	LH2	LHSR	Cin on	Cs on1	Cs on2	C1p	Cp in	Cp out	Note
1	Cp-Cs			O		O			O	O	O		O		
2	Cs-Cp			O		O			O	O	O			O	
3	Cp-Ls		O			X	X	X	O				O		
4	Ls-Cp		O			X	X	X						O	
5	Cs-Lp			O				O	O	O	O				
6	Cp-Cs-Lp			O		X	X	X	O	O	O		O		
7	Lp-Cs-Cp			O	O				O	O	O			O	
8	C1p-Ls -C3p		O			X	X	X	O	O		O		O	
9	Ls-Cp-Cs		O		O					O	O		O		
10	Cp-Ls-Cs		O		O				O		O		O		
11	Ls-Cs-Cp		O		O						O			O	
12	THRU			O		O			O				O	O	

Note 1: O: ON X: At least one relay ON

Note 2: “Ls on” relay is located on CCN-338 SENSOR & RLY DRV card

1.4 Sensors

The unit has following sensors; impedance sensors, pressure sensor, temperature sensor and power supply voltage sensor. The impedance sensors are located on CCN-338 SENSOR & RLY DRV and others are on CDC-1083B CPLR CONTROL.

The impedance sensors are divided into magnitude detector, phase detector, angle detector, resistance (R) detector, conductance (G) detector and VSWR detector. Figure 1.4 shows block diagram of the impedance sensors in the CCN-338 SENSOR & RLY DRV.

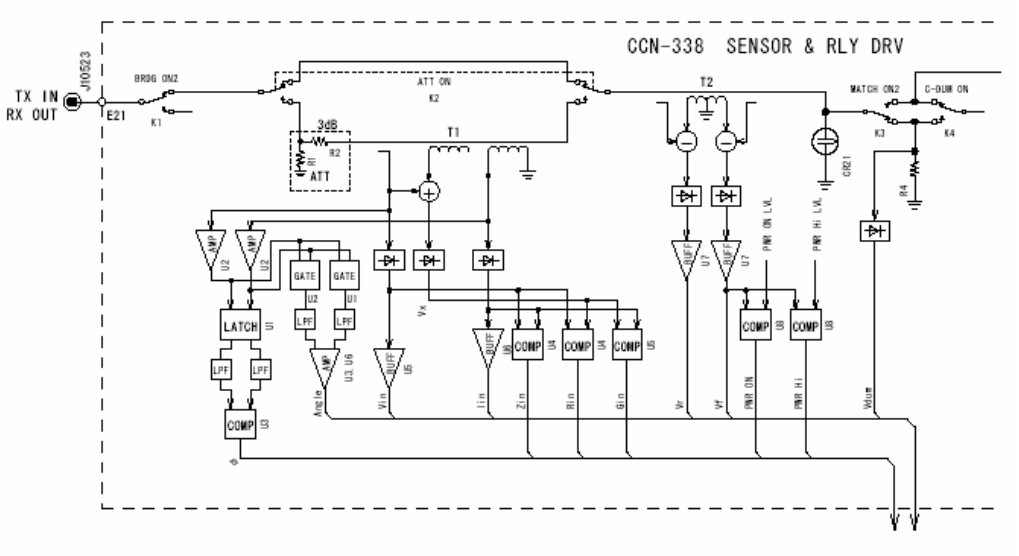


Figure 1.4 Block Diagram of Impedance Sensors

The magnitude (Zin) detector judges magnitude of line impedance. The detector compares the magnitude of line voltage with that of current. If magnitude of line voltage is smaller than line current, in other words line impedance is smaller than 50 Ohm, the signal "Zin<Zo" will be low.

The phase detector judges the phase of line impedance. The detector detects phase difference between line voltage and current. If line voltage lag line current, in other words line impedance is capacitive, the signal "PH<0" will be low.

The angle detector generates DC voltage proportional to the phase difference between line voltage and line current. The signal has no polarity and it will be 5Vdc at maximum phase difference 90 deg.

The resistance detector judges magnitude of real part line impedance. The detector compares the sum of the line voltage and current with the magnitude of line voltage. If the real part of line impedance is smaller than 50 Ohm, the signal "Rin<Zo" will be low.

The conductance detector judges magnitude of real part line admittance (conductance). The detector compares the sum of the line voltage and current with the magnitude of line current. If the line conductance is smaller than 1/50 Siemens, the signal "Gin>Go" will be high.

The VSWR detector detects forward voltage (Vf) and reflected voltage (Vr) of line. Each voltage is compared each other to generate VSWR signals on the CDC-1083B CPLR CONTROL card. The signal "Vf" is also used to generate "PWR ON" and "PWR Hi" signals. The "PWR ON" signal informs the CPU that RF power level is valid and enables tuning operation. The "PWR Hi" signal informs the CPU that RF

power level is too high to tune and enables detune detection.

The pressure sensor detects internal absolute pressure of the unit. The device U42 outputs differential DC voltage “Vo+” and “Vo-” proportional to the pressure followed by the high input impedance differential amplifier composed of U43 and U44A. The gain of the differential amplifier is designed that the output voltage will be approximate 4Vdc with 30-psia pressures. This voltage is provided to CPU and converted digital value to detect pressure-warning level. The comparator U44B detects low-pressure alarm and informs CPU via CPLD as “PRESS ALM”. The alarm level is set to approximate 11.9 psia.

The temperature sensor detects internal temperature of the unit. The device R428 varies its resistance sensitively to temperature and shunt resistors R426 and R427 linearize the resistance. The output voltage of the amplifier U45A is approximately proportional to absolute temperature and will be approximate 2Vdc at 400degree K. This voltage is provided to CPU and converted digital value to compensate the pressure value to it at room temperature.

The power supply voltage monitor observes the combined voltage of 12Vdc and 5Vdc used in the unit. The combined voltage is provided to CPU and converted digital value. If the 12Vdc and /or 5Vdc are failed, CPU detects power supply alarm.

1.5 Bridge Amplifier

The Bridge Amplifier is mounted on CCN-338 SENSOR & RLY DRV. The amplifier amplifies received signal fed from antenna and provides the signal to the RX/EX via PA.

Figure 1.5 shows the block diagram of Bridge Amplifier. The amplifier is composed of single NPN transistor and transformer used for feedback circuit. The impedance transformer is inserted at its input circuit to convert the impedance from 50 Ohm to about 400 Ohm. The approximate gain of the amplifier is 9 to 12 dB at the frequency range from 2 to 30MHz. The internal oscillator and output level detector are incorporated to detect the failure of the amplifier. The frequency of the oscillator is approximate 4MHz.

To protect the amplifier, the input circuit is connected to ground and output is connected to internal 50 Ohm resistor when the unit or other side system is in transmitting state.

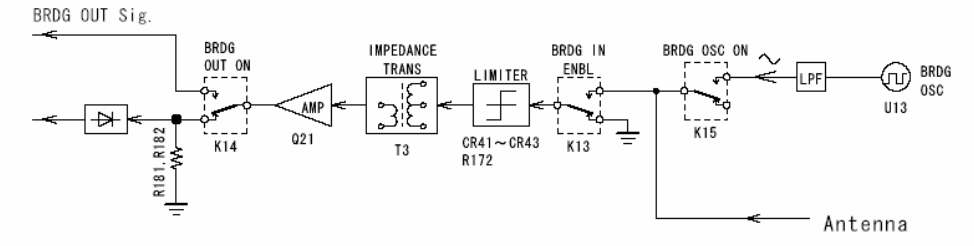


Figure 1.5 Block Diagram of Bridge Amplifier

1.6 CPLR CONTROL (CDC-1083B)

CDC-1083B CPLR CONTROL is composed of CPU, CPLD, EEPROM, analog interface, RS232C interface driver, reference voltage generator, pressure sensor, temperature sensor and voltage sensor. The card administers all operations to be needed and monitoring the state of the unit. Figure 1.6 shows block diagram of the card.

Functions of this card are as follows:

- Serial communication with RX/EX
- Observation of the discrete signals from RX/EX
- Setting of operation mode of PA according to frequency and emission mode
- Observation of the PA alarm
- ON-OFF control of relays of RF matching network
- Observation of impedance signals fed from SENSOR & RLY DRV card
- Measurement and observation of pressure, temperature and power supply voltage
- Storing, restoring and initializing the tuning parameters in the EEPROM
- Serial communication with external PC via RS-232C port
- Execution Built-In-Test (BIT), reporting and recording of the results of BIT

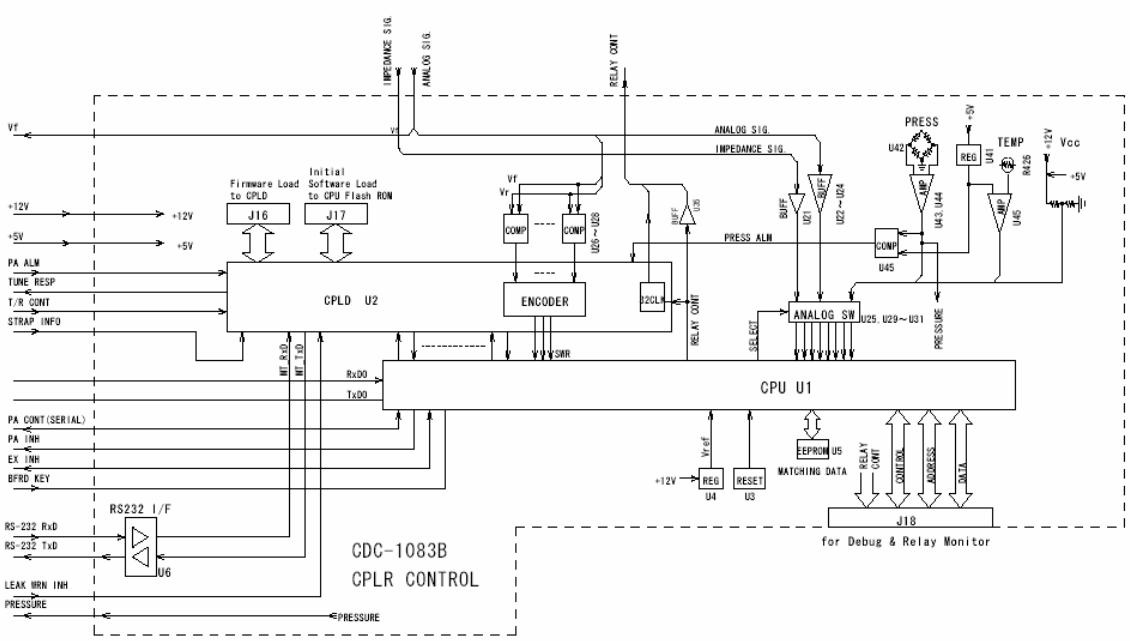


Figure 1.6 Block Diagram of CPLR CONTROL

CPU U1 has a main role in the unit. The H8/3067 series is adopted as the CPU. It is the highly efficient single chip microcomputer, which makes 32-bit H8/300H a core and integrates the peripheral functions needed for system configuration. The H8/300H is 32-bit configuration and is capable of 16Mbytes linear address area. The integrated peripheral functions in the device is composed of 128kbytes ROM, 4kbytes RAM, 16-bit and 8-bit timers, programmable pattern controller (TPC), watch dog timer (WDT), 3-channel serial communication interfaces (SCI), 10-bit A/D converter, D/A converter, I/O ports, DMA controller etc. The CPU can flexibly be changed its configuration and operation mode. The CPU has seven operation

modes that change address and data bus widths. The ROM of adopted CPU in this card has 128kbyte flash ROM that enables users to rewriting its program. The maximum operating frequency is 20MHz. External address and data buses are not used for reduction wide band noise in this card.

CPLD U2 is flexibly programmable logic device that enables users to rewriting hardware configuration. The CPLD has 72 macro cells and 1600 usable gates and maximum system frequency is 67MHz. In this card the CPLD is applied to interface between the CPU and other card or other LRUs.

EEPROM U5 is non volatile memory which has the capacity of 32kbytes and three lines interface. The device directly connected with the CPU. The device stores tuning parameters, strap information, some of the latest tuning failure results and BIT results. The recorded data are able to read by the Maintenance Software "khf1050.exe" via RS-232C port J10522 and some of them are reported to RX/EX. The recorded and read data formats are available in the SRD of ACP.

All analog signals are fed to the CPU and converted from analog voltage to digital data by incorporated 10-bit A/D converter. The converter has 8-port channels selected by time division. Following signals are input to the converter via analog switched U29 to U31;

- Forward power voltage fed from SENSOR & RLY DRV: Vf
- Reflected power voltage fed from SENSOR & RLY DRV: Vr
- Magnitude of RF input voltage (only during tuning operation): Vin
- Magnitude of RF input current (only during tuning operation): Iin
- Absolute Kelvin temperature: Temp
- Magnitude of phase difference between RF voltage and current (only during tuning operation): Angle
- Absolute internal air pressure: Press
- Combined voltage of 12V and 5V regulated power supply: Vcc
- Output level of bridge amplifier: V-BRDG
- RF peak voltage of internal 50 Ohm resistor on the SENSOR & RLY DRV: Vdum

These signals are adopted for judgments to determine the tuning algorithm and failures detection of pressure, power supply voltage, bridge amplifier and sensor.

RS-232C interface driver IC U6 converts bi-directionally between differential signals and TTL level signals. The TTL signals are provided to the CPU via the CPLD.

Reference voltage generator U4 generates stable 5Vdc and provides the CPU it for A/D converting.

Pressure and temperature sensors and voltage monitor is described in "1.4 Sensors".

Connector J16 is a port for programming CPLD with dedicated cables and parallel port of PC.

Connector J17 is a port for programming CPU with dedicated cables and writer and serial port of PC.

Connector J18 is a port for debugging software operation of the CPU and direct monitoring the state of relays via the CCP-260A DEBUG BOARD.

1.7 PS & INTERFACE (CBL-103)

CBL-103 PS & INTERFACE card is composed of power supply switching circuit, voltage regulators, voltage-current converter for APC, RS422 interface driver and surge protection for interface signals. The card supplies 28V, 12V and 5V DC power to all cards and has all interface connectors to communicate with other LRUs.

The power supply switching circuit is comprised of a hot swapping controller IC U51, a switching N-channel FET Q2, a resistor for detecting excessive direct current, an overvoltage detector, an undervoltage detector and PWR CONT controller.

If the PWR CONT pin is short-circuited with the PWR CONT RTN pin, the FET Q1 will turn off. And if the voltage of U51-#1 is over about 1.25Vdc, the FET Q2 will turn on. As a result, 28Vdc power will be supplied to relays and regulator ICs U52 and U53 that are used by CPLR CONTROL card and SENSOR & RLY DRV card. The power on voltage is determined by a voltage divider comprised of R43 and R44. That is to say, the threshold undervoltage of primary power supply is 15 to 16Vdc.

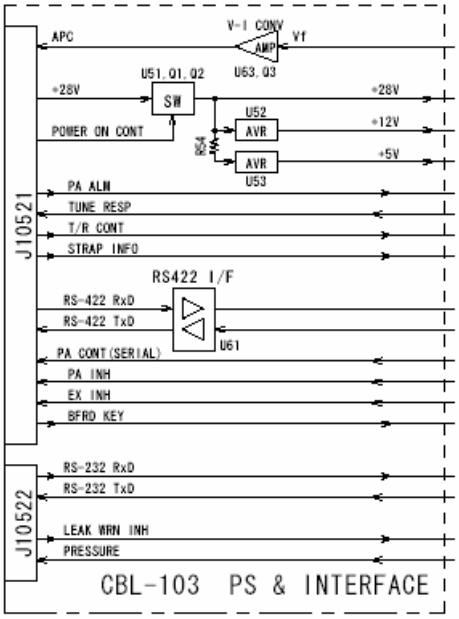


Figure 1.7 Block Diagram of PS & INTERFACE

If the voltage of U51-#5 is over about 1.25Vdc, the FET Q2 will turn off to protect internal circuit devices from broken due to excessive voltage. The threshold voltage is determined to 36 to 38Vdc by series connected Zener diodes CR83 and CR84. This pin is also used for determining the time interval from off state caused by current trip to turning on. The time interval is determined to approximate 180mSec by timing capacitors C48 and C49.

Resistor R45 detects excessive load current. If the current is over 4.5 to 5.1Adc, U51 shut off the FET Q51. Then U51 will try to turn Q2 on at approximate 180mSec intervals until the cause of current trip will be removed.

Two voltage regulator ICs U52 and U53 generate regulated 12Vdc and 5Vdc each. Output voltage of 12Vdc is determined by voltage divider comprised of R51, R52 and R53. The output voltage is controlled as the voltage across the U52-#2 and U52-#3 is approximate 1.2Vdc. As a result the output voltage is 12Vdc approximately.

The voltage-current converter for APC is comprised of a rail-to-rail operational amplifier IC U63 and an NPN transistor Q3. The circuit converts the forward power voltage Vf fed from SENSOR & RLY DRV to direct current for APC feedback system during tuning operation of the unit. The output current is proportional to the “2-Vf”. For example; If Vf is 0V, output current is approximate 20mA. And if Vf is approximate 2Vdc, the current is nearly 0mA. So, when the wire between PA and coupler is cut, namely current is 0mA, PA will reduce its output power. This system will protect both PA and coupler from broken due to excessive RF output power during tuning operation.

RS-422 interface driver IC U61 converts bi-directionally between differential signals and TTL level

signals. The TTL signals are provided to CPU on the CPLR CONTROL card.

Opto-coupler interfaces are adopted for all discrete input signals excluding RS-422 receiving signal and PWR CONT signal to isolate internal circuits from noisy exterior.

All discrete output signals fed from CPLR CONTROL card are outputted to RX/EX and PA via this card.

All discrete input and output pins are protected against induced surge voltage by inserting series resistors and shunt surge absorbers (Silicon Transient Voltage Suppressor: TVS) excluding primary power input. Figure 1.8 shows three kinds of surge protection circuits adopted on this card.

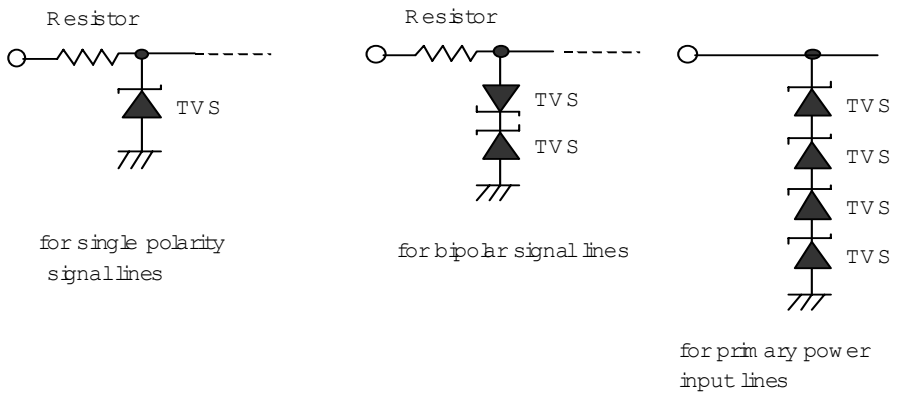


Figure 1.8 Surge Protection Circuits of PS & INTERFACE Card

This card has two interface connectors that are directly mounted for interfacing with external devices. Sub D connector J10521 is adoped for communicating with RX/EX and PA, and J10522 for a serial port of external PC.

1.8 Interface Signals Descriptions

All discrete interface signals of CONTROL connector J10521 are described below Table 1.2 and them of TEST connector J10522 are described in Table 1.3. For details refer to the SRS document.

Table 1.2 Interface Signal Description of KAC 1052 Antenna Coupler J10521

Pin No	Indicate	Source /Destination	I/O	Description	Property
-#20	PRI PWR	External	Input	+27.5 Vdc Primary Power	Power In
-#1	PRI PWR RTN	External	N/A	Primary Power Return	GND
-#21	PWR CNT	External	Input	Power ON/OFF Control	Low in active
-#2	PWR CNT RTN	External	N/A	Power ON/OFF Control Return	GND
-#11	RC COM	RX/EX	Input	Common for Inputs from RX/EX	+15V
-#27	MATCH ON	RX/EX	Input	Matching Circuit ON	Low in active
-#28	BRDG ON	RX/EX	Input	Bridge Amplifier ON	High in active
-#30	BFRD KEY	RX/EX	Input	Buffered Key ON	Low in active
-#33	PA BFRD KEY	PA	Output	Buffered Key ON	Low in active
-#36	PC COM	PA	Input	Common for Inputs from PA	+15V
-#34	PA ALM #1	PA	Input	PA Alarm Signal #1	High in active
-#35	PA ALM #2	PA	Input	PA Alarm Signal #2	High in active
-#3	STRAP A	External	Input	Strap A for Antenna Kind Information	Low in active
-#22	STRAP B	External	Input	STRAP B for Antenna Kind Information	Low in active
-#4	STRAP COM	External	Input	Strap Common	GND
-#23	SPARE	N/A	I/O	Spare Interface Port	Low in active
-#29	CR COM	RX/EX	Output	Common for Outputs to RX/EX	+12V
-#10	TUNE FAIL	RX/EX	Output	Tune Fail Signal	High in active
-#12	TUNE REQ	RX/EX	Output	Tune Request Signal	High in active
-#9	EXTR INHB	RX/EX	Output	Transmission Inhibition of RX/EX	High in active
-#32	CP COM	PA	Output	Common for Outputs to PA	+12V
-#15	PA INHB	PA	Output	Transmission Inhibition of PA	High in active
-#16	PA SI	PA	Output	Serial Data for Setting PA Mode	High in active
-#17	PA SCK	PA	Output	Serial Clock for Setting PA Mode	High in active
-#18	PA RCK	PA	Output	Serial Strobe for Setting PA Mode	High in active
-#19	PA ALM RST	PA	Output		Low in active
-#6	RCA	RX/EX	Input	Serial Receive Data +	RS-422 +
-#24	RCB	RX/EX	Input	Serial Receive Data -	RS-422 -
-#7	CRA	RX/EX	Output	Serial Send Data +	RS-422 +
-#25	CRB	RX/EX	Output	Serial Send Data -	RS-422 -
-#8	BUS COM	RX/EX	N/A	Common for RS-422 BUS	GND
-#14	APC H	PA	Output	APC Feedback +	Current loop
-#37	APC L	PA	Output	APC Feedback -	Current loop return: GND
-#26	EXTR COM	RX/EX	N/A	Exciter Common	GND
-#5, #13, #31	FG	N/A	N/A	Frame Ground	GND

Table 1.3 Interface Signal Description of KAC 1052 Antenna Coupler J10522

Pin No	Indicate	Source /Destination	I/O	Description	Property
-#3	TEST TXD	External PC	Output	Serial Send Data +	RS-232C
-#2	TEST RXD	External PC	Input	Serial Receive Data	RS-232C
-#5	TEST COM	External PC	N/A	Test Common	GND
-#9	LEAK WRN INH	External	Input	Air Leak Warning Inhibition	Low in active
-#7	PRESS	External	Output	Absolute Pressure Level	Analog Voltage
-#4	GND	N/A	N/A	Ground	GND