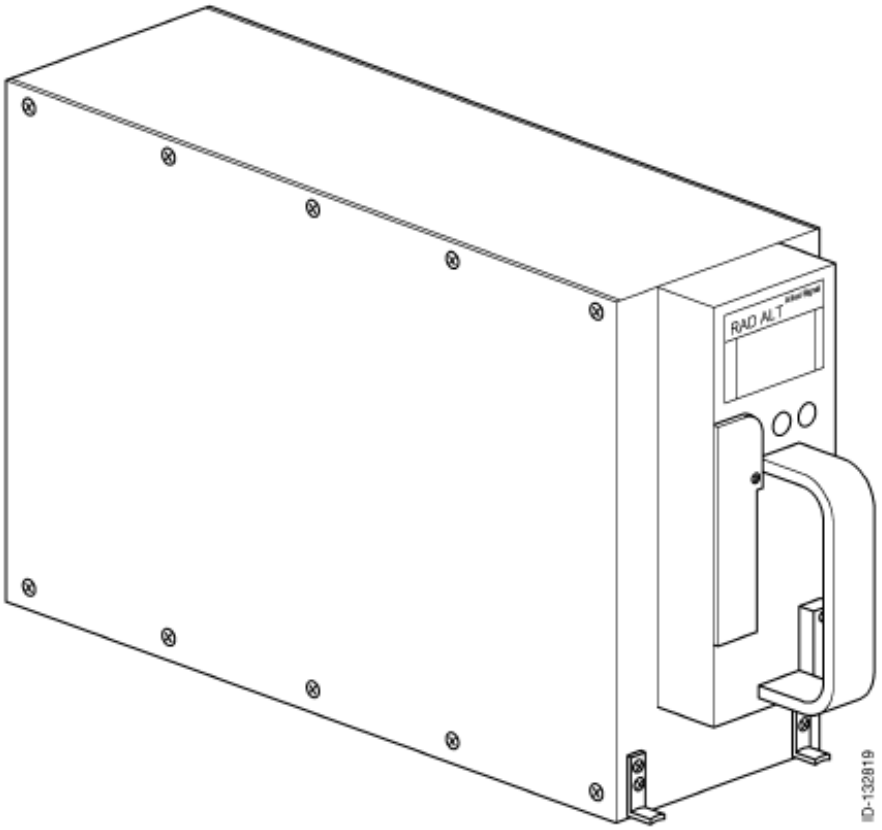


ALA-52B Radio Altimeter
Figure 1

NOTE: This is preliminary version of the Component Maintenance Manual that will be released at later date. The information is adequate as is, but any attached notes and dates will be incorporated in the future version. Views will be cleaner as well, as these are attached pages, which reduce clarity.

NOTE: Honeywell Part Numbers; 066-50007-0432 and 066-50007-0531 are identical hardware. All references to 066-50007-0432 apply also to 066-50007-0531, which was the part number tested.

DESCRIPTION AND OPERATION

1. General

This section contains descriptive information covering the ALA-52B Radio Altimeter, hereafter referred to as the ALA-52B, the radio altimeter, or by its full nomenclature. The ALA-52B Radio Altimeter is illustrated in Figure 1.

A. Purpose of Equipment

The ALA-52B Radio Altimeter is part of the Honeywell International Inc. ALA-52B Radio Altimeter System. A complete description of the system, including installation information, is given in ALA-52B Radio Altimeter System Maintenance Manual I.B. 1152-2 (34-42-04).

The ALA-52B is a lightweight, solid-state, digital airborne altimeter designed to provide accurate, digital height measurements above terrain during aircraft approach, landing, and climb-out phases. It is a low-range altimeter that incorporates two different and independent microprocessors, one of which performs the primary altitude computation while the second independently verifies the computation by comparison.

B. Equipment Part Numbers

Honeywell part numbers assigned to various configurations of the ALA-52B Radio Altimeter are given in Figure 4.

C. Related Publications

Figure 2 lists the publications covering the ALA-52B and test equipment supporting the system.

PUBLICATION	HONEYWELL IDENTIFICATION NUMBER	ATA IDENTIFICATION NUMBER
ALA-52B Radio Altimeter System Maintenance Manual	I.B. 1152-2	34-42-04

Related Publications
Figure 2

2. Configurations Available

ALA-52B Radio Altimeter

Figure 4 lists the available configurations of the ALA-52B and the features contained in each configuration. Figure 5 contains a brief description of each feature.

HONEYWELL PART NUMBER 066-50007	FEATURES			MAXIMUM WEIGHT (LBS/KG)
	BASIC UNIT	FAULT MEMORY	CMC COMPATIBLE	
-0101	X	X	X	8.6/3,9
-0111	X	X	X	8.6/3,9

ALA-52B Radio Altimeter, Configurations Available
Figure 4

ADD: -0531 same X's as previous dashes Weight:9.1 lbs. (4.1 Kg)

RE	DESCRIPTION
Basic Unit	Airborne solid-state radio altimeter that incorporates two different and independent microprocessors, one of which performs the primary altitude computation while the second independently verifies the computation by comparison. The altitude information is supplied to the AFCS and height displays on the instrument panel. Meets RTCA DO-160X lightning protection and 200ms power interrupt transparency requirements. Front panel LCD displays unit's characteristics (part number, serial number), BITE status with fault location help pages, line maintenance values with help pages, and software data loading help screens.
Fault Memory	A nonvolatile, single-chip fault memory that allows the recording of faults associated with a particular flightleg. Sixty-four flight legs are available with each flight leg made up of a flightleg information header containing a fault record section for recording ten airborne faults and three ground faults. When all flight legs have been used, the oldest flight leg shall be reused.

ALA-52B Features
Figure 5 (Sheet 1 of 2)

FEATURE	DESCRIPTION
CMC Interface	The ALA-52B interfaces fault memory and BITE data between radio altimeter and line maintenance Centralized Maintenance Computer (CMC) for the purpose of extracting maintenance information and initiating tests. Designed to conform with ARINC 429 interfaces, and ARINC 604.

ALA-52B Features
Figure 5 (Sheet 2)

3. Leading Particulars

A. Unit Specifications

CHARACTERISTICS	DESCRIPTION
Operating Range of Altitudes	-20 to 7,500 feet
Accuracy	± 1.5 ft. or 2% whichever is greater
Data Outputs	ARINC 429 Range, and CMC Interface
Frequency Range	4.235 to 4.365 GHz
Frequency Deviation	130 MHz
Transmit Power	+26 dBm (Nominal at antenna port)
Antennas	One transmit, one receive, 11 dB gain
Aircraft Installation Delay	40, 57, 80 ft
Pitch Limits	± 20°
Roll Limits	± 40°
Doppler Error	Compensated using dual slope FM ramp
Self-Test	Automatic In-flight, Manual from discrete, ARINC 429, or front panel
Integrity Monitoring	Continuous self-monitoring establishes operational status at all altitudes
Fault Reporting	Conforms to manufacturer formats
Data Loading	Data can be entered via a flash memory card
Data Recording	Real time data can be recorded on a flash memory card
Power Requirements	30 W, 115 VAC, 380 to 420 Hz
Warm-up time	Stable operation after 6 seconds
Weight	9.1 lbs. (4.1 Kg)
Form Factor	ARINC 600 3 MCU
Dimensions	14.04"L X 3.56"W X 7.64"H
Temperature, operating	- 40°C to + 70°C
Temperature, storage	- 65°C to + 85°C
Humidity	0 – 95% Relative Humidity
Altitude	50,000 ft above mean sea level
Certification	TSO C-87, ETSO 2C87

Leading Particulars for -0432 and -0531 Units
Figure 9

C. Environmental Certification for -0432

(1) The ALA-52B Radio Altimeter meets the environmental conditions of the Radio Technical Commission for Aeronautics (RTCA) document number DO-160F Environmental Conditions and Test Procedures for Airline Electronic/Electrical Equipment and Instruments. The environmental certification categories of the ALA-52B are

[A2/D2]ZBAESZXXXXXFXAA(CF)XZZXAR(CF)ZCWMZZZZZXXAC

TEST/CHAPTER of DO-160F		CATEGORY APPLICABLE
Temperature (High/Low)	4.5	Cat. A2
In Flight Loss of Cooling	4.5.5	Cat. Z
Altitude/Pressure	4.6	Cat. D2
Temp Variation	5.0	Cat. B
Humidity	6.0	Cat. A
Operational Shocks	7.2	Cat. E
Crash Safety	7.3	Cat. E (Impulse Test Only)
Constant Acceleration	7.3.3	Cat. E Type R
Vibration	8.0	Cat. S
Vibrations HPC	8.6	Cat. H, Curve R
Explosion	9.0	Cat. X
Waterproofness	10.0	Cat. X
Fluids Susceptibility	11.0	Cat. X
Fungus Resistance	13.0	Cat. F
Salt Spray	14.0	Cat. X
Sand and Dust	12.0	Cat. X
Magnetic Effect	15.0	Cat. A
Power Input and Voltage Spikes	16.0	Cat. A(CF) XZZX
Voltage Spikes	17.0	Cat. A
AF Conducted Susceptibility	18.0	Cat. R (CF)
Induced Signal Susceptibility	19.3	Cat. ZC
RF Susceptibility	20.0	Cat. W
RF Emissions	21.0	Cat. M
Lightning Induced Transient Susceptibility	22.0	Cat. ZZZZZ
ESD (Electrostatic Discharge)	25.0	Cat. A
Flammability/Smoke/ Toxicity	26.0	Cat. C

Note: Category "X" = Tests not applicable.

Environmental Categories for -0432 Units.
Figure 11

4. Brief Description of Equipment

A. Mechanical Description

The ALA-52B Radio Altimeter is contained in a standard ARINC Characteristic 600, 3-MCU case with side panels. Electrical connection to the aircraft wiring is made through an ARINC 600, series number one, multiple-section connector centered vertically.

Figure 8 lists all modules and assemblies in the unit. Figure 9 illustrates the location of the modules and assemblies.

ADD: Rear Interconnect Assembly Unit -0531

ADD: 300-60171-0503

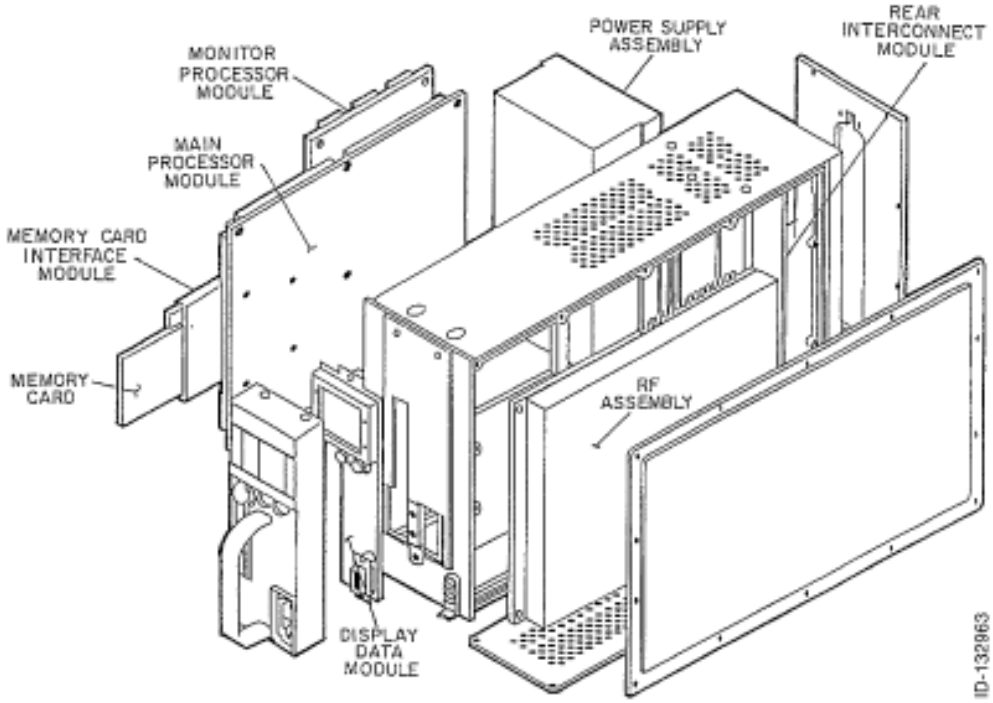
MODULE/BOARD	HONEYWELL PART NUMBER	REFERENCE SERIES	CONNECTORS
Rear Interconnect Assembly	300-60171-0502	1000	W2, J1001
Rear Interconnect Module	300-90246-0502	1200	P1001, J1212, J1213
Main Processor Module	300-90240-0551	2000	J2011 thru J2015, J2024 thru J2028
Power Supply Assembly:	300-60148-0501	3000	W3, W23
Input Filter Module	300-90238-0502	3100	J3102, J3108
Capacitor Module	300-90237-0501	3100	EP1, EP2
Power Supply Module	300-90236-0511	3300	P3302, P3310, P3313
Front Housing Assembly	300-60184-0502	4000	W5
Display Data Module	300-90[illegible]	[illegible]000	J4017, J4032
[illegible]y Card Module	300-90273-0504	5000	J5025, J5030
Monitor Processor Module	300-90234-0501	6000	J6018, J6043, J6044, J6045
RF Assembly:	[illegible]60173-0501	9000	W4, W6, W7, W20, W21
RF Control Module	300-90306-0501	8000	J8010, J8020, J8021, J8027
RF Module	300-90254-0501	9000	J9039, P9033

ADD 300-90234-0502

Alternate for -011 and -0531

All unit Dashes But -0531

ADD: RF Assembly -0531 Unit: 69000712-001;9000;W4, W6,W7,W20,W21
RF CCA Assembly; 69000709-001;9000;J10(W7), J20(W4), J21(W6) J1005 (W21), J1004(W20)



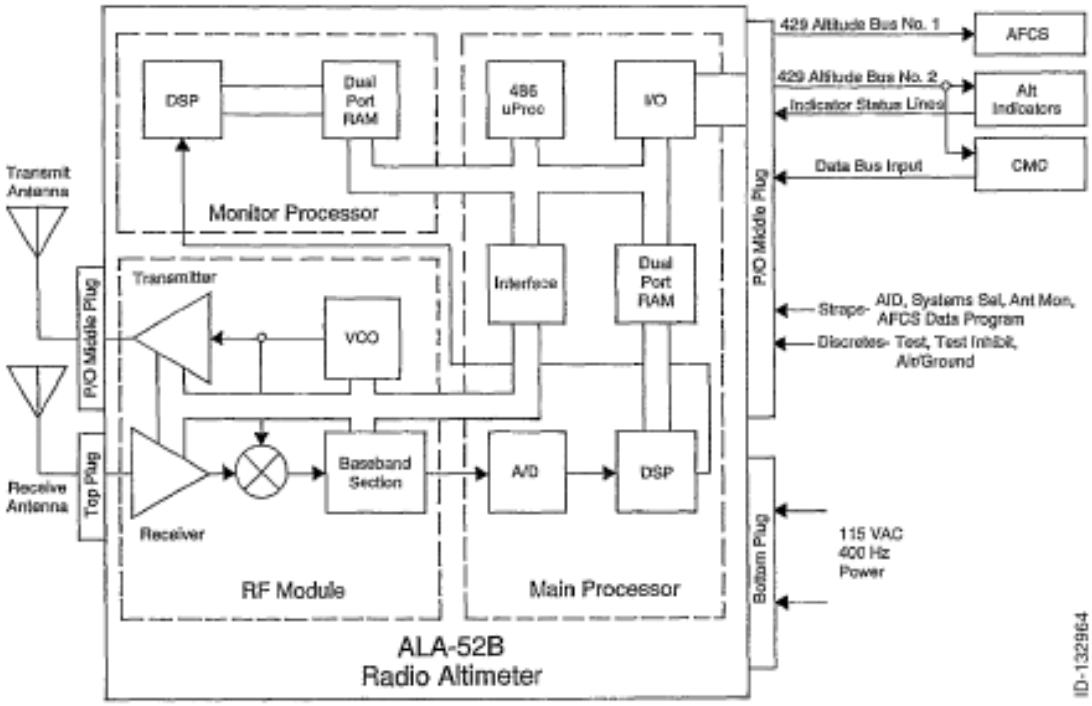
Module and Assembly Location
Figure 9

B. Electrical Description

Figure 10 illustrates the ALA-52B interconnections in the aircraft. Antenna cabling is determined by the setting of the Aircraft Installation Delay (AID) strap pins in the middle plug. The round trip delay from ALA-52B transmitter port to receiver port is set to the AID value for the return signal that corresponds to a reading of zero feet.

The middle plug also contains the ARINC 429 Altitude Bus outputs that connect to the Automatic Flight Control System (AFCS), Cockpit Altitude Indicators. Specially furnished data recording equipment in the form of a "flash card" is available for in-flight test though normally not required. For most installations, ARINC 429 bus number 1 is connected to the Flight Management Control Computer, and ARINC 429 bus number 2 is connected to the Altitude Indicators on the instrument panel. ARINC 429 I/O is also provided for interface with the Centralized Fault Display System (CFDS).

Besides the AID strap pins, System Select strap pins are provided to designate the installed equipment as unit number 1, 2, or 3. The Antenna Monitor strap pin enables antenna monitoring, and the AFCS Data Program strap pins set the mode of operation of the ARINC 429 Altitude buses in case an ALA-52B failure is detected.



ALA-52B Radio Altimeter, Simplified Block Diagram
Figure 10

Discretes from other systems provide test activation, the inhibiting of test, and air/ground indication.

An RS-232 port on the ALA-52B front panel (not shown) provides a ramp test, data loading, and data recording interface.

5. Theory of Operation

A. Overall Operation

The basic objective of the ALA-52B is to provide accurate height above the ground terrain with a high degree of integrity during the approach, landing, and climb out phases of aircraft operation. This is accomplished by transmitting a frequency modulated continuous signal to the ground.

The frequency modulation is a linear dual slope ramp. During the time required for the transmitted signal to bounce off the ground and return to the aircraft, the transmitted signal has changed frequency. When the transmitted signal is mixed with the return signal bounced up from the ground, a baseband signal is produced at a frequency that represents the difference between the transmitted and returned signal frequencies. Since this difference frequency is proportional to the delay between the transmitted and received signals, it is also proportional to the altitude of the aircraft.

The difference frequency signal is amplified sufficiently and applied to two independent digital signal processors (DSP). The amplifier gain increases with frequency to compensate for attenuation due to increased range. The DSPs perform fast Fourier transforms (FFT) and extract the lowest peak frequency. This process is repeated periodically. The results are averaged and verified in the microprocessors before being supplied to the 429 altitude data buses.

The verified digital altitude information is then routed to the peripheral equipment where it is further processed for pilot display, ground proximity warning, and Automatic Flight Control System (AFCS) usage.

B. Block Diagram

In the following paragra

ADD: This is a general block diagram of te RF section that represents the two variations of RF used. Please see detailed description for more information.

(1) RF Module

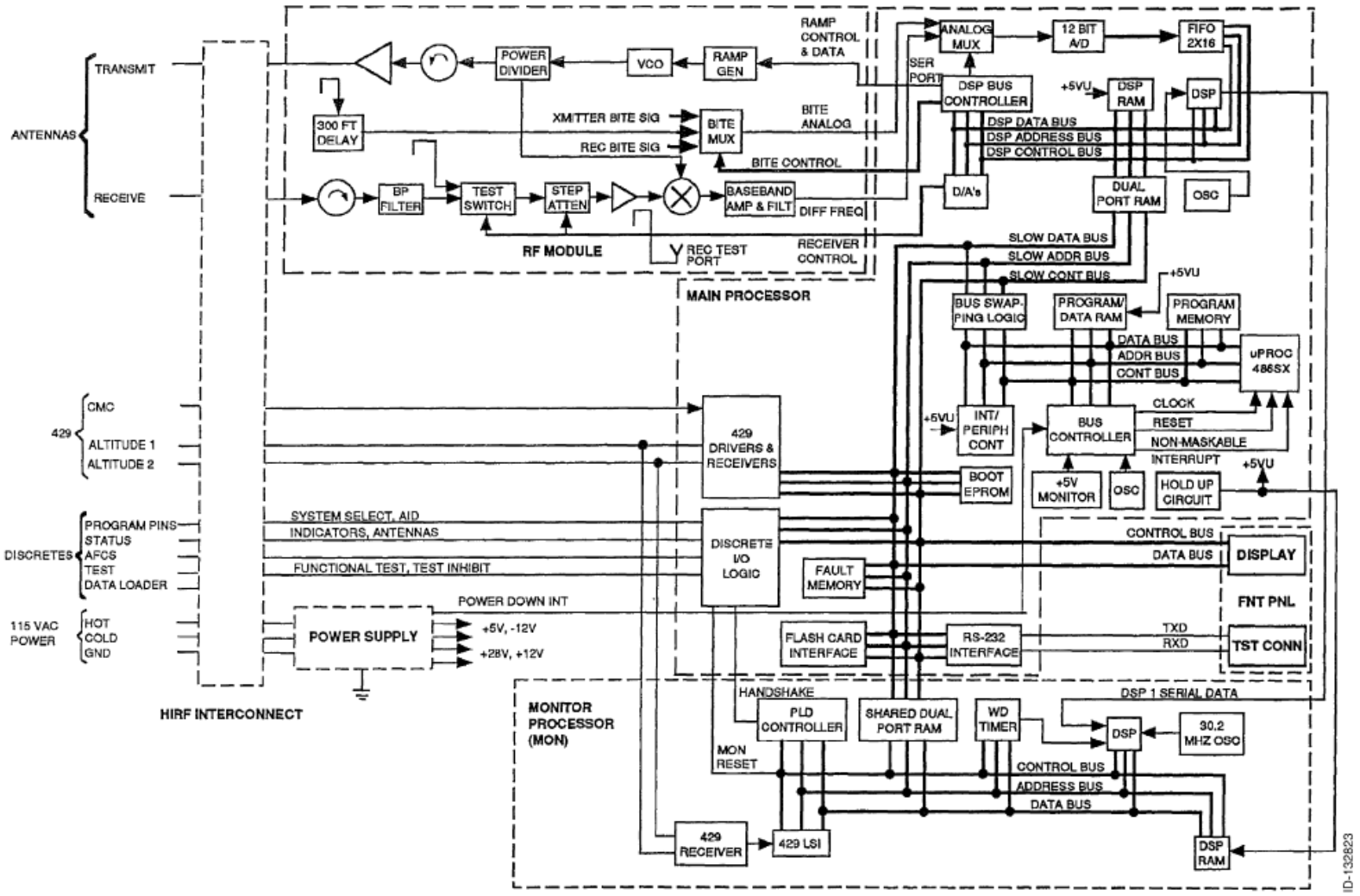
The RF module, controlled by the main processor, transmits and receives the altimeter signal. BITE circuitry is included to both test and continuously monitor the RF module functions.

The process of generating a transmission begins with the voltage controlled oscillator (VCO) output which is split between the transmitter and receiver local oscillator (LO). The transmitted signal is radiated from the transmit antenna located on the underside of the aircraft.

The transmitted signal, after bouncing off the ground below the aircraft, is collected by the receive antenna.

An RF switch is provided to channel the calibrated 300-foot delay element signal through the receiver during self test. The self-test operation performs a full transmitter and receiver check. The self-test operation is activated manually by the pilot or automatically when the ALA-52B is acquiring a signal.

The received signal is mixed with the VCO signal, producing a difference frequency signal that is amplified and fed to an analog-to-digital (A/D) converter on the main processor module.



ALA-52B Detailed Block Diagram

(2) Main Processor Module

The main processor module controls the radio altimeter operation, performs signal processing of the difference frequency and test signals, and controls the aircraft interfaces and the data displayed on the front panel.

The main processor provides all the control signals to generate an up-down linear ramped frequency-modulated carrier wave output, determines the mode of operation, and provides all RF control signals. It also processes the difference frequency signals digitally. The return signal and test signals are converted to digital data streams using an A/D converter. In addition, the main processor module performs BITE, I/O, flash card interface, and monitor processor module interface functions.

The main processor module is divided into three major sections: the digital signal processor (DSP) section, the 486 central processing unit (CPU) microprocessor section, and the input/output (I/O) section.

When replacing the Main Processor Module, refer to paragraph 6., Alignment Procedure, in Section 100, "Testing and Troubleshooting" and paragraph 3., SW Data Recording and Loading in Section 600, "Repair" of this manual.

(a) DSP Section

The DSP section is used to process the analog outputs from the RF module and to generate some of the control signals to the RF module for transmit modulation, automatic gain control, and test signals.

The difference frequency signal from the RF module is digitized using a 12-bit A/D converter. The A/D converter is also used to monitor signals from the BITE test points on the RF module and the power supply voltages. The digitized data from the A/D converter is stored in a first-in first-out (FIFO) memory device which is accessed by the DSP.

The DSP processes the difference frequency and calibration frequency into altitude information.

Data is exchanged with the CPU section through a dual-port random access memory (RAM), providing maximum throughput of both processors.

(b) CPU Section

The CPU section does frame-to-frame processing of the altitude data from the DSP section providing the resulting altitude to the I/O section.

The microprocessor in the CPU section controls all major functions of the radio altimeter. Programmable logic devices serve as the microprocessor controller and provide the interfaces to the memory devices (boot routine, program, fault, and data), the data recorder/data loader flash card, and the front panel display driver.

(c) I/O Section

The I/O section provides the two ARINC 429 altitude outputs as well as ARINC 429 interfaces with other aircraft systems including the Centralized Fault Display System (CFDS).

All discrete inputs external to the radio altimeter are processed by the I/O section. The I/O section also generates the external discrete outputs, which are buffered to prevent damage to the processor circuitry.

The I/O section also contains an RS-232C production test interface. This test interface is also used to update serial number, part number and configuration memory as applicable, utilizing a stand-alone Production Test Mode (PTM) tool or integrated PTM tool in the Quantum Line Tester, when the Main Processor Module is replaced.

(3) Monitor Processor Module

The monitor processor module provides a second signal processing path using a Digital Signal Processor (DSP). The DSP processes the received signal and calibration signal supplied in digital form from the Main Processor A/D converter. Also present are a clock, an ARINC 429 receiver/selector, and static memory.

The primary function of the monitor processor module is to provide the ALA-52B with the integrity that permits Category III operations by acting as an independent monitor for the main processor altitude computations.

(4) Power Supply Module

The power supply module is a self-contained, high-efficiency, switching power supply that converts the 115 VAC, 400 Hz A/C power into the required +5Vdc, +12Vdc, -12Vdc, and +24Vdc operating voltages. A power-down interrupt provides advanced notice of a power loss allowing the processors to temporarily retain their status.

(5) Rear Interconnect Module

To prevent high intensity radiated fields (HIRF) from entering through rear connector cables, an HIRF compartment is formed in the rear of the ALA-52B. The signal and power cables are filtered by using discrete and distributed filter elements and limiting devices on the rear interconnect module located inside this HIRF compartment. The filtered lines are then fed to the appropriate points in the ALA-52B.

The ALA-52B is packaged in an aluminum casting. This seamless main frame ensures that HIRF cannot enter the unit through structural seams. The slots formed by the removable side covers are sealed against HIRF with metal covers.

(6) Display Data Module

The display data module is mounted behind the front panel and provides an interface to an operator through a low-power liquid crystal display (LCD), which is visible from the front of the ALA-52B. In addition to the LCD, the module contains LED "Light Box" backlighting, temperature compensation circuitry, and a PC board containing an associated LCD driver, two pushbutton switches, and a D-sub, nine-pin, RS-232 serial type connector.

The RS-232 front panel connector is used for testing the ALA-52B through a compatible test set or test panel.

The LCD is a bit-mapped display capable of displaying alphanumeric and graphic symbols. Simple messages written in plain language minimize the potential for misunderstanding or incorrect interpretation. The LCD displays the following:

- Part Number/Software Identification
- Status
- Results of Level 1 BITE Tests
- Maintenance Help Pages
- Shop Maintenance Data
- Flight Fault Memory Contents
- Software Loading Status
- Airline Unique Maintenance Messages.

(7) Memory Card Module

The memory card interface is used to load software program data into the CPU or record software program data from the CPU. The memory card module supports Intel® Series 2 FLASH cards through the front panel Personal Computing Memory Card Interface Adapter (PCMCIA) slot. Intel® Series 2 cards with capabilities ranging from 4, 10, and 20 megabytes (up to 64 megabytes, when available) are all supported. The FLASH card is inserted through the front panel. In one mode, data stored on the flash card memory module is used to update program or data memory in the ALA-52B. In another mode, the flash card functions as a data recorder for the software program stored in the CPU.

C. Detailed Theory

(1) General

The following paragraphs describe detailed circuit operation. Each module or group of modules in the ALA-52B is described. Refer to the schematic diagrams in the Testing and Troubleshooting section of this manual.

(2) Rear Interconnect Module (refer to Figure 181)

The rear interconnect module, in addition to providing antenna, power, and signal/data paths between the rear connector of the unit and the ALA-52B internal circuitry, is designed to eliminate or suppress external high intensity radiated fields (HIRF) and/or lightning-induced voltage transients.

To prevent HIRF from entering through rear connector cables, an HIRF compartment is formed in the rear of the ALA-52B. The signal and power cables are filtered by using discrete and distributed filter elements and limiting devices on the rear interconnect module located inside this HIRF compartment. Each active rear connector pin has a ferrite bead on it, which is not shown on the schematic diagram. Each unused pin is plugged by a special insert on the rear connector. The filtered lines are then fed to the appropriate points in the ALA-52B.

The power supply input lines are straight through connections between rear connector J1001 pins BP_2, BP_3, and BP_8/11 to power supply connector J1203 pins 3, 5, and 1, respectively. Capacitor C1201 provides filtering of the ac line.

The I/O signal lines are grouped on the schematic diagram into four categories: 429 inputs, 429 outputs, discrete inputs, and discrete outputs.

Each of the input signal lines is protected by a 100-ohm resistor/5-volt transguard low-pass filter circuit. Each of the output signal lines is protected by an 18-ohm resistor/30-volt transguard low-pass filter circuit.

Transguards CR1201 thru CR1239 are zinc oxide based ceramic semiconductor devices. They are similar to back-to-back Zener diodes, except that they have non-linear current/voltage characteristics with the added advantage of greater current and energy handling capabilities relative to their small physical size.

(3) Main Processor Module (refer to Figure 182)

The main processor module controls the radio altimeter operation, performs signal processing of the difference frequency and test signals, and controls the aircraft interfaces and the data displayed on the front panel.

The main processor module is divided into three major sections: the I/O section, the DSP section, and the 486 microprocessor (CPU) section.

When replacing the Main Processor Module, refer to paragraph 6., Alignment Procedure, in Section 100, "Testing and Troubleshooting" and paragraph 3., SW Data Recording and Loading in Section 600, "Repair" of this manual.

(a) I/O Section

The I/O section of the main processor module provides the necessary signal level conversion (bipolar to TTL and TTL to bipolar) and data format conversion (serial to parallel and parallel to serial) circuitry required to transfer ARINC 429 and discrete input/output information between the I/O module and the main processor data bus.

1 ARINC 429 Inputs

Two standard external 429 inputs (429_INPUT_FL_TST_A/B and CFDS_#1_INPUT_A/B) and one optional external 429 input (DATA_LOADER_INPUT_A/B) are applied through J2012 pin pairs 45/46, 41/42, and 43/44 to 429 receivers U2026, U2032, and U2042 on the main processor module. ICs U2026 (receivers #1 and #2), U2032 (receivers #3 and #4), and U2042 (receivers #5 and #6) are dual 429 receivers used to convert the bipolar input signals from standard 429 levels (+12 to -12 V dc) to standard TTL levels (0 to +5 V dc) required for proper operation of 429 LSI ICs U2057 and U2063.

NOTE: Because 429 signal processing is identical for all three inputs, only one of the signal paths (429_INPUT_FL_TST_A/B) is described in the following discussion.

The TTL level serial data output from pins 8 and 5 of 429 receiver U2026 is applied to input pins 22 and 21 of 429 LSI U2057, where it is shifted into internal registers and stored as 8-bit parallel bytes.

When a valid word is received, a processor interrupt (IOINT*) is generated at pin 27 of U2057. The processor responds to this interrupt by addressing 429 LSI U2057 through pins 6 and 7 and asserting IOCS1* (pin 5) low and WR* (pin 2) high to select the chip and read the data byte (D0-D7) onto the I/O data bus. The IODB0-IODB7 I/O data bus lines are applied to the lower section of bidirectional 429 data buffer U2049, which interfaces 429 LSI #1 (U2057) to the processor slow data bus.

2 ARINC 429 Outputs

Two standard external 429 outputs (OUTPUT_#1_A/B and OUTPUT_#2_A/B) and one optional external 429 output (DATA_LOADER_OUTPUT_A/B) are transmitted through the I/O module through the I/O section of the main processor module.

NOTE: Because 429 signal processing is identical for all three outputs, only one of the signal paths (OUTPUT_#1_A/B) will be described in the following discussion.

To transmit, the main processor places a data byte on the I/O data bus through bidirectional 429 data buffer U2049, addresses and selects 429 LSI #1 (U2057), and asserts WR* low. The data byte present at the D0-D7 inputs to U2057 is clocked out as a serial TTL level data bit stream from pins 3 and 4 of the 429 LSI to input pins 6 and 23 of 429 transmitter #1, U2062. U2062 is an output power driver that converts the TTL input at pins 6 and 23 to bipolar output at pins 13 and 17. The bipolar output from pins 13 and 17 of U2062 (OUTPUT_#1_A/B) is then routed, through pins 57 and 58 of connector J2012, to the rear interconnect board.

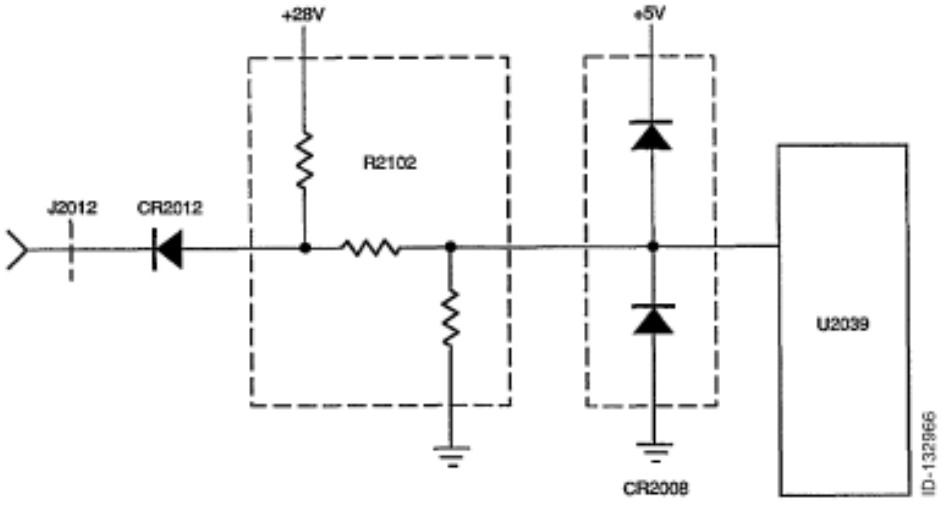
The bipolar output from pins 13 and 17 of U2062 (OUTPUT_#1_A/B) is also routed through multiplexer U2052 and fed back as 429_BITE_INPUT_A/B to 429 receiver U2032, pins 6 and 4, where it is converted to TTL levels and applied to pins 25 and 26 of 429 LSI U2057. This allows the main processor to read and verify the transmitted data.

3 Discrete Inputs

The 16 discrete inputs from the rear interconnect module are applied to the main processor module at pins 11 thru 26 of connector J2012.

Eight of the 16 input lines are applied to the 1A and 2A inputs of discrete input latch U2039 through diode network CR2012, resistor divider network R2102, and diode network CR2008. The other eight lines are applied to the 3A and 4A inputs of discrete input latch U2039 through diode network CR2011, resistor divider network R2096, and diode network CR2009. The outputs from discrete input latch U2039 are placed directly on the processor slow data bus.

Resistor divider networks R2102 and R2096 reduce the bipolar level signals to TTL levels and diode networks CR2008 and CR2009 provide overvoltage protection for the U2039 inputs. Figure 12 is a schematic diagram representation of one of the discrete lines showing the internal network components associated with that line.



Discrete Input Line Circuit Components
Figure 12

4 Discrete Outputs

Discrete output data is placed on the 16-bit processor slow data bus and applied to the 1D and 2D inputs of discrete output/429 TX setup latch U2033. The data is latched and transferred to the 1Q and 2Q outputs with the assertion of control signals TX1 EN* and IOCS5* at pins 48 and 25, respectively. The 1Q outputs are used as strobe and sync pulses to select 429 transmitters 1 thru 4 via the I/O control bus.

The 2Q outputs are the discrete data lines which are applied to power driver U2027. The outputs from power driver U2027 are unregulated 24-volt signal levels that are transmitted through the rear interconnect module through diode network CR2005 and connector J2012.

5 Shut Down Logic

Two discrete inputs (CONTINUOUS_DATA_ENABLE at J2012-25 and INTERRUPT_DATA_ENABLE at J2012-26) are present on the rear connector, but are not connected internally. The unit is strapped for interrupt mode; thus, pin 25 of connector J2012 is high and pin 26 is low.

In the interrupt mode, the low at pin 26 of J2012 is applied through diode network CR2011 and resistor divider network R2096 to pins 1 and 2 of logic gate U2075A where it is inverted to produce a high INT_ENABLE signal on I/O control bus line 30. Logic gate U2075B inverts the high signal back to its original low status before it is latched into discrete input latch U2039.

The high INT_ENABLE signal on I/O control bus line 30 is applied to pin 9 and pin 12 of gates U2075C and U2075D, respectively. With a constant high on these two pins, the outputs at pins 8 and 11 will be determined by the state of the MON1 and MON2 signals at pins 10 and 13. Under normal operating conditions, i.e., no failures or errors detected, the MON1 and MON2 lines will be low, and will not affect the operation of 429 transmitters U2062 and U2074. If a failure is detected, the monitor processor may assert a high MON1 and/or a high MON2 signal which produces a low output from U2075C and/or U2075D. These low outputs are applied to the CLOCK (pin 25) and SYNC (pin 4) inputs of 429 TX #1 U2062 and 429 TX #2 U2074 to shut down transmitter TX #1.

(b) CPU Section

The CPU section does frame-to-frame processing of the altitude data from the DSP section providing the resulting altitude to the I/O section. Programmable logic devices serve as the microprocessor controller and provide the interfaces to the memory devices (boot routine, program, fault, and data), the data recorder/data loader flash card, and the front panel display driver.

Microprocessor U2043, in the CPU section, controls all major functions of the radio altimeter. U2043 is an Intel® 486 SX microprocessor which does not have a math coprocessor. The CLK pin 123 provides the fundamental timing and the internal operating frequency for the microprocessor. Address lines A31 thru A2, together with the byte enables BE0* thru BE3*, define the physical area of memory or I/O space accessed. Address lines A31 thru A4 are used to drive addresses into the microprocessor to perform cache line validations. A31 thru A2 are not driven during bus or address hold. The byte enable signals BE0* thru BE3* indicate active bytes during read and write cycles.

During the first cycle of a cache fill, the external system should assume that all byte enables are active. D31 thru D0 are the data lines for the microprocessor. Lines D0 thru D7 define the least significant byte of the data bus while lines D24 thru D31 define the most significant byte of the data bus. Bypass capacitors C2110, C2113, C2138, and C2141 are for high frequency. C2109, C2111, C2112, C2114, C2137, C2139, C2140, and C2142 are for the current charges that U2043 requires. It is a 25 MHz part running at 12 MHz. R2082-A are pull-up resistors for some of the signals, the intent is to make sure that no noise can get on the line and accidentally actuate that signal.

Data parity pins DP0 thru DP3 are connected to VCC through pull-up resistors because the system does not use parity. The HOLD pin 130 has resistor R2098 to ground tied to it, which disables that signal.

TC1 is a temperature sensor used for data logging all TS temperature, especially for BIT (built in test). It is used to log when failure occurs at whatever temperature, so it can later be used in debugging.

U2043 along with U2058, a programmable logic device, and U2021, an integrated peripheral controller, are the heart of the unit. The bus controller U2058 has all the logic signals and timing required to do chip selects and control U2043.

Y2003 is a 24 MHz clock which is divided by 2, sending 12 MHz to U2043. The 24 MHz is used because there are two edges used in order to control the timing.

The 5 volt monitor and watchdog timer reset provides over and under voltage protection, and is set for about 5 to 7% of the upper 5 volts, which is a requirement for U2043. When the voltage falls below or goes above 5% of 5 volts, which is below 4.75 volts or above 5.25 volts, the reset occurs holding the processor in reset.

Located on pin 72 of U2021 is Y2002, which is a 32.768 KHz crystal that is used to control the real time clock for the software; it controls timing and tagging information.

U2044, U2053, U2059, and U2067 are 128K X 8 CMOS static RAMs, which have been upgraded to 512K X 32 (2 megabytes) worth of RAM. The data RAMs are backed up by +5VU for 20 seconds which decreases power-up time, allowing to resume tasks as a warm start rather than a cold start. The chip select to the RAMs use U2060, which is a NAND gate.

Basically the chip select and reset are used to make sure there are no inadvertent writes to it. During that time, the chip selects are held high to disable the RAMs as the power is going down, to make sure that no exterior writes happen to the RAM.

U2016, U2017, U2029, and U2030 are flash memories for storing the program. These memories are read/write and can be rewritten as long as 12 volts is applied to the device.

The flash memories 12 volt switch circuit consists of U2005-F, Q2003, R2030, R2029, C2052, and C2007. The flash memories 12 volt switch is controlled to make sure that no inadvertent writes happen during operation. It is a switch needed to turn on the 12 volts to the flash memory.

U2002, U2003, U2012, and U2013 are the byte swapping logic. There are two independent buses to accommodate 32-bit and 16/8 bit devices.

The FAST 32-bit bus only talks with the program/data memories and the SLOW bus talks to all other I/O peripherals. For the 32-bit microprocessor U2043 to talk to any 8 or 16-bit devices, the 16 and 8-bit memories require external byte swapping logic for routing data to the appropriate data lines. Separate buses distribute capacitance loading and thus lower signal noise.

U2004 and U2014 are address buffers. Half of U2014 is used to buffer other signals for increase drive and to make sure that the signals are clean going to other sections of the module. U2064 is the control signals buffer, which is all the signals that go to either the I/O section or the DSP section. They are pulled up to make sure that no noise gets on the line and inadvertently actuates it.

U2054 is a D-flipflop, which is used in the I/O discretes circuit. These are various discretes, for example, the FLASH_WR_ENABLE that is used to switch 12 volts and DSP_RESET and RS232_RST that are two different peripherals. Another signal is the LCD_LITE_EN that turns on the backlight on the front panel display. U2050 makes up the input discretes which monitor various inputs; i.e., from the data card and some of the test buttons from the front. U2034 is a 32K byte CMOS EEPROM. This is the storage site for configuration memory and fault memory recorded during the flight legs.

The BOOT block flash memory is where U2043 (Intel 486) gets its initial information and power up. It consists of U2045, which is a 128K X 8 flash memory and a switch. The switch has two settings: SHOP_MODE and NORMAL_MODE. Flash memories are not preprogrammed. They are programmed on the module after they have been soldered. During

SHOP_MODE, it allows 12 volts to access the BOOT block section. This is done so that during flight, even if the 12 volts is inadvertently turned on, the BOOT code can not be overridden. It can only be done in the shop and the unit has to be open. In the NORMAL_MODE, part of the BOOT code can be overridden but that is not essential to the unit so memory cannot be lost.

U2069 is a Universal Asynchronous Receiver/Transmitter (UART) device. The UART performs parallel-to-serial conversion on data characters received from the CPU.

The CPU can read the complete status of the UART at any time during the functional operation. When CS0 and CS1 are high and _CS2 is low, the chip is selected. This enables communication between the UART and the CPU.

INTR, interrupt pin 33 goes high when any one of the following interrupt types has an active high condition and is enabled through the IER: Receiver Line Status; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a master reset operation.

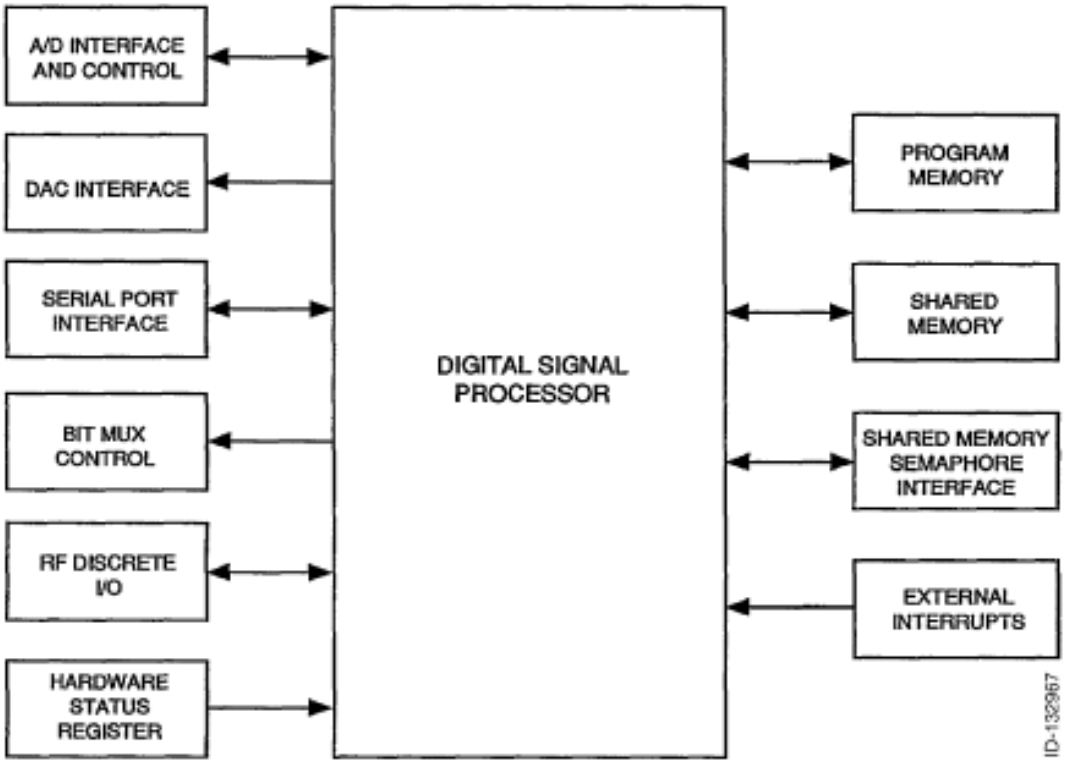
The MAX232 drivers/receivers have on-board charge pump voltage converters which convert the +5 volt input power to the ±12 volts needed to generate the RS-232 output levels. Resistors R2113 and R2114, and capacitors C2194 and C2195 are for protection.

The 5 volt hold-up circuit uses a large capacitor, C2028 acting as a battery to holdup the CPU and DSP RAMs, along with the real-time clock on the module, for warm and cold starts.

J2013 is the 24 pin power supply connector. The +24, +5, +12, and -12 volts have capacitors and inductors for filtering. The PWRDN_INT* signal pin 4 is buffered by two Schmitt trigger inverters and a pull-up resistor and capacitor C2228. This is the power supply signal that tells the unit that the 200ms power hold-up is about to go down, and to store all the information before all power is lost. J2027 is the in-circuit programmable connector. This connector is used to program U2043 once it is soldered to the board, and U2043 can be reprogrammed as many times as necessary.

(c) DSP Section

The DSP section is used to process the analog outputs from the RF module and to generate some of the control signals to the RF module for transmit modulation, automatic gain control, and test signals. Figure 13 presents the overall block diagram for the DSP. Figure 14 presents the overall memory map for the DSP.



Overall DSP Block Diagram
Figure 13

ACCESS	SIZE	ADDRESS RANGE	WAIT STATES	TYPE
Boot Loader ROM (Internal)	4k x 32	000000h-000FFFh	ONE	Read Only
FIFO Reset		200000h	ONE	Write Only
RF Discrete Outputs (D0 - D5)		200001h	ONE	Write Only
RF Discrete Input		200002h	ONE	Read Only
Main BIT MUX (D0 - D5)		200005h	ONE	Write Only
A/D Sample MUX Select		200006h	ONE	Write Only
DSP Hardware Status Register		200007h	ONE	Read Only
DPRAM Semaphore Control		200008h-200009h	ONE	Write Only
DAC Ports: 8 Bit DAC 12 Bit DAC		 200010h-200013h 200014h-200017h	ONE	Write Only
Serial IO Selection		20000Ah	ONE	Write Only
Boot Ready Reset		20000Bh	ONE	Write Only
A/D Sample BIT Select		200019h	ONE	Write Only
FIFO	4k x 18	300001h	ONE	Read Only
DPRAM	4k x 8	400001h-400FFFh	ONE	Read/Write
Registers (Internal)	6k	808000h-8097FFh	ZERO	
RAM Block 0 (Internal)	1k x 32	809800h-809BFFh	ZERO	Read/Write
RAM Block 1 (Internal)	1k x 32	809C00h-809FC0h	ZERO	Read/Write
Interrupt/Trap Branches (Internal)	64 x 32	809FC1h-809FFFh	ZERO	Read/Write
Program Memory - SRAM	32k x 32	A00000h-A07FFFh	ZERO	Read/Write

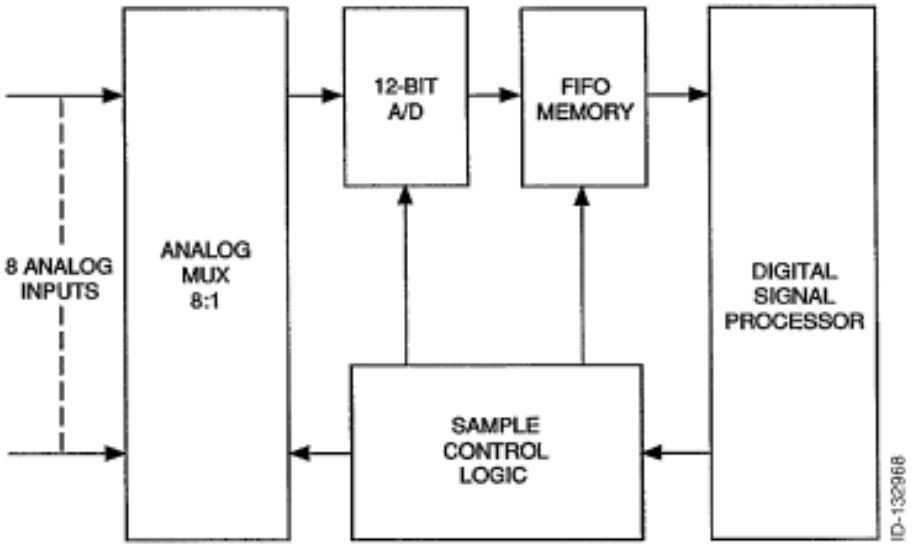
NOTE: Each wait state adds an additional 66 nanoseconds to external bus access.

Overall DSP Memory Map
Figure 14

The BASEBAND signal, which is the output from the RF on the RF control module, goes into differential amplifier U2041-A. U2041-A buffers the output that is going into analog mux U2047 pin 6. U2056-B is another buffer on that same signal which buffers the signal going to the monitor processor.

U2056-A is another differential amplifier buffering the CALIBRATION_OUTPUT signal, which is the signal coming from the RF control module. It buffers the signal going into analog mux U2047 pin 7. Another differential amplifier is U2041-B, which buffers the CALIBRATION_OUTPUT signal going to the monitor processor.

U2047 is a CMOS latched eight channels-to-one analog multiplexer, which switches between the CALIBRATION_OUTPUT signal and the BASEBAND_OUTPUT signal or any of the other inputs. Under normal operation U2047 is alternately sampling the BASEBAND_OUTPUT and the CALIBRATION_OUTPUT. The output of U2047 goes to U2055, which is a 12-bit A/D converter. U2047 output is controlled by the mux addresses 0 thru 2, which are generated by the I/O controller U2065. Figure 15 presents the A/D converter block diagram.



A/D Converter Block Diagram
Figure 15

The difference frequency signal from the RF module is digitized using a 12-bit A/D converter U2055. The A/D converter is also used to monitor signals from the BITE test points on the RF module and the power supply voltages. The digitized data from the A/D converter is stored in a FIFO memory device which is accessed by the DSP.

Normal operation consists of switching between U2056-A and U2041-B sampling the BASEBAND_OUTPUT and the CALIBRATION_OUTPUT. The output of U2055 then goes to U2046 and U2051, which are 2048 X 9 input FIFOs. The output of the FIFOs goes to the CPU data bus where the CPU has access to the contents of the FIFO. Another mode of operation is byte sampling. The CPU determines that it wants to look at either the BIT_MUX_OUT pin 20 of J2014 coming from the RF control module or the bit mux U2038. This allows the CPU to monitor different voltages. The bit mux U2038 output has a mux on the RF control module which allows the CPU to monitor RF test points. U2038 allows monitoring of the power supply voltages +24, +12, and -12 and also a loop back DAC output (DAC8_0). It also allows monitoring of the temperature sense on the main processor CPU side. DSP_SQUELCH is not used. DSPBD0, 1 and 2 are used to determine which one of the inputs are being monitored. The DSP writes to a latch inside the mux to select which of the 8 inputs it is going to look at.

The output of the FIFO is accessed by U2007, which is the CNI digital signal processor (DSP). The DSP processes the difference frequency and calibration frequency into altitude information. U2023 is a 1-of-8 decoder/demultiplexer for the program/data memory chip select. U2035-A is a logical O-ring of DSPBOOT or DSPA23 for the READY* signal. When there is an access to DSPA23, which is program memory, or in BOOT mode which is start-up, then the CPU is ready all the time, and there are no wait states on the memory accesses. External memory and peripheral wait states are controlled by the primary-bus control register. The bit map is presented in Figure 16.

U2018, U2008, U2009, and U2019 are 32 k X 8 SRAMs, which make up the program/data memory. These are zero wait state memories that use 15 ns RAMs, that are 32 k deep. This makes a 32 k by 32-bit RAM array where the program is stored after boot up.

U2022 is a dual ported RAM where the communications between the DSP and the main processor takes place. It is 4 k deep by 8-bit wide where by the main processor and DSP can access any location. It is partitioned such that the DSP does not access the main processor portion of the RAM. This is where all the commands from the main processor go to the DSP, and the altitude spectrum data from the DSP goes to the main processor.

ADDRESS	BIT	NAME	SET TO	DESCRIPTION
808064h	0	HOLDST	don't care	Hold status bit. (Read Only)
808064h	1	NOHOLD	0	Port hold signal
808064h	2	HIZ	0	Internal hold
808064h	4-3	SWW	10	Software wait mode Logical-OR of RDY* and RDY*atcnt
808064h	7-5	WTCNT	bbb	Software wait state count 000 = Zero wait states 111 = 7 wait states
808064h	12-8	BNKCMP	00000	Bank compare
808064h	31-13	Reserved	0 - 0	Reserved

Primary-Bus Control Register Bit Map
Figure 16

U2036 is a 16-bit data bus buffer. This is divided into two 8-bit functions. The 1A and 1B function buffers the lower 8-bits of the data bus. On 1B there is DSPD0 which is not buffered, that passes through U2036 and comes out as DSPBD0 which is buffered. The other function 2A and 2B allows reading of the discrete inputs from the RF control module. RF1_FIN0 and RF2_FIN0 are functions which are defined, on the RF control module.

U2031 is a 16-bit latch providing latched outputs to the RF control module. DSPBD0 thru DSPBD7 is the buffered data bus and DSPD8 thru DSPD15 is unbuffered data. Outputs DSPL0 thru DSPL15 go through U2010 and U2061, where they are then routed to the two connectors going to the RF control module J2014 and J2015.

U2010 and U2061 are t-filters, consisting of two 100 ohm resistors in series with a 39 pF capacitor to ground in between them. This filters out any digital noise from going over to the RF section.

U2040 is a quad 8-bit digital-to-analog converter. Output 0 of U2040 goes through another filter U2078 and is routed to the RF control module on connector J2015 pin 28, as IF_AGC voltage. This voltage allows the DSP to control the gain of the receiver i-f. Output 2 goes out on pin 22 of J2015 which is RAMP_REF. The other two outputs on U2040 are not used on the radio altimeter. Each D/A converter output VOUTA for example, is addressed by setting DSPA0 and DSPA1 to a zero and then writing the value on the DSP data bus, the lowest seven bits. Then VOUTB will be writing a one to A0 and a zero to A1, and then writing the value and etc.

U2037 is a quad 12-bit digital-to-analog converter. The value for the output is written on the data line D0 thru D11. Each output is accessed by writing to an address A0 or A1, selecting one of the outputs, and then putting the value on the data bus outputs. U2037 is double buffered on the input, so there is a _LDAC function which is controlled by the I/O controller. When the CPU writes to the latch, it goes through an input latch and then when the _LDAC goes low, the input latch is written to the output. This function is there so that all the outputs will be synchronized. Each of these outputs goes to U2077.

U2077 is a quad SPST analog switch. U2077 along with U2076, and C2216, C2217, C2218, and C2219 make up a quad sample and hold. The output of the D/A converter has spikes on it, which would cause problems, so when the D/A converter is changing voltage, the switch U2077 opens and the capacitors hold the previous value. Once the D/A converter has finished settling out, U2077 closes and samples the output of the D/A converter. U2076 is a quad op-amp buffer for the capacitors. Again these outputs go to U2078 which is a low pass filter, and output VOUTA from the D/A converter after being sampled and going through the low pass filters, goes to the RF control module on pin 22 of J2015. This output is used for the RAMP_REF on the RF control module.

U2065 is a high density in-circuit programmable logic device (PLD). It is programmed by the _RESET, _ispEN, SDI, MODE, and SCLK inputs which go to a connector on the main CPU.

This I/O controller PLD has many functions, one of which is to control which input is sampled, like the analog mux U2047 on the input. The main processor generates a timer clock which is DSPCLK1. DSPCLK1 controls the sampling rate of the A/D converter U2055.

Figure 17 presents memory-mapped DSPCLK1 locations.

ADDRESS	DESCRIPTION
808030h	DSPCLK1 Global-Control Register
808034h	DSPCLK1 Counter Register
808038h	DSPCLK1 Period Register

Memory-Mapped DSPCLK1 Locations
Figure 17

It goes into a state machine in the I/O controller and the I/O controller generates the address to be sampled and the sample command _SAMPLE. This goes to the analog mux and to the A/D converter. It generates an A/DSC*, which stands for A/D start conversion. The A/DSC* goes to the A/D converter which starts the conversion. The mux address lines 0 thru 2 determine which of the inputs will be sampled. The A/D converter U2055 has an end-of-conversion output EOC on pin 42, which goes high when the conversion is over, that comes into the I/O controller. The I/O controller then generates an A/DOE* which goes to the FIFOs U2046 and U2051, and what is on the data outputs of the A/D converter is then loaded into the FIFOs, where the DSP can read them.

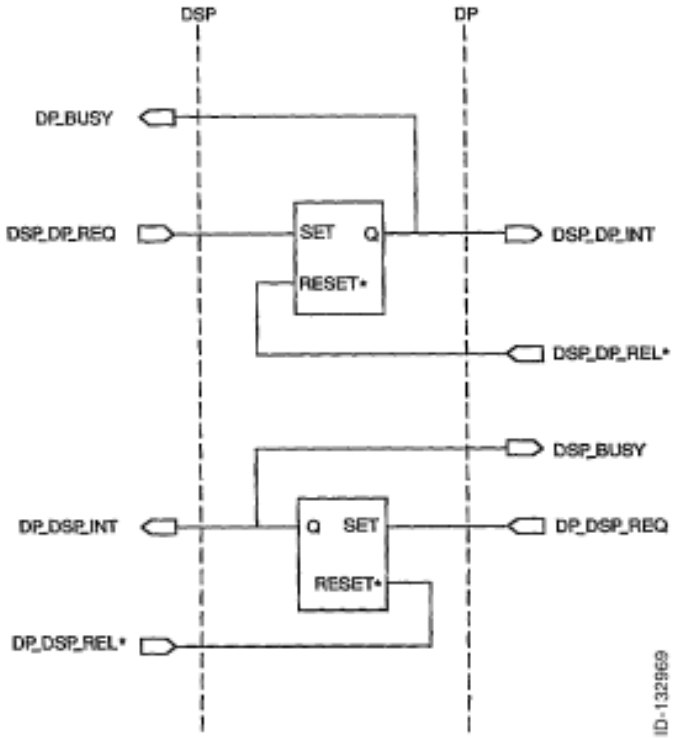
Another function of the I/O controller, based on the timer clock DSPCLK1, is to generate a sample command which goes to the analog switch U2077 which tells it when to sample the output of the 12-bit D/A converter. Another function is chip select generation which is _CS0 thru _CS8. These are decodes of the address inputs DSPA0 thru DSPA4 and DSPA20 thru DSPA23, to generate DSPCS0* thru DSPCS8*. Another function tied to the timer clock DSPCLK1 is _LDAC which is the command to load the output latch of the 12-bit D/A converter. Another function of the I/O controller is generating serial clock out (SCLKOUT) and serial data out (SDATOUT) which goes to the RF control module. On the serial port from the DSP the frame is ANDed with the clock, generating a gated clock on SCLKOUT, which then is routed with SDATOUT through U2015 and U2070 which are low pass filters to pins 48 and 50 on J2014.

This is used to load the ramp generator with the ramp value to be used in that sweep. It also allows to read back the DATA_OUT_FSYNC on pin 52 of J2014. The data is then read back through input that goes into the I/O controller U2065 on pin 8 (SD2IN). It is put onto the RX_CLK, RX_FRAME, and RX_DATA so it can be verified that what was sent out was loaded properly into the ramp generator. Another function that the I/O controller generates is interrupt, _INT0 thru _INT3. The external DSP interrupts are defined in Figure 18.

INTERRUPT	NAME	DESCRIPTION
0	INT0*	FSYNC
1	INT1*	New message in shared memory
2	INT2*	NA
3	INT3*	NA

External Hardware Interrupts
Figure 18

The shared memory (DPRAM) in the DSP is the interface to the DP. Control of the interface is provided by two hardware semaphores located in the DSP I/O controller. The hardware interface consists of two set-reset latches as shown in Figure 19.



Shared Memory Hardware Semaphores
Figure 19

The signal definitions are as follows:

1 DP_BUSY: Indicates the DP busy state.
   0: Current message has been accepted by the DP.
   1: Current message has not yet been accepted by the DP.
2 DSP_DP_INT: Interrupt request line from the DP.
   0: No new message in shared memory.
   1: There is a new message in shared memory.
3 DSP_DP_REQ: Inform DP of new message.
4 DP_DSP_REL*: Inform DP current message has been accepted.

DP_BUSY and DP_DSP_INT are status bits and are read from the DSP hardware status register.

Any write access to DSP_DP_REQ and DP_DSP_REL* sets the corresponding function. The address mapping for these control signals are presented in Figures 20 and 21.

ADDRESS	NAME	DESCRIPTION
200009h	DSP_DP_REQ	Set DSP-DP shared memory interrupt.
200008h	DP_DSP_REL*	Clear DP-DSP shared memory interrupt.

DSP Shared Memory Interface Control Signals
Figure 20

ADDRESS	DESCRIPTION
DP_DSP_REQ	Set DP-DSP shared memory interrupt.
DSP_DP_REL*	Clear DSP-DP shared memory interrupt.

DP Shared Memory Interface Control Signals
Figure 21

When the processor first comes up DSPBOOT is active, so that the memory is ready all the time. Inside the DSP itself is a wait-state register that comes up, set for seven wait-states. After the reset clears for the processor, it runs on seven wait-states until initialized and then it runs from zero wait-states.

(4) Input Filter Module (refer to Figure 183)

The aircraft 115 V ac, 400 Hz input power is connected to P1208, which is then fed to pins 1 and 5 of connector J3108 on the input filter module. Inductors L3101 and L3102, capacitors C3101 to C3104, resistors R3101 and R3102, diodes CR3101 to CR3104, transformer T3101, thermistor RT3101, and varistor RV3101 comprise the input filter module, which keeps noise from the power supply from passing into the aircraft 115 V ac power system.

The EMI filter network consists of inductors L3101 and L3102, transformer T3101, and capacitors C3102 to C3104, which provide the ac input to the full-wave rectifier.

The full-wave rectifier circuit consists of diodes CR3101 to CR3104. The full-wave rectifier supplies 150 V dc to the power supply module in two parallel outputs at connectors J3102/P3302.

The current limit and surge protection circuit consist of RT3101, RV3101, R3101, and R3102. The resistance of thermistor RT3101 varies with the temperature and limits surge current. Varistor RV3101 provides surge and transient protection, and R3101 and R3102 are bleeder resistors across the output.

Capacitor C1 is the hold-up energy storage capacitor connected to terminals EP3101 and EP3102. This capacitor is located on a chassis as a capacitor module (P/N 30090237-0501) and is part of the power supply assembly. The power supply assembly consist of the input filter module, capacitor module, and power supply module.

(5) Power Supply Module (refer to Figure 184)

The power supply module is a self-contained, high-efficiency, switching power supply that converts the 115 V ac, 400 Hz ac power into the required dc operating voltages. Four voltages (+5V, +12V, -12V, and +24V) are supplied including a power-down interrupt that provides advanced notice of a power loss allowing the processors to temporarily retain their status.

T3301 is a planar flyback transformer driven by Q3301 (power MOSFET) controlled by U3302, a pulse width modulator control IC. The primary of transformer T3301 is connected between the rectified filtered 115 V ac (160 V dc) input and the power MOSFET Q3301. When Q3301 turns on, it grounds the other terminal of the transformer applying approximately 160 V dc across the primary.

This voltage causes a ramp of current in T3301 and a corresponding voltage level on the current sensing resistors R3329 and R3330 between Q3301 and the return path of the input voltage. When the voltage in the current sensing resistors reaches the appropriate level, it causes the pulse width modulator U3302 to remove the drive to Q3301 causing it to turn off.

When Q3301 turns off, the transformer T3301 "flies back" and transfers the energy stored in the primary of the transformer, during Q3301 on time, to the secondary. This energy is stored in the output filters and, in 5 volt and 24 volt cases, if is delivered to the output connector.

In the case of the +12 volt and -12 volt outputs, the energy is retransformed by output regulators U3303 and U3304. This cleans and regulates these output voltages. They are delivered to the output connector.

When an input voltage interruption occurs, the power-down interrupt signal (PRWDN_INT) is asserted. This signal gives a 15 millisecond warning prior to the 5 volts going out of regulation.

Internal to the power supply there is additional control circuitry to keep the supply from operating if the input voltage is too low, circuitry that provides initial internal start-up voltage and circuitry that then overrides this start-up voltage.

U3301-B is a differential comparator used for under voltage detection. The effect of U3301-B is to cause and maintain the interruption of power to the main circuit upon the reduction or failure of voltage.

If the output on pin 7 of U3301-B is low, transistor Q3302 turns off. Because pin 7 is low, the voltage on the VCC points is too low to turn on. VCC must be at least 15.5 volts to turn on and if it drops below 8.5 volts, it will turn off. Normal VCC voltage is approximately 11.5 volts. The override start-up circuit consists of Q3302 and surrounding components. Q3302 is turned on for override start-up.

U3305 is an optocoupler utilizing an LED and a phototransistor for maintaining a high degree of isolation between the input and output. The 5 volt output is resistor divided to 2.5 volts by R3326, R3301, and R3302, and fed into the adjust pin of CR3301. Because this power supply is an off-line type, U3305 is required to cross the input/output isolation boundary.

The output of CR3301 then drives the optocoupler giving a dc level on the primary isolated side of the supply that corresponds to the 5 volt output. This dc level is used by U3302 to vary the output pulse width that drives the power MOSFET Q3301. This varying pulse width is what controls the 5 volt output regulation. This is the primary feedback path.

(6) Display Data Module (refer to Figure 185)

The display data module provides an interface to an operator through a low-power liquid crystal display (LCD) that is visible from the front of the ALA-52B. In addition to the LCD, the module contains an LED "Light Box" backlighting, temperature compensation circuitry, and a PC board containing an associated LCD driver, two pushbutton switches, a 26-pin connector, and a D-sub, nine-pin, RS-232 serial type connector.

The RS-232 front panel connector is used for testing the ALA-52B through a compatible test set or test panel.

The display data module is a custom module manufactured for Honeywell International Inc. by Vikay Industrial. Basically, the module is an 80 by 64 graphics display and is non-repairable except for pushbutton switches S4001 and S4002, and connectors J4017 and J4032. It uses a SED1560 SMOS chip, which has all the controls and comes in tab form, and is directly attached to the glass. Also, the circuitry consists of op-amps U4001 and U4003.

U4001 buffers the signals to increase drive to the signals because the lines pick up a lot of capacitance on the actual display. U4003 is the temperature adjustment. Liquid crystals have a tendency to solidify when they go cold or expand too much when they go hot. U4003 tracks the temperature and tries to make up for it so that there is a viewing range of about 0 to 50 degrees centigrade.

On the module are the two front panel pushbutton switches S4001 and S4002 which are for TEST1 and TEST2. Also the display has LED backlighting, which consist of 48 diodes in a parallel configuration. It uses a Darlington switch to turn them on and off. This is a full graphics display module.

(7) Memory Card Module (refer to Figure 186)

The memory card interface is used to load software program data into the CPU or record software program data from the CPU. The CPU module supports Intel® Series 2 FLASH cards through the Personal Computing Memory Card Interface Adapter (PCMCIA) slot. Intel® Series 2 cards with capabilities ranging from 4, 10, and 20 Mbytes (up to 64 Mbytes, when available) are all supported.

To allow booting-up from an Intel® Series 2 FLASH card, the upper 4 Mbytes of the 32 Mbyte address space is remapped to the lowest 4 Mbyte area. This logic is implemented using a dual 4-input NAND gate U5003 and a quadruple 2-input AND gate U5002. The following discussion provides an explanation:

For growth, the CPU module provides address lines A0 thru A25 to the PCMCIA slot. This is a 64 Mbyte address space. Series 1 FLASH cards do not decode A22 or above (not connected). Series 2 FLASH cards have active address inputs A0 to A24 implying that reading and writing to addresses beyond this 32 Mbyte address space causes wraparound. If a series 2 FLASH card is used to boot from, when the processor attempts to fetch the instruction at the reset vector (address FFFFFFFOh) which would be a read to an illegal address, the series 2 card returns OFFFFh data, the result being that the processor does not read its correct reset vector.

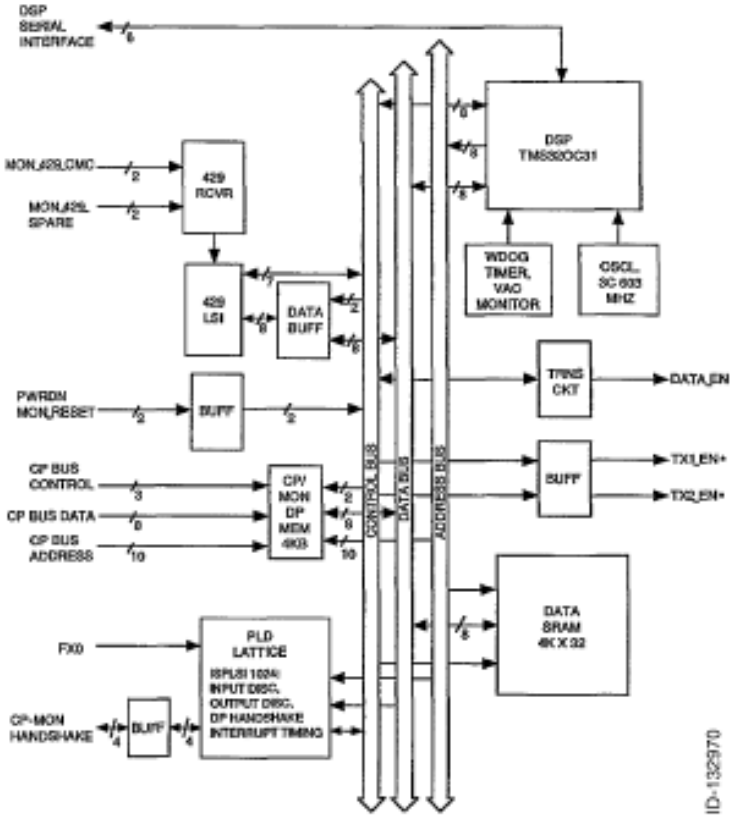
To overcome this problem and allow series 2 cards to be used to boot from, logic is added to the upper addresses that sets A22-A25 to a logic zero when they are all logic high. This effectively re-maps the upper 4 Mbyte of the 32 Mbyte address space to the lower 4 Mbytes.

Normally, after the processor performs its power-on self test, it jumps to the reset vector and begins executing from the on board FLASH bank. In order to allow booting from the FLASH card, the Bus Controller U2058 logic will swap the memory space of the FLASH card and the on board FLASH memory. The swap is made depending on the state of input discrete BOOT_CARD. If low (grounded), the memory swapping takes place which is accomplished by connecting a jumper between pins 1 and 2 of J2028.

(8) Monitor Processor Module (refer to Figure 187)

The monitor processor module provides a second signal processing path using a Digital Signal Processor (DSP). The DSP processes the received signal and calibration signal supplied in digital form from the main processor A/D converter. Also present are a clock, an ARINC 429 receiver/selector, and static memory.

The monitor processor module monitors how the main processor module is processing the signals. There are three interfaces between the main processor module and the monitor processor module. First is the shared memory interface, which is U6001, second is the 429 interface, which is U6010 and U6012, and third is the DSP serial interface. Figure 22 presents the overall block diagram for the monitor processor module.



Overall Monitor Processor Block Diagram
Figure 22

(a) Shared Memory Interface

The shared memory (DPRAM) in the MON is the interface to the main processor module (CPU). Control of the interface is provided by two hardware semaphores located in the programmable logic device (PLD) U6011. There is no non volatile memory on the monitor processor module. The monitor gets its program through the shared memory interface, which is U6001. After power-up the signal MON_RESET (TP1) will be held active

main processor module loads the monitor program in the shared memory. Then the main processor takes the monitor out of reset causing MON_RESET to go high. The DSP automatically loads its program to the static RAMs U6005, U6006, U6008, and U6009.

(b) 429 Interface

The monitor processor module listens to the 429 transmitters on the main processor module. There are two modes, interrupt and continuous. In the continuous mode, the monitor processor module will not shut off the transmitters. In the interrupt mode if there is something wrong with either module, the monitor processor module automatically shuts off the 429 transmitters on the main processor module. The signals that are used to shut off the transmitters are XMON_BUS_DIS_#1 (pin 74), XMON_BUS_DIS_#2 (pin 75), and XMON_DATA_ENABLE (pin 76) from connector J6018. In a default, as long as there is power to the monitor processor module the transmitters are turned off.

(c) DSP Serial Interface

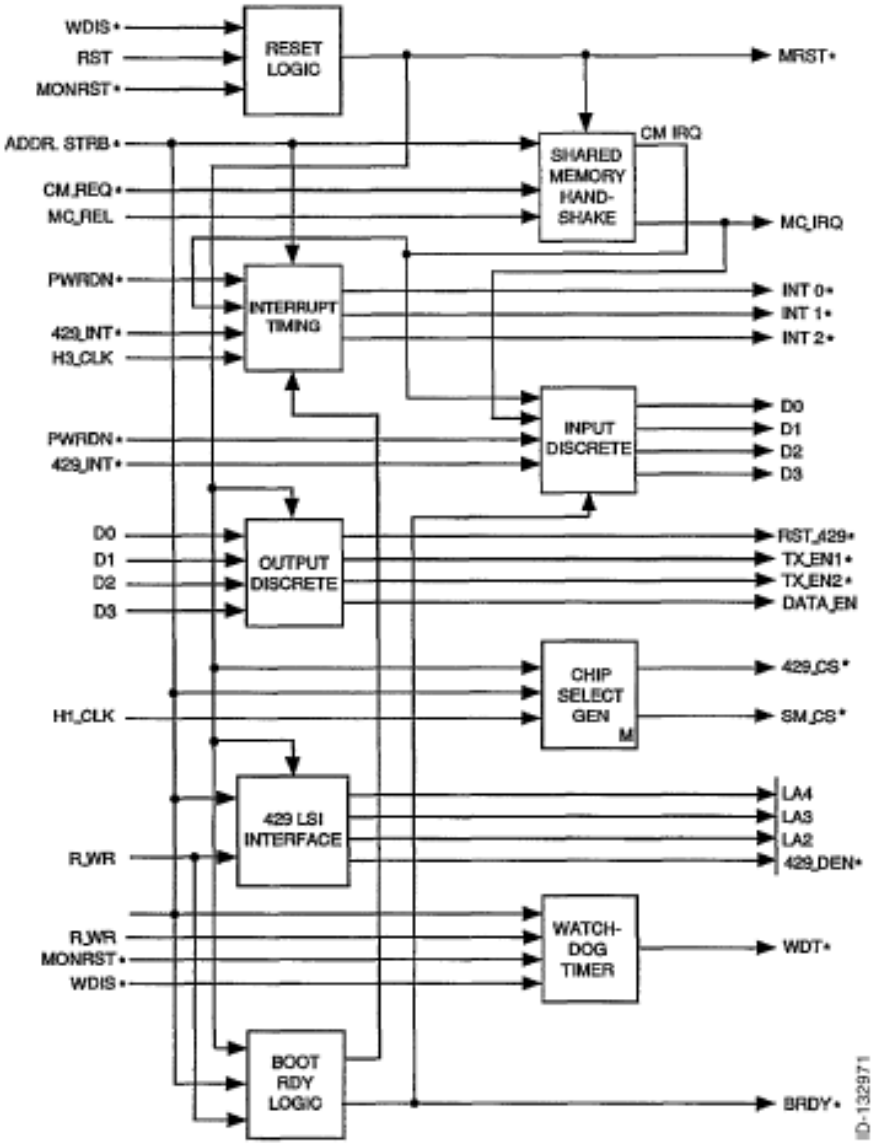
DSP serial interface is connector J6044, which are two DSPs talking to each other directly. One is on the monitor processor module which is U6003, and the other is on the main processor module which is U2007.

(d) Programmable Logic Device

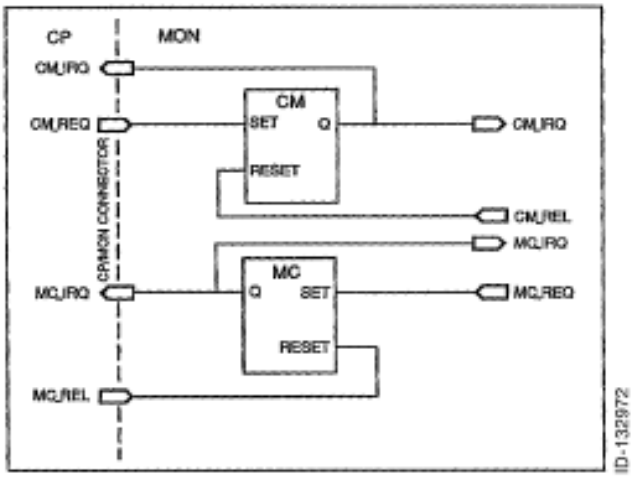
U6011 is a programmable logic device which is programmed on the module, using J6043 connector. Figure 23 is a block diagram of U6011.

Implemented inside the device are reset logic function, interrupt timing, input discrete, output discrete, chip select generation for the 429 and dual port Ram, 429 interfaces, data enable and address lines LA2, LA3 and LA4, watchdog timer logic, boot ready logic, and shared memory logic.

The communications for the shared memory is done with two flip-flops implemented in the programmable logic device as shown in Figure 24.



U6011 Functional Block Diagram
Figure 23



Shared Memory Hardware Semaphores
Figure 24

The signal definitions are as follows:

1 CM_REQ - CP to MON Request
- Input pulse from CP
- Latched to generate CM_IRQ.

2 CM_IRQ - CP to MON Interrupt
- Active high interrupt to MON, generated from CM_REQ signal from CP
- Routed to CP/MON connector to be read by CP before next message is sent
- Can also be read by MON as Input Discrete Bit DO
- Cleared by CM_REL.

3 CM_REL - Clear CP to MON Interrupt
- Any write to Address 60 0000C or reset will clear the CP to MON Interrupt.

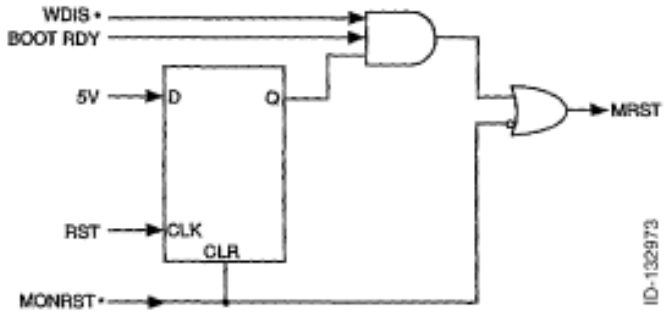
4 MC-REQ - MON to CP Request
- Any write to Address 60 0010 sets MON to CP Interrupt.

5 MC_IRQ - MON to CP Interrupt
- Active high interrupt to CP, sent through CP/MON connector
- Read by MON before next message is sent as D1 of Input Discretes
- Generated by MC_REQ, cleared by MC_REL.

6 MC_REL - Clear MON to CP Interrupt
- Input pulse from CP/MON connector clears MON to CP Interrupt
- Reset also clears the interrupt.

Each flip-flop has a request, clear, and a latched output. The latch of the communication from main processor to monitor processor has a CM prefix on the signal (control to monitor). In the other direction, the flip flop has a MC prefix on the signal (monitor to main). CM_IRQ and MC_IRQ are the latched outputs. When the main is requesting the monitor's attention, it sends a request signal CM_REQ to the input of pin 3 of U6011. The signal is then latched and becomes CM_IRQ and will remain latched until the monitor processor module services the interrupt, and issues a clear signal. Once the latch is cleared, CM_IRQ goes disabled.

The monitor processor module's DSP can be reset by: external reset from main processor module, 5 volt supply dipping below threshold value, or watchdog timer reset. After monitor DSP has been reset by either 5 volt monitor or watchdog timer, it will stay reset until main processor issues a reset. When WDIS test point is strapped to ground, both 5 volt monitor and watchdog timer are disabled. In addition, BOOT RDY must be written to in order to enable the watchdog function. Until then, watchdog cannot cause reset. Figure 25 is a diagram of the reset logic.



Reset Logic
Figure 25

U6004 is the supervisor and reset circuitry which has watchdog timer functions, reset function, and overvoltage monitor function. The output reset signal goes to the programmable logic device U6011.

U6007 is an address decoder which generates memory chip select. U6013 generates the ready signal (RDY) for the DSP which is U6003. J6045 is an emulator connection used for development. U6002 is a 16 bit buffer which buffers both signals coming in and going out.

(10) RF Module for 066-50007-0432 and 066-50007-0531 Units

General

The RF module transmits and receives FM modulated C-Band signals that are used to determine the altitude above the ground. When the transmitted signal is mixed with the return signal bounced up from the ground, a baseband signal is produced at a frequency that represents the difference between the transmitted and return signal frequencies. The baseband signal frequency is directly proportional to the altitude above the ground. This analog baseband signal is the primary output from the RF module.

A simplified block diagram of the RF circuitry is shown in Figure 4 (below).

The transmitted signal, centered at 4.3 gigahertz with a maximum possible span of +/-100 megahertz is radiated from the transmit antenna located on the underside of the aircraft, and is subsequently (after bouncing off the ground) collected by the receive antenna. A directional coupler picks off some of the transmit signal which is mixed with the received signal, producing a difference signal that is amplified, filtered and fed to an analog-to-digital converter on the main processor module.

The BITE circuitry is also included to both test and continuously monitor the RF module functions. A portion of the transmit signal is also fed into a bulk acoustic wave device that provides a reflected signal calibrated to a time delay equivalent to 300 feet (0.616µsec). Cal mixer extracts a signal corresponding to the difference frequency between transmit and delay element signals. The difference frequency signal is fed through a multiplexer to the A/D converter on the main processor board for calibration and self-test purposes.

The PLD receives control signals from the DSP of the processor module and directs them to appropriate circuitry on the RF module. A major function of this PLD is to control the DDS which provides a nearly ideal linear frequency sweep as a reference signal to the PLL within the transmitter chain.

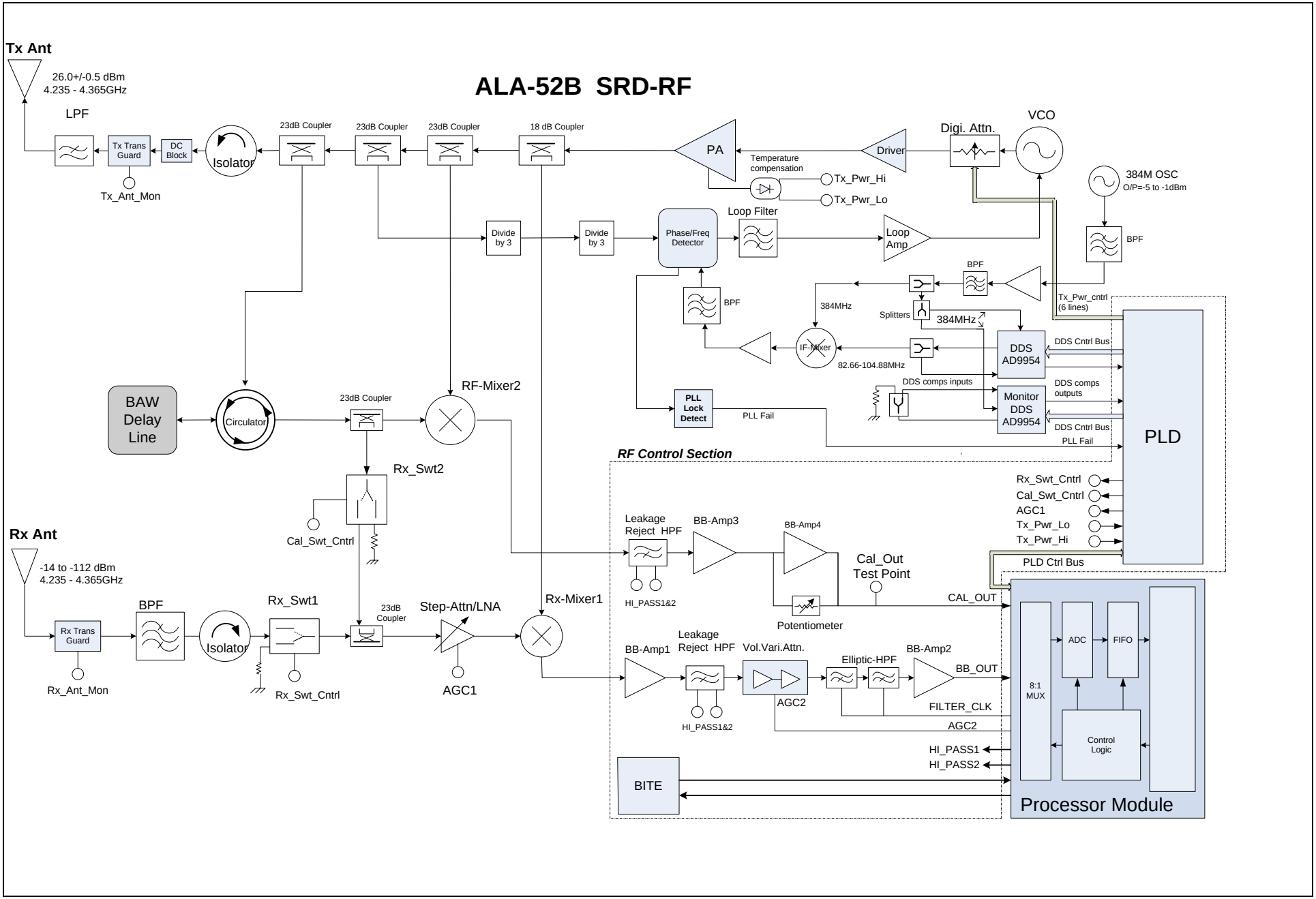

ALA-52B SRD-RF
Tx Ant
26.0+/-0.5 dBm
4.235 - 4.365GHz
LPF
Tx Trans Guard
DC Block
Isolator
Tx_Ant_Mon
23dB Coupler
23dB Coupler
23dB Coupler
18 dB Coupler
PA
Temperature compensation
Tx_Pwr_Hi
Tx_Pwr_Lo
Driver
Digi. Attn.
VCO
384M OSC
O/P=-5 to -1dBm
BPF
Loop Filter
Loop Amp
Divide by 3
Divide by 3
Phase/Freq Detector
BPF
BPF
384MHz
Splitters
384MHz
IF-Mixer
82.66-104.88MHz
DDS AD9954
DDS Cntrl Bus
Tx_Pwr_cntrl (6 lines)
DDS comps inputs
DDS comps outputs
Monitor DDS AD9954
DDS Cntrl Bus
PLL Fail
PLL Lock Detect
PLL Fail
PLD
BAW Delay Line
Circulator
23dB Coupler
RF-Mixer2
Rx_Swt2
Cal_Swt_Cntrl
RF Control Section
Rx_Swt_Cntrl
Cal_Swt_Cntrl
AGC1
Tx_Pwr_Lo
Tx_Pwr_Hi
PLD Ctrl Bus
Rx Ant
-14 to -112 dBm
4.235 - 4.365GHz
Leakage Reject HPF
BB-Amp3
BB-Amp4
Cal_Out Test Point
HI_PASS1&2
Potentiometer
CAL_OUT
BPF
Rx_Swt1
23dB Coupler
Step-Attn/LNA
Rx-Mixer1
Rx Trans Guard
Isolator
Rx_Ant_Mon
Rx_Swt_Cntrl
AGC1
BB-Amp1
Leakage Reject HPF
Vol.Vari.Attn.
Elliptic-HPF
BB-Amp2
BB_OUT
AGC2
FILTER_CLK
AGC2
HI_PASS1&2
HI_PASS1
HI_PASS2
BITE
8:1 MUX
ADC
FIFO
Control Logic
Processor Module

Figure 4

RF Module Circuit Description:

A. Transmitter Chain

The transmitter chain is driven by a VCO based PLL that is controlled by a DDS. The transmitter chain supplies the receiver LO as well as the required input for the calibration circuitry. The DDS is programmed by the PLD which is controlled by the Processor Module. A second DDS, called the monitor DDS is driven with the same frequency set-up as the main DDS in order to provide a comparison reference to the main DDS. The lock-detect signals from the compared DDSs and the PLL are used by the PLD to monitor the failure modes of the DDSs and the transmitter chain.

1. Reference Oscillator

The transistor based oscillator is powered by a 128 megahertz single tone crystal, Y1 and amplified by a X3 multiplier, Q5 to 384 megahertz. The 384 megahertz signal is filtered by a comb-line filter and amplified by a gain block, U14 and filtered again before providing the clock signal to the DDSs (U18, U32) and an LO signal to the IF mixer (U24). Two 3 decibel splitters are employed to split the signal into three outputs, two with equal amplitude and phase at 0dBm and one with 3dBm. The 0dBm signals are used to reference the DDSs (DDS1-REF, DDS2-REF). 3dBm signal is used as IF_LO signal.

2. DDS

a. Both of the DDSs (U18, U32) are driven by the PLD (U512) to generate a frequency sweep between 82.66 megahertz to 104.88 megahertz (approximate maximum sweep) with the external reference clock 384 megahertz. The main DDS (U32) output is feeding the IF mixer as well as the PLD where it is compared with that from the monitor DDS.

b. The linear frequency ramp generator U32 includes an on-chip comparator. The comparator signals are square waves. The bandwidth is greater than 200 megahertz and has a common-mode input range of 1.3 volts to 1.8 volts. This signal helps eliminate phase noise and jitter.

c. The linear frequency ramp generator U32 output frequency range is 82.66 megahertz to 104.88 megahertz. The DDS frequency sweep output (DDS_OUT) on U32-20 and -21 is routed through, transformer T3, a 120 megahertz low pass filter and a 3 decibel coupler to mixer U24. The signal from the ramp generator is mixed with the 384 megahertz IF signal so that the linear frequency modulation is translated up in frequency to 466.66 megahertz to 488.88 megahertz. These frequencies correspond to 4.200 gigahertz and 4.400 gigahertz divided by 9 in the PLL circuit.

.

3. IF Mixer

a. The DDS_OUT signal and the IF_LO signal are routed to IF mixer U24. The output on U24-4 has a frequency range of 466.6 megahertz to 488.8 megahertz (upper sideband). The output of U24 is routed through an amplifier U27 & a 477 megahertz band-pass filter to PFD U33-3.

4. PLL

a. The PLL consists of PFD (U33), loop filter (U28), VCO (G1), digital attenuator (U20), preamp (U19), power amplifier (U12) and two successive divide by 3 frequency dividers (U21, U25)

for a total frequency division by 9. The power amplifiers and the digital attenuator are included in the PLL in order to improve the phase linearity of the overall transmitter. The loop bandwidth is approximately 1 megahertz which is required by the fast sweep and the desired ramp linearity. An external PLL lock detect circuitry which is driven from the PFD U33 provides the status of the PLL to the PLD.

b. The phase-frequency detector PFD U33 is used in low noise phase locked loop. It detects the phase/frequency difference between the 477 megahertz signal provided by the up-converted DDS signal and the frequency divided signal derived from the 4.3 gigahertz VCO to generate output pulses that are proportional to the phase and frequency difference between the two signals. The reference signal is the RF output of U24 from the 477 megahertz band-pass filter (466.6 to 488.9 megahertz) applied to U33-3. The second signal is the PLL_FDBK_VCO and the compliment PLL_FDBK_NVCO from frequency divider U25. The phase-frequency detector U33 uses the phase difference between the two signals to supply frequency up and down pulses to comparator U28. The output of U28, a dc voltage, is used to tune the VCO G1.

5. VCO

a. The VCO G1 has a range of 4.2 to 4.4 gigahertz. The power output is a typical 5.0dBm typical from a single supply of +3.3 V dc. The control voltage from U28 on G1-22 (VTUNE) increases the output frequency of the VCO as the voltage increases. The control voltage range is 3.5 to 7.0 V dc.

6. Digital Attenuator

a. The RF output of VCO G1 is routed to digital attenuator U20-2. Digital attenuator U20 has a range of 2.4 to 8.0 gigahertz, with an insertion loss of less than 3.8 decibel and attenuation accuracy is ±0.5 decibel. The attenuator can be set between 0 to 31.5 decibels with 0.5 decibel steps. Six control voltage inputs, switch between 0 and +3 to +5 V dc, are used to select each attenuation state. The digital attenuator U20 is controlled by the PLD U512 for dynamic power control that is required or board to board variation and temperature variation.

7. Driver Amp, Power Amp and Power Detector

a. The RF output of Digital Attenuator U20-2 is connected to driver amplifier U19-3. The driver amplifier U20 provides about 20 decibels of gain and the PA, U12 has 27 decibels of gain. Both operate with 5 volt supply and consume about 130mA and 600mA respectively. The PA provides an internal power detector which uses an external temperature two comparators whose output is sent to PLD U512, which in turn control the digital attenuator to control the power. The temperature compensated detector enables the power to be controlled within +/-1 decibel over the operating temperature range. PA U12 is capable of delivering up to 29dBm power.

8. Couplers

a. The RF output of the power amplifier U12 is on U12-12. The output is routed through three 23-decibel couplers and one 18-decibel coupler. The 18 decibel coupled signals are used for receive mixer LO U12. Two 23 decibel coupled signals are used for cal mixer LO U11 and for calibration signal generation using BAW device U6. One 23 decibel coupler is used to sample

the output signal and feed back to the PFD U33 through frequency dividers U21 and U25. There are also two more 23 decibel couplers for test signal injection before LNA, U7.

b. Each directional coupler consists of two microstrip coupled lines with a gap dimension of which depends on the coupling requirements. The coupling length is quarter wavelength and one port of each directional coupler is terminated by 50 OHMS shielded resistors (R10, R36, R88, R89, R90, R121). The printed structure of coupler provides 0.25 decibel maximum loss.

9. Isolator

a. An isolator, U38, is placed between the power amplifier and the transmit antenna to minimize reflections from the transmit antenna and associated cables and connectors and improve the VSWR. This is a SMT device and provides 20 decibel minimum isolation with 0.5 decibel of maximum insertion loss.

10. Low-Pass Filter

a. A printed microstrip low pass filter is employed to attenuate the harmonics up to 18 gigahertz. This filter provides 30 decibel and 15 decibel for 2nd and 3rd harmonics respectively and a maximum insertion loss of 0.25 decibel. The return loss of this filter is better than 18 decibel. The output of the low-pass filter is routed to transmit antenna connector J1004-1.

11. DC block and the Transguards

a. A high-voltage matched capacitor circuitry and transguard are used in the transmitter chain to provide protection of the DC antenna monitoring circuit from voltage transients which are caused by lightning.

12. RF FPGA

a. The FPGA supports a 24 bit serial interface between the DSP and RF module. The DSP uses the DATA_IN and DATA_CLK signals to transfer 24 bit serial data sequences to the FPGA that provide it with RX_SWT_CTRL signal, control the U3 Calibration RF switch with the CAL_SWT_CTRL signal and control power to the U7 LNA with the RF_AGC signal. The FPGA returns received DATA_IN data on the DATA_OUT line when RDATA_EN is low and the FSYNC signal when RDATA_EN is high.

b. The FPGA generates the FSYNC and DOWN_UP signals based on the system select information provided by the 24 bit serial interface. The frequency of the DOWN_UP signal is 145 Hz for system select 1, 150 Hz for system select 2 and 155 Hz for system select 3. The FSYNC frequencies are one-half the DOWN_UP frequencies. Assertion of the RAMP_CLR signal cause the FSYNC and DOWN_UP signals to be held low.

c. The FPGA gets ramp rate information by reading ADC U510 using the A2D_CS, A2D_SCLK and A2D_DOUT signals. The ADC input is the DAC12_0 signal and its voltage is proportional to the ramp rate required by the DSP.

d. The FPGA programs the main DDS U32 using the DDS1_CS, DDS1_SDIO and DDS1_SCLK signals. The DDS1_SDO signal provides the FPGA read-back capability of the DDS internal registers. Signals DDS1_RESET and DDS1_IOSYNC are used to reset the DDS. Similar signals support the monitor DDS U18.

e. Both DDS are programmed with identical ramp information based on system select and the ramp rate information from the ADC. For system select 1 the DDS are programmed such that the lower transmitter frequency is held constant at 4.235 gigahertz, for system select 2 the upper transmitter frequency is held constant at 4.365 gigahertz and for system select 3 the transmitter frequency range is held centered at 4.3 gigahertz.

f. The FPGA FUD signal is used to initially program the DDS for a single 4.3 gigahertz transmitter frequency. During normal operation the FPGA PS0 signal is then used to program the DDS registers with new ramp rate and frequency range data. The PS0 signal also controls the ramp frequency direction of the DDS.

g. The FPGA uses the TX_PWR_DET_LO and TX_PWR_DET_HI signals from comparator U514 to level the transmitter power. The FPGA periodically adjusts the TX_.5dB_CTRL to TX_16dB_CTRL signal lines in 0.5 decibel steps until both TX_PWR_DET_LO and TX_PWR_DET_HI signals are high.

h. The FPGA provides limited fault detection reporting to the main processor module via the FAULT_EB and FAULT_EF signals. Via the bite fault multiplexer U4 when the tri-state FAULT_EB signal is pulled low the LRU will generate an EB fault and similarly polarity changes in FAULT_EF signal will cause the LRU to report an EF fault. Only when the RF_AGC signals at FPGA pins 27 and 24 miss-compare will the EF fault be generated. Transmitter leveling faults, miss-compare faults between the two DDS outputs, 384 megahertz clock frequency or 20megahertz clock frequency (G500) accuracy faults, or transmitter PLL loop faults occurring when the PLL_LOCK_DET signal goes low cause the EB fault to be generated.

B. Receiver Chain

The heart of the receiver chain is the double balanced mixer. The signal received from the Rx antenna is mixed with a sample of the transmitter signal to produce a low frequency signal that is proportional to the altitude to the ground. An LNA with bypass switch is employed to adjust the LNA gain between the two states as required by the received signal amplitude. A Band Pass Filter provides the required dc block for the receiver chain while the transguard provides protection for the antenna monitoring circuit from voltage transients which are caused by lightning.

1. Bandpass Filter

a. The receiver input is from RX antenna connector J1005-1. The receive RF signal from the antenna is routed through a 4.3 gigahertz bandpass filter. This printed bandpass filter uses parallel coupled, half-wave long microstrip resonators, coupled along half of their length with the adjacent resonators. The seven-resonator bandpass filter provides 2.5 decibel loss in the bandpass and 50 decibel attenuation for the multilayer spiral parasitic signal at 5.03 gigahertz and overall out of band attenuation to reject out of band HIRF up to 18 gigahertz.

2. Receive/Calibration switches

a. The output of the bandpass filter is routed through a isolator U17 to the LNA through the RF switch U1. The RF switch U1 is a broadband high isolation, non-reflective SPDT. The receiver and calibration switches (U1 and U3) provide the facility to channel the appropriate signal through the receiver chain and are used for the self-test and noise floor test. The

switches are non-reflective, high isolation switches and provides about 50 decibel of isolation at 4.3 gigahertz with 1.5 decibel insertion loss. The high isolation on the PCB is achieved through co-planner wave guide design instead of microstrip.

b. The RF switch operates with complementary negative control voltage logic of -5 to 0 V dc and does not need bias supply. Control signals are generated by the PLD through CMOS level shifters (U2) since the PLD operates with 3.3 volts. The switch control voltages are also being monitored by the MUX U4.

c. The control of the RF switch is by the control signals on U1-15 and U1-16. Refer to Table 6 for the U1 control truth table. The RF1 output is not used and grounded through resistor R5.

Table 6. U1 Control Truth Table

Control Input Signal Path State			
U1-16 (A)	U1-15 (B)	RFC to RF1	RFC to RF2
High	Low	On	Off
Low	High	Off	On

3. Low Noise Amplifier/Step Attenuator

a. The receiver front-end C-band low noise amplifier, U7 has a typical noise figure of 1.8 decibel and provides 12 decibel of gain for lower level signals (high altitudes), and 6 decibel attenuation (total loss 18 decibel) for the higher level signals (low altitudes). The amplifier is under the binary control of the PLD U512. The low noise amplifier insures with minimum noise figure for signals received at high altitudes.

4. RX Mixer.

a. The receive mixer (U10) is a double balanced mixer with built-in LO amplifier and work with +2 dBm of typical LO signal. This provides 8 decibels of conversion loss, 32 decibels LO/RF isolation, and 25 decibels LO/IF isolation. In the receive path, the RF signal on U10-8 is from the Rx antenna through the RF switch U1. The LO signal to U10-1 is from the 23 decibels coupler on the output of the power amplifier U12-12. The two signals are mixed to provide the IF baseband signal (IF_TO_BB) on U10-5.

C. Cal Signal Chain

A directional coupler picks off some of the transmitter signal and feeds it to a bulk acoustic wave device that provides a reflected signal calibrated to a time delay equivalent to 300 feet (0.616μsec). Calibration mixer extracts a signal at the difference frequency between transmit and delay element signals. The output is filtered and amplified and processed by the CPU for calibration and self-test purposes.

1. Delay-Line

a. The 300-foot bulk acoustic wave SMT delay line U6 with 0.603 to 0.616μsec delay consists of a cylindrical rod of quartz crystal for the propagation of an acoustic wave. This one-port delay line uses only one transducer for both input and output and therefore we haven't included a circulator that properly directs the input to the BAW and output of the delayed signal to the calibration mixer. The circulator prevents the transmitter sample signal from directly being

applied to the calibration mixer. The BAW delayed signal incurs 28 to 38 decibels of insertion loss at 4.3 gigahertz.

2. Circulator

a. The circulator, U5, is a counterclockwise SMT device and provides 22 decibels minimum isolation at 0.5 decibels maximum insertion loss. A the delay-line at port-2 to produce the delayed signal. The reflected signal is extracted from port-3 and fed to the cal mixer.

3. Calibration Mixer

a. The device used for calibration mixer U11 is the same as receive mixer U10. In the calibration path, the RF signal on U11-8 is from the circulator U5 output. The LO signal, CAL_LO_MIX on U11-1 is from the 23 decibels coupler on the output of the power amplifier U12-12. The two signals are mixed to supply the IF calibration baseband signal (CAL_TO_BB) on U11-5.

4. IF Sections

a. U506, U507, and U505 are the calibration output amplifier chain. U506 acts as a selectable high-pass filter controlled by HI_PASS1 and HI_PASS2 signals which comes from the DSP. In the case of the calibration signal, it allows for increased high pass filtering in the response to the calibration IF. With switch 2 (S2) of U506 open, C532 is not part of the circuit and the high pass response is determined by C533. With S2 closed, C532 is then in parallel with C533 and is the dominant factor in determining the response of the input stage of the filter.

b. The input signal CAL_TO_BB goes through C533, which gives it a high-pass response. The signal then goes into U507 which is a non-inverting amplifier with a gain of 20.

c. The output of U507 goes to C534 which produces a high-pass response. This is also selectable by HI_PASS2. With switch 4 (S4) of U506 open, R66 is not part of the circuit and the response is determined by C534 and R536. With S4 closed, the response is determined by C534 and the parallel combination of R536 and R66 to determine the cutoff frequencies/response. The output goes to U504, which is an inverting amplifier with a gain of 2. This gain can be adjusted using the pot R34. Next, the output goes through C512 for high-pass filtering and becomes CAL_OUT, which goes to the differential amplifiers in the DSP section.

d. The IF input signal IF_TO_BB is ac coupled to transistor Q1, which is a common emitter amplifier. The output from the collector of Q1 is filtered by C36 (low-pass) and C528 (high-pass) and then it is applied to high-pass amplifier U505. Overall, Q1 and U505 have 30 decibels of gain and low noise. The output of U505 goes through R533 and then into a selectable high-pass filters which is determined by HI_PASS1 and U506. With switch 1 (S1) and U505 open, C45 is not part of the circuit and the response is determined by C531 and the input impedance of U502 which is 100-ohms. With S1 closed, C45 is in parallel with C531 and becomes the dominant capacitor for the response. The response is essentially C45 and 100 ohms. The output of the high-pass filter goes to U502-A, which is a 40 decibels gain voltage controlled amplifier. It is controlled by the IF_AGC which comes in on pin 28 of J21. The voltage at pin 16 of U502-A and pin 9 of U502-B varies from 0 to 2.5 volts.

e. The gain of U502 can varied from 0 decibel gain to 40 decibels gain. The output of U502-A goes through a high-pass filter (C505) and then it is routed to the pin7 of U502-B. U502-B is

a 0 to 40 decibels voltage controlled amplifier. Its gain goes from 0 to 40 decibels gain when the input on pin 9 goes from 1.25 to 2.5 volts. Overall, from pin 2 of U502-A to pin 11 of U502-B, there is up to 80 decibels gain available depends up on the IF_AGC control signal. The output is low-pass filtered through R503 and C503 and goes into the first of two switched capacitor filters.

f. Components U500 and U501 are switched capacitor elliptical filters which have a response equivalent to an eight-pole elliptical filter. The cutoff is determined by the FILTER_CLK which comes from the DSP section. The cutoff is at 43 KHz. The output of these filters have an uncommitted op-amp with which resistors R1, R2, R3, and capacitors C1 and C2, are a dual, two-pole low-pass filter to reduce the amount of clock noise on the output. The output of U500 is connected to U501, which is essentially the same circuit, to give it a very sharp cut-off to prevent high frequencies going to the DSP. The output at pin 5 of U501 goes through high-pass filter C507 to pin 3 of amplifier U503 which has a gain of 15 decibels. The output of U503 goes through R22 and is the BASEBAND_OUT which goes to the DSP section.

5. BITE MUX

a. The BITE MUX U4 is a CMOS latched 16-bit to 1 analog multiplexer. The BITE MUX has different voltages on its inputs which are monitored by the DSP section. On input 1 (S1) and 2 (S2), 2.5V and 3.3 volts going to the RF section are monitored. Also, input 2 (S2) provides FAULT_EB signal which can be decoded to a set of RF circuitry failures. Inputs 3 (S3) thru 4 (S8) are the RX_SWT_CNTRL signal voltage which is monitored. Input 7 (S7) is the FAULT_EF signal voltage which is monitored. Input 7 (S6) is the CAL_SWT_CNTRL signal voltage, which is monitored. Input 8 (S8) is the RF_AGC signal voltage which is monitored. Input 9 (S9) is the +12_DIG volts which is monitored. Input 10 (S10) is the +5V_RF which is monitored. Input 11 (S11) is the -12_DIG volts which is monitored. Input 12 (S12) is the -5_DIG volts which is monitored. Input 13 (S13) is the TX_ANT_MON which is monitored and should look like a short when connected to an antenna. Input 14 (S14) is the RX_ANT_MON which is monitored and should look like a short if its connected. Input 15 (S15) is the RAMP_OFFSET signal voltage which is monitored. Input 16 (S16) is the TX_POWER_MON which is monitored. U508-A is a buffer amplifier to buffer the output going to the DSP section.

6. Power Supply Filtering

(a) The power supply filtering consists of L507, L501, L505, and L504. RF CCA contains voltage regulators U13, U16, U22, U23, U29, U30, U34, U509 and U515 linear regulators to generate a clean +1.8V, +2.5V, +3.3V, +5.0V, +10V, and -5V for various RF and digital ICs. Component U5 is switching regulator to convert 12V to +6V DC with 85 percent efficiency. This device contains internal short circuit protection also.

NOTE: The schematics for the new RF Module described above can be found in attached “AOIALA-52B3 RF Module Schematics”. This is only change from previously test and approved AOIALA-52B unit.

NOTE: The alignment procedure for the new RF Module described above can be found in attached “AOIALA-52B3 RF Module Alignment Procedures”.

NOTE: The Acceptance Test Procedure (ATP) for the new -0432 and -0531 units can be found in attached “AOIALA-52B3 Acceptance Test Procedures”