1. Introduction

The Aircraft Environment Surveillance System (AESS) system is Honeywell's new generation of surveillance products that integrate into one Line Replaceable Unit (LRU) functions that are currently provided by individual avionics systems: Traffic Collision Avoidance System (TCAS), Mode S Transponder, Enhanced Ground Proximity Warning System (EGPWS) and Weather/Predictive Windshear Radar. The general purpose of the system is to alert the crew of weather, terrain and aircraft traffic hazards on the aircraft flight path. Figure 1 below provides an overview of the AESS system and identifies system components.

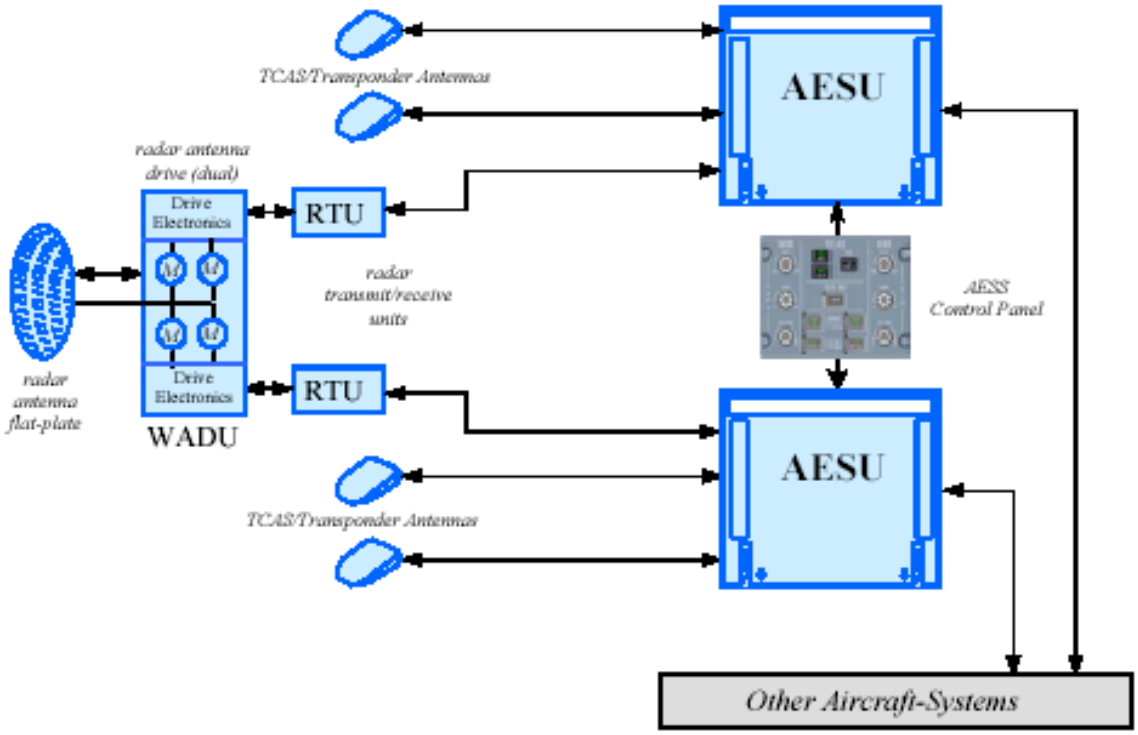


Figure 1: AESS System

The AESS performs the following functions:

- provides the flight crew with situational awareness regarding terrain, weather, and traffic
- responds to traffic interrogations from ground stations and other aircraft
- provides visual and aural alerting to the crew in case of terrain, weather, and traffic conflicts
- manages alert prioritization
- provides system resource failure monitoring and reporting (BITE)
- manages reconfiguration of system resources as part of normal operational procedures or upon resource failures
- provides data loading capability for application software and data bases.

Only the Traffic Collision Avoidance System (TCAS) and Mode S Transponder (XPDR) are applicable to this document referred to as AESU TPL-100 and indicated in the figure below.

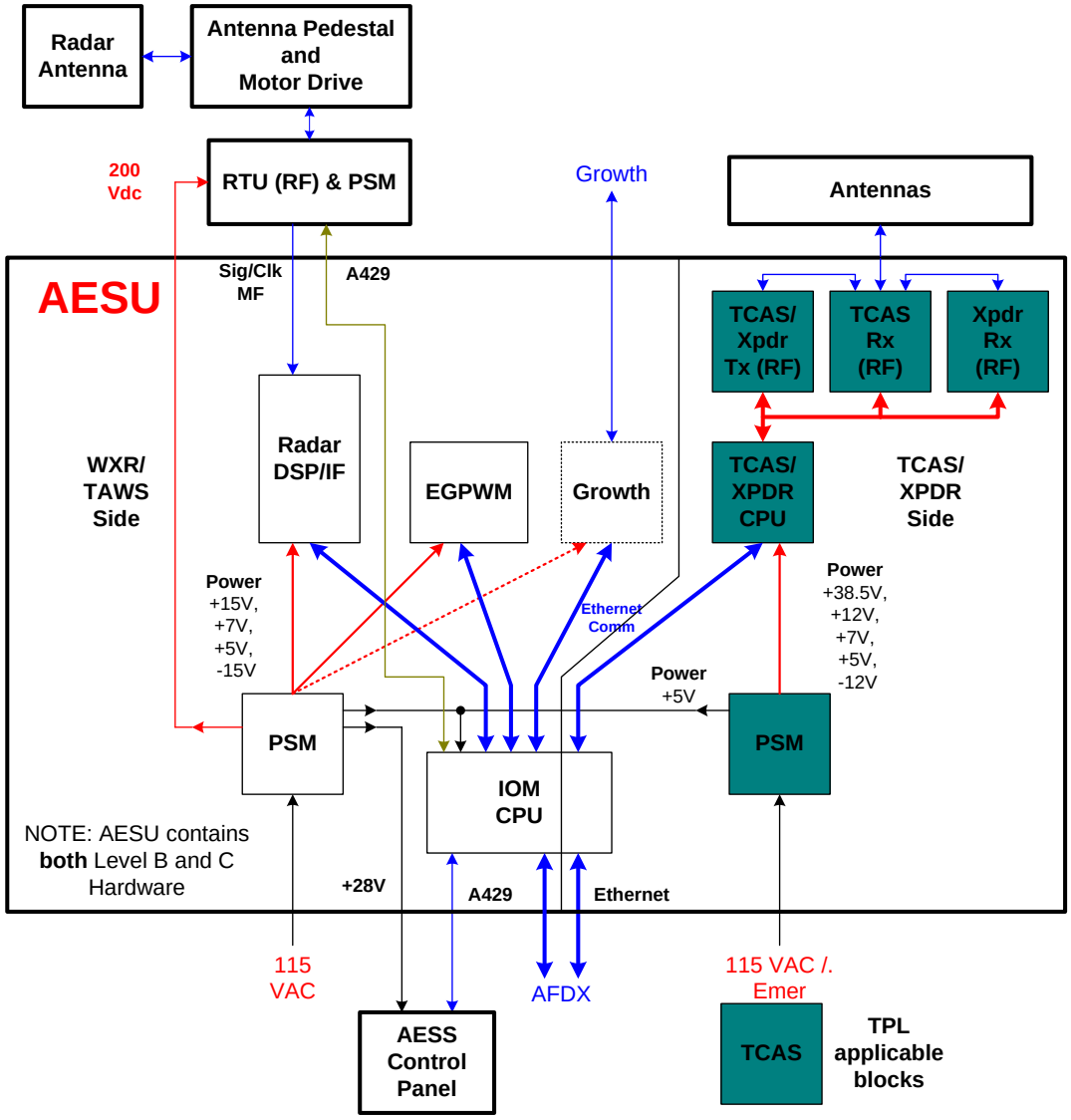
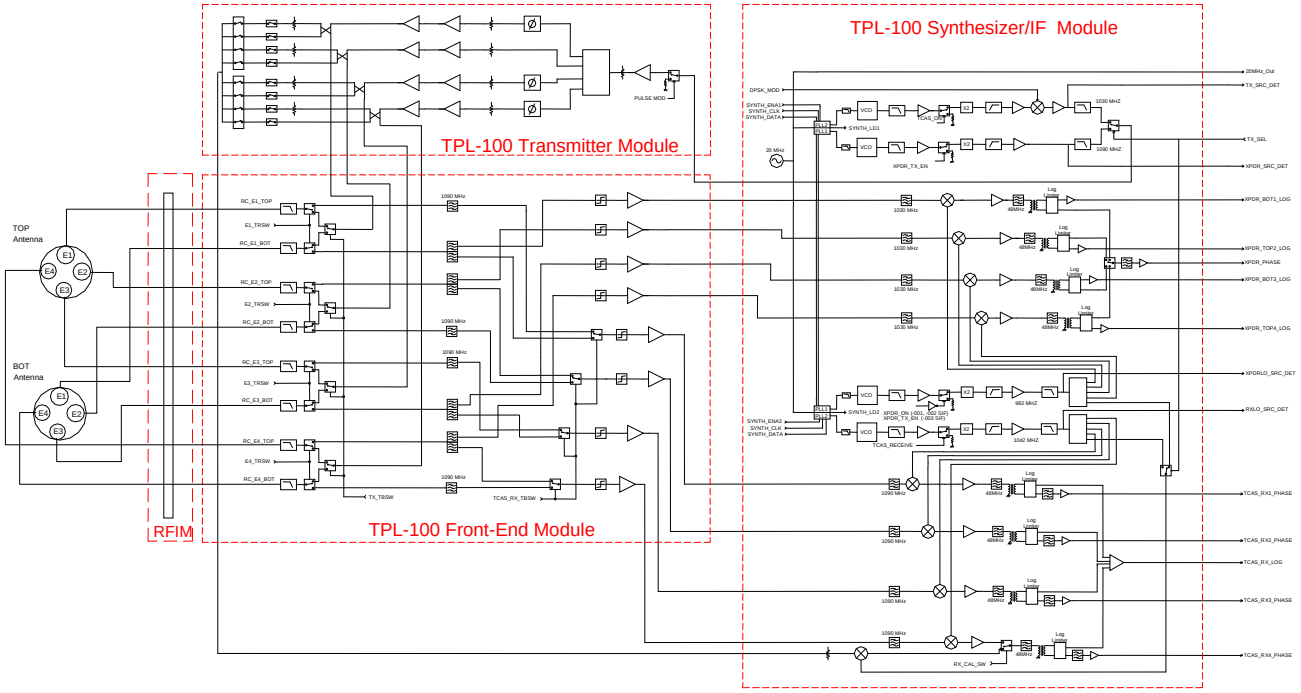


Figure 1-2: AESS Hardware End Items

2. AESU TPL-100 RF Theory of Operation

TPL-100A RF Block Diagram

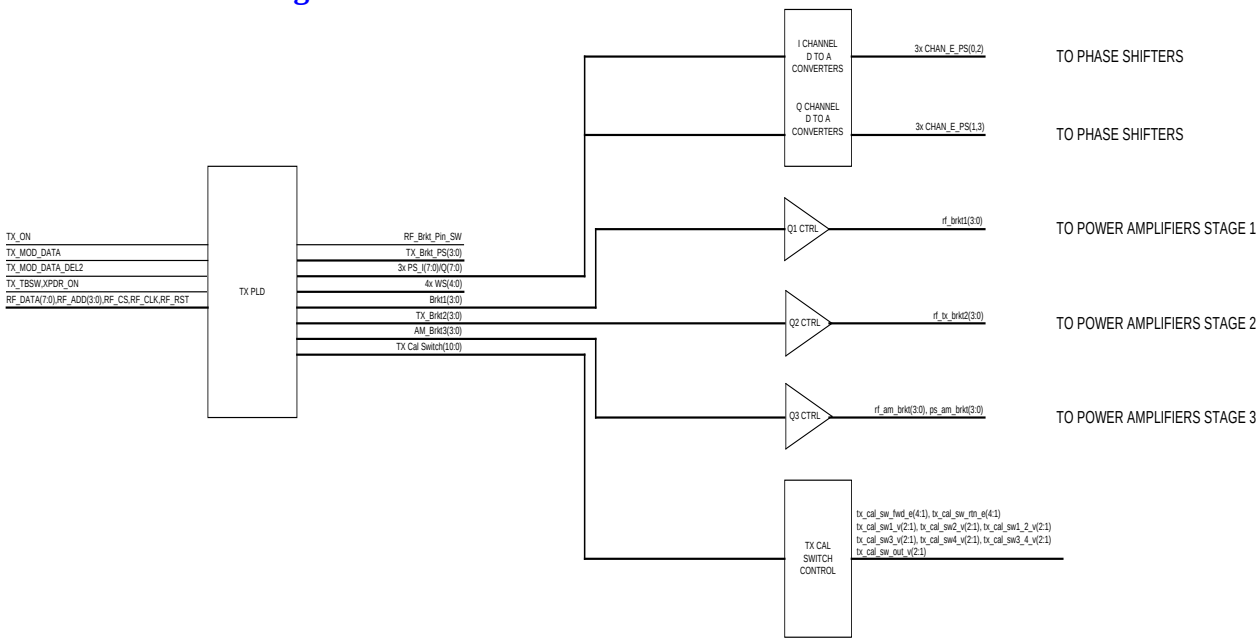


2.1. AESU TPL Transmitter Assembly

The transmitter consists of the following primary sub circuits:

- Digital interface control
- RF modulator / pulse forming network
- Four power amplifier channels
- RF amplifier bias control
- Integrated phase shifters
- Integrated Whisper/Shout attenuators
- Transmitter calibration

2.1.1. AESU TPL Digital Interface Control



The digital interface control consists of a PLD, three sets of 8-bit digital to analog converter(s) (DAC), three sets of bias drivers and four quad analog switches.

The PLD contains one-time programmable logic gates configured to drive the phase shifters, digital attenuators, RF power amplifier gates, RF modulation signals and transmitter calibration switches. The PLD inputs are the timing brackets which drive the RF power amplifier gates, 4 address lines, 8 data lines and chip select, clock and reset lines. The output levels of the PLD are 3.3V Transistor-Transistor Logic (TTL).

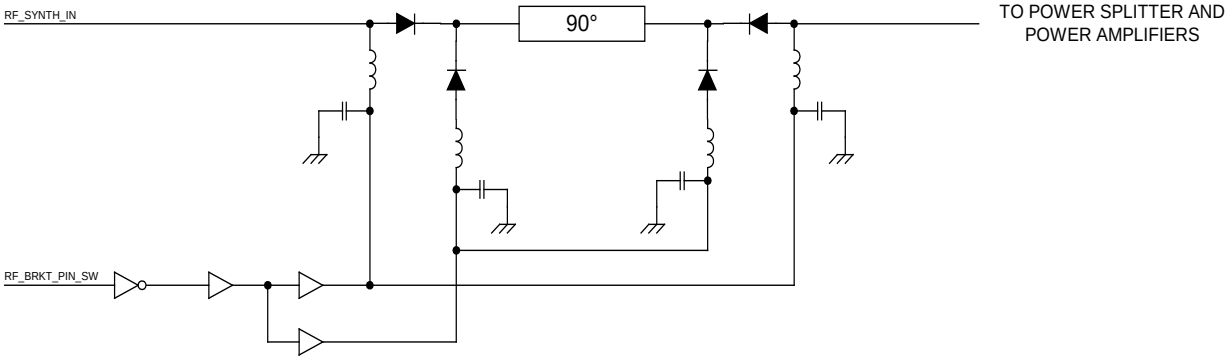
RF channels 1, 3 and 4 contain phase shifters. Channel 2 is the reference channel and does not use a phase shifter. Three pairs of 8-bit DACs control the three RF phase shifters. Each 8-bit DAC controls an I channel or a Q channel of the associated phase shifter.

Each DAC takes a TTL input from the PLD and outputs an analog level to the associated phase shifter in the RF channel.

Bias drivers which take TTL signals from the PLD control the timing of each of the three stages of the power amplifier channels. A current source controls stage 1. A bias control circuit controls the voltage levels at the gates of stages 2 and 3.

The transmitter calibration circuit consists of a network of Monolithic Microwave Integrated Circuit (MMIC) switches controlled using four quad analog switches. The PLD controls the analog switches using a logic map to switch the selected RF path to the calibration output connector.

2.1.2. AESU TPL RF Modulator / PFN

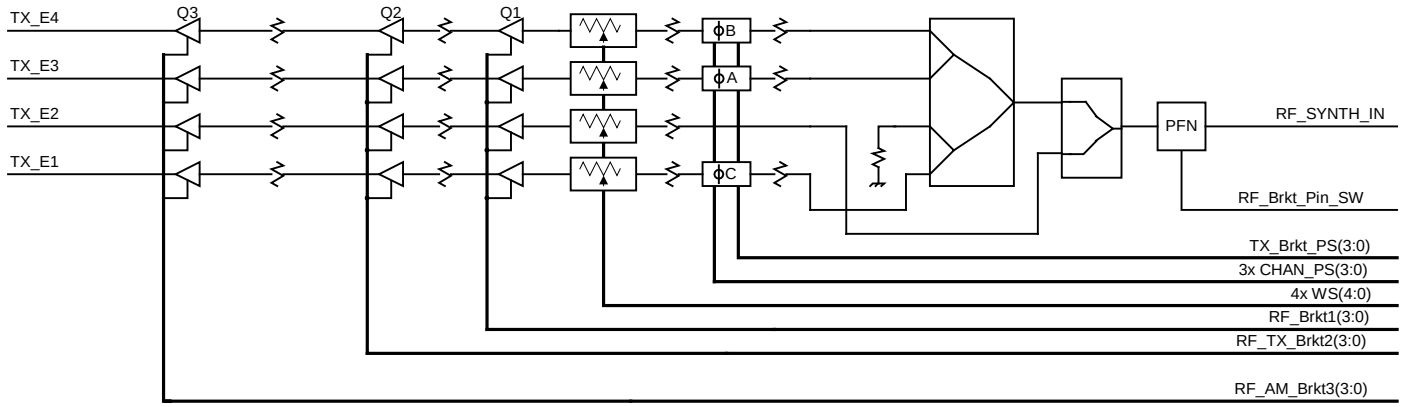


The PFN directly modulates the RF signal generated from the receiver assembly.

The PLD drives a TTL signal to an inverter gate at RF_BRKT_PIN_SW. The inverter gate shifts the voltage level into the PFN and drives the control amplifiers. The control amplifiers drive the PIN diodes of the RF circuit and modulate the RF signal received at RF_SYNTH_IN. The positive-intrinsic-negative (PIN) diodes in the RF circuit attenuate or pass the RF signal as they are activated by the control amplifiers.

The 90 degree phase shift, comprised of lumped components, increases the attenuating capability of the RF circuit.

2.1.3. AESU TPL Four power amplifier channels



The four power amplifiers comprise 3 stages. Each stage is gated on during the transmit cycle.

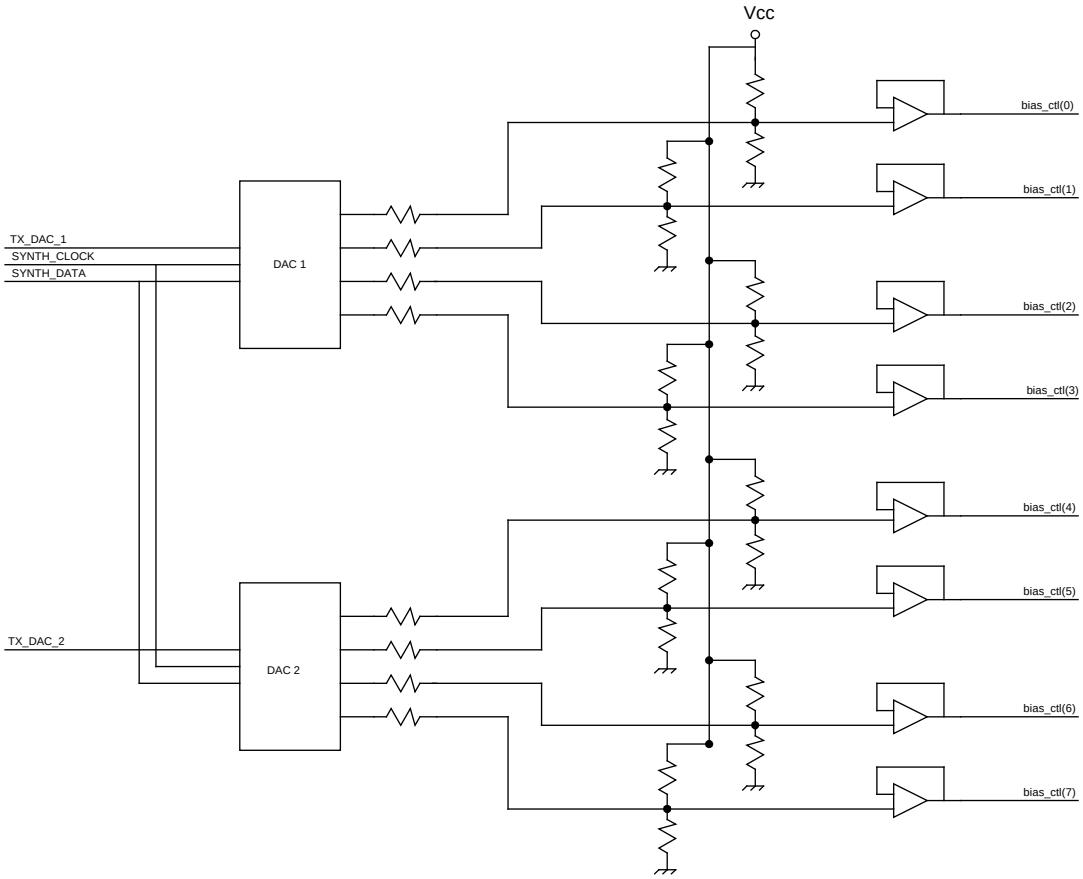
The first stage uses a MMIC gain block capable of delivering +9 dbm.

The second stage is a commercial IC which is made up of 3 stages. It is capable of delivering 10 watts of power. The gain is controlled by adjusting the level of each gate voltage driven separately by rf_tx_brkt2(0), rf_tx_brkt2(1), rf_tx_brkt2(2), and rf_tx_brkt2(3) . The gain is adjusted to compensate for temperature variation of the chain. The drain voltage is set to 26 volts.

The output stage is a laterally diffused metal oxide semiconductor (LDMOS) device capable of delivering 200 watts. The gate voltage is adjusted for a drain current of 1.8 amp when no RF signal is present. The gate voltages

are independently controlled with rf_am_brkt3(0), rf_am_brkt3(1) , rf_am_brkt3(2), and rf_am_brkt3(3). The drain voltage is set to 32 volts using 4 linear voltage regulators.

2.1.4. AESU TPL RF amplifier bias control



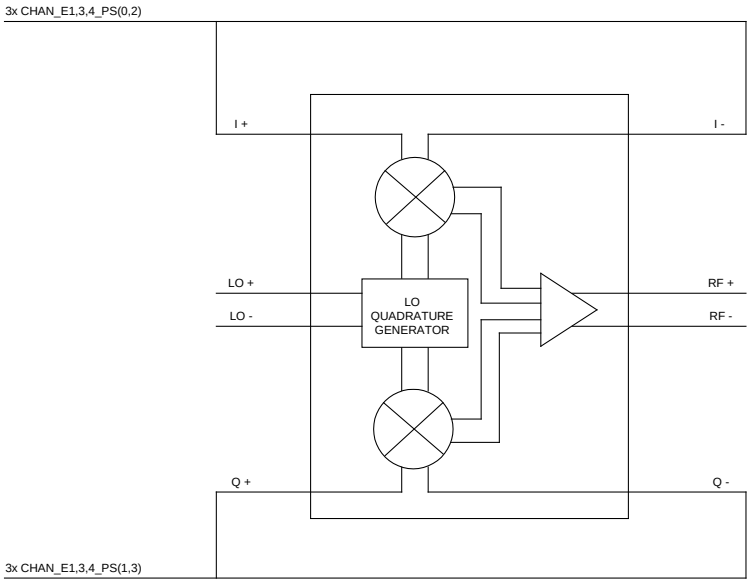
The peak current of the stage 1 IC is set to 27ma using feedback amplifiers Q13, Q14, Q15, and Q16.

The gate signal timing pulses tx_brkt2(0), tx_brkt2(1), tx_brkt2(2), tx_brkt2(3) going to the 2nd stage amplifier MHVIC910HR2 are ac coupled to prevent excessive duration of the transmitted pulse. The level of each gate signal bias_ctl(0), bias_ctl(2), bias_ctl(4), bias_ctl(6) is adjusted by measuring the drain current in each IC. The current is measured by measuring the voltage across R468 (1 ohm). This voltage is proportional to the 26 volt power supply going to the power amplifier.

The gate bias to the output stage is adjusted to control the drain current. The power supply voltage to the metal-oxide semiconductor field-effect transistor (MOSFET) driver is adjusted to control the 4 gate bias lines (bias_ctl(1), bias_ctl(3), bias_ctl(5), bias_ctl(7)) . The gate bias is ac coupled to prevent CW transmission in the case of a digital fault. The drain current is measured by measuring the voltage across 1 ohm resistor, R468.

Software turns on each stage individually to make current measurements.

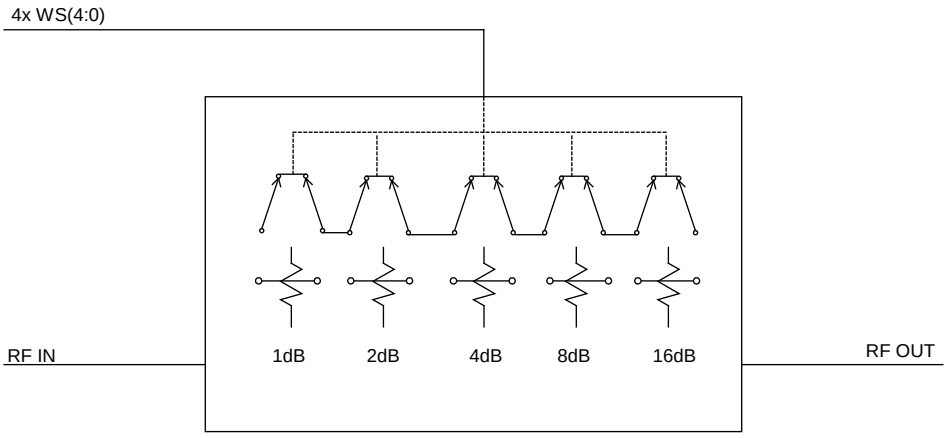
2.1.5. AESU TPL Integrated phase shifters



The 3 phase shifters use I/Q modulators to adjust the phase. The Q and I input levels are differential signals coming from 8 bit DACs.

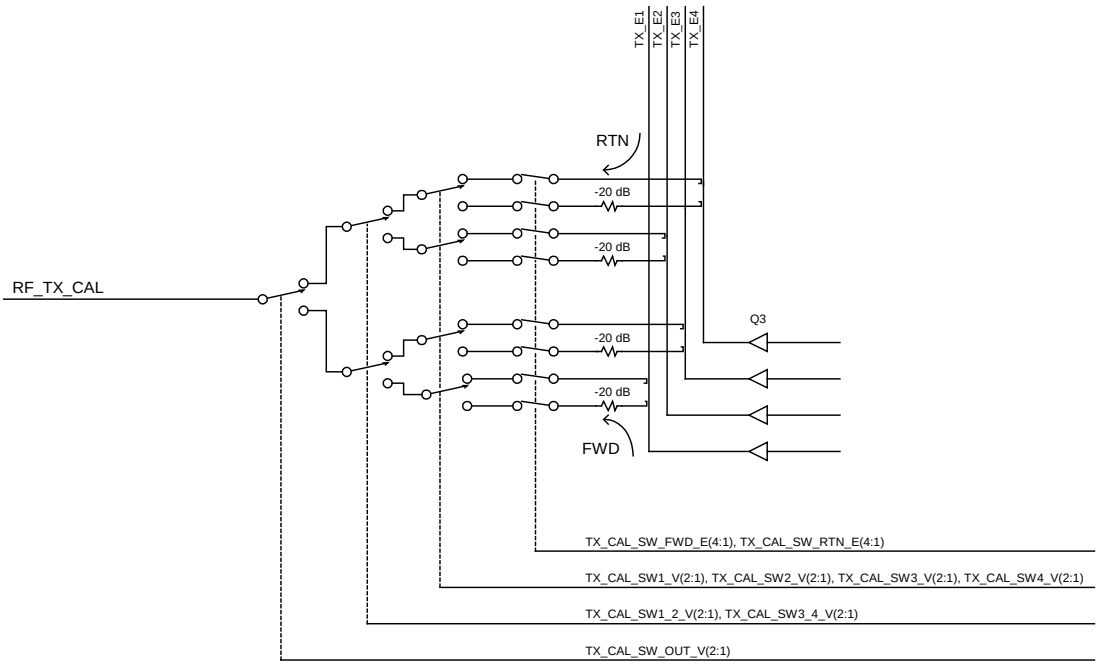
The I and Q input signals also adjust the gain by up to 6 db. They are labeled chan_e1_ps(3:0) ,chan_e3_ps(3:0), chan_e4_ps(3:0). The phase shifters are turned on only during the transmit cycle by TTL signals rf_tx_brkt_ps(0), rf_tx_brkt_ps(2), and rf_tx_brkt_ps(3).

2.1.6. AESU TPL Integrated WS attenuators



Each of the four power amplifier channels uses a WS attenuator. The WS attenuators use a commercial MMIC which is a 5-bit digital attenuator with integral TTL driver. The PLD directly controls the WS attenuator for each channel independently through signals WS_E1(4:0), WS_E2(4:0), WS_E3(4:0) and WS_E4(4:0). The attenuation step size is 1dB and provides 31dB of total attenuation range.

2.1.7. AESU TPL Transmitter calibration



The transmitter calibration network consists of four printed couplers and three sets of MMIC switches.

At the output of each of the four power amplifier channels there is a printed coupler used to sample the RF power level at the output of the transmitter. The forward arm of each coupler contains a 20dB attenuator to protect the MMIC switches in the calibration network.

The first set of MMIC switches are single pole – single throw and switch either the forward or return arm of the printed coupler into the calibration network. These are controlled using the TX_CAL_SW_FWD_E(4:1) and TX_CAL_SW_RTN_E(4:1) signals.

The second set of MMIC switches selects the channel which is to be calibrated. These are controlled using the TX_CAL_SW1_V(2:1), TX_CAL_SW2_V(2:1), TX_CAL_SW3_V(2:1) and TX_CAL_SW4_V(2:1) signals.

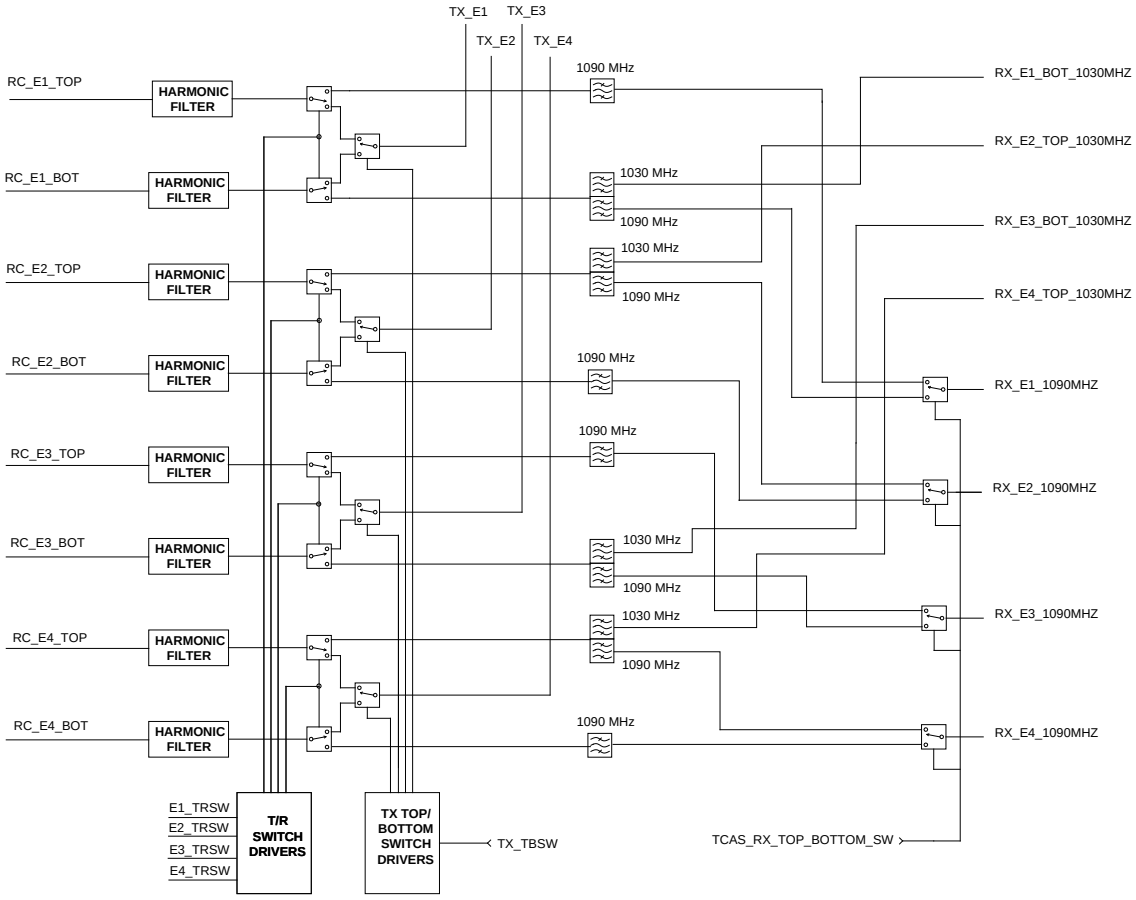
The third set of MMIC switches connects the selected channel to the output connector. These are controlled using the TX_CAL_SW1_2_V(2:1) and TX_CAL_SW3_4_V(2:1) and TX_CAL_SW_OUT_V(2:1) signals.

2.2. AESU TPL Receiver Assembly

The receiver consists of the following primary sub circuits.

- RF Switch
- LNA
- IF
- Synthesizer

2.2.1. AESU TPL RF Switch



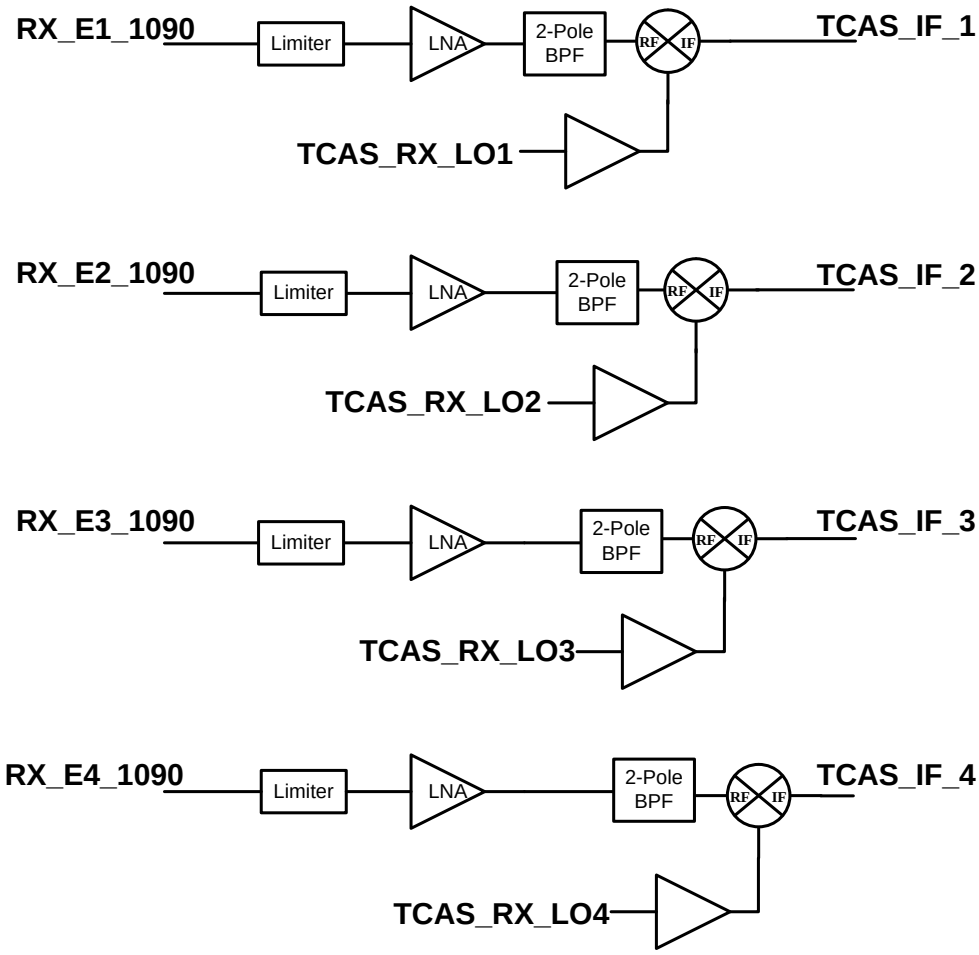
The RF switch section contains the transmit top/bottom antenna switch, transmit/receive switch, TCAS receive top/bottom switch, transmit top/bottom switch drivers, and transmit/receive switch drivers. The RF switches consists of an arrangement of one-quarter wavelength microstrips with pin diodes that provide multiple RF signal pathways. The transmit top/bottom switch has common control for the four channels and the transmit/receive switch has individual control for each channel. Each of the eight antenna inputs has a harmonic filter before the RF switches.

The transmit/receive switching elements are controlled individually by four power MOSFET drivers and are controlled by the logic signals E1_TRSW, E2_TRSW, E3_TRSW, and E4_TRSW. The transmit TOP/BOTTOM switching elements are controlled by logic signal TX_TBSW. Switching time is 400 nanoseconds (ns), or less. The transmit top/bottom switch provides 20 dB minimum isolation between elements. The transmit/receive switch provides 20 dB minimum isolation between paths.

The RF Switch section also contains the first stage of filtering for the receive signals. High-Q ceramic 2-pole bandpass filters are used in each receive signal path to attenuate out of band signals.

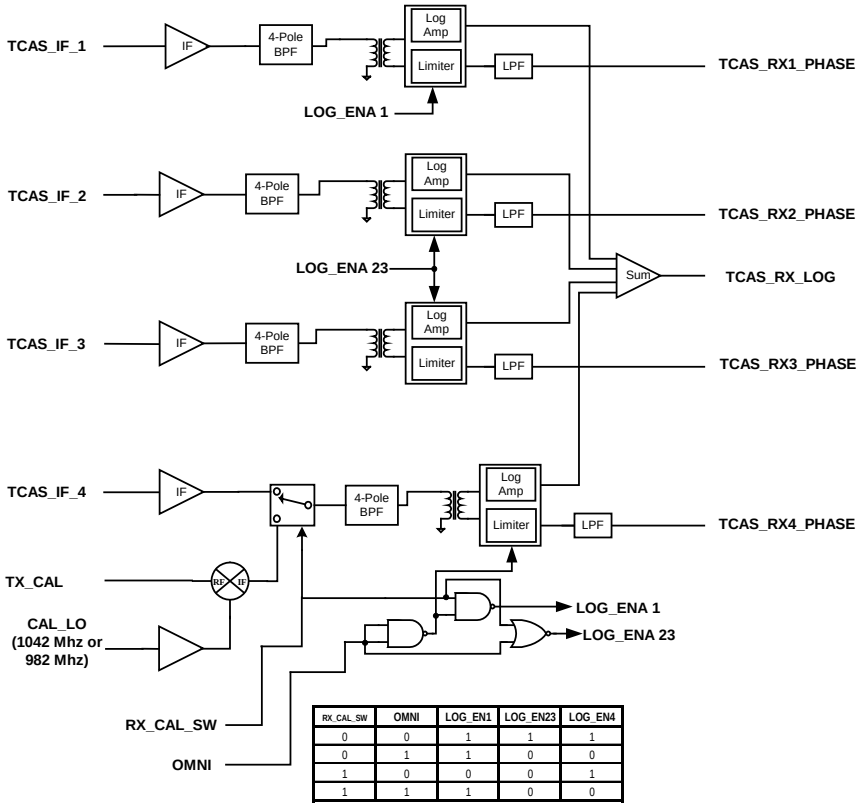
RX_ Ex_1030MHz and RX_Ex_1090MHz signals are then routed to the Limiter/LNA sections of the receiver. TX_E1 through TX_E4 are each routed to a connector that brings in the transmit signal from the transmitter module.

2.2.2. AESU TPL Rx 1090 MHz - LNA



The LNA section is shown. This section includes a limiter, LNA and 1090 MHz bandpass filtering for the input RF signals for the four receiver channels. This section rejects image frequencies and any other noise outside the selected band. The low-level received signals in each receiver channel are boosted to a higher level by the LNA, and then filtered by filtered by high-Q ceramic 2-pole bandpass filters,. A diode limiter circuit is used for protection from high input power. The 1090 MHz received signal is mixed with the 1042 MHz RX_LO (1-4) to produce the 48 MHz IF output for each channel that is sent to the IF section. Each 1042 MHz RX_LO signal is applied to a RF gain block amplifier to apply proper signal strength for the mixers.

2.2.3. AESU TPL Rx 1090 MHz – IF

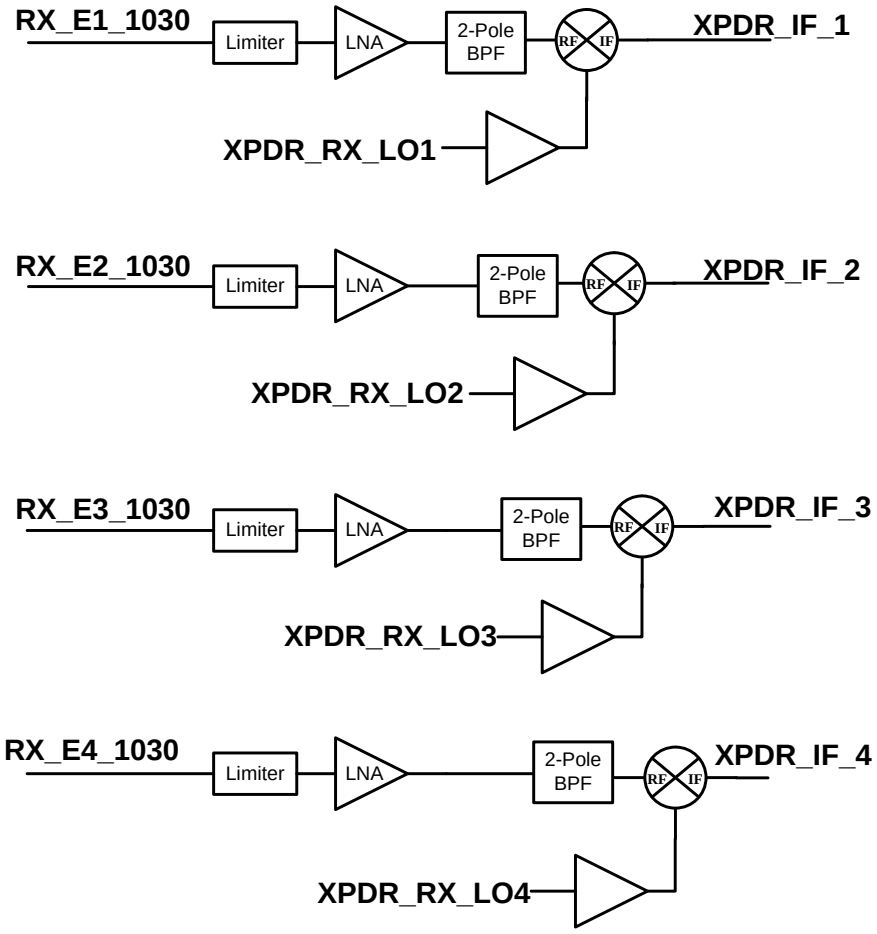


RX_CAL_SW	OMNI	LOG_EN1	LOG_EN23	LOG_EN4
0	0	1	1	1
0	1	1	0	0
1	0	0	0	1
1	1	1	0	0

The IF section, shown in block diagram, provides an additional stage of amplification for each of the four receiver channels provides additional filtering for the 48MHz IF signals, and divides each channel into limited video to the digital module, and a summed log signal to the digital module.

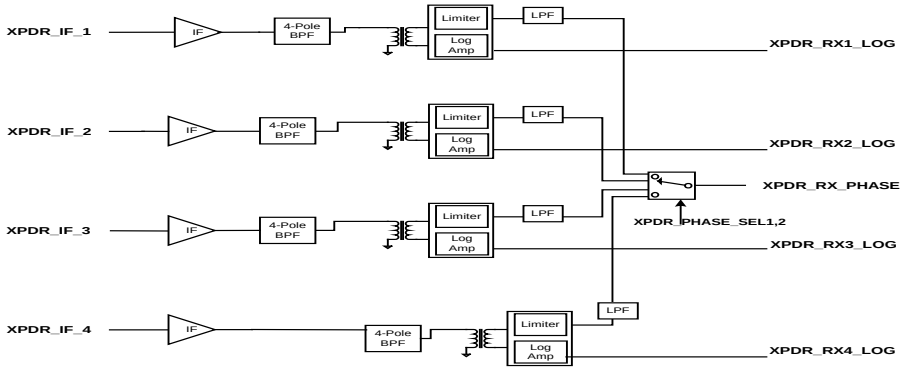
The IF inputs from the LNA section (TCAS_IF_1, IF_2, IF_3, and IF_4), that are received replies from the antenna are each amplified and filtered through a 4-pole band pass filter (BPF). The IF_4 signal differs from the other channels in there is a single pole double throw (SPDT) which can route in the TX_CAL signal for transmitter calibration of 1090 MHz and 1030 MHz transmissions. These signals are then applied to a limiting-logarithmic amplifier. A lumped element low pass filter (LPF) further filters the limiting signal. Each log amplifier produces an output that is a logarithmic function of its input. The outputs from the four log amplifiers are applied to a log summer and buffer circuit, which produces a negative pulse output scaled to 20 millivolts (mV) per dB. The TCAS_RX_LOG output is routed to the digital module where it is decoded to determine range and altitude.

2.2.4. AESU TPL Rx 1030 MHz - LNA



The LNA is shown. This section includes LNA and 1030 MHz bandpass filtering for the input RF signals for the four receiver channels. This section rejects image frequencies and any other noise outside the selected band. The low-level received signals in each receiver channel are boosted to a higher level by the LNA, and then filtered by high-Q ceramic 2-pole bandpass filters. A diode limiter circuit is used for protection from high input power. The 1030 MHz received signal is mixed with the 982 MHz RX_LO (1-4) to produce the 48 MHz IF output for each channel that is sent to the IF section. Each 982 MHz RX_LO signal is applied to a RF gain block amplifier to apply proper signal strength for the mixers.

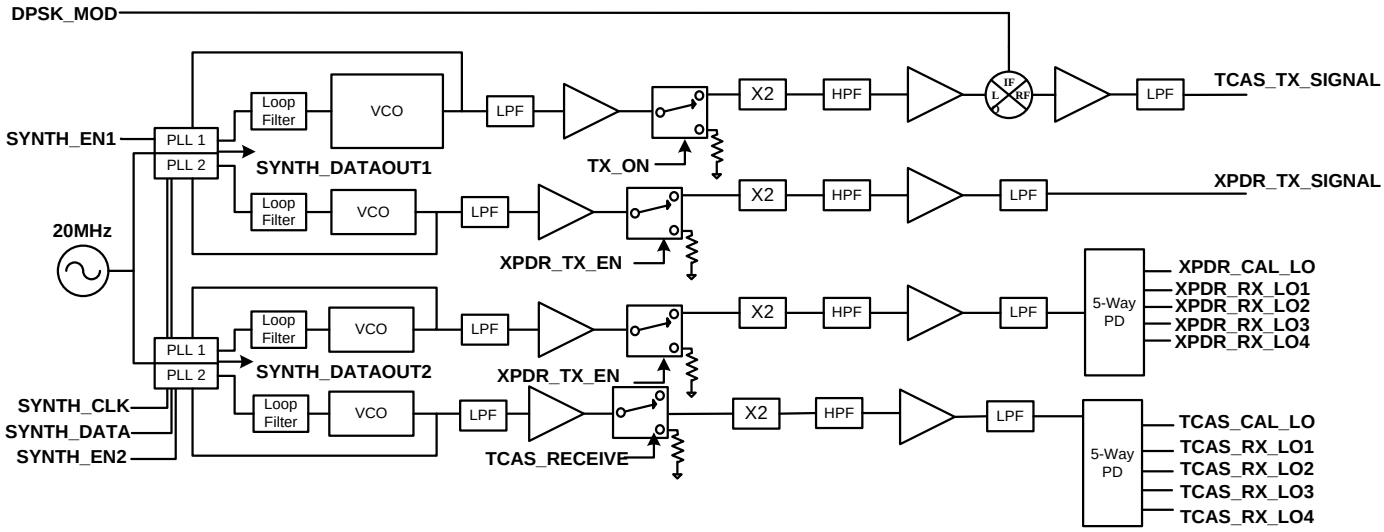
2.2.5. AESU TPL Rx 1030 MHz - IF



The IF section, shown in block diagram, provides an additional stage of amplification for each of the four Transponder receiver channels provides additional filtering for the 48MHz IF signals and divides each channel into limited video to the digital module, and a summed log signal to the digital module.

The IF inputs from the LNA section (XPDR_IF_1, IF_2, IF_3, and IF_4) that are received replies from the antenna are each amplified and filtered through a 4-pole BPF. These signals are then applied to a limiting-logarithmic amplifier. A lumped element LPF further filters the limiting signal. Each log amplifier produces an output that is a logarithmic function of its input. The outputs from the four limiter amplifiers are selected by a switch and the XPDR_RX_PHASE signal is routed to the digital module where it is decoded along with the four XPDR_RX_LOG outputs.

2.2.6. AESU TPL Tx and Rx Synthesizers



The synthesizer, shown in block diagram, produces the TX_SIGNALs, CAL_LOs, TCAS_RX_LO (1-4), XPDR_RX_LO (1-4) and 20 MHz. The TCAS_TX_SIGNAL generates the following frequencies, 1030MHz (TCAS_TX_SIGNAL), 1087MHz, 1090MHz, and 1093MHz (XPDR_TX_SIGNAL) as selected by TX_SEL to the transmitter. The calibration LO (CAL_LO) frequency is 982 MHz (XPDR_CAL_LO) or 1042 MHz (TCAS_CAL_LO) as selected by TX_SEL. The transponder receiver LO (XPDR_RX_LOx) frequency is 982MHz. The TCAS receiver LO (TCAS_RX_LOx) frequency is 1042MHz.

Each signal is generated from a single 20 MHz crystal oscillator, which is installed in an oven for precise performance over a wide range of operation temperatures. The 20 MHz signal is applied to two separate dual Phase Lock Loop (PLL) IC. Each PLL circuit operates a voltage controlled oscillator with a loop filter to generate the synthesized frequency. The synthesized frequencies are 521MHz for the TCAS_RX_LO, 545 MHz for the XPDR_TX_SIGNAL, and 491 MHz for the XPDR_RX_LO. The TCAS_TX_SIGNAL can generate four different synthesized frequencies, 515, 543.5, 545, and 546.5 MHz, depending on transmitter operation.

The following synthesized signals TCAS_TX_SIGNAL, XPDR_TX_SIGNAL, XPDR_RX_LO, and TCAS_RX_LO are applied to hybrid LPF and RF gain block. A single pole double throw (SPDT) RF switch is used as an on-off switch. The switch's second output is an RF termination. This is controlled by a TTL signal for each synthesized frequency. The synthesized frequency is then doubled to obtain the output frequency. It is filtered with a hybrid band pass filter (HBF) and isolated with RF gain block.

The TCAS_TX_SIGNAL is routed to the DPSK mixer, where it can be mixed with a modulated DPSK signal that is generated by 250ns pulse square wave with a 50% duty cycle from the digital module. An additional RF gain stage is used for isolation and then the signal is further filtered by hybrid LPF and then sent directly to the transmitter module.

The XPDR_RX_LO and TCAS_RX_LO frequencies are filtered by a hybrid LPF. Each signal is routed to the calibration mixer and the RX_LO is split into five signals by an RF power divider. Four of these signals become Local Oscillator(s) (LO)s for the main receive channels. The fifth signal from each divider is routed to the cal mixer.

The 20MHz signal from the oven controlled crystal oscillator (OCXO) is buffered and then routed through the Front Interconnect to the digital module.

3. AESU TPL Modulation Scheme

3.1. 1090Mhz Mode S Transmissions

Pulse Position Modulation

4 Pulse Preamble

Pulse width	0.5 usecs
Pulse position	0, 1, 3.5, and 4.5 usecs
Rise/Fall time	50-100/50-200 nsecs.

56 or 112 Data Bits (Manchester encoding)

Pulse width	0.5 usecs
Data rate	1Mhz
Pulse position	"1" – first 0.5 usec data chip "0" – second 0.5 usec data chip
Rise/Fall time	50-100/50-200 nsecs.

3.2. 1090Mhz Mode A/C Transmissions

Pulse Position Modulation

2 Framing Pulses positioned at 0 and 20.3 usecs

Up to 13 data pulses positioned every 1.45usecs between framing pulses.

1 SPI pulse positioned at 24.65 usecs

Pulse width	0.45 usecs
Rise/Fall time	50-100/50-200 nsecs.

3.3. 1030Mhz Mode A/C Transmissions

Pulse Position Modulation

5 Pulse spacing	@ 0, 2, 4, 21, 23 usecs for Mode C @ 0, 2, 4, 8, 10 usecs for Mode A.
Pulse width	0.8 usecs.
Rise/Fall time	50-100/50-200 nsecs.

3.4. 1030Mhz Mode S Transmissions

Pulse Position/DPSK Modulation

Pulse Position Modulation

P1, P2, and P6 pulses positioned at 0, 2, and 3.5 usecs

P1/P2 Pulse width	0.8 usecs for P1 and P2
P6 Pulse width	16.25 usecs for 56 Bit message 30.25 usecs for 112 Bit message.
Rise/Fall time	50-100/50-200 nsecs.

DPSK Modulation

Modulation rate and type	4Mhz DPSK during P6
Preamble	7 bits "0000010" at start of P6
Data rise time	<80 nsecs while maintaining spectral limits.

4. AESU Identification Plate

HPN620-1967-127 (top label)

HPN620-1967-128 (bottom label)