

Transmitter Alignment Procedure

There are no alignment manual adjustments for the TPL-100A transmitter. Shown below is the test procedure.

TPL-100A Transmitter Test

1. Introduction

2. Test Panel Setup

- 2.1 Select board number or type in TX BOARD window.
- 2.2 Left mouse click in BITE TX3 window, select Current Monitor.
- 2.3 Drop down menu in DMM SELECT, select 36V supply.
- 2.4 Enable "TRIGGER", "TX_MOD", "TX_MD2", "TX_ON" signals by selecting buttons to left of each.

3. Continuity Test

Connect transmitter module 722-4506-012 to test fixture and attach all power and RF connections.

- 3.1 Turn on +7V supply only.
 - 3.2 Check the +7V supply for current limiting.
 - 3.3 Check the Digital Attenuator bits for shorts:
Set attenuators for all channels to maximum attenuation, using the "gang" setting, -31dB.
 - 3.3.1 Load programmable logic device (PLD)
 - 3.3.2 Monitor +7V supply for current limiting
 - 3.4 Check the in-phase quadrature (IQ) digital to analog converter (DAC) bits for shorts:
 - 3.4.1 Set all bits to DACs by loading "128" in the in-phase (I) and quadrature (Q) fields and "gang" all DACs.
 - 3.4.2 Load PLD
 - 3.4.3 Monitor +7V supply for current limiting
- ### **4. Set Timing, Set Driver and Output Bias Levels:**
- 4.1 Enable "TRIGGER", "TX_MOD", "TX_MD2", "TX_ON" signals by selecting buttons to left of each.
 - 4.2 Go to OPERATE drop down menu, select SETUP, disable remaining two columns, go back to OPERATE.
 - 4.3 Set timing column1 to 2 μ s, column2 to 500nS, column3 to 800nS, column4 to 750nS, column5 to 2 μ s
 - 4.4 Adjust bias control for each driver and output stage, using slider or rocker switch to set proper bias.
 - 4.5 Record bias current and bit setting for driver and output of each channel

Bias Control Procedure

1. Turn on external +7V and +36V power supplies
2. Enable TX_ON and TX_MOD by selecting buttons to left of each.

3. Disable all timing columns except column 6 (AM mod). Go to OPERATE drop down menu, select SETUP, disable remaining two columns, go back to OPERATE.
4. Set column 6 timing to 4 μ s
5. OFF μ s window: set period off time to 320 μ s
6. N FILTER window: reset filters to 4 samples.
7. Zero and null pulses: select RESET, NULL & SET DELTAS filters buttons.
8. In BIAS CONTROL REGISTER: Set each driver (DRVR) and each output (OUTP) stage one at a time.
9. Enable AUTO located in BIAS CONFIG area.
10. Select LOAD FIFO then CONFIG/START

5. Timing Requirements

Use Crystal Detector with 20dB pad,

Oscilloscope settings: BW @ 20 MHz, 500nS/ Div, 200mV/Div, Avg @ 16 samples

Measurement of risetime, falltime and pulse width:

Rise and fall time measured between 1dB and 20dB below peak power level.

Pulse width measured at 6dB below peak power level.

Spec: Risetime 50 – 100nsec, Fall time, 50 – 200nsec, Pulse Width, 750 – 850nsec

5.1 Set Automatic Gain Control (AGC)-3dB, W/S att. -6dB Ch.1,3 &4

5.2 Set W/S -9dB Ch.2

5.3 Set pulse width to 800nS (“TX_MD2”)

5.4 Check rise, fall and pulse width

5.5 Set AGC-3dB, W/S att. -26dB Ch.1,3 &4

5.6 Set W/S -29dB Ch.2.

5.7 Set pulse width to 800nS.

5.8 Check rise, fall and pulse width

6. Power Out:

Spectrum analyzer settings: Freq. 1030 MHz, Span 200 MHz, Res. BW 3 MHz, Swp 3.5s, + offset. Use spectrum analyzer to measure 2nd harmonic.

Assure input to PPM/spectrum analyzer is padded, protected from high power. Use PPM to measure power out and Cal port power.

Cal Port measurements: From CAL CHANNEL window select CHANNEL (1,2,3 or 4) FORWARD

6.1 Set timing 6mS rep, 1 μ s width

6.2 Set phase to 0

6.3 Set AGC to 6dB Ch. 1,3 & 4

6.4 Set W/S attenuator to 0

6.5 Record data

TX Cal Reverse Path

6.6 Make sure RF is off and that all stages of the amplifier are biased off. Test can be done using either a signal generator and spectrum analyzer or a vector network analyzer (VNA).

- 6.7 Using external generator, inject 0dBm Continuous Wave (CW) power into the output of each channel and measure the output power at the TX_CAL output connector, J6. Use the tx control software to set the output to each channel return path.

Pulse Droop

Spec: -.5dB max

- 6.8 Set pulse width to 30 μ s

- 6.9 . Set AGC-3dB, W/S att. -6dB Ch.1,3 &4

- 6.10Set W/S -9dB Ch.2

- 6.11Check pulse droop, in dB, between 1 μ s and 29 μ s for each channel

7. Spectrum (ATCRBS)

Measure each channel alone, with all other channels off.

- 7.1 Set AGC to 3 dB channels 1,3 &4.
- 7.2 W/S att. to 3 dB channels 1,3 &4.
- 7.3 W/S att. to 3 dB channel 2.
- 7.4 Set up spectrum analyzer as follows: Freq: 1030 MHz, Span 200 MHz, Res BW 3 MHz
- 7.5 Take peak marker reading, set delta marker.
- 7.6 Set spectrum analyzer lower freq to 970 MHz, upper freq to 990 MHz and Res BW to 100 KHz.
- 7.7 Take reading at 970 MHz delta marker and 990 MHz delta marker.
- 7.8 Set spectrum analyzer lower freq to 1070 MHz, upper freq to 1090 MHz and Res BW to 100 KHz.
- 7.9 Take reading at 1070 MHz delta marker and 1090 delta marker.

8. Relative Phase, Each Ch

Each channel measured alone.

Use AD 8302 phase detector.

- 8.1 Set AGC to -3dB Ch. 1, 3 & 4
- 8.2 Set W/S att. to -6 Ch. 1,3 & 4 .
- 8.3 Ch.2 set to -9dB
- 8.4 Record voltage setting of phase detector output from scope.

9. Relative Phase, All Chs Coupling to Ch 2

Gang IQ so channels 1,3 &4 change together.

- 9.1 Set AGC to -3dB Ch. 1, 3 & 4
- 9.2 Set W/S att. to -6 Ch. 1,3 & 4
- 9.3 Ch.2 set to -9dB.
- 9.4 Measure Pout for Ch.2 for phase shift of Ch. 1,3 & 4