IC-FR3000 VHF REPEATER

CIRCUIT DESCRIPTION

1 RECEIVER CIRCUITS

1-1 RF CIRCUIT (RX UNIT)

RF signals from the antenna connector pass through the tunable Band-pass filter (D3, L2, D4, L3) and then applied to the RF amplifier (Q1) after passing through the band-pass filter of 2 steps(C207,L6,C208,L7).

Variable-capacitor diodes are employed at the band-pass filters that track the filters and Are controlled by CPU (LOGIC UNIT IC33) via the buffer IC (IC5).

1-2 1ST MIXER AND 1ST IF CIRCUIT (RX UNIT)

The 1st mixer circuit (IC1) converts the received signals to a fixed frequency of the 1st IF signal with a 1st local output signal. By changing the PLL frequency, only the desired frequency will pass through the band-pass filter at the next stage of 1st mixer circuit.

The RF signals are mixed with 1st LO signals at the 1st mixer (IC1) to produce a 31.65 MHZ 1st IF signal.

The 1st IF signal is output from IC1 pin 4,5 and passed through the crystal band-pass filter (FI1) to suppress unwanted harmonic components.

The filtered signal is amplified at the IF amplifier (Q3). The amplified signal is applied to the 2nd mixer and IF circuit (IC2).

1-3 2ND IF AND DEMODULATOR CIRCUITS (RX UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal (455kHz).

A double conversion super-heterodyne system (which converts receive signal twice) improves the image rejection ratio and obtains stable receiver gain

The FM IC (IC2) contains the 2nd mixer, limiter and noise amplifiers, FM detector, active filter circuits, etc A 2nd LO signal (31.195 MHz).

The 31.65 MHZ 1st IF signal from the IF amplifier (Q3) is applied to the 2nd mixer section of the FM IF IC (IC2, pin 16), and is mixed with the 2nd LO signal (31.195 MHz) to be converted to a 455 kHz 2nd IF signal.

The 2nd IF signal is applied to the FM demodulator circuits、and passes through the ceramic band-pass filter (Fl5 or Fl6) The filtered signal is fed back to the IC, and amplified at the limiter amplifier section (pin 5) ,then demodulated into AF signals at the quadrature detector section (pins 10, 11).

1-4 AF AMPLIFIER CIRCUIT (LOGIC UNIT)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.
The AF signals pass through the AF mute switch (IC16), and are then applied to the volume control unit. The level controlled AF signals applied to the AF power amplifier. (IC17, pin 1) The power amplified AF signals are applied to the internal speaker (SP I) via the [SP] jack (J9) therefore, the AF output level is according to the [VOL] setting and also the squelch conditions.

2 TRANSMITTER CIRCUITS

2-1 MICROPHONE AMPLIFIER CIRCUIT (LOGIC UNIT)

The microphone signal from a FRONT unit is inputted into a LOGIC unit from J4. the inputted microphone signal - microphone amplifier (IC1D), MIX amplifier (IC2D) with other abnormal-conditions incoming signals, Pre-Emphasis (C2, R5, IC2C), HPF (IC2 B, A), a limiter (IC3A), MIX amplifier (IC3B) with signaling, and a Splatter filter (IC4A, B, C) - a passage - after that - TX unit -- it is led to an abnormal-conditions circuit.

2-2 REPEATER OPERATIONS (LOGIC UNIT)

While a receiving AF signal (DISC) is led to a speaker output system at the time of relay AF Repeater operation, in order to process also as an abnormal-conditions signal, it is led to a D/A converter (IC25) through IC14. After being set as a suitable level by IC25, it goes to a limiter (IC3A). 5/2-TONE from Signaling (encoding) CPU, and a DTME output (IC33, pin 43) -- IC3 -- it is inputted into LPF, which consists of C and D It, is compounded with a voice signal by IC3B after that. CTCSS and a DTCS signal (IC33, pin 44) pass along LPF of IC4D, and are led to TX unit. TX IC6 compounds it with a voice signal, and abnormal conditions are simultaneously hung on VCO and a PLL standard oscillation.

2-3 DRIVE CIRCUITS (TX UNIT) / POWER AMPLIFIER CIRCUITS (PA UNIT)

The RF signal from the TX VCO is amplified at the buffer amplifier (Q1), and is then applied to the pre-amplifier (PA UNT Q4). The amplified signal is amplified drive amplifier (PA UNIT IC2) is a power amplifier which provides stable 50 W output power with a 13.6 V DC power source.
Output power amplified signal passes through the TX LPF (C98, L20, C2, L7, C3, L6, C1, C100, C48, C73),and is then applied to the SWR detector (D4).
The LPF suppress high harmonics components. The signal is applied to the antenna

connector after being passed through the reverse power detector circuit (D2) The detected voltage at the reverse detector circuit is applied to the CPU (LOGIC UNIT : lC33, pin 46/47) to switch from high power to low power automatically when the SWR become worse.

2-4 APC CIRCUIT (PA UNIT)

The APC circuit protects the power amplifier (IC2) from a mismatched output load and stabilizes the RF power.

The SWR detector circuit (D2) detects forward signals and reflection signals at D4 respectively.

When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. The output voltage of the controls the power amplifier (IC2) to reduce the output power.

3 PLL CIRCUITS

3-1 GENERAL

A PLL circuit provides stable oscillation of the transmit frequency and receive local frequency. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

3-2 VCO CIRCUIT

TX-VCO CIRCUIT (TX VCO UNIT)

An oscillated signal from the TX-VCO circuit (Q1, D1-D4) passes through the buffer amplifiers (TX UNIT Q3) and TX PLL IC (TX UNIT lC2, pin 10) And is then pre-scaled in the PLL IC based on the divided ratio (N-data). The reference signal is generated at the reference oscillator (TX UNIT X1, 12.8MHz).

The reference signal is also applied to the PLL IC. The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 18,20. The output signal is passed through the loop filter and is then applied to the TX VCO circuit as lock voltage.

RX-VCO CIRCUIT (RVCO UNIT)

An oscillated signal from the RX-VCO circuit (Q1, D1-D4) passes through the buffer amplifiers (RX UNIT Q14) and RX PLL IC (RX UNIT lC4, pin 10) And is then pre-scaled in the PLL IC based on the divided ratio (N-data). The reference signal is generated at the reference oscillator (RX UNIT X3, 12.8 MHz).

The reference signal is also applied to the PLL IC The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 6 The output signal is passed through the loop filter and is then applied to the RX VCO circuit as lock voltage.

4 LOGIC CIRCUITS (LOGIC UNIT)

The backup circuit IC 37 is EEPROM and memorizes the setting information on apparatus, such as a clone. The LED control Q18, Q19, and Q20 is the current buffers for driving LED (FRONT unit). The temperature information (REGTEMP, PATEMP) from the reading REG unit and PA unit of temperature information goes into IC32, changes periodically, and is inputted into CPU by turns (TEMP).

RINGER (call correspondence number) is detected in the detection circuit, which consists of a telephone connection circuit and RINGER detection methods C375, R131, D5, D1, C100, C103, R143, R145, and IC48. If the RING signal inputted into CPU is in agreement at the ON/OFF time set up by the clone, it will start OFF-HOOK operation. - While operating RL1 with the HOOKC signal from the OFF-HOOK operation CPU, operate RL2 by DP signal from IC47 No. 18 pin, and make L1/L2 terminal into a closed loop.

- Perform 2 line-4 line conversions by flow IC46 (network IC) of the signal in OFF-HOOK. A receiving AF signal amounts to T6 through IC7D. It is led to L1/L2 terminal through IC46 after that. The voice signal from L1/L2 terminal amounts to T8 through IC46, and is led to TX abnormal-conditions line. A Dial Tone Multi Frequency is detected by IC31 (decoding IC). After detecting RINGER and becoming OFF-HOOK, IC30 changes to the call side by DTSEL2 signal from CPU, and the Dial Tone Multi Frequency from a TELAFO line is led to IC31. - If IC45 detects tone (intermittence sound which is 480Hz) during ON-HOOK operation OFF-HOOK operation, an ON-HOOK signal will be outputted to CPU. If an ONHOOK signal is in agreement with the ON/OFF time of a clone setup, a HOOKC signal and an IC47 DP signal will be controlled, and RL1/RL2 are controlled so that L1/L2 terminal serves as open loop.