TZ202021- HDD
Bridge Hardware Design

Version **1.00**

Date **04-Apr-2012**

The following people have read, understood and agreed to the information contained within the above document.

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Document History

The following table summarizes all changes to this report. Details of document change authorization can be obtained on request from the Toumaz document control system.

Issue	Description of Revision	Author	Date
1.00	First Issue	ATM	04-Apr-2012

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Contents

1 Scope

1.1 Reference Documents

TZ202020-HDS Bridge Hardware Design Specification Document Ref 100001152344 Issue 1.60, 02-Mar-2011.

1.2 Abbreviations

ADC	**A**nalogue to **D**igital **C**onverter
BS	**S**ensium **B**ase **S**tation
CE	**C**onformité **E**uropéenne – conformance marking
CRC	**C**yclic **R**edundancy **C**heck
ECG	**E**lectro**c**ardio**g**ram
FAE	**F**ield **A**pplication **E**ngineer
FCC	**F**ederal **C**ommunications **C**ommission – US Standard Agency
FMEA	**F**ailure **M**ode and **E**ffect **A**nalysis
GPIO	**G**eneral **P**urpose **I**nput **O**utput
GUI	**G**raphical **U**ser **I**nterface
HDS	**H**ardware **D**esign **S**pecification
IDC	**I**nsulation **D**isplacement **C**onnector
IFU	**I**nstructions **F**or **U**sers
ISM	**I**ndustrial **S**cientific and **M**edical
ISP	**I**n **S**ystem **P**rogramming
ITU	**I**nternational **T**elecommunications **U**nion
ITU-T	**ITU – T**elecommunications
MAC	**M**edia **A**ccess **C**ontroller
MFP	**M**anu**f**acturing **P**lan
MII	**M**edia **I**ndependent **I**nterface,
MTBF	**M**ean **T**ime **B**etween **F**ailures
NSP	**N**etwork **S**ervice **P**rotocol
NVRAM	**N**on-**V**olatile **R**andom **A**ccess **M**emory
OTA	**O**ver **T**he **A**ir
PCB	**P**rinted **C**ircuit **B**oard
PoE	**P**ower **o**ver **E**thernet
PSU	**P**ower **S**upply **U**nit
QUG	**Q**uick **U**ser **G**uide
RF	**R**adio **F**requency
RFM	**R**adio **F**requency **M**odule
RX	**R**eceiver
SAW	**S**urface **A**coustic **W**ave (Filter)
SDB	**S**ensor **D**evelopment **B**oard
SDRAM	**S**ynchronous **D**ynamic **R**andom **A**ccess **M**emory
SPI	**S**ystem **P**acket /nterface
TBC	**T**o **B**e **C**onfirmed
TDK	**T**elran **D**evelopment **K**it
TX	**T**ransmitter
UMI	**U**niversal **M**etering **I**nterface
USART	**U**niversal **S**ynchronous **A**synchronous **R**eceiver **T**ransmitter
USB	**U**niversal **S**erial **B**us
UTS	**U**nit **T**est **S**pecification
WiFi	Brand name for IEEE 802.11b Direct Sequence

2 Design overview

2.1 Description

The Toumaz Bridge comprise of:

- Bridge PCB assembly, TZ202021,
- Two Bases station daughter boards, TZ202025.
- System firmware.
-

There will be two versions of the Toumaz Bridge operating at RF frequency bands of 868 and 915 MHz.

2.2 The top level Accessories

Power Over Ethernet, IEEE 802.3af compatible, Injector is required to supply power to the bridge and provide a connection to an Ethernet system. This device is not supplied by Toumaz UK Limited.

2.3 User Manual Requirements

One user manuals is required for the Toumaz Bridge, these are:

1. Toumaz Bridge User Guide: “Toumaz Bridge TZ2020-IFU_vx yy”, where x is a major version number and yy the minor version.

The purpose of the Toumaz Bridge User Guide is to give the User of the Bridge more in depth details of the operation and installation of the Toumaz Bridge.

3 Design Specification

3.1 Toumaz Bridge, TZ202021.

The Toumaz Bridge, TZ202021 hardware design comprises of the following files:

Schematic: TZ202021_SCH_ISSx_y.dsn
PCB Assembly: TZ202021_ASY_ISSx_y.zip
PCB layout: TZ202021_PCB_ISSx_y.brd

PCB Fabrication TZ202021_ODB_ISSx_y.tgz
TZ202021_PCB_ISSx_y.zip

where x_y are the major and minor version numbers.

3.1.1 Functional Specification.

The Bridge is designed to .

A block diagram of the Bridge is shown in Figure 1 and a physical layout of the PCB assembly in Figure 2. The functionality of the Bridge will be described in the following subsections of 3.1.1 and the external hardware connections in section 3.2.

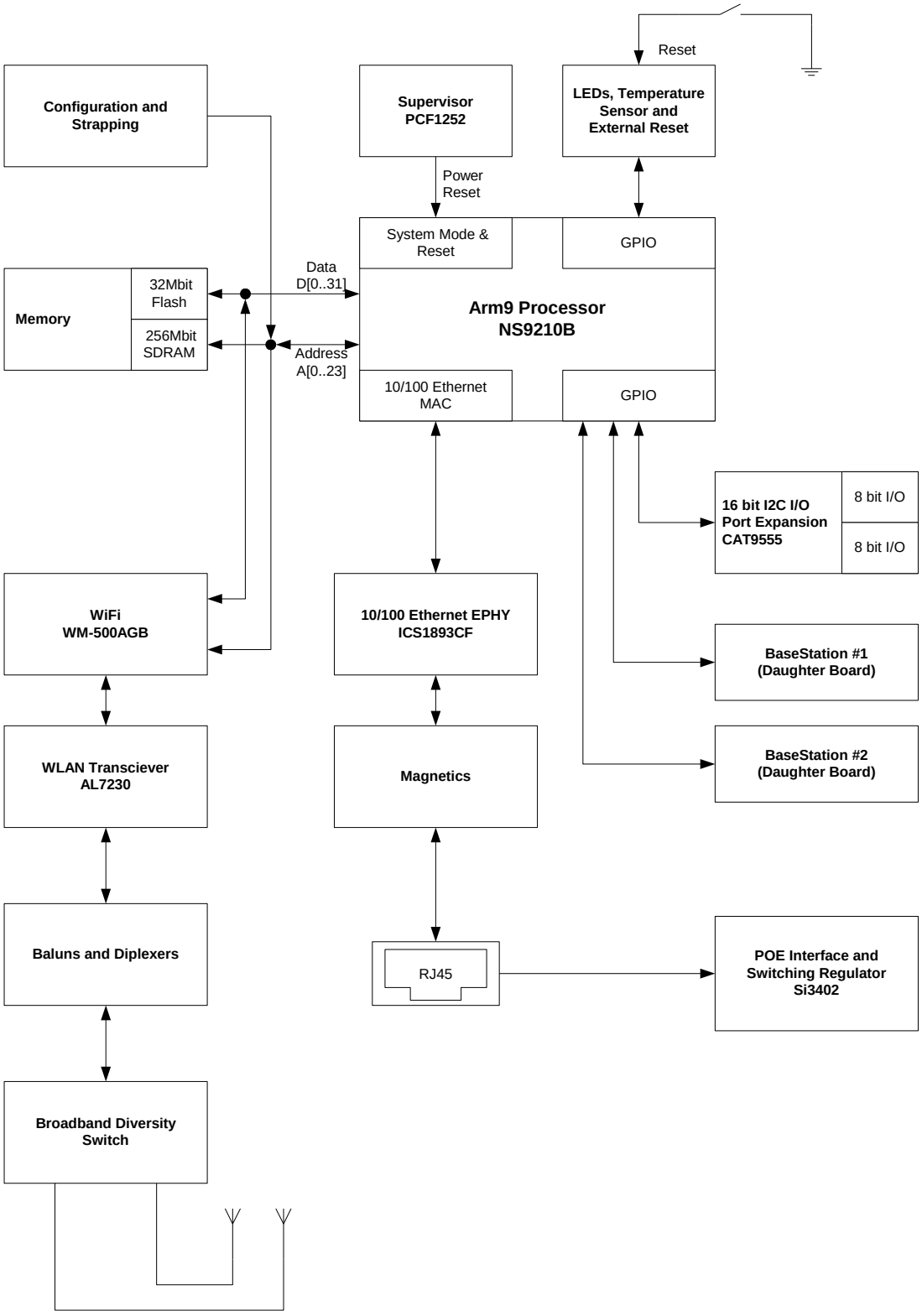

Figure 1. Toumaz Bridge Block Diagram

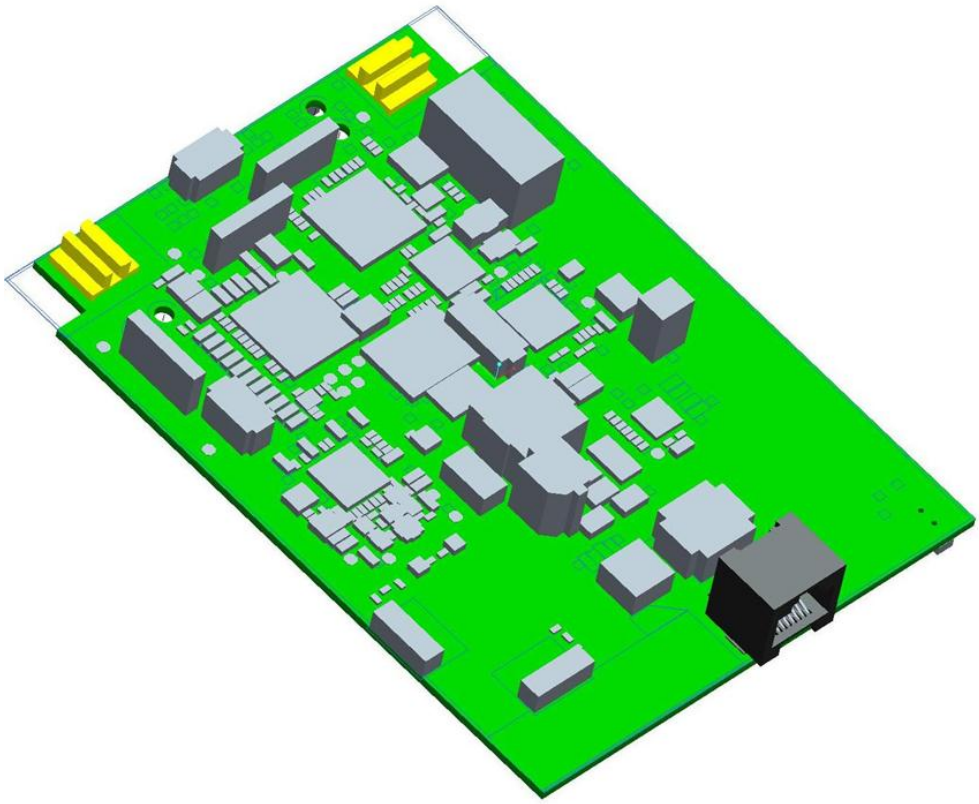

Figure 2. Bridge Physical View

3.1.1.1 Processor and Memory

The processor used in the Bridge is a NS9210 ARM9 177 BGA device located at U1.

Two memories devices are installed on the Bridge PCB, a 256 Mbit SDRAM, expandable to 512 M bits, and a 32Mbit Flash EEPROM, expandable to 64 M bits. All control signals for the memories are generated by the processor, U1, these include chip select, output enables and write enables.

3.1.1.2 Power Supply Functions.

Power enters the bridge via the Rj45 Ethernet connector and is regulated by U26, Si3402, to create a 3.3V power line, 3V3. This is filtered by L3 and L4 to form the Processor supply voltage, 3V3uP. This voltage is also used to supply directly I2C peripherals and indirectly other sections of the Bridge PCB.

U1, Processor Core Voltage of 1V8 is provided by regulator U20, from 3V3uP voltage.

WiFi subsystem, U6 WM500ABG takes its 3.3V power, 3V3_Piper from 3V3uP via L21. U6 also uses a 1V8_Piper voltage created by regulator U24, TLV70218, from the 3V3uP power.

The WiFi Transport Layer device, U9 Airoha AL7230, takes a 2.8V core supply from the 3V3uP via regulator U17, TPS79928, and a Power Amplifier Supply, 3V3_PA from 3V3uP via L19.

Both U6 and U9 use a 20MHz Oscillator that requires powering from a 2.8V source. The Bridge creates a 2V8_OSC from the 3V3uP signal using U19, TPS79928.

3.1.1.3 Power Supervision and Reset Function.

U37, PCF1252-7T provides a “Threshold detector and reset” for the Ethernet and Processor circuit based up the 3V3uP voltage. Reset and save times are set by C267 and are 1.1ms and 0.11ms respectively.

As 3V3uP rises past a VTRIP of3.05 V (typical), a negative reset pulse of 1.1ms is generated at RESET. VTRIP is a precise factory-programmed trip point.

The POWER_GOOD_3V3uP and OVERVOLTAGE_3V3uP signals are used to drive the green part of the POWER GOOD LEDs D7 and D10, depending upon which device is fitted, in accordance with the following table.

POWER_GOOD_3V3uP (U37 /POWF)	OVERVOLTAGE_3V3uP (U37 COMOUT)	LED D7/D10 (Green section)
Output Low – Power Failure or Not yet fully Powered	Output Low	OFF
Output Low – Power Failure or Not yet fully Powered	Output High – Over Voltage	OFF
Output High – Power established and Good	Output Low	ON – Normal Operating State
Output High – Power established and Good	Output High – Over Voltage	OFF

No other use is made of the POWER_GOOD_3V3uP and OVERVOLTAGE_3V3uP signals.

3.1.1.4 Configuration Resistors.

The Bridge Motherboard is configured via a number of resistors as described below.
Board Identification

CPU Address line	A17	A16	A15	A14	A13	A12	A11	A10	A9
Board \ Fit Resistor	R28	R29	R30	R31	R32	R33	R34	R35	R36
Dev. Board ISS 1.0	0	0	0	0	0	0	0	1	1
TZ202021 ISS 2.0	0	0	0	0	0	0	0	0	1
TZ202021 ISS 3.0	0	0	0	0	0	0	0	1	0
Bridge 2.0 Proto 1	1	1	1	1	1	1	1	1	0
Bridge 2.0 Proto	1	1	1	1	1	1	1	0	1

The highlighted line in the above table indicates the current release of Bridge Mother Board.

PLL Reference Clock
The PLL reference Clock is set by Resistors R19, R21 to R24. Only R19 is fitted giving a CPU clock of 64MHz.

PLL Output Divider
The PLL divider is set by resistors R25 and R26. Neither are fitted giving an OD = 0.

PLL Bypass
The PLL Bypass is not selected by not installing R27.

Boot from Flash
R20 is installed so that the Bridge Motherboard can be booted from flash.

System Mode
Resistors R2, R3 and R4 set the processor mode of operation. All of these resistors are installed to that the system mode is set to normal operation with ARM debug enabled.

3.1.1.5 I2C Functions.

Temperature Sensor, U25, LM73, I2C address 0x90 (Write) 0x91 (Read) functions to measure Bridge PCB temperature.

16 Bit I2C Port, U3 CAT9555YI, I2C address 0x40 (Write) 0x41 (Read) functions:

Bit No.	Function	Comment
0	UP RESET BS1 N	
1	UP RESET BS2 N	
2	SRVR OK	
3	SRVR BAD	
4	LINK OK	
5	LINK BAD	
6	BS1 GPIO3	
7	BS2 GPIO3	
8	BS1 BOARD DET	
9	BS1 BOARD DET	
10	BS OK	
11	BS BAD	
12	BS1 FREQ ID	
13	BS2 FREQ ID	
14	NC	
15	NC	

8 bit ADC, U16, ADC081c027, I2C address 0xA2 (Write) 0xa3 (Read). This device is used to measure the voltage level, TX_PWR set by the WiFi transceiver, U9 AL7320

3.1.1.6 Basestation SPI Functions and Serial Debug Port.

Base Stations 1 and 2 are controlled via separate SPI busses and are connected via J3 and J4 respectively. The SPI signals for base station 1 are configured by resistors R123, R124, R131 and R13. The SPI signals for base station 2 configured by resistors R125, R126, R133 and R134.

The Serial Debug port, J12 shares the serial receive signal with the Base station SPI data input signals BS1_SPI_MISO and BS2_SPI_MISO. Serial data input from J12 is only used during debug / manufacturing test mode of the Bridge

3.1.1.7 Ethernet Function.

The Ethernet functionality is provide by the processor U1 with the physical connection to the Ethernet provided by U21, ICS1893CKILF, transformer T1 and RJ45 connector, J14. The processor communicates all data and E-Phy commands to and from U21 via a Media Independent Interface, MII bus

3.1.1.8 WiFi Function and Transport Layer.

The WiFi Functionality of the Bridge is built around U6 the WM500ABG Piper Chip whilst the WiFi Transceiver of the Bridge is built around U9, the Airhoa AL7320 chip. A detailed block diagram for the WiFi Subsystem is shown in Figure 3.

The balanced transmitter outputs from the WiFi Transceiver, U9, pass through 2.4GHz and 5.4GHz Baluns (U7 and U12 respectively) before frequency domain multiplexing in diplexer, U8. The transmitted signal then passes

to a Diversity Switch, U10, and thence to one of two antenna circuits. The WiFi Controller Chip U6 selects which of the antennas to use for transmit and receive after passing through an antenna matching circuit. Included in each antenna matching circuit is a co-axial switch that can be used to measure the transmitted power of the WiFi system. The switch can also be used to attach an external antenna.

Transmission power is controlled by WiFi Transceiver, U9 and is measured during calibration by an 8 bit ADC, U16 , see section 3.1.1.5. The results are recorded to memory for use when altering the transmit power during normal operations.

The received WiFi signal enters via the antennas and the Diversity Switch, U10. The signals are frequency domain de-multiplexed in diplexer, U14 and pass to the WiFi Transceiver, U9 via signal matching circuits.

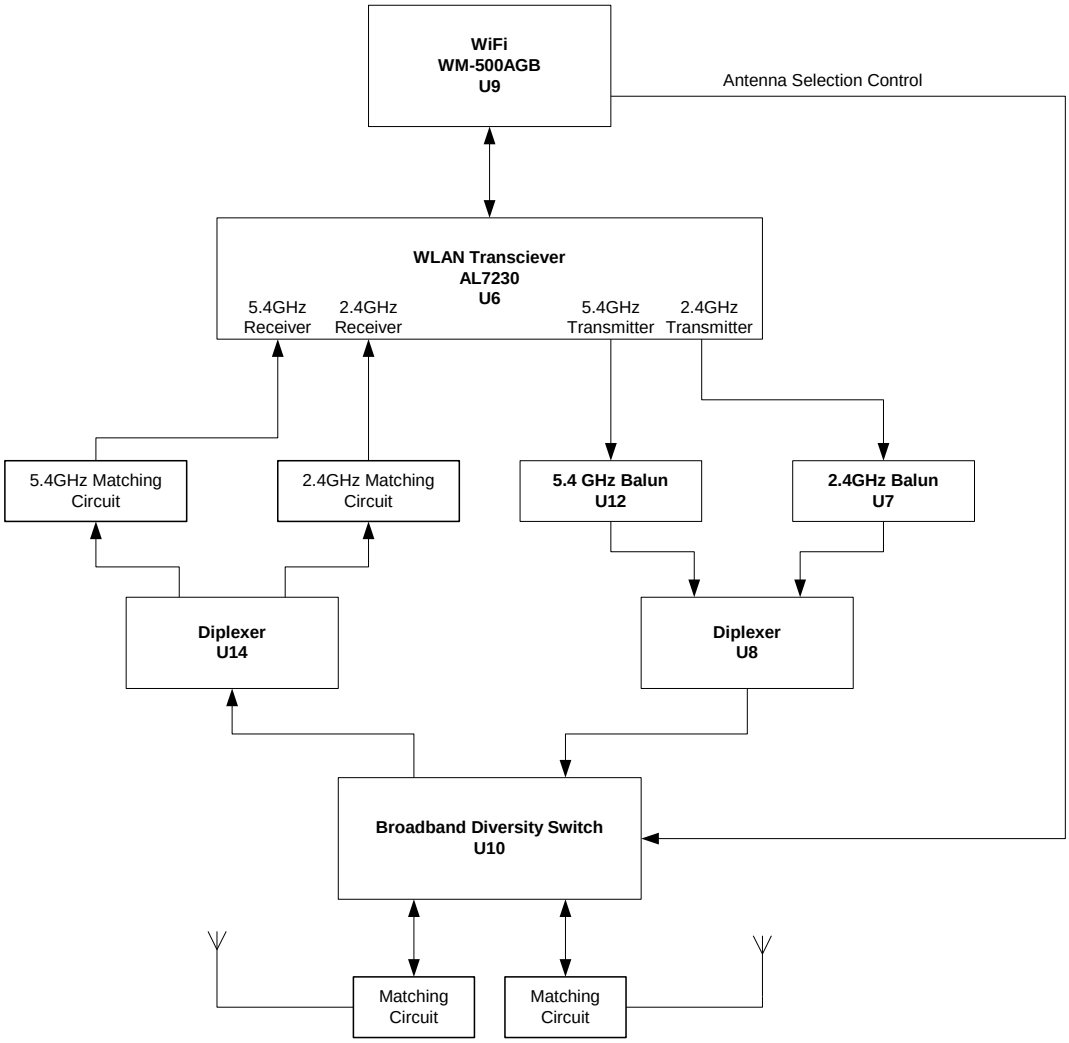

Figure 3. Detailed WiFi Subsystem Block Diagram.

3.2 External Hardware Connections

3.2.1.1 JP1 External Connector

Pin No.	Function
1	3V3uP
2	TDI
3	TRST_N
4	TCK
5	TMS
6	TDO
7	RTCK
8	SRST_N
9	Not Connected
10	GND

3.2.1.2 J3 Basestation #1 (Daughter Board) Connector

Pin No.	Function	Pin No.	Function
1	GND	2	GND
3	BS #1 Board Detect	4	BS #1 SPI MOSI
5	BS #1 Radio Debug TX	6	BS #1 SCS
7	BS #1 SPI MOSI	8	BS #1 GPIO0
9	BS#1 GPIO3	10	GND
11	BS#1 SPI CLK	12	BS #1 GPIO1
13	BS#1 Application Debug TX	14	RESET BS #1 N
15	BS #1 EECS	16	BS #1 FREQ ID
17	GND	18	3V3
19	CLK 32KHz Out	20	3V3
21	GND	22	GND

3.2.1.3 J4 Basestation #2 (Daughter Board) Connector

Pin No.	Function	Pin No.	Function
1	GND	2	GND
3	BS #2 Board Detect	4	BS #2 SPI MOSI
5	BS #2 Radio Debug TX	6	BS #2 SCS
7	BS #2 SPI MOSI	8	BS #2 GPIO0
9	BS#2 GPIO3	10	GND
11	BS#2 SPI CLK	12	BS #2 GPIO1
13	BS#2 Application Debug TX	14	RESET BS #2 N
15	BS #2 EECS	16	BS2 FREQ ID
17	GND	18	3V3
19	CLK 32KHz Out	20	3V3
21	GND	22	GND

3.2.1.4 J8 External Connector

Pin No.	Function
1	GND Test Point

3.2.1.5 J9 External Connector

Pin No.	Function
1	GND Test Point

3.2.1.6 J10 External Connector

Pin No.	Function
1	GND
2	Not Connected
3	Not Connected
4	Base Station #1 Radio Debug TX
5	Base Station #1 Application Debug TX
6	Not Connected

3.2.1.7 J11 External Connector

Pin No.	Function
1	GND
2	Not Connected
3	Not Connected
4	Base Station #2 Radio Debug TX
5	Base Station #2 Application Debug TX
6	Not Connected

3.2.1.8 J12 External Connector

Pin No.	Function
1	GND
2	Not Connected
3	Not Connected
4	Debug UART SPI RX
5	Debug UART TX
6	Not Connected

3.2.1.9 J13 External Power Connector

Pin No.	Function
1	3V3
2	GND

Not normally fitted.

3.2.1.10 J14 PoE RJ45 Ethernet Connector

Pin No.	Function
1	TX+
2	TX-
3	RX+
4	+V
5	+V
6	RX-
7	-V
8	-V

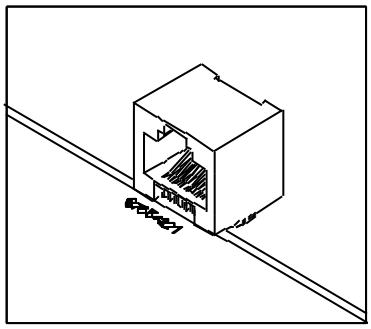

Figure 4. PoE Ethernet Connector View showing pin layout.

3.2.1.11 J15 Expansion RJ45 Connector

Pin No.	Function
1	Not Connected
2	Not Connected
3	Not Connected
4	Not Connected
5	Not Connected
6	Not Connected
7	Not Connected
8	Not Connected

J15 is not fitted to the PCB assembly.

3.2.2 'Wire' Test Points

The following table contains a list of through hole test points to which wires, or other items may be attached All of the signals shown in the following table are those attached to the test point. Where a signal name is not available the name of the nearest device pin is used together with the name of its function if on the schematic diagram.

Test Point	Signal	Installation State
TP1	RESET_N_uP	Not fitted
TP2	2V8_REG	Not fitted
TP3	3V3_PA	Not fitted
TP4	ACT_N	Not fitted
TP5	3V3Up	Not fitted
TP6	2V8_OSC	Not fitted
TP7	1V8_PIPER_REG	Not fitted
TP8	GND	Not fitted
TP9	ANT_SEL_N	Not fitted
TP10	ANT_SEL	Not fitted
TP11	TX_PWR	Not fitted
TP12	1V8	Not fitted
TP13	A1	Not fitted
TP14	A2	Not fitted
TP15	D16	Not fitted
TP16	D24	Not fitted
TP17	A10/AP	Not fitted
TP28	3V3 from J13	Not fitted
TP29	GND from J13	Not fitted
TP30	ETHERNET_RESET_N	Not fitted

3.2.3 Probe Test Points

The following table contains a list of surface mount PCB shape test points to which may be probed by oscilloscope, or other measuring devices. All of the Probe Test Points can be found on the bottom layer of the TZ202021 PCB assembly. All of the signals shown in the following table are those attached to the test point. Where a signal name is not available the name of the nearest device pin is used together with the name of its function if on the schematic diagram.

Test Point	Signal	Test Point	Signal	Test Point	Signal
N23	BS1_RADIO_DBG_TX	N132	U19.4 NR	N208	3V3uP
N24	BS2_RADIO_DBG_TX	N133	U17.4 NR	N209	VGA4
N46	BS2_EECS	N134	3V3_PA	N210	VGA3
N47	MII_CRS	N135	1V8_PIPER_REG	N211	VGA2
N49	U26.18 SWO	N140	BS_BAD	N212	VGA1
N67	SYS_MODE_2	N141	1V8uP	N213	VGA0

Test Point	Signal	Test Point	Signal	Test Point	Signal
N68	SYS_MODE_1	N142	BS_OK	N214	TX_ON
N69	SYS_MODE_0	N145	LINK_BAD	N215	RXHP
N70	I2C_SCL/GPIO_A0	N146	LINK_OK	N216	LNA1
N71	I2C_SDA	N147	SRVR_BAD	N217	LNA0
N72	PIPER_RESET_N	N148	SRVR_OK	N218	ANT_SEL_N
N73	BS2_GPIO3	N149	U38.4	N219	ANT_SEL
N74	UP_BS2_TXD	N150	POWER_GOOD_3V3uP	N220	PA2G_ON
N75	UP_BS2_RXD	N151	LINK_BAD (Top Mount)	N221	RX_ON
N76	UP_BS1_RXD	N152	LINK_OK (Top Mount)	N222	PA5G_ON
N77	INT_IOEXP	N153	SRVR_BAD (Top Mount)	N223	POWER_GOOD_3V3uP (Top Mount)
N78	BS2_SCS	N154	SRVR_OK (Top Mount)	N224	U9.41 RBIAS
N79	BS1_EECS	N155	U38.4	N225	U9.36 CP
N80	UP_BS1_TXD	N156	FACTORY_DEFAULTS_N (SW1.1 & SW1.4)	N226	2V8
N81	BS1_GPIO3	N157	BS1_SPI_CLK	N227	VCC_PLL
N82	BS1_SCS	N158	BS1_SPI_MOSI	N228	U9.21 VCCMOD
N83	PIPER_INT_N	N159	BS1_SPI_MISO	N229	U9.39 DECCAP
N84	DBG_UART_SPI_RXD	N160	BS1_GPIO0	N230	2V8_REG
N85	BS_SPI_CLK	N161	BS1_GPIO1	N231	2V8_OSC
N86	FACTORY_DEFAULTS_N	N162	RESET_BS1_N	N232	3V3_Piper
N87	BS_SPI_TXD	N163	BS_BAD	N233	1V8
N88	DBG_UART_TXD	N164	BS2_SPI_CLK	N234	U20.4 PG
N89	BS1_FREQ_ID	N165	BS2_SPI_MOSI	N235	U20.2 FC
N90	U37.3 COMIN	N166	B2S_SPI_MISO	N236	MII_RXD0
N91	U37.1 CT	N167	U38.4 (Top Mount)	N237	MII_RXD1
N92	OVERVOLTAGE_3V3uP	N168	BS2_GPIO0	N238	MII_RXD2
N93	POWER_GOOD_3V3uP	N169	BS2_GPIO1	N239	MII_RXD3
N94	U37.6 RESET	N170	RESET_BS2_N	N240	MII_TXD0
N95	ETHERNET_RESET_N	N171	BS1_APP_DBG_TX	N241	MII_TXD1
N96	RESET_N_uP	N172	BS2_APP_DBG_TX	N242	MII_TXD2
N97	UP_RESET_BS1_N	N173	CLK_32KHZ_OUT	N243	MII_TXD3
N98	UP_RESET_BS2_N	N174	CT1	N244	MII_RXER
N99	LINK_OK	N175	CT2	N245	MII_RXDV
N100	X2_SYS_OSC	N176	SP1	N246	MII_RXCLK
N101	BS1_BOARD_DET	N177	SP2	N247	MII_TXCKL
N102	BS2_BOARD_DET	N178	U26.8 RCL	N248	ETH_ACT_N
N103	RTCK	N179	U26.9 & U26.21 VNEG	N249	U21.51 P1CL
N104	TCK	N180	U26.15 VSSA	N250	ETH_LINK_N

Test Point	Signal	Test Point	Signal	Test Point	Signal
N105	TRST_N	N181	U26.17 & U26.19 VSS	N251	U21.54 P3TD
N106	TMS	N182	POE_IN	N252	U21.56 P4RD
N107	TDO	N183	3V3 from J13 after R201	N253	U21.12 19TCSR
N108	TDI	N184	GND from J13 after R202	N254	U21.13 100TCSR
N109	BS2_FREQ_ID	N185	L31 FB1 Junction	N255	U21.2 AMDIX_EN
N110	SRVR_OK	N186	U26.3 VDD	N256	U21 VDD
N111	SRVR_BAD	N187	U26.1 EROUT	N258	SP2
N112	LINK_BAD	N188	C270, R195 & C269 junction	N259	SP1
N113	BS_OK	N189	U26.2 SSFT	N260	CT1 (RC network)
N114	NS_TA_STRB	N190	MII_COL	N261	CT2 (RC network)
N115	Flash reset / Temporary Unprotect	N191	SP_GPIO	N262	U26.4 ISOSSFT
N116	PIPER_SPI_CLK	N192	MII_TXEN	N263	SRST_N
N117	PIPER_SPI_DATA	N193	MII_TXD3	N266	TX_PWR
N118	PIPER_SPI_EN_N	N194	MII_TXD2	N267	TP_AP
N119	PIPER_20MHZ	N195	MII_TXD1	N268	TP_AN
N120	ADC10_33_VDD	N196	MII_TXD0	N269	TP_BP
N121	ADC10_VDD_33	N197	MII_TXCKL	N270	TP_BN
N122	ADC10_18_VDD	N198	MII_RXER	N271	TXP
N123	DAC10_33_VDD	N199	MII_RXDV	N272	TXN
N124	DAC10_18_VDD	N200	MII_RXD3	N273	RXP
N125	ADC8_VDD	N201	MII_RXD2	N275	RXN
N126	PLL_VDD	N202	MII_RXD1	N276	SW1.3 and SW1.2
N127	VCMDA	N203	MII_RXD0	N277	3V3 from J13
N128	VBGDA	N204	MII_RXCLK	N278	GND from J13
N129	VCMAD	N205	MII_MDC	N279	VIN8
N130	VBGAD	N206	MII_MDIO	N300	TP_AP TP_AN centre point
N131	U9.51 GC6	N207	U1.L15 SYS_PLL_DVDD	N301	TP_BP TP_BN centre point

3.2.4 Operating Environment

Temperature: +0°C to +70°C

3.2.5 Switches and User Interface

Switch, SW1, is included in the design to reset the Toumaz Bridge back to 'Factory Default Settings'.

Switches SW2 and SW3, are present to enable WiFi calibration by attaching an SMA conversion adapter. These switches may also be used to fit an external antenna to the Bridge and isolate its own antennas.

No other user interfaces are provided.

3.2.6 Visual Indicators

The following LEDs are used to indicate the state of the Bridge:

- D3, bi-colour Base Station Status LED (Not normally fitted),
- D5, bi-colour Link Status LED (Not normally fitted),
- D8, bi-colour Link Status LED (Top Mount),
- D6, bi-colour Server Status LED (Not normally fitted),
- D9, bi-colour Server Status LED (Top Mount),
- D7, bi-colour Power Good and Server OK LED (Not normally fitted),
- D10, bi-colour Power Good and Server OK LED (Top Mount).

3.2.7 Power Management

Power for the Bridge is taken from the 'Power Over Ethernet' connector J24, see section 3.2.1.10 for pinout.

A regulator is to be used to down convert the 3V3 from the FTDI FT223RQ USB interface chip to 1.2V to supply the TZ1053 RF chip.

3.2.8 Operating Environment

Temperature: +0°C to +70°C

3.2.9 Hardware Enclosure

A purpose designed, wall mountable, enclosure has been design for the Toumaz Bridge PCB assemblies. Details of this enclosure are in document ……..

3.2.10 Size and Weight

The overall size of the Bridge PCB is: 61.47 x 18.67 mm

Weight of Bridge Mother Board PCB assembly is approximately: 61.25 ±0.35 gms.

Weight of Bridge Daughter board PCB assembly is approximately: 3.6 ± 0.1 gms

Combine Weight of Bridge Mother Board and Bridge Daughter board PCB assemblies without the enclosure assembly is approximately: 68.4 ± 0.5 gms

Weight of Bridge enclosure approximately: 160.3 ±0.1 gms.

3.2.11 Enclosure Markings

- PCB will have:
  - Lead Free Marker.
  - UL marking for PCB material e.g. UL 94V-0.
  - TZ202021 plus issue level.
  - An identifier for each layer making up the PCB.
- Enclosure assembly will have:
  - A Unique Serial Number.
  - The Telran Chip ID.
  - CE marking on European/ 868 MHz devices.
  - FCC marking on the 915 MHz version.

3.3 Test and Verification

Manufacturing and design verification testing are described in document: “TZ202021-UTS-ISS 1.0 Test Procedure, Issue 1.00, ?-?-2012”.

3.4 Bridge Storage and Packaging

The Toumaz Bridge and accessories will be enclosed in a rigid container that can be used for storage and shipping.

The Packaging to be marked with:

- Contents Product Label,
- Frequency of Use,
- A barcode to identify the Toumaz Bridge,
- Vendor specific labels.

3.5 Toumaz Bridge Equipment Hazards

3.5.1 Personal Hazards

No personal hazards nave been identified.

3.5.2 Equipment Hazards

Static sensitive components are used on the components of the Toumaz Bridge PCBAs and therefore handling of this unit shall be in accordance with ESD Handling Procedures.

ESD Symbol

An FMEA (Failure Mode and Effects Analysis) should be carried out to determine the effects of failures of the modules within the Toumaz Bridge and subsequent consequences.

3.6 Device Lifetime and Shelf Life

3.7 Manufacturability

The components of the Toumaz Bridge have been designed for manufacture. The design uses multi-sourced components where practicable to ensure that shortages etc. do not have an impact on manufacture.

3.8 Reliability

To ensure that the RFM in particular is reliable over time an MTBF figure should be calculated according to MIL-HDBK-217F or similar standards. Note the operating conditions of the Toumaz Bridge will be ‘Ground, Benign’.

4 Regulatory compliance standards

4.1 Mandatory

FCC Part 15 C

4.2 Design Aims