TZ202025/6-HDD

Bridge ISM Base Station PCBA Hardware Description Document

Version **1.00**

Date **29-June-2012**

The following people have read, understood and agreed to the information contained within the above document.

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Document History

The following table summarizes all changes to this report. Details of document change authorization can be obtained on request from the Toumaz document control system.

Issue	Description of Revision	Author	Date
1.0	DRAFT	Chris Nunn	29 June 12

This document is based on template TQ-RND-F27 Iss 1.11 19th April 2011

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1 Scope

This document describes the overall system design for the TZ202025 (US) & TZ202026 (EU) PCBAs showing how the design will meet the design requirements.

1.1 Reference Documents

[1]

[2]

[3]

1.2 Abbreviations

ADC	Analogue to Digital Convertor
AFC	Automatic Frequency Control
EEPROM	Electrically Erasable Programmable Read Only Memory
FSK	Frequency Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial Scientific Medical (RF bands)
LBT	Listen Before Talk
LDO	Low Drop Out (Regulator)
LO	Local Oscillator
LNA	Low Noise Amplifier
MAC	Media Access Control
MDD	Medical Device Directive
N/A	Not Applicable
PA	Power Amplifier
PCB	(Bare) Printed Circuit Board
PCBA	Printed Circuit Board Assembly
R&D	Research & Development
RF	Radio Frequency
RTTE	Radio and Telephone Terminal Equipment Directive.
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
TDMA	Time Division Multiple Access
UHF	Ultra High Frequency (300 MHz → 3 GHz)

VCO	Voltage Controlled Oscillator
VXO	Voltage (Controlled) Crystal Oscillator
WLAN	Wireless Local Area Network

2 Overview

2.1 Operating Frequency

There are 2 Base Station versions, one for the US and a second for the EU.

There part numbers and operating frequencies are listed in Table 1.

Table 1 Base Station Versions

	US Version	EU Version
Bridge Model Number	TZ202020	TZ202021
Base Station PCBA Number	TZ202025	TZ202025
Operating Frequency	903 to 928 MHz	863 to 870 MHz

2.2 System

The TZ202025/6 forms part of the TZ202020/21 Bridge. This, in turn, forms part of a hospital patient monitoring system.

The Bridge receives patient Vital Signs data (heart rate, respiration rate and body temperature) from a patient worn device (the digital patch) via a radio using a UHF ISM band, Table 1, and passes them onto the hospital infra-structure via either Ethernet or WLAN - Figure 1.

The Bridge is powered using PoE from either the hospital IT system or via a customer supplied PoE injector.

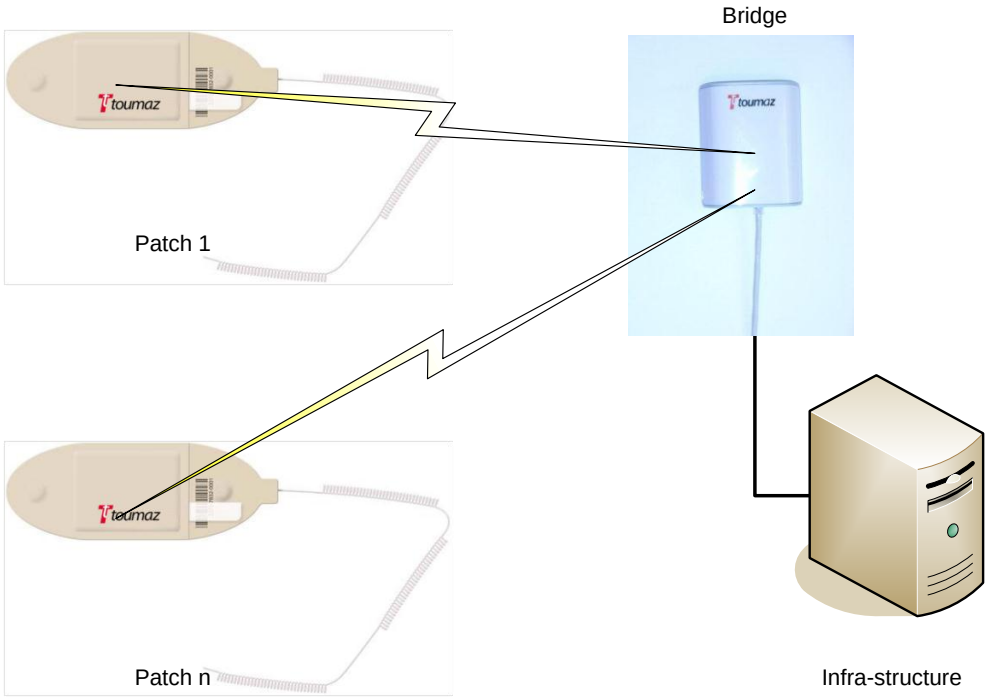

Figure 1 Bridge within Patient Monitoring System

The Bridge consists of a motherboard and 2 daughter boards within a plastic enclosure.

Each daughter board is a UHF ISM radio transceiver with an integral antenna. Under control of the mother board processor this receives the vital signs data from the digital patches and passes the information onto the motherboard.

The motherboard has the main microprocessor system, Ethernet, WLAN and PoE supply circuits.

3 Functional Description

3.1 System

The system consists of 3 main functional blocks, power supply, digital and RF. The analogue front end of the TZ1031 is not utilized on the Base Station. The block diagram is shown in Figure 2 and the schematic diagram in § 6.

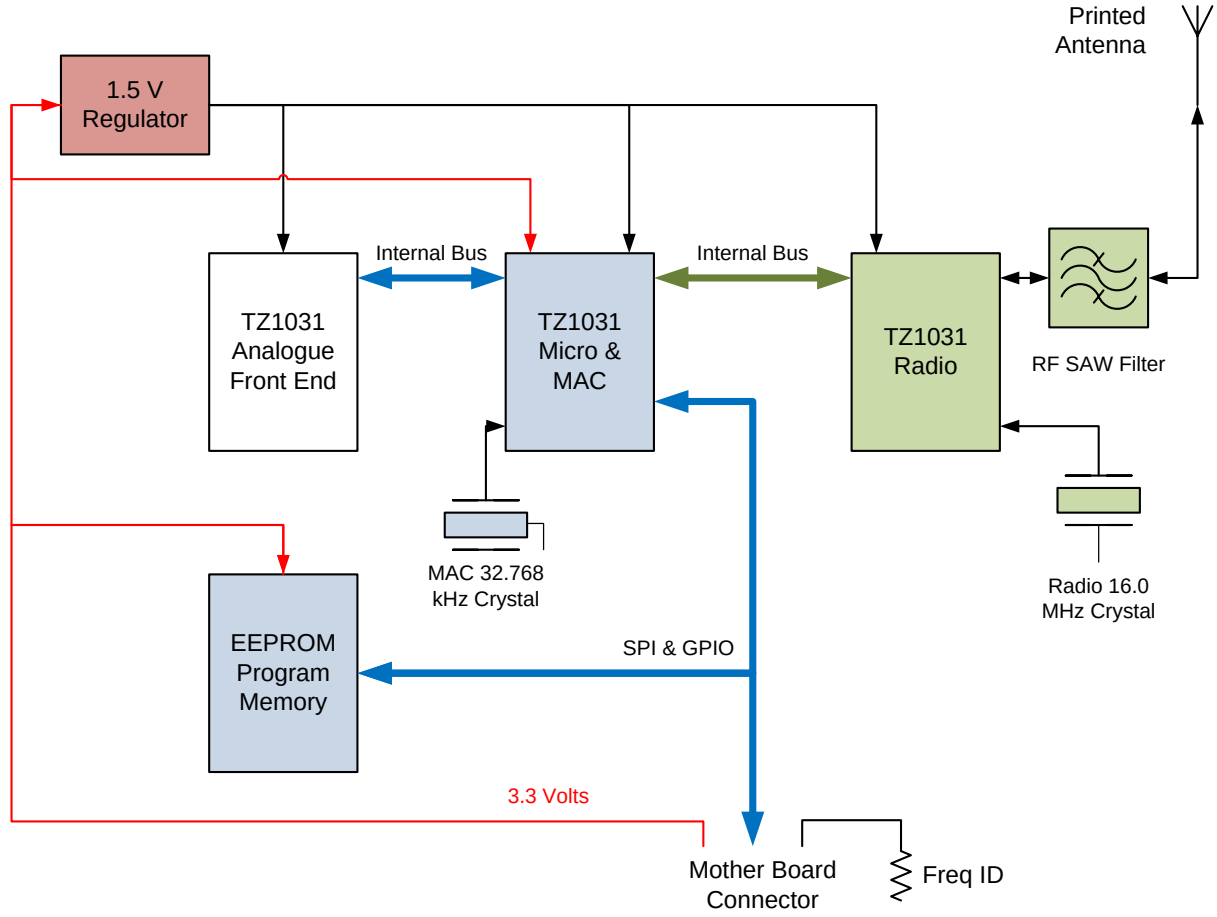

Figure 2 TZ202025/6 System Block Diagram

3.2 Power

The power for the TZ202025/6 is supplied on pins 18 & 20 of the Mother Board Connector, J5. This directly supplies the EEPROM, TZ1031 GPIOs and Voltage Regulator. A 1.5 V fixed regulator, U1, supplies the main TZ1031 digital and RF sub-systems.

Bulk decoupling is provided on both the input and output of the regulator. Further decoupling is provided at each IC within the digital and RF sub-systems.

3.3 Digital

The digital system has 2 main elements, the TZ1031 IC's 8051 µController, U1, and a 25AA256 EEPROM, U4.

These and the motherboard connector are linked by a control and data signal running at a nominal 3.3 V. The signals comprise of an SPI bus, serial buses, reset and frequency ID signals.

The 8051's code is contained in the EEPROM and is read after a hard reset. The reset is controlled by the main processor on the mother board. The SPI bus is used between the EEPROM & 8051 and is also connected to the mother board processor. This allows the EEPROM to be updated by the mother board and also by during manufacture via the test points on the PCB. The µC uses the 16 MHz clock from the RF sub-system.

The main communications link between the base station and the motherboard processor is via a bi-direction serial link, with another serial link allowing base station debug data to be captured, although this is only used during R&D.

A resistor is fitted to the US version of the PCB to identify the frequency band.

3.4 RF Transceiver

3.4.1 Overview

The radio transceiver contained within the TZ1031, consists of a transmitter, receiver and common frequency synthesiser. There are external impedance matching circuits and SAW filter, Figure 3. The radio is controlled by a MAC system.

The radio operates in a TDMA system using the same uplink and downlink frequency. The base station communicates with up to 8 digital patches over a 16 second schedule, allowing up to 2 seconds for each digital patch. It operates on a single frequency channel within the operating band. This channel is chosen on as the quietest available during switch on or when interference occurs.

The radio uses LBT to ensure that it does not interfere with other base stations or devices using the same frequency channel as itself.

The MAC is hardware encoded within the TZ1031 and is controlled by the 8051. The MAC timing during RF communications is derived from a low power 16.0 MHz crystal oscillator (Y2) while the timing between RF bursts is from a 32.768 kHz crystal oscillator (Y1).

The transceiver system consists of a separate super-heterodyne transmit and receive chains with a common Local Oscillator system. The channel spacing is 200 kHz.

The transceiver uses FSK modulation with a deviation of ± 50 kHz and data rate of 50 kbits/s. The data is subject to Forward Error Correction (Hamming) and is whitened. This occurs in hardware to minimise power consumption. If the data is not received and acknowledged it is re-sent.

3.4.2 Transmitter

Figure 3 shows the major parts of the transceiver system.

The transmit section of the Sensium transceiver comprises I Q modulation from baseband up to an IF of approximately 100 MHz followed by a final up conversion by 800 MHz to a final transmit frequency of around 900 MHz at a maximum level of around –6 dBm conducted. The output impedance of the PA is matched to 50 Ω by 2 external inductors (L3 & 4). An internal TX / RX switch connects the PA external SAW filter (U5) which in turn is connected to a ceramic chip antenna (ANT1).

The 3rd harmonic of the 1st IF is not in the RF band. The lower sideband of final up-conversion is around 700 MHz and is filtered by the PA tuning and external RF SAW.

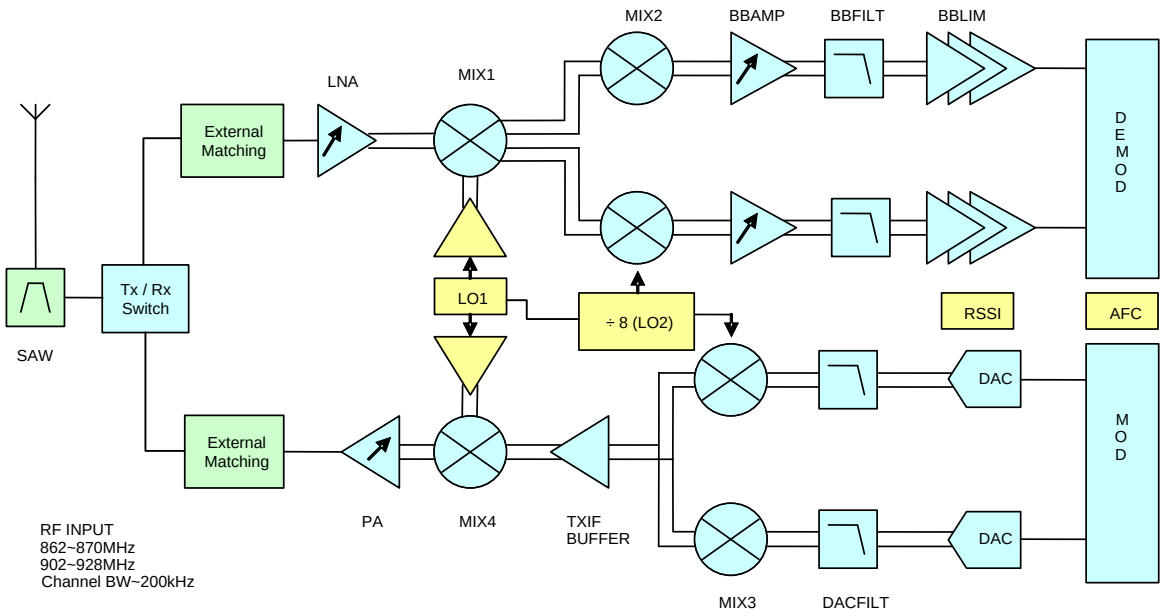

Figure 3 Transceiver Block Diagram

3.4.3 Receiver

Following the SAW filter and TX / RX switch, external components (L5 & C15) match the LNA to 50 Ω. The receiver mixes the wanted signal down to a sliding IF frequency at approximately 100 MHz followed by conversion to I & Q baseband. The image frequency is approximately 200 MHz away from the wanted and is filtered using the RF SAW.

The receiver locks it's LO to the received signal using an AFC loop to keep the receiver on the same frequency as the transmitter. This is not a phase locked system and uses the 1010 preamble at the start of the TX burst to acquire the correct frequency. The loop maintains phase synchronization over the whole received RF packet burst.

3.4.4 Synthesiser

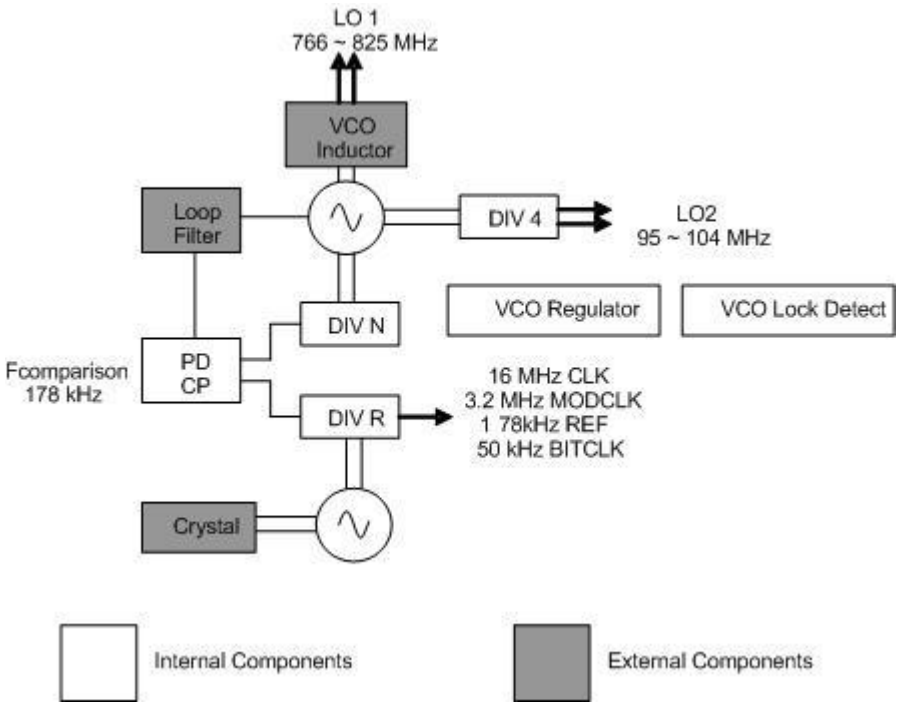

Figure 4 VCO Block Diagram

The on-chip VCO is uses internal balanced inductors which resonate with a variable internal capacitance. The VCO charge-pump output is fed via 2nd order low-pass loop to the variable capacitor. With the exception of C31, the filtering is internal. The VCO loop bandwidth is approximately 10 kHz. The block diagram is shown in Figure 4.

3.4.5 Voltage Controlled Crystal Oscillator (VXO)

A crystal provides the 16.000 MHz reference for the frequency synthesiser system. In receive the crystal oscillator is tuned by the AFC loop to match the bridge transmitter's frequency.

4 Regulatory compliance standards

Both EU & US versions are part of product that is required to meet certain regulatory conditions. Generally the product is tested as part of an overall system and is not evaluated independently.

4.1 EU

The EU system must comply with both the RTTE & MDD directives.

4.1.1 RF

The EU version of the product is designed to meet EN 300 220.

4.1.2 Safety

Both versions of the product are designed to comply with IEC 60950.

4.1.3 EMC

The EU version of the product is designed to comply with both IEC 60601-1-2 and EN 301 489-3.

4.2 US

4.2.1 RF

The US version of the product is designed to comply with the relevant sections of 47 CFR Ch. I Part 15.

4.2.2 Safety

Both versions of the product are designed to comply with IEC 60950.

4.2.3 EMC

The product is designed to comply with IEC 60601-1-2.

5 Mother Board Connector (J5) Signals

Pin No.	Function	Direction
1	GND	-
2	GND	-
3	Board Detect	Output
4	SPI MOSI	Output
5	GPIO<2>	Bi-Directional
6	SCS	Input
7	SPI MISO	Input
8	GPIO<0> (UART)	Output
9	GPIO<3> (EEPROM CS)	Bi-Directional
10	GND	-
11	SPI CLK	Bi-Directional
12	GPIO<1> (UART)	Input
13	GPIO<4>	Bi-Directional
14	RESET N	Input
15	EECS	Input
16	FREQ ID	Output
17	GND	-
18	3V3	-
19	CLK 32KHz Out	Output
21	GND	-
20	3V3	-