Operation Description based on Block diagram

Intel Pro/Wireless 2100 MiniPCI is integrated into our laptop PC as 802.11b adapter.
The single-band 2.4GHz Intel Pro/Wireless 2100 MiniPCI Adapter is a single PCB design using Intel's 82531ME (named as ARDON in the block diagram and schematics) and proprietary 802.11b CCK baseband processor (named as DELAWARE) and Phillips SA2400 radio chipsets.
In addition to these chips, the RF front-end consists of additional components such as antenna connectors, diversity switch, bandpass filters, baluns, transmit / receive switch, power amplifier (PA), and low-noise amplifier (LNA).

[Component Description]

1)82531ME (ARDON)

The 82531ME chip incorporates media access control (MAC) logic and a MiniPCI host interface.
It communicates with the Baseband processor through a special parallel interface called the Host-Bus (H-BUS) interface.

2)802.11b CCK baseband processor

This is the external Complementary Code Keying (CCK) baseband processor and incorporates the low level MAC tasks for 802.11b. It contains integrated analog functions such as transmit Inphase/Quadrature Phase (I/Q) digital-to-analog converters (DACs), receive I/Q analog-to-digital converters (ADCs), DACs for Automatic Gain Control (AGC) and clock adjustments, ADC for RX and TX AGC, and on chip clock power down control circuitry. The DSP is designed to serve as the Physical Layer Entity for CCK.

3)SA2400 Radio

The SA2400 from Phillips is a fully integrated single IC RF transceiver designed for 2.4GHz.
It is a direct conversion radio architecture and combines a low-noise automatic gain control, receive and transmit filters, and input/output buffers into a single IC.

[Mode Description]

1)Transmit Mode

The SA2400 generates a differential RF signal at the desired operating frequency.Since this is zero-IF type design, it beats the I/Q modulation directry up to the appropriate frequency of operation set by its built-in PLL. Upon exiting from the SA2400, this differential signal is transformed to single ended form using a dicrete balun circuit (not shown in the diagarm).From the output of the balun, the signal is band pass filtered with a ceramic 2400 to 2500MHz Band Pass filter (BPF).
The filtered signal is then attenuated using a 6dB, 50ohm resistive pi-attenuator network. A MAX2242 chip scale RF Power amplifier (PA) IC is used to amplify the low level filtered composite signal to approximately +20dB levels.
At the output of the PA, a ceramic 2400 to 2500MHz Low Pass Filter (LPF) is used to reduce harmonic content in the amplified signal.
From this point the signal is routed through the single band antenna diversity switch to one of the two U.FL antenna connectors. A discrete logic IC (not shown in the diagram) is used to decode antenna switching information from the CCK baseband processor IC in order to correctly operate the antenna switch.
An RF signal level of approx. –5dBm at the output of the SA2400 IC can be expected to produce an amplified RF signal of approximately +16dBm at the antenna connectors.

2)Receive Mode

During receive, the signal is first routed through a ceramic 2400 to 2500MHz band pass filter (BPF) and through a single transistor, Low Noise Amplifier (LNA). The amplified and filtered signal is then attenuated via a 6dB, 50ohm receive pi-attenuator network. A 50ohm to 100ohm integrated balun is then used to convert the single ended signal to a differential voltage which can be applied to the receive terminals on the SA2400 IC.

The LNA and attenuator form an isolation network which is required to isolate the low level Voltage Controlled Oscillator (VCO) frequency leakage from the antennas. An isolation network helps to reduce DC offsets that occur when switching antennas in diversity applications.

Inside the SA2400, the received signal is first amplified with an AGC amplifier and then mixed down in frequency (from RF to DC) using a quadrature I/Q up/down mixer. From here the down-converted signal is then low-pass filtered using Chebychev 5^{th} order active filters. A DC cancellation mechanism is able to reduce DC offsets by 70dB hence clipping of the baseband signals can be avoided.

The baseband I/Q signals are transmitted differentially via current signals which are converted to voltage by the external resistor networks. These differential analog I/Q voltage levels are read by the 6 bit ADCs inside of the CCK baseband processor.

The CCK baseband processor is used to demodulate the I/Q signals to produce packets of data which are communicated to the 82531ME upper MAC and onwards to the host system via the MiniPCI bus.