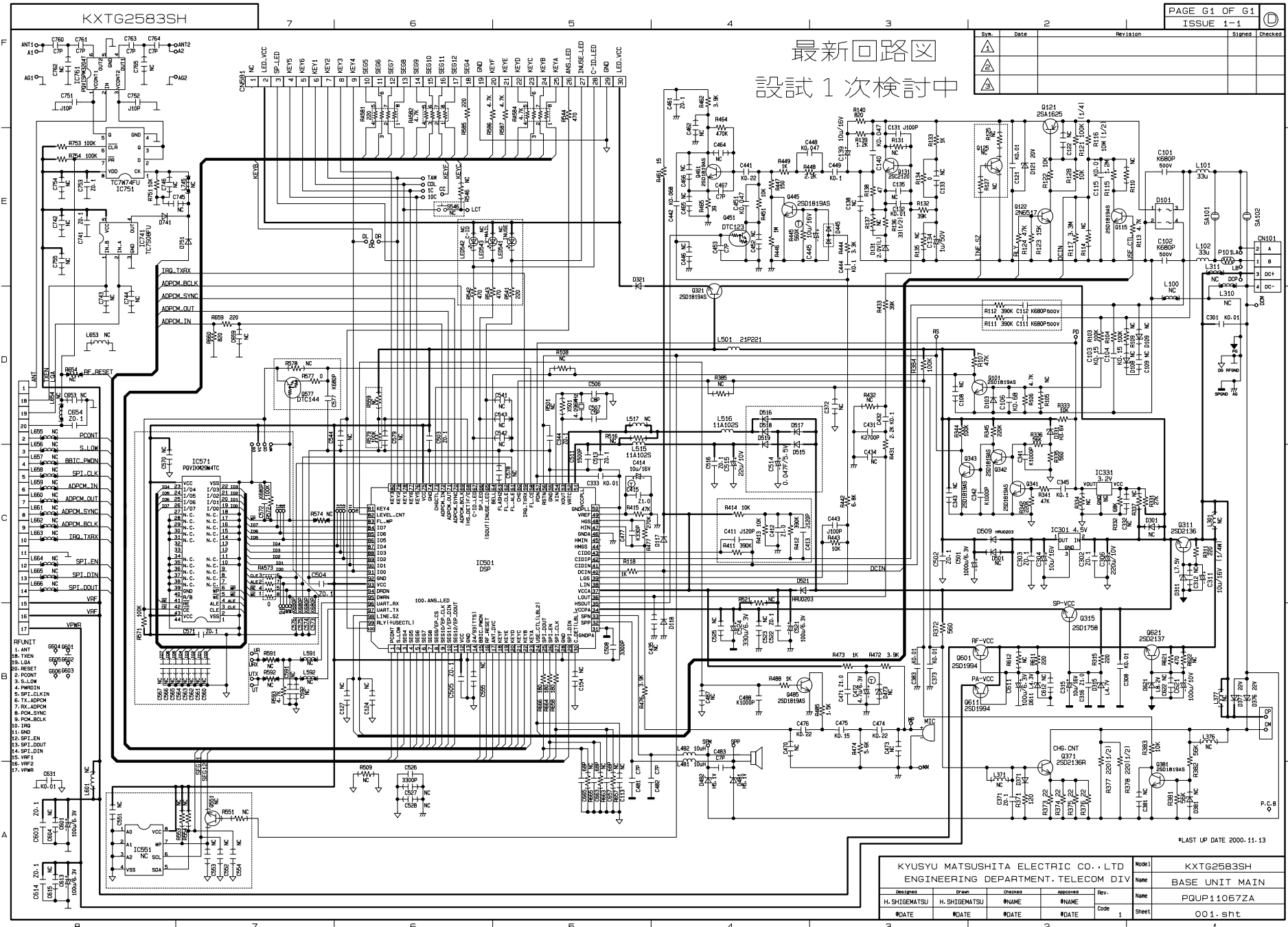


最新回路図
設計 1 次検討中

Syn.	Date	Revision	Signed	Checked



- FFUNIT
- 1. ANT
 - 2. TXEN
 - 3. LOA
 - 4. RESET
 - 5. POINT
 - 6. S.LOW
 - 7. P.WIN
 - 8. TX.ABDM
 - 9. PCK.SYNC
 - 10. TRD
 - 11. END
 - 12. SP1.EN
 - 13. SP1.DOUT
 - 14. SP1.DIN
 - 15. VRF1
 - 16. VRF2
 - 17. VPHR

*LAST UP DATE 2000.11.13

KYUSUY MATSUSHITA ELECTRIC CO., LTD		Model	KXTG2583SH
ENGINEERING DEPARTMENT, TELECOM DIV		Name	BASE UNIT MAIN
Design	Draw	Checked	Approved
H. SHIGEMATSU	H. SHIGEMATSU	NAME	NAME
DATE	DATE	DATE	DATE
1	2	3	4
Sheet	1	2	3
001.sht			