

To: Angela Tang

Inc Blandine - DT 4/9

HL 17 pages

for R5128 & HP-88.

# 900MHz ISM BAND RF MODULE FOR CORDLESS TELEPHONE

MODEL NAME : SBM-3020A-HIW  
SBM-3020A-BIW

| PREPARED<br>BY | CHECKED BY | APPROVED BY |
|----------------|------------|-------------|
|                |            |             |

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|                |           |
|----------------|-----------|
| ETL SEMKO ③    |           |
| Incoming Date: | 19/4/01   |
|                | Action By |
|                | 1.5       |

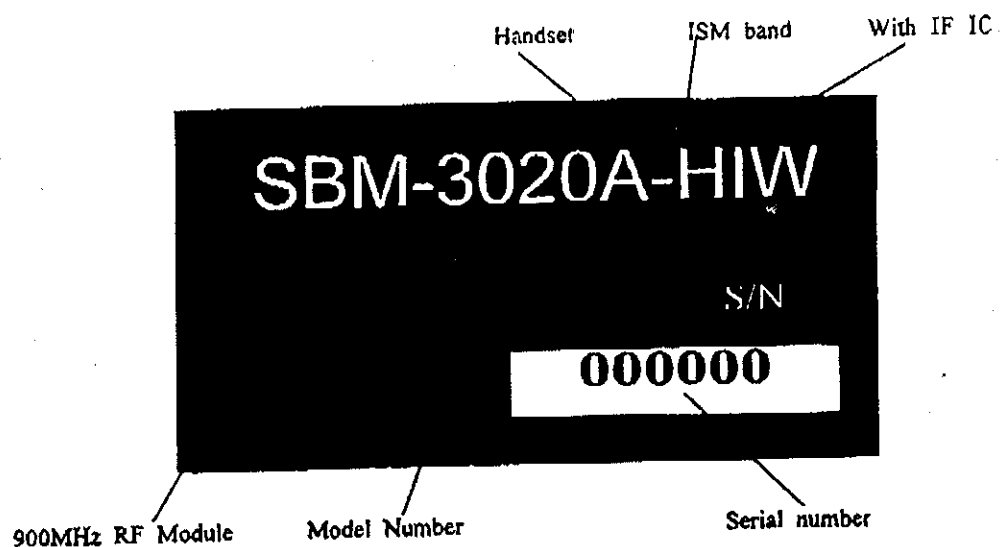
# 1. General description

## 1.1 Feature

This RF Module ( SBM-3020A ) shall be applied to cordless telephone for 900MHz USA ISM Band

## 1.2 PRODUCT LABEL

- (1) COLOR : BLACK
- (2) CONTENTS : See the following table



Rev. 1.1 : Details mechanical pin position drawing is added.

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## 1.4 SPECIFICATION.

| General Specifications |                                   |                                                                                                       |
|------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------|
|                        | Items                             | Specifications                                                                                        |
| 1                      | Maximum TX Frequency range        | Base : 902.80 ~ 904.750 MHz<br>Handset : 925.30 ~ 927.250 MHz                                         |
| 2                      | Maximum Tx VCO Frequency range    | Base : 451.40 ~ 452.375 MHz<br>Handset : 462.65 ~ 463.625 MHz                                         |
| 3                      | Maximum RX Frequency range        | Base : 925.30 ~ 927.25 MHz<br>Handset : 902.80 ~ 904.75 MHz                                           |
| 4                      | Maximum RX VCO Frequency range    | Base : 936.00 ~ 937.95 MHz ( Upper Heterodyne )<br>Handset : 892.10 ~ 894.05 MHz ( Lower Heterodyne ) |
| 5                      | Channel Number<br>Channel Spacing | 40 CH Full Duplex ( Recommended )<br>50 KHz ( Recommended )                                           |
| 6                      | IF frequencies                    | 10.7 MHz for 1 <sup>st</sup> IF<br>450KHz for 2 <sup>nd</sup> IF                                      |
| 7                      | Modulation                        | FM                                                                                                    |
| 8                      | Standard Test Modulation signal   | Modulated audio Frequency : 1KHz<br>Standard modulation : +/-8KHz ( Recommended )                     |
| 9                      | TX Frequency stability            | Max. +/-3ppm ( 0°C to +50°C )                                                                         |
| 10                     | Nominal test temperature Range    | Each : 25°C +/- 5°C                                                                                   |
|                        | Extreme temperature Range         | Base : 0°C to +50°C<br>Handset : 0°C to +50°C                                                         |
| 11                     | Antenna Impedance                 | 50 ohm +/- 25 ohm                                                                                     |
| 12                     | Power Supply Current              | TX and RX : TBD<br>RX : TBD                                                                           |
| 13                     | Test Power Supply Voltage         | Base : 4.8Vdc. +/-0.1Vdc<br>Handset : 3.6VdC +/-0.1Vdc                                                |
|                        | Extreme Supply Voltage Range      | Base : 4.7 to 5.3Vdc<br>Handset : 3.2 to 4.3Vdc                                                       |

Note : All items are specified on SBM3020GA ( Test fixture ).

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## TX Specifications

Test Condition : Room Temperature (  $25 \pm 3^\circ\text{C}$  ) / Nominal Power Supply Voltage/CCITT Filter OFF

|   | Items                    | Specifications         | Condition                               |
|---|--------------------------|------------------------|-----------------------------------------|
| 1 | Frequency Tolerance      | $\leq \pm 1\text{ppm}$ |                                         |
| 2 | Tx Power                 | -2dBm +/- 3dBm         |                                         |
| 3 | Modulation               | 8KHz +/-3KHz           | Audio Frequency : 1KHz<br>Level : 150mV |
| 4 | Modulation S/N           | $\geq 30\text{dB}$     | Same as item 3                          |
| 5 | TX VCO reference voltage | 1 - 2V                 | Channel 20                              |
| 6 | Spurious Emissions       | $\leq -60\text{ dB}$   | 25KHz ~ 88MHz                           |
|   |                          | $\leq -60\text{ dB}$   | 88MHz ~ 216MHz                          |
|   |                          | $\leq -50\text{ dB}$   | 216MHz ~ 1GHz                           |
|   |                          | $\leq -50\text{ dB}$   | 1GHz                                    |

## RX Specification

Test Condition : Room Temperature (  $25 \pm 3^\circ\text{C}$  ) / Nominal Power Supply Voltage/CCITT Filter OFF

|   | Items                         | Specification         | Condition                                                  |
|---|-------------------------------|-----------------------|------------------------------------------------------------|
| 1 | Receiving Sensitivity         | $\leq -112\text{dBm}$ | 1KHz +/-8KHz Deviation<br>12dB Sinadder                    |
| 2 | Demodulation Audio S/N        | $\geq 45\text{dB}$    | 1KHz +/-8KHz Deviation<br>RF Input Level : -47dBm          |
| 3 | Demodulation Audio Distortion | $\leq 3\%$            | Same as item 2                                             |
| 4 | Audio Output Level            | 250mV +/-3dB          | Same as item 2                                             |
| 5 | Adjacent Channel Rejection    | $\geq 45\text{dB}$    | 2 Signal Method<br>Unwanted signal are shifted a +/- 50KHz |
| 6 | Image Frequency Rejection     | $\geq 45\text{dB}$    | Same as item 5                                             |
| 7 | VCO locking time              | Max : 16mS            | When channel is changed                                    |
| 8 | RX VCO Reference voltage      | 1 - 2V                | At Channel 20                                              |

**Note : All items are specified on SBM3020GA ( Test fixture ).**

**\*\* RX test method of item 5 & 6 \*\***

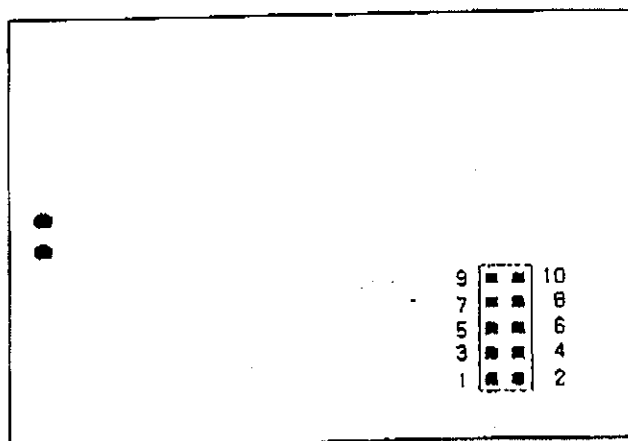
Wanted signal : 1KHz Audio signal +/-8KHz deviation

Unwanted signal : 400Hz Audio signal +/-8KHz deviation

**\*\* Specification are defined when sensitivity is dropped from a 12dB sinadder to 6dB sinadder by strength of the unwanted signal. \*\***

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# PIN CONFIGURATION



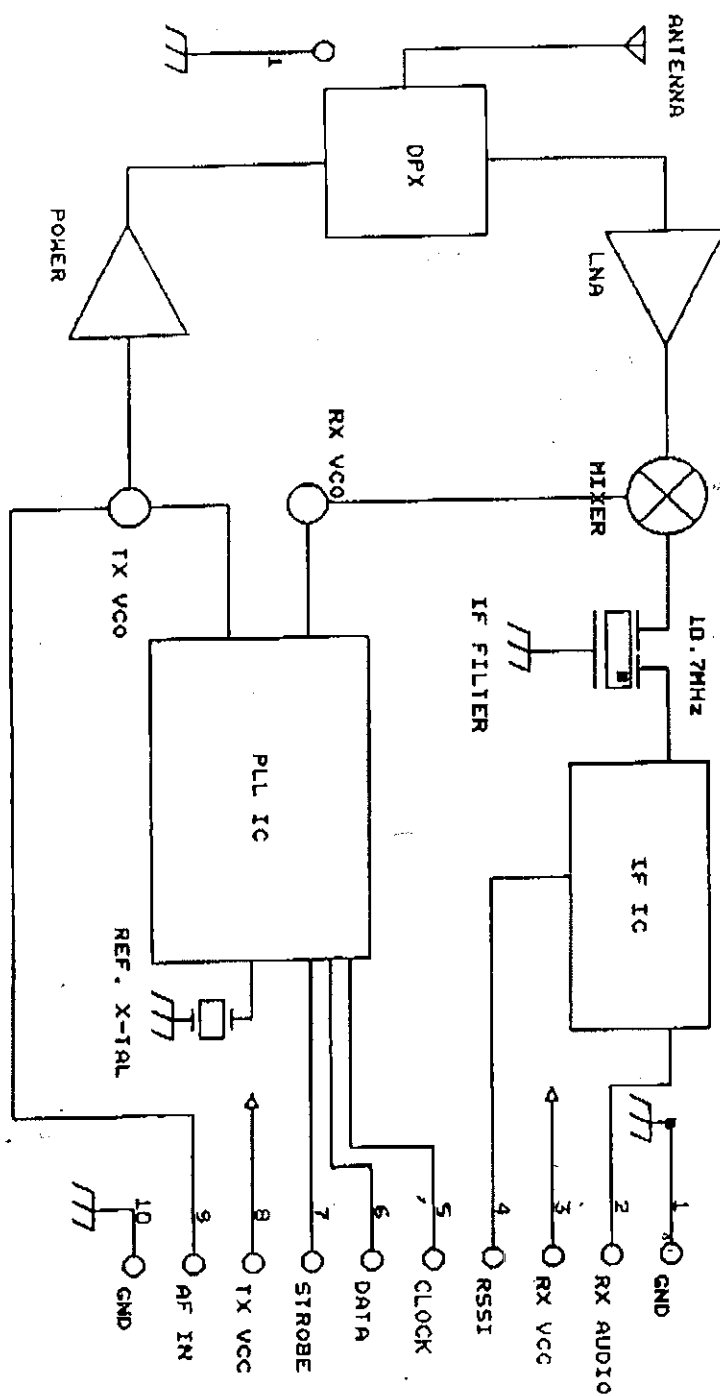
(TOP VIEW)

## [ DETAIL ]

| PIN NO | PIN NAME | I/O | FUNCTION               |
|--------|----------|-----|------------------------|
| 1      | AF IN    | In  | MODULATION VOICE INPUT |
| 2      | Tx-VCC   | In  | Tx PART VOLTAGE        |
| 3      | Rx-VCC   | In  | Rx PART VOLTAGE        |
| 4      | X-OUT    | OUT | 6MHz X-TAL OUTPUT      |
| 5      | DATA     | In  | PLL DATA               |
| 6      | CLOCK    | In  | PLL CLOCK              |
| 7      | CE       | In  | PLL ENABLE             |
| 8      | GND      | In  | GROUND                 |
| 9      | AF-OUT   | Out | DEMODULATION AUDIO OUT |
| 10     | C/S      | Out | CARRIER SENSE          |

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### 3. BLOCK DIAGRAM

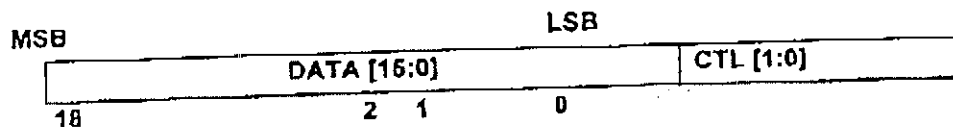


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## 4. Programming Description

### 2.1 MICROWIRE™ Interface

The descriptions below detail the 18-bit data register loaded through the MICROWIRE™ Interface. The 18-bit shift register is used to program the 12-bit Main and Aux R counter registers and the 16-bit Main and Aux N counter registers. The shift register consists of a 16-bit DATA field and a 2-bit control (CTL [1:0]) field as shown below. The control bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the 4 appropriate latches (selected by address bits). Data is shifted in MSB first.



#### 2.1.1 Register Location Truth Table

When LE transitions high, data is transferred from the 18-bit shift register into one of the 4 appropriate internal latches depending upon the state of the control (CTL) bits. The control bits decode the internal register address.

| CTL [1:0] |   | DATA Location   |
|-----------|---|-----------------|
| 0         | 0 | AUX_R register  |
| 0         | 1 | AUX_N register  |
| 1         | 0 | MAIN_R register |
| 1         | 1 | MAIN_N register |

#### 2.1.2 Register Content Truth Table

|        | SHIFT REGISTER BIT LOCATION |    |    |    |             |    |    |    |   |   |   |   |            |   |          |   |   |   |   |   |
|--------|-----------------------------|----|----|----|-------------|----|----|----|---|---|---|---|------------|---|----------|---|---|---|---|---|
|        | First Bit                   |    |    |    |             |    |    |    |   |   |   |   |            |   | Last Bit |   |   |   |   |   |
|        | 17                          | 16 | 15 | 14 | 13          | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5          | 4 | 3        | 2 | 1 | 0 |   |   |
| AUX_R  | FOLD                        |    |    |    | AUX_R_CNTR  |    |    |    |   |   |   |   |            |   |          |   |   |   | 0 | 0 |
| AUX_N  | AUX_B_CNTR                  |    |    |    |             |    |    |    |   |   |   |   | AUX_A_CNTR |   |          |   | 0 | 1 |   |   |
| MAIN_R | CP_WORD                     |    |    |    | MAIN_R_CNTR |    |    |    |   |   |   |   |            |   |          |   |   |   | 1 | 0 |
| MAIN_N | MAIN_B_CNTR and MAIN_A_CNTR |    |    |    |             |    |    |    |   |   |   |   |            |   |          |   | 1 | 1 |   |   |

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## Programmable Reference Dividers

### 2.2.1 AUX\_R Register

If the Control Bits (CTL [1:0]) are 0 0 when LE transitions high, data is transferred from the 18-bit shift register into a latch which sets the Aux PLL 12-bit R counter divide ratio. The divide ratio is programmed using the bits **AUX\_R\_CNTR** as shown in table 2.2.3. The divider ratio must be  $\geq 2$ . The FoLD word bits control the multifunction FoLD output as described in section 1.2.5.

| SHIFT REGISTER BIT LOCATION |    |    |    |           |    |    |    |                  |   |   |   |          |   |   |   |   |   |
|-----------------------------|----|----|----|-----------|----|----|----|------------------|---|---|---|----------|---|---|---|---|---|
| First Bit                   |    |    |    |           |    |    |    |                  |   |   |   | Last Bit |   |   |   |   |   |
| 17                          | 16 | 15 | 14 | 13        | 12 | 11 | 10 | 9                | 8 | 7 | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
| AUX_R                       |    |    |    | FoLD[3:0] |    |    |    | AUX_R_CNTR[11:0] |   |   |   |          |   |   |   | 0 | 0 |

### 2.2.2 MAIN\_R Register

If the Control Bits (CTL [1:0]) are 1 0 when LE transitions high, data is transferred from the 18-bit shift register into a latch which sets the Main PLL 12-bit R counter divide ratio and various control functions. The divide ratio is programmed using the bits **MAIN\_R\_CNTR** as shown in table 2.2.3. The divider ratio must be  $\geq 2$ . The charge pump control word (CP\_WORD[3:0]) sets the charge pump gain and the phase detector polarity as detailed in 2.4.

| SHIFT REGISTER BIT LOCATION |    |    |    |              |    |    |    |                   |   |   |   |          |   |   |   |   |   |
|-----------------------------|----|----|----|--------------|----|----|----|-------------------|---|---|---|----------|---|---|---|---|---|
| First Bit                   |    |    |    |              |    |    |    |                   |   |   |   | Last Bit |   |   |   |   |   |
| 17                          | 16 | 15 | 14 | 13           | 12 | 11 | 10 | 9                 | 8 | 7 | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
| MAIN_R                      |    |    |    | CP_WORD[3:0] |    |    |    | MAIN_R_CNTR[11:0] |   |   |   |          |   |   |   | 1 | 0 |

### 2.2.3 12-Bit Programmable Main and Auxiliary Reference Divider Ratio (MAIN/AUX R Counter)

| MAIN_R_CNTR/AUX_R_CNTR |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------------|----|----|---|---|---|---|---|---|---|---|---|---|
| Divide ratio           | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 2                      | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3                      | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| •                      | •  | •  | • | • | • | • | • | • | • | • | • | • |
| 4,095                  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTE: Legal divide ratio: 2 to 4,095.

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## Programmable Feedback (N) Dividers

### 2.3.1 AUX\_N Register

If the Control Bits (CTL[1:0]) are 0 1 when LE transitions high, data is transferred from the 18-bit shift register into the AUX\_N register. The AUX\_N counter is a 16-bit counter which is fully latch which sets the Aux PLL 16 bit programmable N counter value. The AUX\_N counter is a 16-bit counter which is fully programmable from 240 to 65,535 for 1.1 GHz option or from 56 to 32,767 for 500 MHz option. The AUX\_N register consists of the 4-bit swallow counter (AUX\_A\_CNTR), the 12 bit programmable counter (AUX\_B\_CNTR). Serial data format is shown below. The divide ratio (AUX\_N\_CNTR [13:0]) must be  $\geq 240$  (1.1 GHz option) or  $\geq 56$  (500 MHz option) for a continuous divide range. The Aux PLL N divide ratio is programmed using the bits AUX\_A\_CNTR, AUX\_B\_CNTR as shown in tables 2.3.2.

| SHIFT REGISTER BIT LOCATION |    |    |    |    |    |    |    |   |   |   |   |                 |   |   |   |   |   |
|-----------------------------|----|----|----|----|----|----|----|---|---|---|---|-----------------|---|---|---|---|---|
| First Bit                   |    |    |    |    |    |    |    |   |   |   |   | Last Bit        |   |   |   |   |   |
| 17                          | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5               | 4 | 3 | 2 | 1 | 0 |
| AUX_B_CNTR[11:0]            |    |    |    |    |    |    |    |   |   |   |   | AUX_A_CNTR[3:0] |   |   | 0 | 1 |   |

### 2.3.2 6-BIT Swallow Counter Divide Ratio (Aux A COUNTER)

1.1 GHz option

| Swallow Count | AUX_A_CNTR |   |   |   |
|---------------|------------|---|---|---|
| (A)           | 3          | 2 | 1 | 0 |
| 0             | 0          | 0 | 0 | 0 |
| 1             | 0          | 0 | 0 | 1 |
| .             | .          | . | . | . |
| 15            | 1          | 1 | 1 | 1 |

Notes: Swallow Counter Value: 0 to 15

500 MHz option

| Swallow Count | AUX_A_CNTR |   |   |   |
|---------------|------------|---|---|---|
| (A)           | 3          | 2 | 1 | 0 |
| 0             | X          | 0 | 0 | 0 |
| 1             | X          | 0 | 0 | 1 |
| .             | .          | . | . | . |
| 7             | X          | 1 | 1 | 1 |

Notes: Swallow Counter Value: 0 to 7  
X = Don't Care condition

### 2.3.3 12-BIT Programmable Counter Divide Ratio (Aux B COUNTER)

| AUX_B_CNTR   |    |    |   |   |   |   |   |   |   |   |   |   |
|--------------|----|----|---|---|---|---|---|---|---|---|---|---|
| Divide Ratio | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 3            | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4            | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| .            | .  | .  | . | . | . | . | . | . | . | . | . | . |
| 4,095        | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTES: Divide ratio: 3 to 4,095 (Divide ratios less than 3 are prohibited)  
AUX\_B\_CNTR  $\geq$  AUX\_A\_CNTR.  
See section 2.3.7 for calculation of VCO output frequency.

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### 2.3.4 MAIN\_N Register

If the Control Bits (CTL[1:0]) are 1 1 when LE transitions high, data is transferred from the 18-bit shift register into the MAIN\_N register latch which sets 16 programmable N divider value. The Main N divider is a 16-bit counter which is fully programmable from 992 to 65,535 for 2 GHz option and from 240 to 65,535 for 1.1 GHz option. The MAIN\_N register consists of the 5-bit (2 GHz option) or 4 bit (1.1 GHz option) swallow counter (MAIN\_A\_CNTR) and the 11 bit (2 GHz option) or 12 bit (1.1 GHz option) programmable counter (MAIN\_B\_CNTR). Serial data format for the MAIN\_N register latch shown below. The divide ratio must be  $\geq 992$  (2 GHz option) or  $\geq 240$  (1.1 GHz option) for a continuous divide range. The divide ratio is programmed using the bits MAIN\_A\_CNTR and MAIN\_B\_CNTR as shown in tables 2.3.6 and 2.3.6. The pulse swallow function which determines the divide ratio is described in section 2.3.7.

2 GHz option

2 GHz option

| SHIFT REGISTER BIT LOCATION |    |    |    |    |    |    |    |   |   |   |                 |   |   |   |   |   |   |
|-----------------------------|----|----|----|----|----|----|----|---|---|---|-----------------|---|---|---|---|---|---|
| First Bit                   |    |    |    |    |    |    |    |   |   |   | Last Bit        |   |   |   |   |   |   |
| 17                          | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6               | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_B_CNTR[10:0]            |    |    |    |    |    |    |    |   |   |   | AUX_A_CNTR[4:0] |   |   |   | 1 | 1 |   |
| MAIN_N                      |    |    |    |    |    |    |    |   |   |   |                 |   |   |   |   |   |   |

1.1 GHz option

1.1 GHz option

| SHIFT REGISTER BIT LOCATION |                  |    |    |    |    |    |    |   |   |   |   |          |                 |   |   |   |   |
|-----------------------------|------------------|----|----|----|----|----|----|---|---|---|---|----------|-----------------|---|---|---|---|
| First Bit                   |                  |    |    |    |    |    |    |   |   |   |   | Last Bit |                 |   |   |   |   |
| 17                          | 16               | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5        | 4               | 3 | 2 | 1 | 0 |
| MAIN_N                      | AUX_B_CNTR[11:0] |    |    |    |    |    |    |   |   |   |   |          | AUX_A_CNTR[3:0] |   |   | 1 | 1 |

### 2.3.5 5-BIT Swallow Counter Divide Ratio (Main A COUNTER)

2 GHz option

| Swallow Count | MAIN_A_CNTR |   |   |   |   |
|---------------|-------------|---|---|---|---|
| (A)           | 4           | 3 | 2 | 1 | 0 |
| 0             | 0           | 0 | 0 | 0 | 0 |
| 1             | 0           | 0 | 0 | 0 | 1 |
| •             | •           | • | • | • | • |
| 31            | 1           | 1 | 1 | 1 | 1 |

NOTE: Swallow Counter Value: 0 to 31

1.1 GHz option

| Swallow Count | MAIN_A_CNTR |   |   |   |
|---------------|-------------|---|---|---|
| (A)           | 3           | 2 | 1 | 0 |
| 0             | 0           | 0 | 0 | 0 |
| 1             | 0           | 0 | 0 | 1 |
| •             | •           | • | • | • |
| 15            | 1           | 1 | 1 | 1 |

NOTE: Swallow Counter Value: 0 to 15

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## 2.3.6 Programmable Counter Divide Ratio (Main B COUNTER)

2 GHz option

|              | MAIN_B_CNTR |   |   |   |   |   |   |   |   |   |   |
|--------------|-------------|---|---|---|---|---|---|---|---|---|---|
| Divide Ratio | 10          | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 3            | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4            | 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| •            | •           | • | • | • | • | • | • | • | • | • | • |
| 2,047        | 1           | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTES: Divide ratio: 3 to 2,047 (Divide ratios less than 3 are prohibited)  
 MAIN\_B\_CNTR ≥ MAIN\_A\_CNTR.

See section 2.3.7 for calculation of VCO output frequency.

1.1 GHz option

|              | MAIN_B_CNTR |    |   |   |   |   |   |   |   |   |   |   |
|--------------|-------------|----|---|---|---|---|---|---|---|---|---|---|
| Divide Ratio | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 3            | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4            | 0           | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| •            | •           | •  | • | • | • | • | • | • | • | • | • | • |
| 4,095        | 1           | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTES: Divide ratio: 3 to 4,095 (Divide ratios less than 3 are prohibited)  
 MAIN\_B\_CNTR ≥ MAIN\_A\_CNTR.

See section 2.3.7 for calculation of VCO output frequency.

## 2.3.7 Pulse Swallow Function

The N divider counts such that it divides the VCO RF frequency by (P+1) for A times, and then divides by P for (B - A) times. The B value (B\_CNTR) must be ≥ 3. The continuous divider range for the Main PLL N divider is from 992 to 65,535 for 2 GHz option, from 240 to 65,535 for 1.1 GHz option, and from 56 to 32,767 for 500 MHz option. Divider ratios less than the minimum value are achievable as long as the binary counter value is greater than the swallow counter value (B\_CNTR ≥ A\_CNTR).

$$F_{vco} = N \times (f_{osc} / R)$$

$$N = (P \times B) + A$$

- f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)
- f<sub>osc</sub>: Output frequency of the external reference frequency oscillator (input to OSC<sub>IN</sub>).
- R: Preset divide ratio of binary programmable reference counter (R\_CNTR)
- N: Preset divide ratio of main programmable Integer N counter (N\_CNTR)
- B: Preset divide ratio of binary programmable B counter (B\_CNTR)
- A: Preset value of binary 4-bit swallow A counter (A\_CNTR)
- P: Preset modulus of dual modulus prescaler (P = 32 for 2 GHz option, P=16 for 1.1 GHz option, and P=8 for 500 MHz option)

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## 2.4 Charge Pump Control Word (CP\_WORD)

30. Tone's level & Pulse's M-B Ratio display

LSB

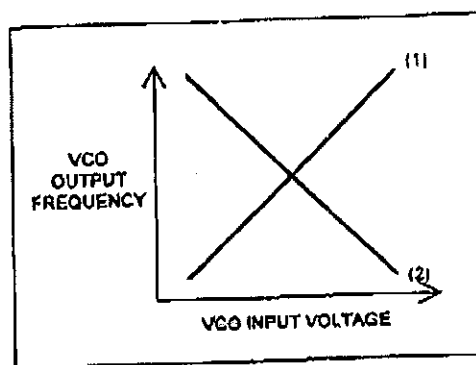
| MSB         |              |            |             | LSB |
|-------------|--------------|------------|-------------|-----|
| AUX_CP_GAIN | MAIN_CP_GAIN | AUX_PD_POL | MAIN_PD_POL |     |

31. M-B RATIO fault lamp

| BIT          | LOCATION   | FUNCTION                      | 0        | 1        |
|--------------|------------|-------------------------------|----------|----------|
| AUX_CP_GAIN  | MAIN_R[17] | Aux Charge Pump Current Gain  | LOW      | HIGH     |
| MAIN_CP_GAIN | MAIN_R[16] | Main Charge Pump Current Gain | LOW      | HIGH     |
| AUX_PD_POL   | MAIN_R[15] | Aux Phase Detector Polarity   | Negative | Positive |
| MAIN_PD_POL  | MAIN_R[14] | Main Phase Detector Polarity  | Negative | Positive |

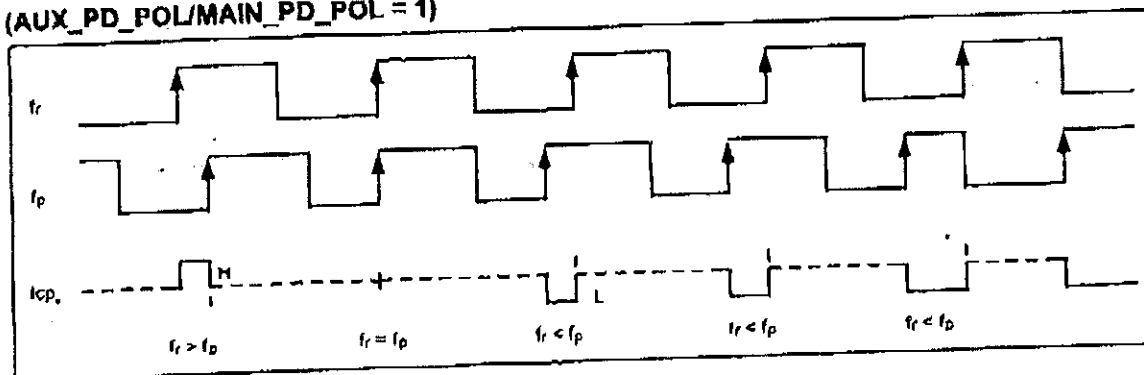
AUX\_CP\_GAIN (MAIN\_R[17]) and MAIN\_CP\_GAIN (MAIN\_R[16]) are used to select charge pump current magnitude either low gain mode (160 uA typ) or high gain mode (1600 uA typ)  
 AUX\_PD\_POL (MAIN\_R[15]) and MAIN\_PD\_POL (MAIN\_R[14]) are respectively set to one when Aux or Main VCO characteristics are positive as in (1) below. When VCO frequency decreases with increasing control voltage (2) PD\_POL should set to zero.

### 2.4.1 VCO Characteristics



### 2.4.2 Phase Comparator and Internal Charge Pump Characteristics

(AUX\_PD\_POL/MAIN\_PD\_POL = 1)



NOTES:  $f_r$  is phase detector input from reference counter,  $f_p$  is phase detector input from programmable N counter.

Phase difference detection range:  $-2\pi$  to  $+2\pi$

The minimum width pump up and pump down current pulses occur at the CPo pin when the loop is locked.

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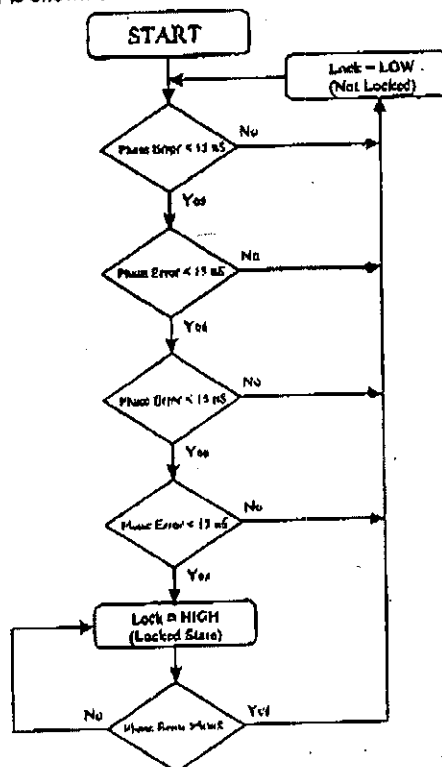
## 2.5 Fout/Lock Detect Programming Truth Table (FoLD)

| FoLD      |           |           |           | Fo/LD OUTPUT STATE               |
|-----------|-----------|-----------|-----------|----------------------------------|
| 3         | 2         | 1         | 0         |                                  |
| AUX_R[17] | AUX_R[16] | AUX_R[15] | AUX_R[14] |                                  |
| 0         | 0         | 0         | 1         | "1"                              |
| 0         | 0         | 0         | 0         | "0"                              |
| 0         | 0         | 1         | X         | Main lock detect                 |
| 0         | 1         | 0         | X         | Aux lock detect                  |
| 0         | 1         | 1         | X         | Main "and" Aux lock detect       |
| 1         | 0         | 0         | X         | Main reference counter output    |
| 1         | 0         | 1         | X         | Aux reference counter output     |
| 1         | 1         | 0         | X         | Main programmable counter output |
| 1         | 1         | 1         | X         | Aux programmable counter output  |

NOTE: See section 2.5.3 for AUX\_R[14] description.

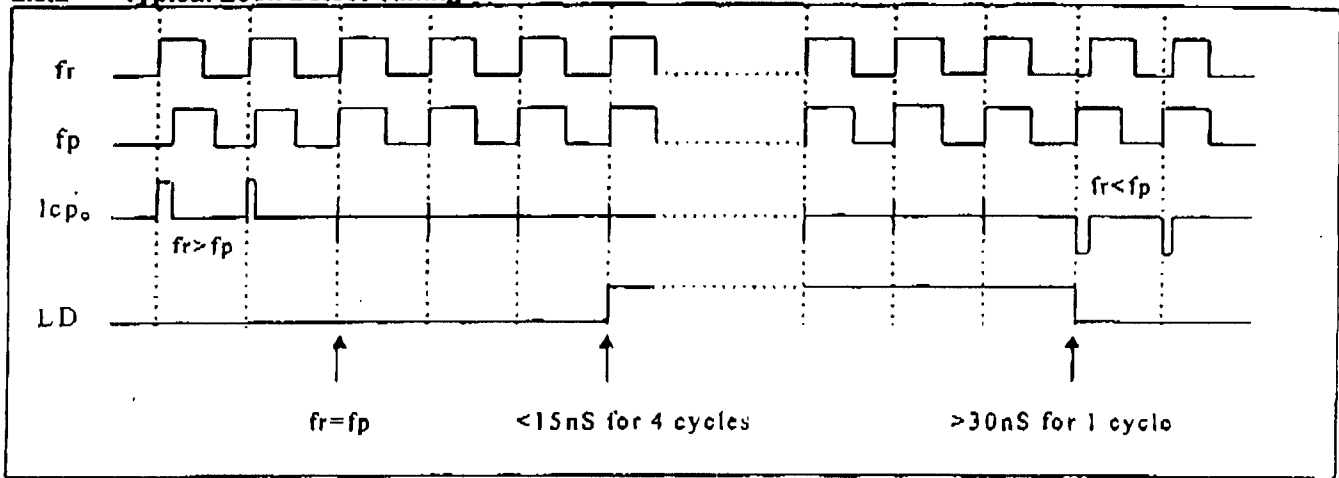
### 2.5.1 Lock Detect Digital Filter

The Lock Detect Digital Filter compares the difference between the phase of the inputs of the phase detector to a RC generated delay of approximately 15 nS. To enter the locked state (Lock = HIGH) the phase error must be less than the 15 nS RC delay for 4 consecutive reference cycles. Once in lock (Lock = HIGH), the RC delay is changed to approximately 30 nS. To exit the locked state (Lock = LOW), the phase error must become greater than the 30 nS RC delay. When the PLL is in the powerdown mode, Lock is forced LOW. A flow chart of the digital filter is shown below.



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### 2.5.2 Typical Lock Detect Timing



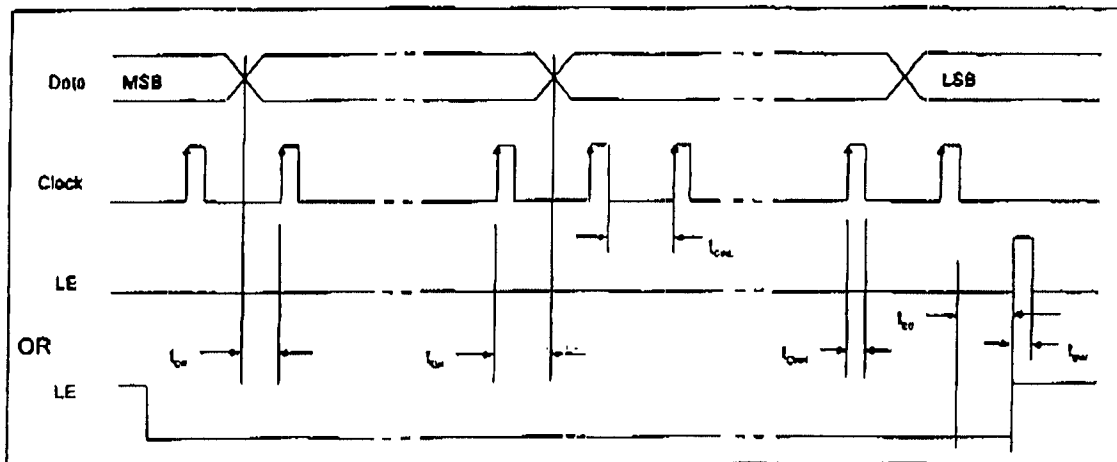
### 2.5.3 OSC Mode Programming

The OSCout pin can be optimized for operating with an external crystal resonator or an external reference frequency source (i.e. TCXO). If the application uses an external reference frequency source, the current dissipation of the LMX1600/01/02 can be reduced with the Logic Mode (0.5 mA typ.). Crystal Mode should be used when an external crystal resonator is used. Logic Mode is used when an external reference frequency source is used. In Logic Mode, OSCout should be connected to a 30 pF capacitor to ground for optimum performance.

When the FoLD output state is selected to CMOS high/low levels, the OSC Mode is forced to Crystal Mode.

| FoLD             |           |           |           | OSCout       |
|------------------|-----------|-----------|-----------|--------------|
| 3                | 2         | 1         | 0         |              |
| AUX_R[17]        | AUX_R[16] | AUX_R[15] | AUX_R[14] |              |
| 0                | 0         | 0         | 1         | Crystal Mode |
| 0                | 0         | 0         | 0         | Crystal Mode |
| All other states |           |           | 0         | Logic Mode   |
|                  |           |           | 1         | Crystal Mode |

### 2.6 SERIAL DATA INPUT TIMING



NOTES: Data shifted into register on clock rising edge. Data is shifted in MSB first.

TEST CONDITIONS: The Serial Data Input Timing is tested using a symmetrical waveform around  $V_{cc}/2$ . The test waveform has an edge rate of 0.6 V/nsec with amplitudes of 2.2 V @  $V_{cc} = 2.7$  V.

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RESIDENT

(2)

| MARK | DATE | MEMO | CHECK |
|------|------|------|-------|
| A    |      |      |       |
| A    |      |      |       |

TO: IDT  
DATE: MAY. 24. 68

ATTN: MR. S. D. PARK / RLD

RE: MECHANICAL DRAWING FOR RS MODULE.

DEAR MR. PARK, PLS FIND ATTACHED

REVISE MECHANICAL DRAWING.

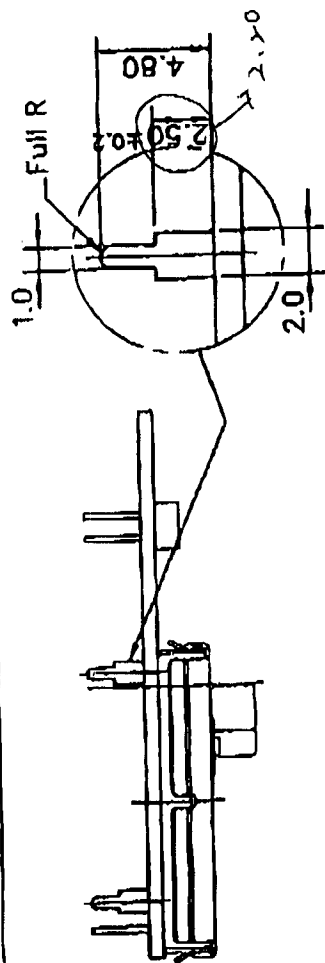
TOTAL PAGES:

THANKS AND BEST REGARDS  
CEIVE

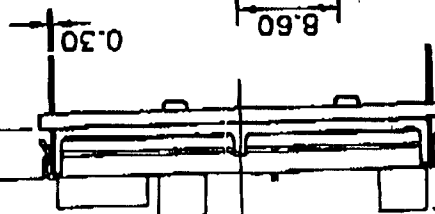
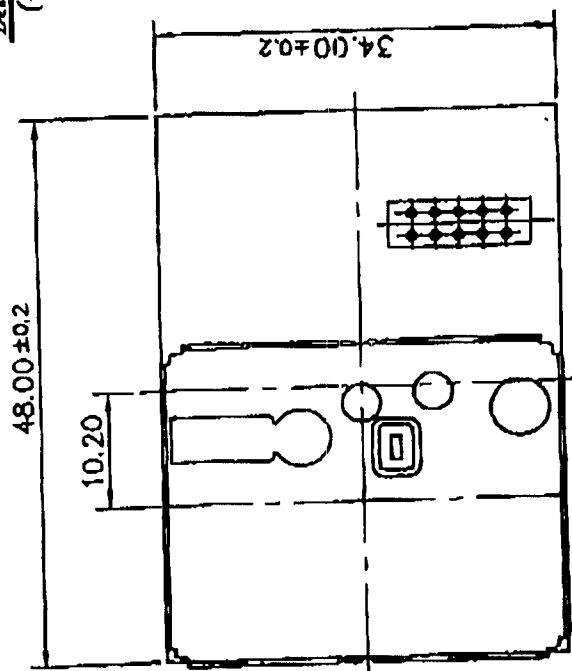
K. 3. K. 202

24 MAY 1968

BY: PDD-TELECOM



Detail (S-2/H)  
(472)



8.5 W/DX

PODTEL - 811 KMH

**KJ HAN - W MUJ CHEUNG!**



SU PARK YS JEONG ELI  
SPETER- GC KO / F NG /

TL SHUM

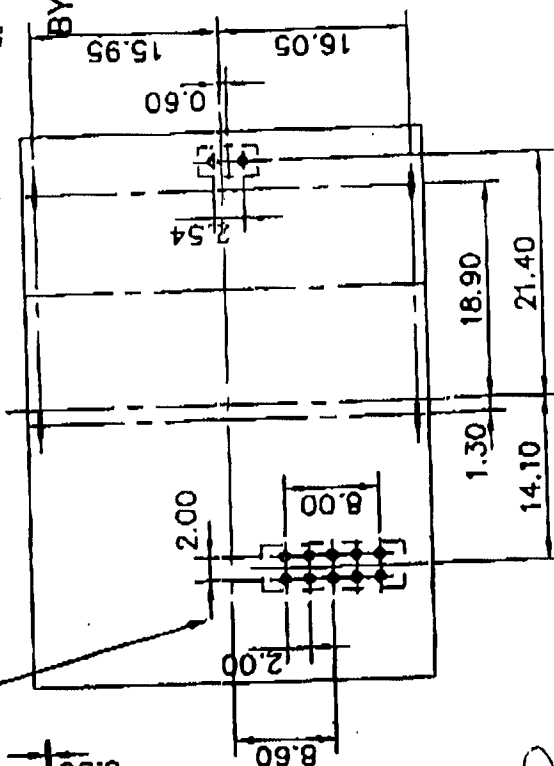
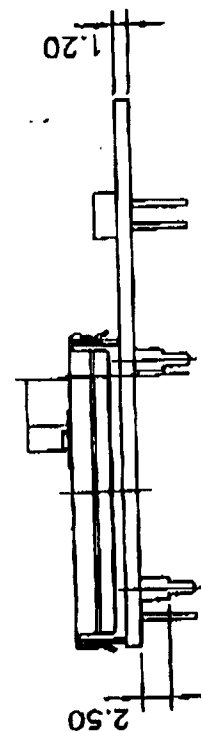
WY HO - G21  
KI HO - XS LEUNGAL WONG

SH KONG - NI LEE EC KANG!

YK KIM, IK YEUNG, I

KK YIP, THO:J CHAN, KL MAN

K'WONG, SP'WONG

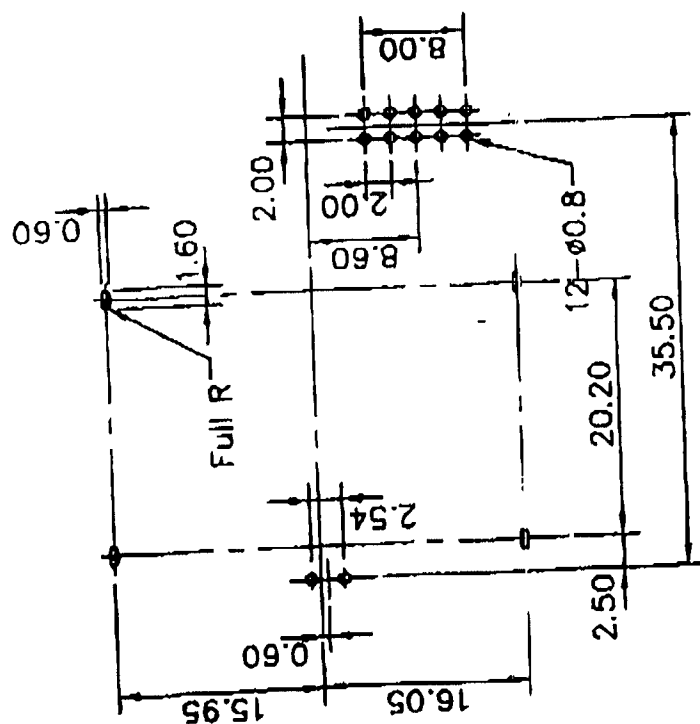
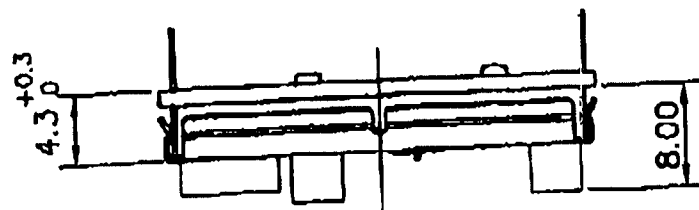
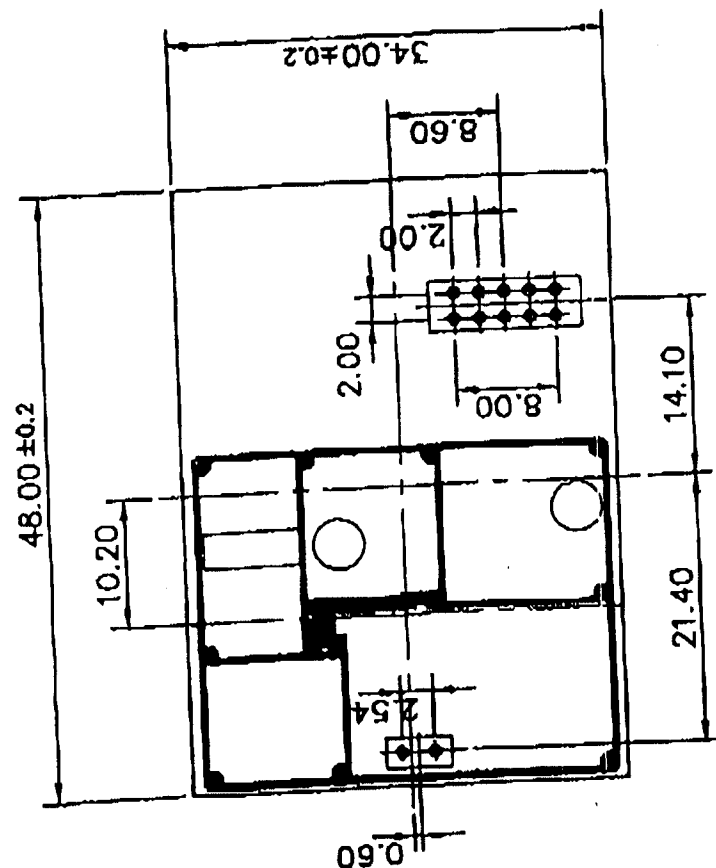
KIRKCH-  
STUEGE

| NO | NOMENCLATURE  | MATERIAL  | Q'TY           | SPECIFICATION | TREAT    | REMARKS |
|----|---------------|-----------|----------------|---------------|----------|---------|
| 1  | A             | 0.05      | 0.1            | SCALE 1/1     | DATE     | OD.5.23 |
| 2  | B             | 0.07      | 0.2            | ANGLE ±       | REV      |         |
| 3  | C             | APPROVAL  | MODEL          | SBM 3020A     | UNIT M/M |         |
| 4  | DRAWING CHECK | PART NAME | Module(Narrow) |               |          |         |

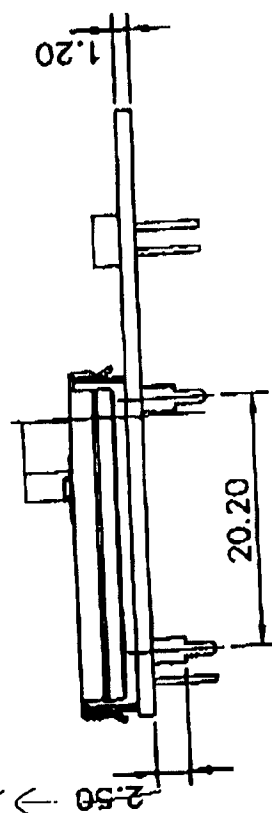
# RESIN

$$\left(\frac{1}{2}\right)$$

| MARK | DATE | MEMO | CHECK |
|------|------|------|-------|
| △    |      |      |       |
| △    |      |      |       |



[PCB Hole]



| NO                     | NUMERATURE | MATERIAL | Q'TY   | SPECIFICATION  | TREAT | REMARKS  |
|------------------------|------------|----------|--------|----------------|-------|----------|
| 1~4                    | 4~16       | 18~63    | 63-250 | SCALE 1/1      | DATE  | 00.5.23  |
| A                      | 0.05       | 0.07     | 0.1    | ANGLE ±        | REV   |          |
| DRAWING CHECK APPROVAL |            |          |        | SBM 3020A      |       | UNIT M/M |
| DETAILS                |            |          |        | M (d) (Narrow) |       | ⊕        |