EXHIBIT 12

CB TRANSMITTER POWER

12.0 CB Transmitter Power

The dissipation rating of all the semiconductors or electron tubes which supply RF power to the antenna terminals of each CB transmitter does not exceed 10W.

インフィ.エレクトロニクス ジャパン 株式会社 殿 製品名 2SC2078 仕様書No

納入仕様書

ご承認欄

初制機種	共通
部品名	TRANSISTOR
部品番号	ST2C2078

朱書訂正をもって承認とする

承認 T.E. JAPAN 技術部

承認	検討	担当
技術 9.12.84 茂木		技術 84.9.10 田口

(21-1502) TRC-421 初制
1980年8月27日発行の承認図は廃棄とする

発行 東京三洋電機株式会社
半導体事業部
群馬県邑楽郡大泉町坂田180 ☎0276(63)1111大代表

FCC ID: AAO2F-1703

2SC2078-D 　納 入 仕 様 書　2/6

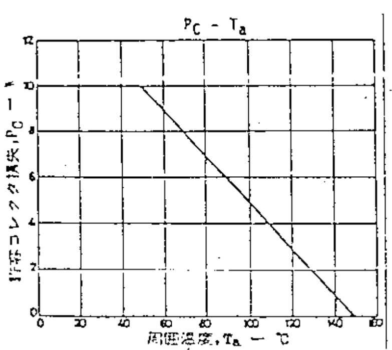
ダディ.エレクトロニクス ジャパン株式会社 殿 　製品名 2SC2078

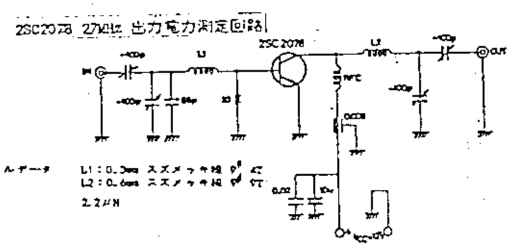
仕様書No. ST9541-A
発行日84年8月30日
前回仕様書No.
前回発行日　年　月　日
※この納入仕様書の有効期間は発行日より（本仕様書3年間、暫定仕様書3ケ月、仮仕様書1ケ月）とさせていただきます。また、ご返却のない場合は、ご承認されたものとして処理させていただきます。

1. 構　造：シリコン NPN エピタキシャルプレーナ型トランジスタ
2. 外　形：JEDEC:TO-220AB
3. 絶対最大定格（Ta＝25℃）
   V_{CBO}：80V, V_{CER}：75V, V_{EBO}：5V
   I_C：3A, i_{CP}：5A
   P_C (Ta＝25℃)：1.2W, (Tc＝25℃)：10W
   Tj：150℃, Tstg：−55〜+150℃
4. 電気的特性（Ta＝25℃）

記号	条件		最小値	標準値	最大値	単位
I_{CBO}	V_{CB}=40V, I_E=0				10	μA
I_{EBO}	V_{EB}=4V, I_C=0				10	μA
$V_{CE(sat)}$	I_C=1A, I_B=0.1A			0.15	0.6	V
$V_{BE(sat)}$	I_C=1A, I_B=0.1A			0.9	1.2	V
f_T	V_{CE}=10V, I_C=0.1A		100	150		MHz
cob	V_{CB}=10V, f=1MHz			45	60	pF
h_{FE}	V_{CE}=5V, I_C=0.5A	~~B~~	~~25~~		~~50~~	
	〃	C	40		80	
	〃	D	60		120	
	〃	E	100		200	
$V_{(BR)CBO}$	I_C=100μA, I_E=0		80			V
$V_{(BR)CER}$	I_C=1mA, R_{BE}=150Ω		75			V
$V_{(BR)EBO}$	I_E=100μA, I_C=0		5			V
Po	V_{CC}=12V, f=27MHz		4			W
	Pi=0.2W					
η	指定測定回路		60			%

備　考





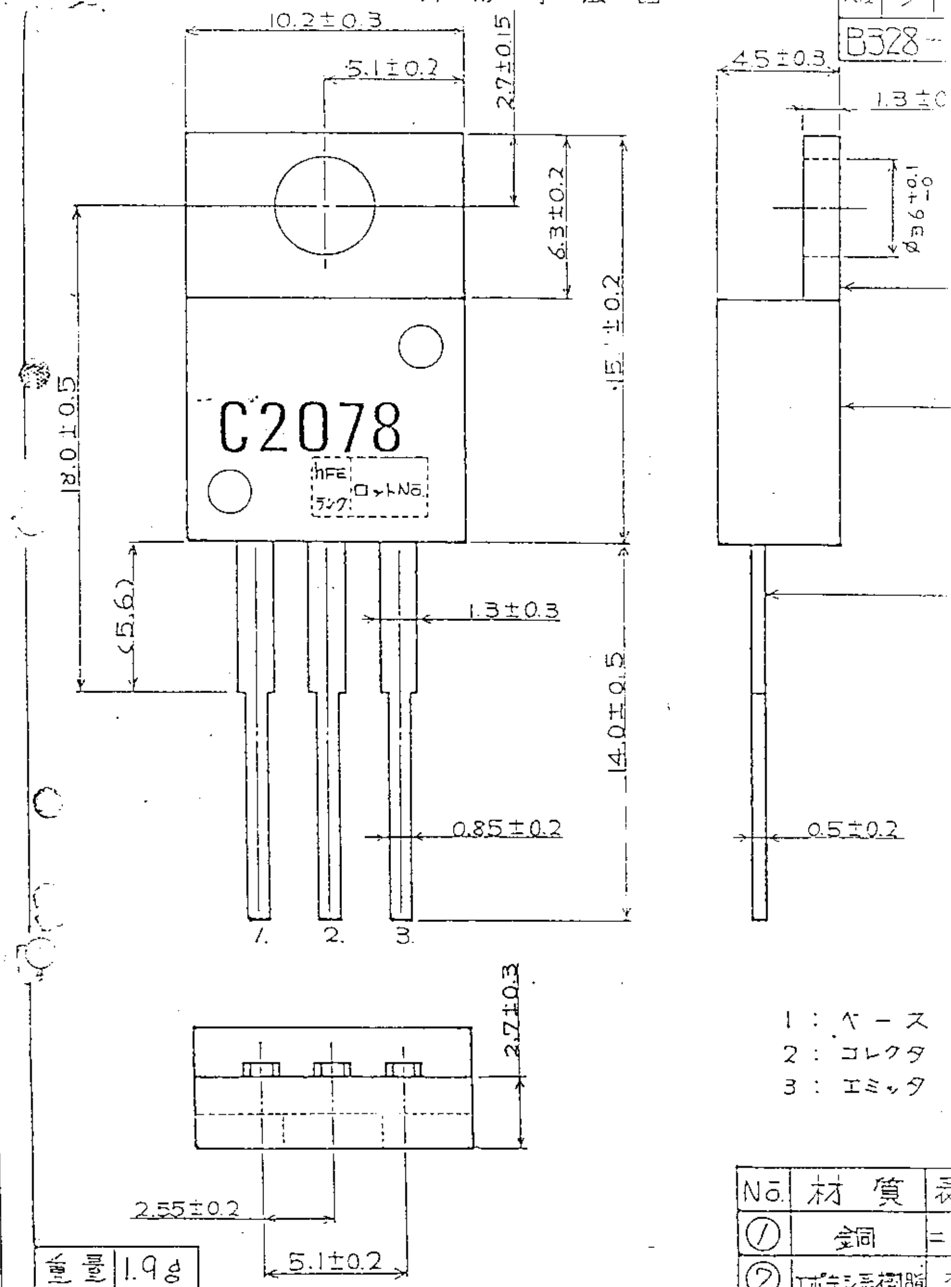
承認	査閲	作成

(8-2409)

SANYO／東京三洋電機株式会社　半導体事業部　C0012

No. 1

外形寸法図



1：ベース
2：コレクタ
3：エミッタ

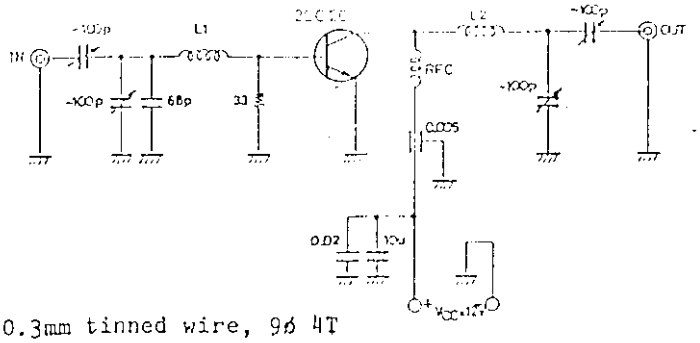
No.	材質	表
①	銅	ニッ
②	エポキシ系樹脂	
③	銅	ハン

重量 1.9g

注　図面上に現れない樹脂バリが付着する場合があります。

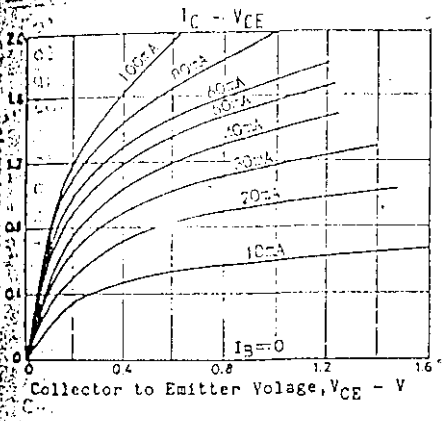
作成		作成日	83年3月5日	製品名	2SC2078	図番	
査閲	58.3.-5	承認		外形	EIAJ SC-46 / JEDEC TO-220AB / SANYO TO-220	製図No.	2－5

2SC2078 27MHz Output Power Test Circuit

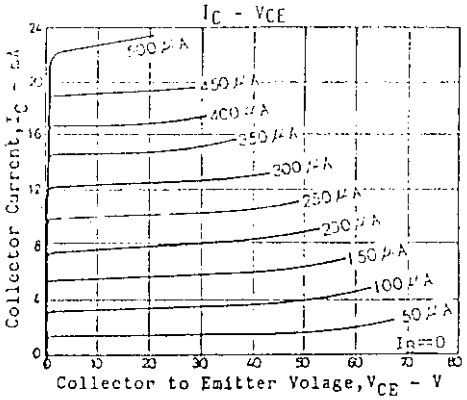


Coil data L1: 0.3mm tinned wire, 9ϕ 4T
L2: 0.6mm tinned wire, 9ϕ 4T
RFC 2.2uH

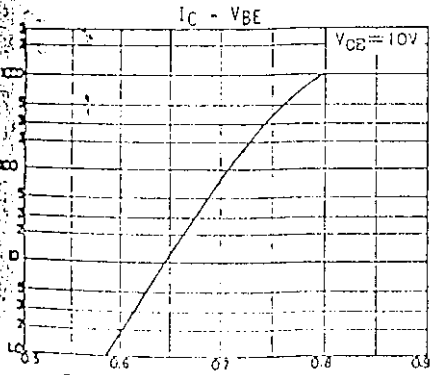
I_C - V_{CE}



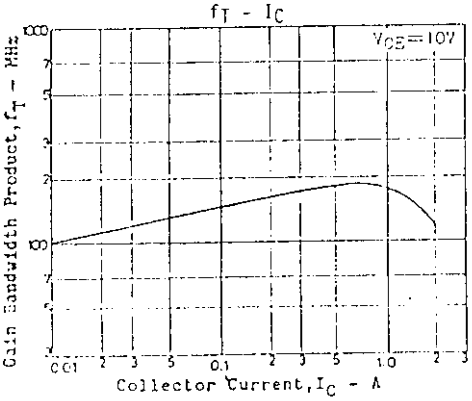
I_C - V_{CE}



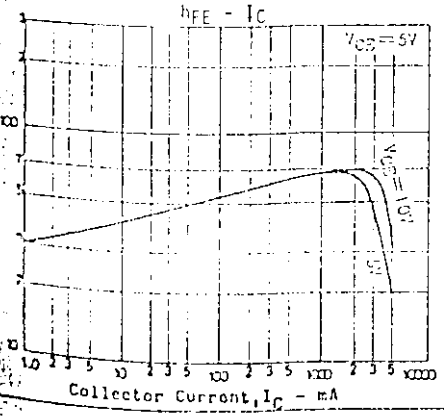
I_C - V_{BE}



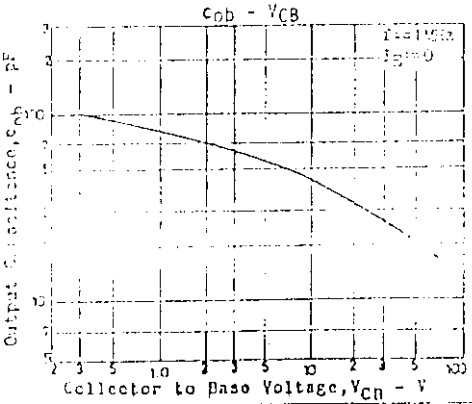
f_T - I_C



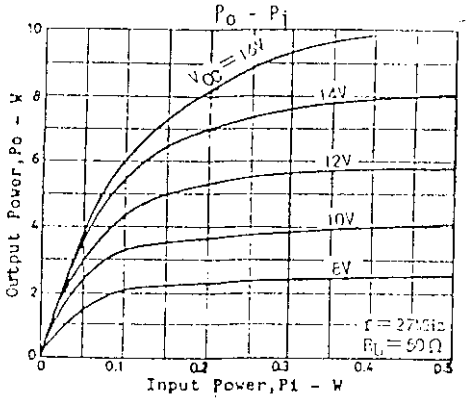
h_{FE} - I_C

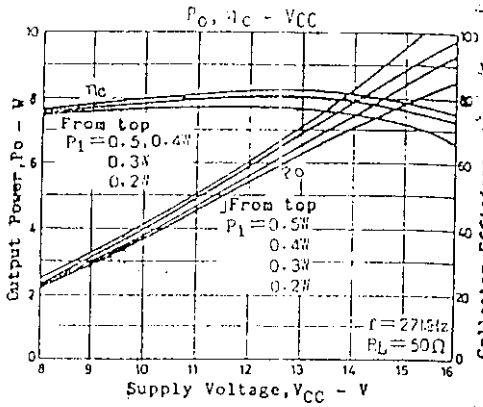


C_{ob} - V_{CB}



E3


Po - Pi
Output Power, Po - W
Input Power, Pi - W
VCC = 15V
14V
12V
10V
8V
f = 27MHz
RL = 50Ω


Po, ηc - VCC
Output Power, Po - W
Collector Efficiency, ηc - %
Supply Voltage, VCC - V
ηc
From top
Pi = 0.5, 0.4W
0.3W
0.2W
Po
From top
Pi = 0.5W
0.4W
0.3W
0.2W
f = 27MHz
RL = 50Ω

E4

FCC ID: AAO21-1703

西紀 1985年 4月 7日

韓國T.C電子 貴中

承認仕様書

本書に捺印をもって承認とする

承	認		
承認	作成	検討	担当
技術	技術	技術	技術

韓国電子株式会社

TCE KOREA

韓国電子株式会社半導体営業部

区分	品名	規格	備考
IC	KIA7217AP	KEC規格	

KOREA ELECTRONICS CO., LTD.

SEMICONDUCTOR

TECHNICAL DATA

MAXIMUM RATINGS

(Minimum working voltage is 9V)

Characteristic	Symbol	Rating	Unit
Operating Supply Voltage	V_{CC}	18	V
Quiescent Supply Voltage	V_{CCQ}	25	V
Output Peak Current	$I_{O(peak)}$	4.5	A
Power Dissipation	P_D	7.5	W
Operating Temperature	Topr	-20~75	°C
Storage Temperature	Tstg	-55~150	°C

ELECTRICAL CHARACTERISTICS

V_{CC}=13.2V, R_L=4Ω, R_g=600Ω, R_f=82Ω

Unless otherwise specified f=1kHz, Ta=25°C

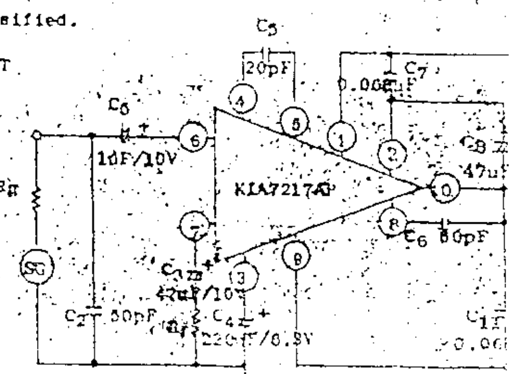
Characteristic	Symbol	Test Condition	Min.	Typ.
Quiescent Current	I_{CCQ}	-	-	-
		VCC=16V	-	-
Output Power	P_{OUT}	THD=10%	4.4	5
		V_{CC}=13.2V, THD=10%	5.7	6.8
		V_{CC}=13.2V, R_L=2Ω, THD=10%	-	8.2
Maximum Output Power	P_{OM}	V_{CC}=13.2V	-	9.5
Total Harmonic Distortion	THD	P_{OUT}=1W	-	0.15
		P_{OUT}=100mW	-	0.2
		P_{OUT}=1W, R_L=2Ω	-	0.25
Voltage Gain (Note)	Gv	V_{IN}=2.45mV$_{rms}$	52	-
Input Resistance	R_{IN}	V_{OUT}=2V$_{rms}$	30	40
Output Noise Voltage	V_{NO}	R_g=10kΩ BW=50~20kHz	-	-

(Note) In regard to the value of voltage gain (closed loop voltage), i possible to be classified.

TEST AND APPLICATION CIRCUIT

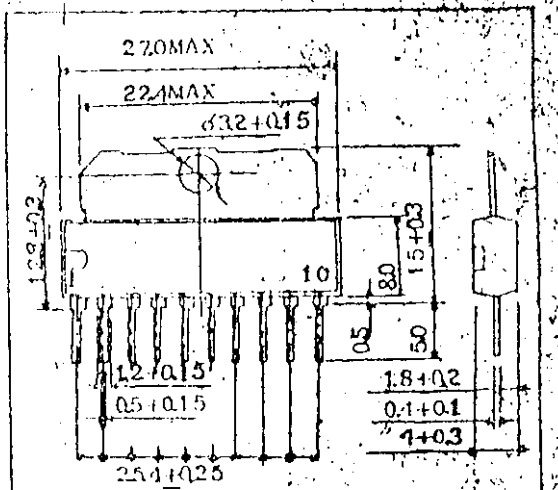
1) 방열Tab은 접속하지 않거나 혹은 PIN⑧과 동전위로 할것

2) Polyester Film Condenser 를 사용할것. (C_7, C_{11})



TENTATIVE

Unit, in mm



- o 5.6W Audio Power Amp 出力段に 適合
- o Car stereo Car Radio 출력단에 적합함.
- * 5.6W Audio Power Amplifier
- * Car Stereo, Car Radio Output

- * 출력 5.6W (Typ.)
  出力 ($@V_{CC}$=13.2V, R_L=4Ω, THD=10%)
- * 출력 0.2W (Typ.)
  出力 ($@V_{CC}$=13.2V, R_L=2Ω, THD=10%)
- * 최대출력 0.5W (Typ.)
  最大出力 ($@V_{CC}$=13.2V, R_L=4Ω)
- * 저왜율 : THD=0.15%($@P_{OUT}$=1W, G_V=55dB)
  低歪率 THD=0.07%($@P_{OUT}$=1W, G_V=44dB)
- * 동작 전원전압 범위가능 V_{CC}=9~18V 動作電源電圧の範囲広い
- * PCT 공정으로 저잡음임. 低雑音
- * 부하 단락, 전류제한 보호 회로 내장 過熱遮断, 電流制限 保護回路内蔵
- * 열보호 회로 내장 熱保護回路内蔵
- * Surge 보호 회로 내장 保護回路内蔵
- * Output Power 5.6W(Typ.) ($@V_{CC}$=13.2V, R_L=4Ω, THD=10%)
- * Output Power 0.2W(Typ.) ($@V_{CC}$=13.2V, R_L=2Ω, THD=10%)
- * Maximum Output Power 0.5W(Typ.) ($@V_{CC}$=13.2V, R_L=4Ω)
- * Low Distortion
  THD=0.15%(Typ.) ($@P_{OUT}$=1W, G_V=55dB)
  THD=0.07%(Typ.) ($@P_{OUT}$=1W, G_V=44dB)
- * Operating Supply Voltage Range : V_{CC}=9~18V
- * 'PCT' Process to Insure Low Noise Characteristic
- * Current Limiting for Short-Circuit Protection
- * Built in Thermal Shut-down Circuit
- * Built in Surge Voltage Protection Circuit

The NJM4558/4559 integrated circuit are a dual high-gain operational amplifier internally compensated and constru -cted on a single silicon chip using an advanced epitaxial process.

Combining the features of the NJM741 with the close parameter matching and tracking of a dual device on a mono -lithic chip results in unique performance characteristics. Excellent channel separation allow the use of the dual device in single NJM741 operational amplifier applications providing density. It is especially well suited for applications in di -fferential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are ma -ndatory.

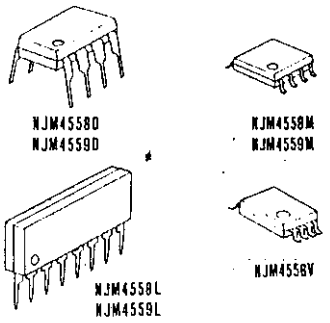
2

■ Absolute Maximum Ratings (Ta=25°C)

Supply Voltage	V^+/V^-	±18V
Differential Input Voltage	V_{ID}	±30V
Input Voltage (note)	V_I	±15V
Power Dissipation	P_D (D-Type)	500mW
	(M,V-Type)	300mW
	(L-Type)	800mw
Operating Temperature Range	T_{opr}	−20~+75°C
Storage Temperature Range	T_{stg}	−40~+125°C

(note) For supply voltage less than ±15V,the absolute maximum input voltage is equal to the supply voltage.

■ Package Outline

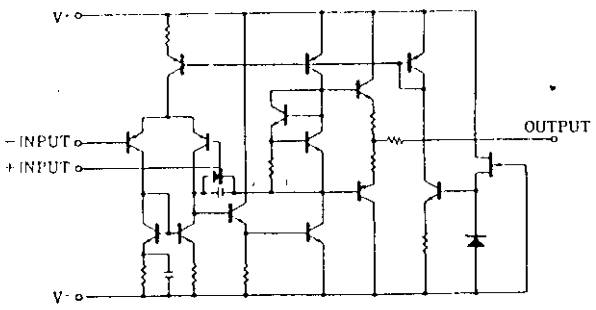


*S-Type(SIP-9)available

■ Electrical Characteristics (V^+/V^- = ±15V, Ta=25°C)

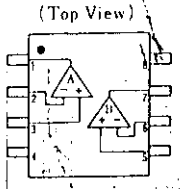
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 10k\Omega$	–	0.5	6	mV
Input Offset Current	I_{IO}		–	5	200	nA
Input Bias Current	I_B		–	25	500	nA
Input Resistance	R_{IN}		0.3	5	–	MΩ
Large Signal Voltage Gain	A_V	$R_L \geq 2k\Omega$, V_O = ±10V	86	100	–	dB
Maximum Output Voltage Swing 1	V_{OM1}	$R_L \geq 10k\Omega$	±12	±14	–	V
Maximum Output Voltage Swing 2	V_{OM2}	$R_L \geq 2\Omega$	±10	±13	–	V
Input Common Mode Voltage Range	V_{ICM}		±12	14	–	V
Common Mode Rejection Ratio	CMR	$R_S \leq 10k\Omega$	70	90	–	dB
Supply Voltage Rejection Ratio	SVR	$R_S \leq 10k\Omega$	76.5	90	–	dB
Supply Current	I_{CC}		–	3.5	5.7	mA
Slew Rate						
NJM4558	SR		–	1	–	V/μS
JM4559	SR		–	2	–	V/μS
Equivalent Input Noise Voltage	V_{NI}	RIAA, R_S = 1kΩ, 30kHz LPF	–	1.4	–	μVrms
Unity Gain Bandwidth	GB					
NJM4558				3		MHz
NJM4559				6		MHz

■ Equivalent Circuit (½ Shown)



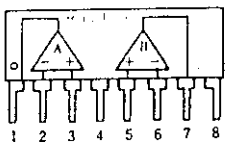
■ Connection Diagram

D,M,V-Type
(Top View)



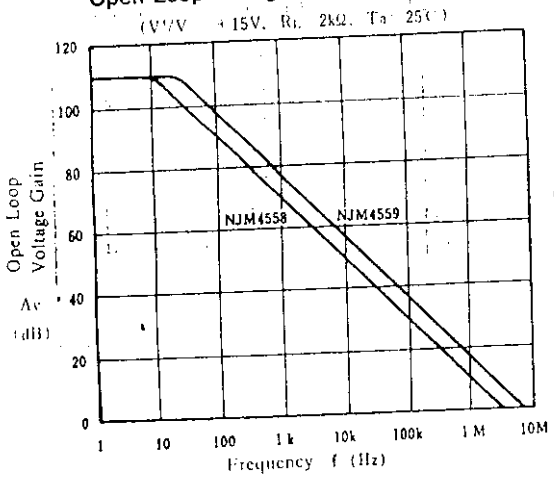
PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V−
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V+

L-Type

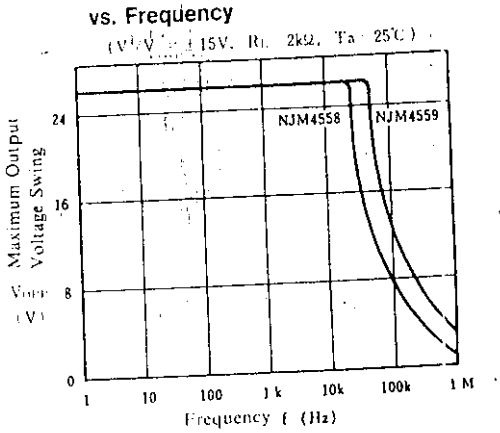


■ Typical Characteristics

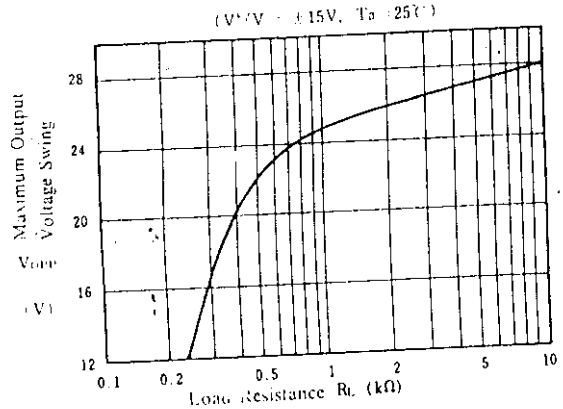
Open Loop Voltage Gain vs. Frequency



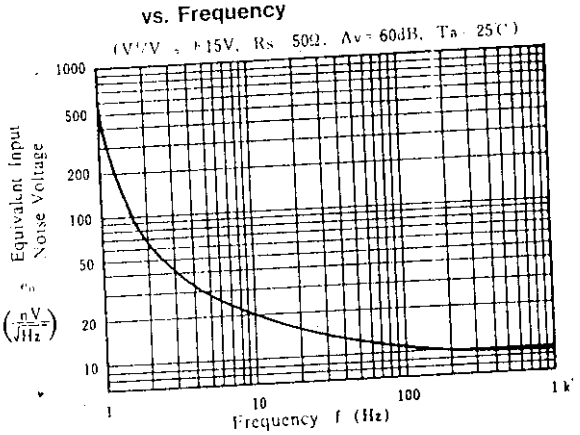
Maximum Output Voltage Swing vs. Frequency



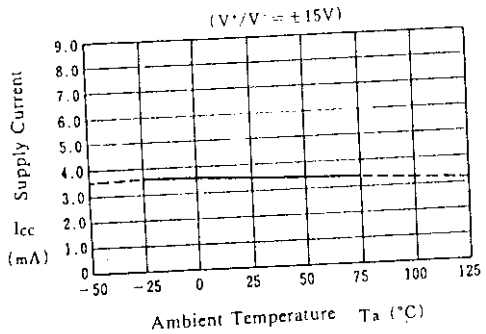
Maximum Output Voltage Swing vs. Load Resistance



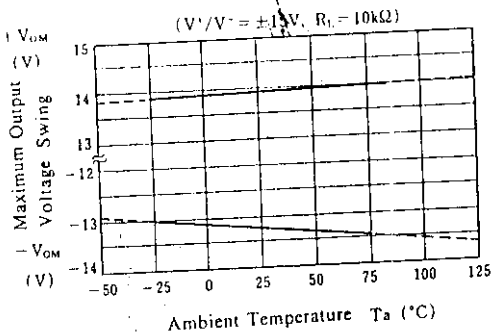
Equivalent Input Noise Voltage vs. Frequency



Supply Current vs. Temperature



Maximum Output Voltage Swing vs. Temperature



納入仕様書

ご承認欄

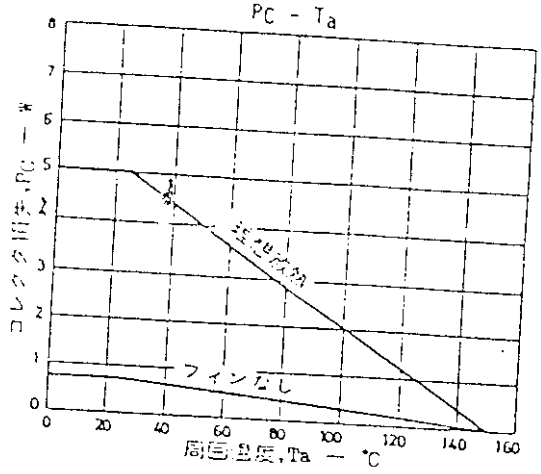
朱書訂正をもって承認とする

初制機種	共通
部品名	TRANSISTOR
部品番号	ST2C2314-D,E,F

承認		
T.E.JAPAN技術部		
承認	検討	担当
技術		技術
9.12.'84		'84.9.11
茂木		田口

ST2-1502 / TR-042 初制

1980年7月1日発行の承認図は廃棄とする。



発行 東京三洋電機株式会社
半導体事業部
群馬県邑楽郡大泉町坂田180 ☎0276(63)2111大代表

担当

技術業務課

納入仕様書

サンヨー・エレクトロニクス・ジャパン株式会社 殿　製品名　2SC2314

仕様書No. ST954J-A
発行日84年 8月30日
前回仕様書No.
前回発行日　　年　　月　　日

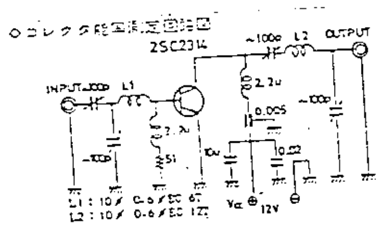
※この納入仕様書の有効期間は発行日より（本仕様書3年間、暫定仕様書3ケ月、仮仕様書1ケ月）とさせていただきます。
また、ご返却のない場合は、ご承認されたものとして処理させていただきます。

1. 構　造：シリコン NPN エピタキシャルプレーナ型トランジスタ
2. 外　形：JEDEC:TO-126
3. 絶対最大定格（Ta＝25℃）
   - V_{CBO}：75V
   - V_{CEO}：45V
   - V_{EBO}：5V
   - I_C：1A
   - i_{CP}：1.5A
   - P_C (Ta=25℃)：750mW
   - P_C (Tc=25℃)：5W
   - Tj：150℃
   - Tstg：−55～+150℃
   - V_{CER} (R_{BE}=150Ω)：75V
   - 動作温度範囲　−30～+60℃

4. 電気的特性（Ta＝25℃）

記号	条件		最小値	標準値	最大値	単位
I_{CBO}	V_{CB}=40V, I_E=0				1.0	μA
I_{EBO}	V_{EB}=4V, I_C=0				1.0	μA
$V_{CE(sat)}$	I_C=500mA, I_B=50mA			0.2	0.6	V
$V_{BE(sat)}$	I_C=500mA, I_B=50mA			0.9	1.2	V
f_T	V_{CE}=10V, I_C=50mA		180	250		MHz
Cob	V_{CB}=10V, f=1MHz			15	25	pF
hFE	V_{CE}=5V, I_C=500mA	D	60		120	
	〃	E	100		200	
	〃	F	160		320	
$V_{(BR)CBO}$	I_C=10μA, I_E=0		75			V
$V_{(BR)CER}$	I_C=1mA, R_{BE}=150Ω		75			V
$V_{(BR)CEO}$	I_C=1mA, R_{BE}=∞		45			V
$V_{(BR)EBO}$	I_E=10μA, I_C=0		5			V
Po	V_{CC}=12V, f=27MHz, PIN=35mW		1.0	1.8		W
ηc	指定測定回路参照		60			%

○コレクタ効率測定回路図



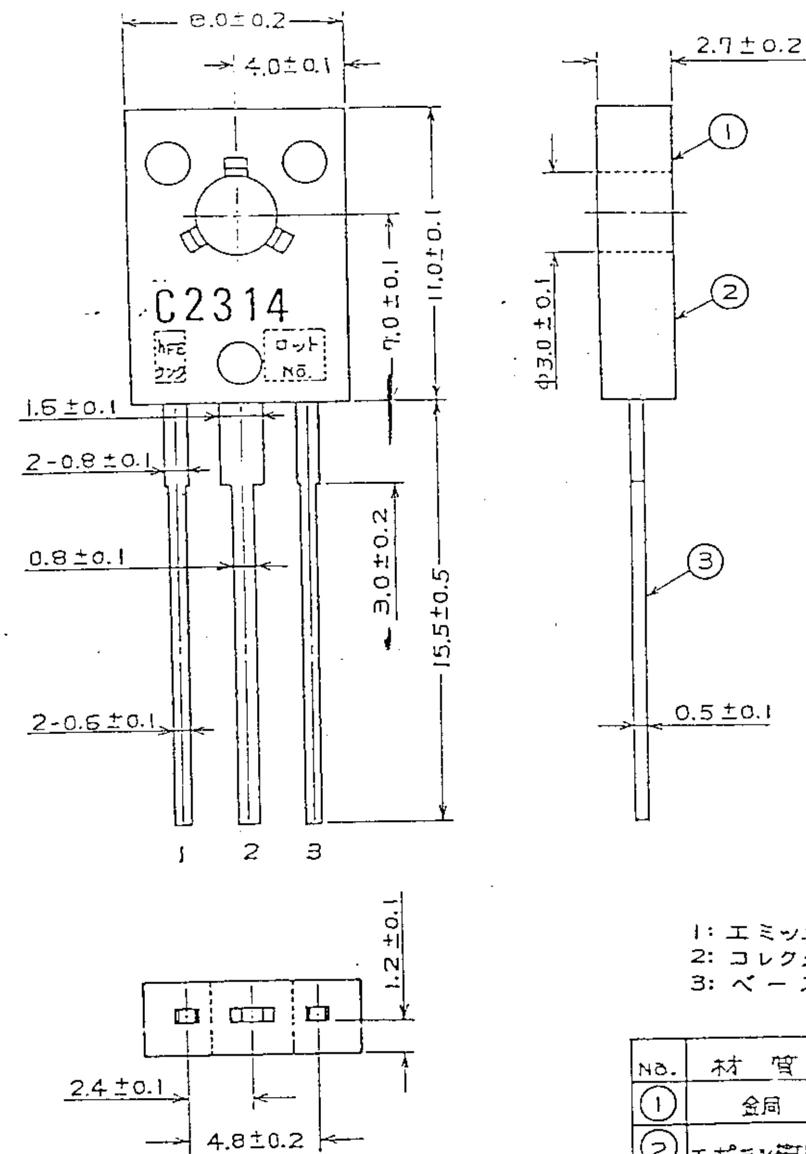
承認	査閲	作成

(8-2711)

SANYO／東京三洋電機株式会社　半導体事業部　C0014

No. 1

外形寸法図



1: エミッタ
2: コレクタ
3: ベース

No.	材質	表
①	金属	
②	エポキシ樹脂	
③	金属	

(注) 図面上に現われない樹脂バリが付着する場合もあります。

作成	M. NOTAKA	作成日	'80年5月9日	機種名	2SC2314	図番	
承認	'80.5.9	承認		外形	EIAJ / JEDEC TO-126 / SANYO TO-126	製造No	—

SANYO　東京三洋電機株式会社 半導体事業部

Tandy Electronics
A Division of Tandy Corporation
200 Taylor Street • Suite 700 • Fort Worth, TX 76102 • Telephone (817) 339-0100 • Fax (817) 878-6669

July 15, 1998

Mr. Bill Inglis
Federal Communications Commission
Equipment Authorization Division
7435 Oakland Mills Road
Columbia, Maryland 21046

Dear Mr. Inglis:

Included in this package is the requested information regarding specification sheets for the PLL and a description of how the Tandy CB Radios protect against out-of-band operation. Also included is the synthesizer block diagram and an explanation of the operation for the circuitry it represents.

This documentation covers the following Tandy CB Radio products:

RadioShack Cat #	FCC Identifier	FCC Ref #
21-1702	AAO21-1702	681
21-1703	AAO21-1703	681
21-1704	AAO21-1704	681

Please do not hesitate to contact myself, Dwayne Campbell, or Linda Dickerson if we may provide additional information or any assistance.

Best regards,

Mike Lonergan, Sr. Manager
Tandy Electronics
Ph: 817-415-4832
Fx: 817-415-2729

cc: Dwayne Campbell
Linda Dickerson

2/21

Tandy Electronics (China) Limited
TEL : 86-0752-2261383 FAX : 86-0752-2261798

July.15.98

To: Federal Communications Commission
1919 M Street NW Washington, DC 20554-1300

Attn:

Subj: 21-1704 FCC

In our circuit, we are using the scan up or scan down controls by preprogrammed PLL control IC and the internal "divide by" of the PLL may prevent out of band operation. So, user may not easily to change the design to operate the band other than CB channel.
Thanks you for your attention to this issue and your prompt to release of FCC grant is very much appreciated.

Best Regards,

David Fu
R&D Director

CC: MRL— TED / Peter Chiang— TRS

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THEORY OF OPERATION

GENERAL

The TRC-504 is a 40-channel, crystal controlled mobile transceiver which consists of a PLL-synthesizer circuit, a receiver circuit, a transmitter circuit. Power is supplied by a car battery (13.8 VDC). Refer to the Block and Schematic Diagrams as you read the following descriptions.

PLL SYNTHESIZER

The TRC-504 uses a Phase-Locked- Loop (PLL) circuit to synthesize local-oscillator frequencies for receiving and transmitting. It employs one IC and only one crystal. IC1 is a CMOS LSI circuit containing a reference oscillator, phase detector, reference divider (1/4096) and a programmable divider.

The programmable divider directly divides the output of the VCO (voltage-controlled oscillator) circuit down to a 2.5 kHz signal. The VCO circuit consists of D15, Q18 and T6. crystal X1 provides reliable frequency standard which controls the local-oscillator frequency divider inside IC1 counts down the oscillator signal to 1/4096 (2.5 kHz) and passes it on to the phase detector, where it is compared with the 2.5 kHz signal from the programmable divider. An error voltage is generated by th phase detector which is proportional to the phase difference between the two 2.5 kHz signals.

This error voltage from pin 27 of IC1 appears at the capacity collectors of Q15 and Q16 (active low pass filter circuit), where the error voltage is integrated and harmonics and noise are filtered out. The resulting DC voltage is applied to the varicap diode D15. Its capacity varies with the applied DC voltage. Because of this capacity change, the output frequency of the VCO circuit is circuit is corrected. With proper circuit design and precise adjustments, the VCO frquency is accurate and precise when the system I "locked".

This means that the phase detector senses no phase differences between the two 2.5 kHz signals, and the VCO circuit generates a frequency that is as accurate and stable as the reference crystal oscillator X1.

The VCO circuit is in the form of a Hartley oscillator and the varicap diode D15 and T6 constitute the tank circuit. The VCO circuit generates a signal ranging from 13.4625 to 16.710 Mhz. IC1 also includes an unlock-signal-detector circuit. When the phase is unlocked (when th phase detector senses a phase difference between the two 2.5 kHz signals), the output at pin 18 of IC1, which is normally open, will be shorted to ground. This means that VCO frequency (1/2 carrier for transmitting) is "sunk" to pin 18 of IC1 and the transmitter circuits are inhibited.

TRANSMITTER CIRCUIT

RF Amplification

The output of doubler amp Q21 is fed through doubler tuning (27 Mhz) T7 and T8 to the base of RF amp Q27. The output is then supplied through tuning circuit T9 to RF driver amp Q28. The Q28 output capacitance is divided by tuning circuit L7, C103, and C104 and passed through tuning circuit L8 to the base of final RF amp stage Q29. The Q29 output is supplied to the antenna through L13.

Suppression of Spurious Radiation

The tuning circuit (between frequency synthesizer and final amp Q29) and 3-stage "PI" network (C107, C11, C108, L12, C2, L13 and C1) serve to suppress spurious radiation. The network serves to match Q29 impedance to the antenna and to reduce spurious content to acceptable levels. In-band spurious is reduced to acceptable levels by filtering.

Limiting Power

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During factory alignment, the series base resistor (R114) of final amp Q29 is selected to limit the available power.

Modulation
The mic input is fed to mic amp Q25 and then to modulator IC3 which feeds the signal to the modulation transformer T5. The signal is stepped up at T5 and modulated by the B + voltage. Then it is fed through diode D13 to the collectors of Q28 and Q29 to modulate both these stages.

Limiting Modulation
A portion of the modulating voltages is rectified by Q23 to turn on Q24, which attenuates the mic input to mic amp Q25. The resulting feedback loop keeps the modulation from exceeding 100 percent for inputs approximately 40 dB greater than required to produce 50 percent modulation. The attack time is about 18 msec and the release time is about 300 msec.

RECEIVER CIRCUIT

Receiver
The receiver is a double conversion superhetrodyne with the first IF at 10.695 MHz and the second IF at 455 kHz. The synthesizer supplies the first local oscillator frequency (10.695 MHz below the receiver frequency) and the second local oscillator frequency (10.240 Mhz). The detector (Q7) output provides reverse AGC to all previous stages except Q6. The AGC voltage is also amplified by Q7 and used to drive RF attenuator Q30. Squelch amp and audio amp are included in IC2. IC3 functions as a speaker driver in receiving.

INDICATORS

Channel Indication
When the OUT/CH9/CH19 switch is set to OUT, the channel can be selected by the channel selector SW1 or SW302/SW303, and indicated by the 2 digits/7 segments LED LD201. LD201 lights dynamically by the outputs from IC1. The output from pin 8 of IC1 controls the lighting of the first digit through Q14, and the output from pin 9 of IC1 controls the lighting of the second digit through q13. The outputs from pin 1 to pin 7 of IC1 control the lighting of each segment of each digit.

Ch9/ch19/PA Indication
When the OUT/CH9/CH19 switch is set to CH9(CH19), LD201 flashes and displays "9" ("19").
When the CB/PA/MON switch is set to PA, LD201 displays "PA".
When the CB/PA/MON switch is set to MON and PTT switch is push in , LD201 displays "PA".

RX/TX Indication
LD202 (green) functions as a RX indicator during receiving and LD203 (red) functions as a TX indicator during transmission.

Back Light Indicator
LD204-LD211 functions as back light indicator.

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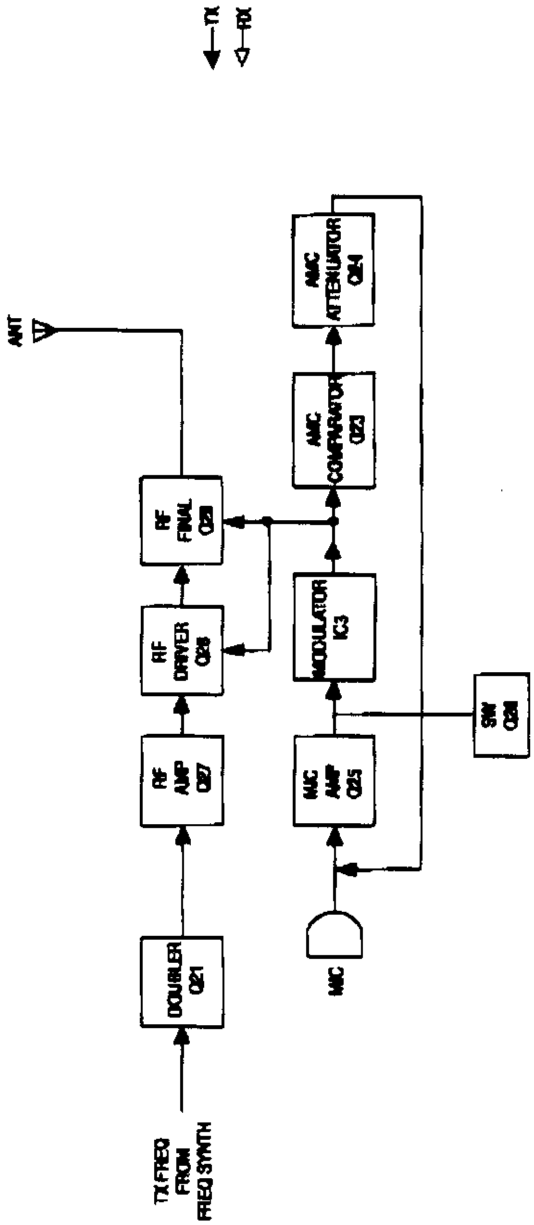
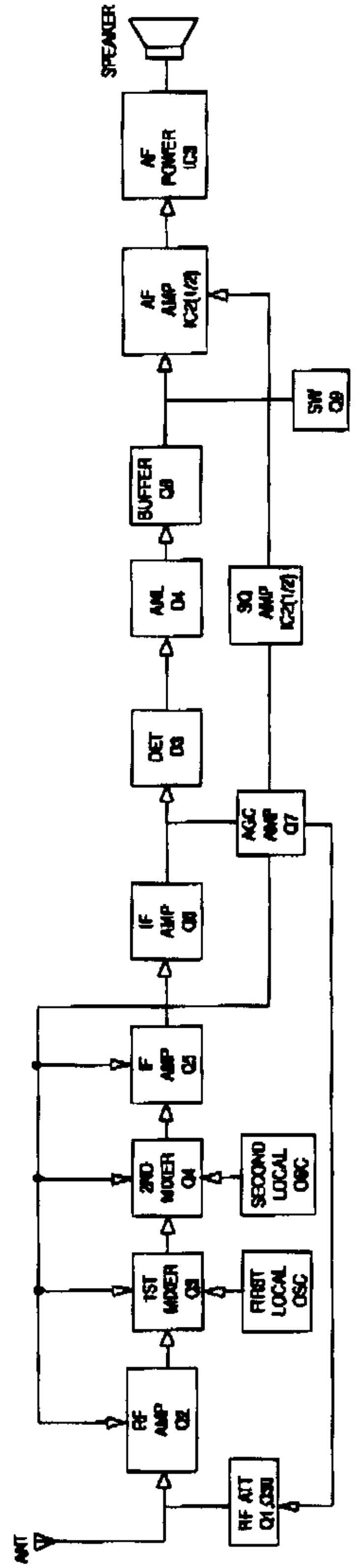
TRANSMITTER



RECEIVER



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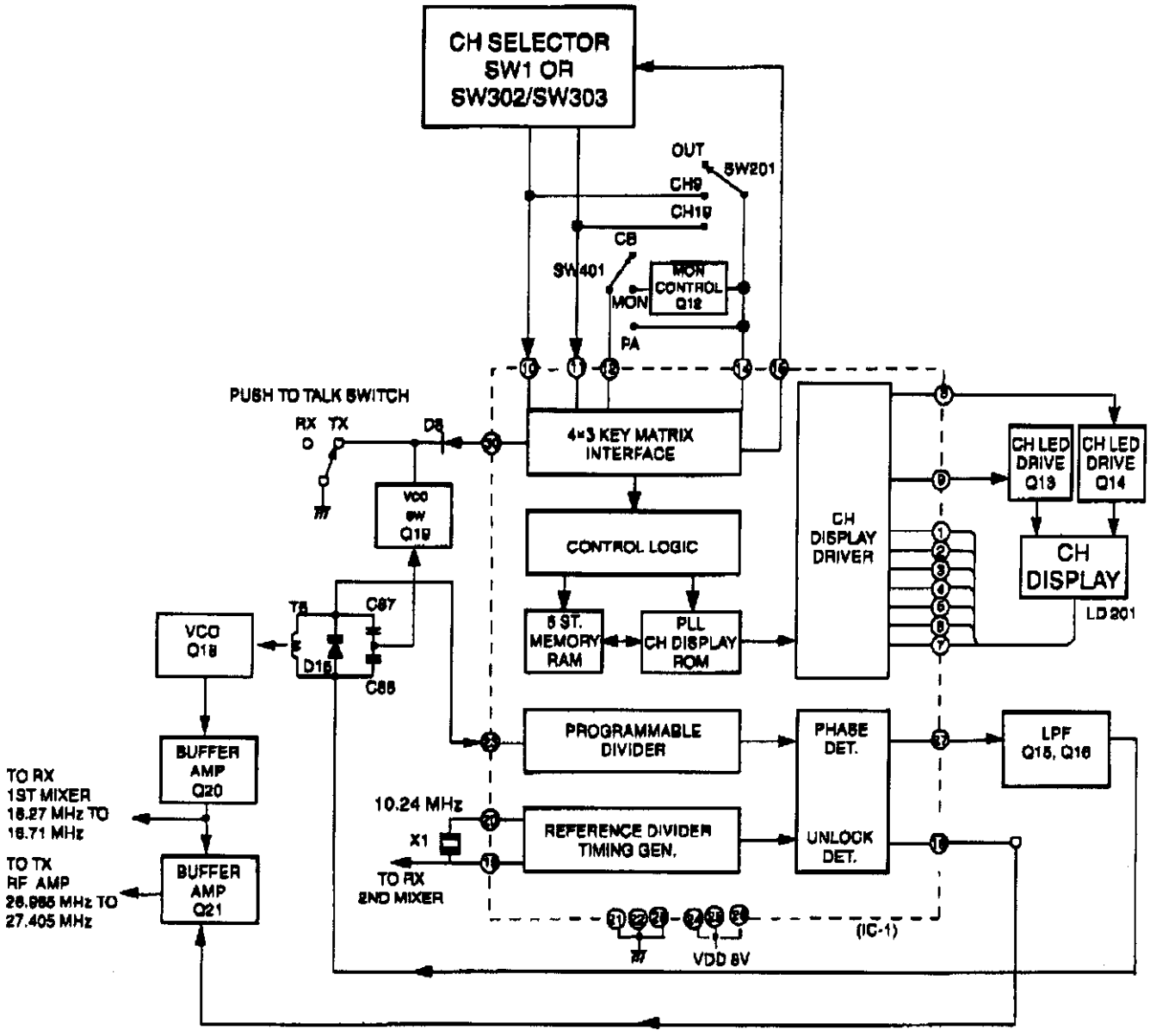
BLOCK DIAGAMS

FREQUENCY SYNTHESIZER



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LC7185-8750

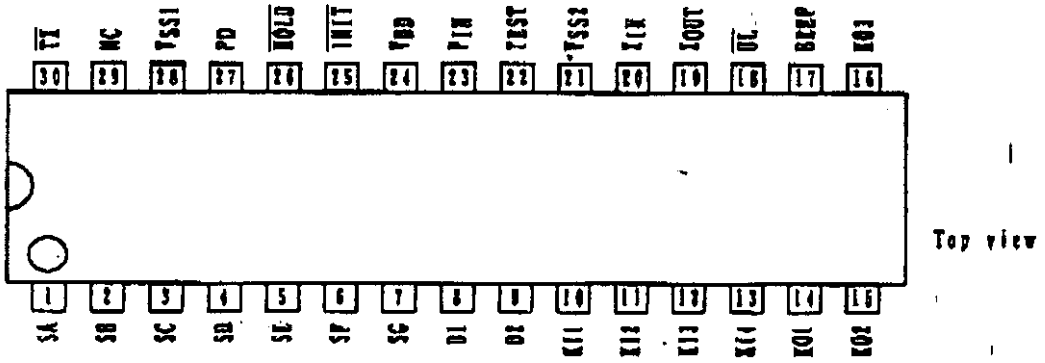
1. Case Outline : DIP-30S(400mil) Plastic Package

2. Function · Application : This 27MHz Band. PLL Frequency Synthesizer LSI Chip is Designed Specifically for CB Transceivers.

3. Absolute Maximum Ratings at Ta=25℃, V_{SS}=0V

Item	Symbol	Condition	Rated level	Unit
Maximum power supply voltage	VDD max	Pin VDD	−0.3 to +9.0	V
Input voltage	VIN(1)max	Pins $\overline{HOLD}$, $\overline{TX}$	−0.3 to +15	V
	VIN(2)max	Input pins other than VIN(1)max	−0.3 to VDD+0.3	
Output voltage	VO(1)max	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	−0.3 to +15	V
	VO(2)max	Pins $\overline{UL}$, BEEP	−0.3 to +15	
	VO(3)max	Pin PD	−0.3 to VDD+0.3	
	VO(4)max	Output pins other than mentioned above	−0.3 to VDD+0.3	
Output current	IO(1)max	SA, SB, SC, SD, SE, SF, SG	0 to 30	mA
	IO(2)max	Pins D1, D2	0 to 10	
	IO(3)max	Pin $\overline{UL}$	0 to 20	
	IO(4)max	Pin BEEP	0 to 10	
Allowable power dissipation	Pd max	Ta≤85℃	350	mW
Operating temperature	Topg		−40 to +85	℃
Storage temperature	Tstg		−55~+125	℃

Pin Assignment



Top view

4. Allowable Operating Range at Ta=-40 to +85℃, V_{SS}=0V

Item	Symbol	Condition	min	typ	max	Unit
Power supply voltage	VDD		5.0		8.0	V
Input "H" level voltage	VIH(1)	Pins $\overline{HOLD}$, $\overline{TX}$	0.7VDD		12	V
	VIH(2)	Pin $\overline{INIT}$	3.2		VDD	
	VIH(3)	Pins KI1, KI2, KI3, KI4	0.6VDD		VDD	
Input "L" level voltage	VIL(1)	Pins $\overline{HOLD}$, $\overline{TX}$	0		0.3VDD	V
	VIL(2)	Pin INIT	0		1.3	
	VIL(3)	Pins KI1, KI2, KI3, KI4	0		0.4VDD	
Output voltage	VOUT(1)	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	0		13	V
	VOUT(2)	Pins $\overline{UL}$, BEEP	0		8	
Input frequency	f IN(1)	Pin XIN (Sine wave, capacitor coupled)	1.0	10.24	15	MHz
	f IN(2)	Pin PIN (Sine wave, capacitor coupled)	10		30	
Input amplitude	VIN(1)	Pin XIN (Sine wave, capacitor coupled)	0.5		1.5	Vrms
	VIN(2)	Pin PIN (Sine wave, capacitor coupled)	0.15		1.5	
Required oscillating frequency	X'tal	Pins XIN, XOUT (CI≦50Ω)	5.0	10.24	15	MHz

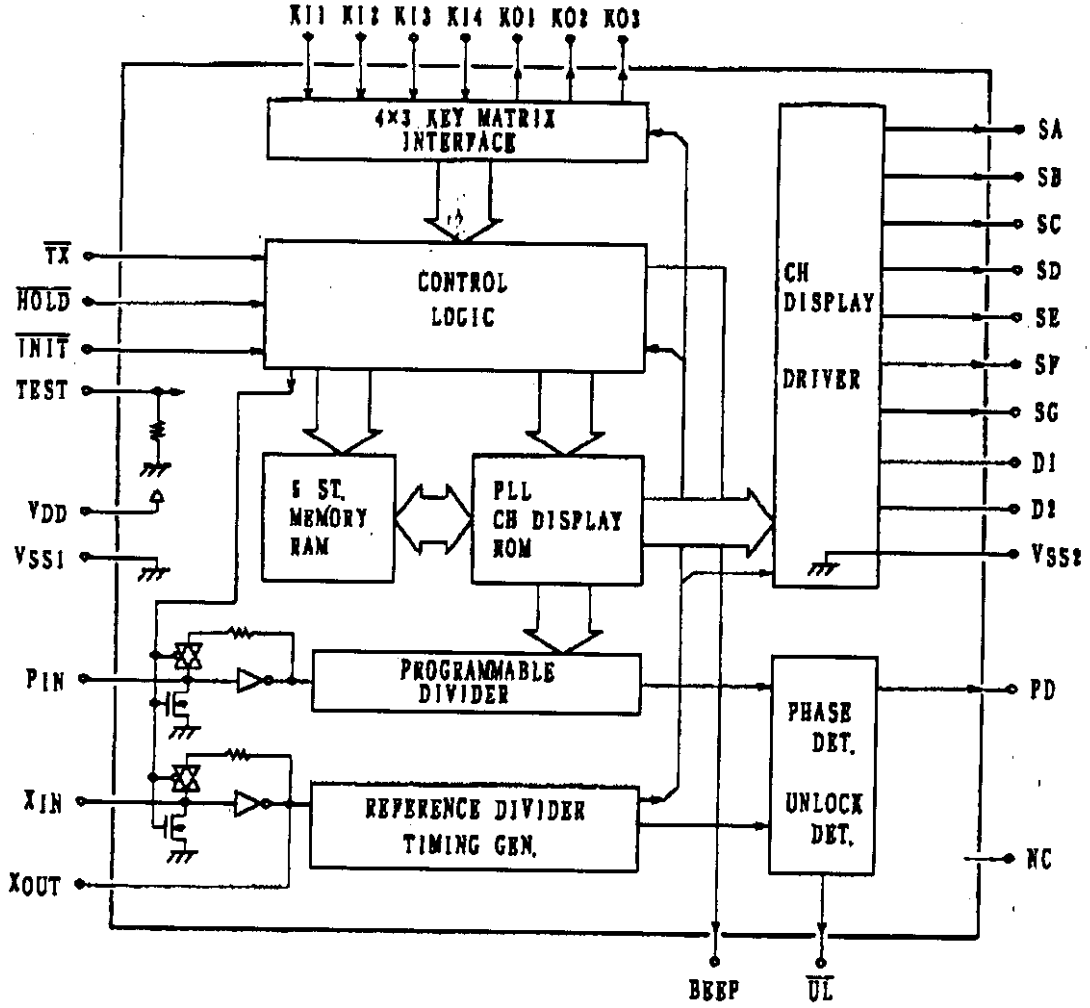
5. Electrical Characteristics at Ta=-40 to +85℃, V_{SS}=0V

Item	Symbol	Condition	min	typ	max	Unit
Internal feedback resistance	Rf(1)	Pin XIN		1.0		MΩ
	Rf(2)	Pin PIN		500		kΩ
Pull-down resistor	Rpdn	Pins KI1, KI2, KI3, KI4, TEST	30	50	70	kΩ
Input "H" level current	IIH(1)	Pins $\overline{HOLD}$, $\overline{TX}$, VI=12V			5.0	μA
	IIH(2)	Pin $\overline{INIT}$, VI=VDD			5.0	
	IIH(3)	Pin XIN, VI=VDD			25	
	IIH(4)	Pin PIN, VI=VDD			50	
Input "L" level current	IIL(1)	Pins $\overline{HOLD}$, TX, VI=VSS			5.0	μA
	IIL(2)	Pin $\overline{INIT}$, VI=VSS			5.0	
	IIL(3)	Pin XIN, VI=VSS			25	
	IIL(4)	Pin PIN, VI=VSS			50	
Output "H" level voltage	VOH(1)	Pins KO1, KO2, KO3, IO=1mA	VDD-2.0	VDD-1.0	VDD-0.5	V
	VOH(2)	Pin PD, IO=0.5mA	VDD-1.0			

Item	Symbol	Condition	min	typ	max	Unit
Output "H" level voltage	VOL(1)	Pins KO1, KO2, KO3, IO=20μA	0.6	1.0	1.4	V
	VOL(2)	Pin PD, IO=0.5mA			1.0	
	VOL(3)	Pin BEEP, IO=2mA			1.0	
	VOL(4)	Pins SA, SB, SC, SD, SE, SF, SG, IO=20mA			1.0	
	VOL(5)	Pins D1, D2, IO=5mA			1.0	
	VOL(6)	Pin $\overline{UL}$, IO=10mA			1.0	
Output off-leak current	IOFF(1)	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2, VO=13V			5.0	μA
	IOFF(2)	Pins $\overline{UL}$, BEEP, VO=8V			5.0	μA
"H" level tristate off-leak current	IOFFH	Pin PD, VO=VDD		0.01	10.0	nA
"H" level tristate off-leak current	IOFFL	Pin PD, VO=VSS		0.01	10.0	nA
Power supply voltage	IDD(1)	Normal mode, (PLL operates) fIN(2)=20MHz (PIN), VIN(2)=0.15Vrms, X'tal=10.240MHz, $\overline{TX}$=$\overline{HOLD}$=$\overline{INIT}$=VDD, Other inputs=VSS, Other outputs=OPEN		5	10	mA
	IDD(2)	Hold mode, VDD=3.0V			5	μA
		(memory backup), VDD=8.0V, $\overline{HOLD}$=VSS, $\overline{TX}$=$\overline{INIT}$=VDD, Other inputs=VSS, Other outputs=OPEN			15	

*Be careful thet the dielectric strength of pins SA, SB, SC, SD, SE, SF, D1, D2, $\overline{UL}$, BEEP are weak.

Block Diagram



Pin descriptions

$\overline{TX}$: Transmit/receive select

$\overline{HOLD}$: Hold mode select

$\overline{INIT}$: Initial input

TEST : Test point(input)

VDD, VSS1, VSS2 : Power supply

PIN : Programmable divider input

XIN, XOUT : X'tal OSC (10.240MHz)

$\overline{UL}$: Unlock detected output

PD : Charge pump output

NC : NC pin

SA to SG : Segment drivers (CH for display)

D1, D2 : Digit output (CH for display)

KI1 to 4 : Key inputs

KO1 to 3 : Key scan outputs

BEEP : Beep-tone control output

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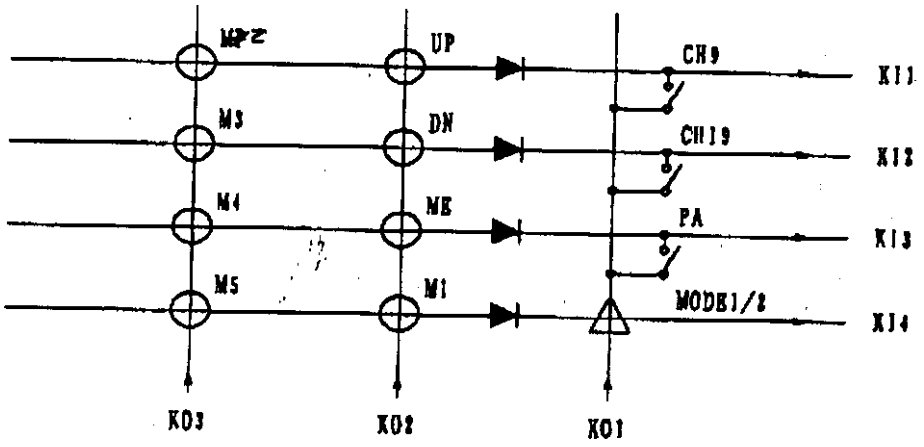
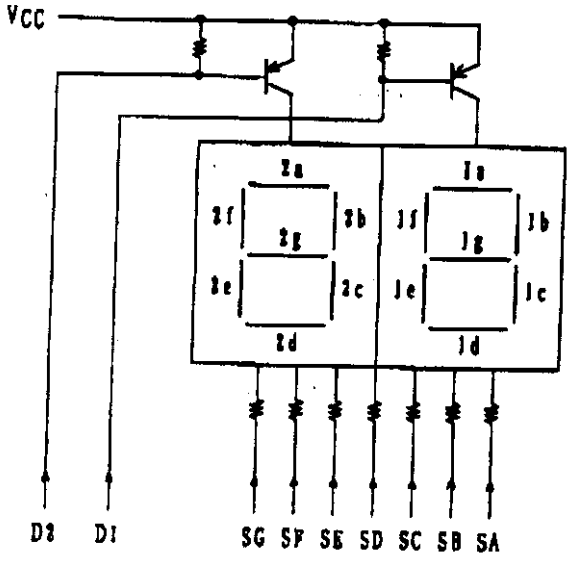
6. KEY MATRIX

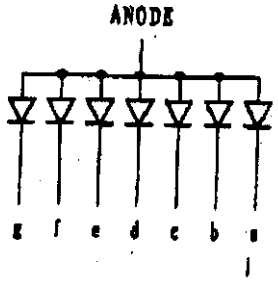


CH9 : Emergency CH9 recall
CH19 : Emergency CH19 recall
PA : Public announcement display
MODE1/2 : Display Mode
UP : CH up/scan
DN : CH down/scan

ME : Station Memory Enable
M1 to M5 : Station Memory recall
UP/DN/ME/M1 to M5 : Momentary SW
CH9/CH19/PA : Slide SW
MODE1/2 : Diode

7. LED (COMMON ANODE/7 Segment)





	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

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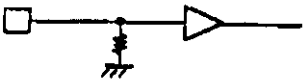
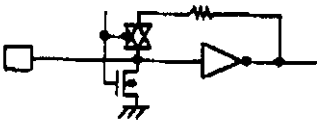
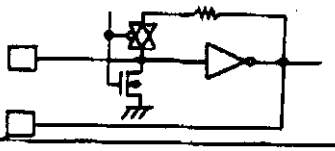
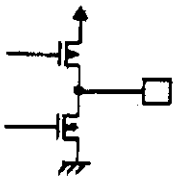
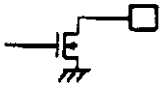
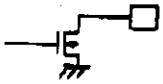
LC7185-8750

8. Pin description

Pin name	Pin No.	Type	Description
$\overline{TX}$	30		· Transmit/receive select $\overline{TX}$="0"·····transmit, TX="1"·····receive
$\overline{HOLD}$	26		· Hold mode select $\overline{HOLD}$="0"·····Hold mode select ="1"·····Normal mode select
$\overline{INIT}$	25		· Initial reset $\overline{INIT}$="0"·····Initial reset
TEST	22		· LSI testing terminal Used in VSS or open.
VDD	24		· Power supply(+) Normal mode : 5.0V to 8.0V Hold mode : ≧3.2V
VSS2	21		· Channel display LED driver ground
PIN	23		· Programmable driver input 150mVrms min Hold mode : Programmable diviver is disabled.
XIN XOUT	20 19		· Crystal oscillator X'tal : 10.24MHz connection Hold mode : oscillator is disabled.
PD	27		· Charge the pump output of the phase comparator. When the signal (fV)that has divided the PIN terminal output at N has a higher frequency than the reference signal (fR), or when the phase of fV exceeds that of fR, a negative pulse will be output. When the two phases match each other, the result is high impedance. · fV> fR OR leading : Positive Pulses · fV< fR OR leading : Negative Pulses · fV= fR and Phase coincedence : High Impedance Hold mode : High impedance
VSS1	28		· PLL circuit and controller ground
NC	29		· No connection
$\overline{UL}$	18		· Unlock detected output Fixed to low level during unlock, change of channel, PA mode, or hold mode. OPEN : locked
BEEP	17		· Beep-tone control output During station memory operation During input/output to the emergency channel During a change of channel During initial reset When hold mode is resumed Fixed low level (scanning stop) Tr : OFF (during 5 ms) →OPEN

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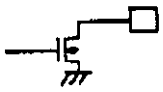
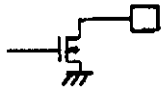
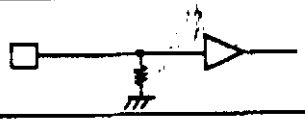
LC7185-8750

Pin name	Pin No.	Type	Description
SA to SG	1 to 7		· Segment drivers for the display (COMMON ANODE/7Segment)
D1 D2	8 9		· Digit output (150H z) for the display (COMMON ANODE/7 Segment) Hold mode : Trgoes off.
KI1 to KI4	10 to 13		· Key inputs Input from the key matrix
KO1 ? KO3	14 to 16		· Key scan output(75H z) Output to the key matrix Hold mode : fixed to low level (scanning stop)

9. Operation

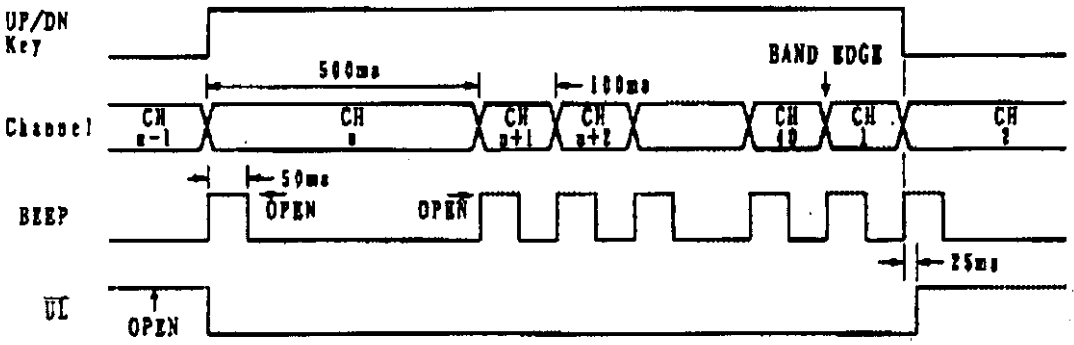
(1) Channel up/down

1. Manual up/down
Pressing the UP key increments by one channel and pressing the DN key decrements by channel. When the upper (lower) bent edge is reached, it returns to the lower (upper) bent edge.

2. Auto up/down (auto scanning)
Holding the UP (or DN) key down for 500msec or longer starts auto scanning. For both up and down scanning, each channel takes 100msec to scan.

3. The unlock detected line ($\overline{UL}$) is asserted (low) when the up (or DN) key is pressed and deactivated 25msec after the key is released (see diagram below)

4. The beep-tone control line (BEEP) is asserted (open) for 50msec after each new channel is selected (see diagram below).



(2) Selecting an emergency channel (CH9/CH19)

1. When the CH9 to CH19 switch is turned ON, a beep tone control signal is output (50 milliseconds) while the preceding channels are being stored in the memory.

2. While the CH9 or CH19 switch is turned ON, operation is impossible even if a UP/DN, ME, or M1 to M5 key other than $\overline{TX}$ or PA switch is pressed.

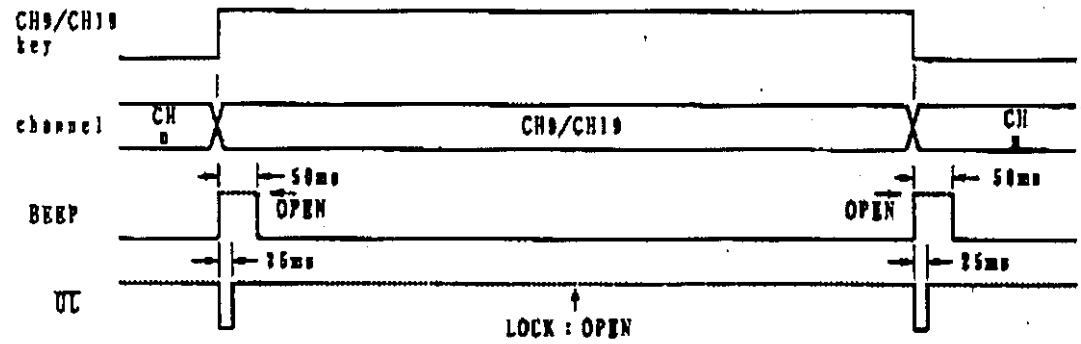
3. When the CH9 or CH19 is turned OFF during CH9 or CH19 transmission, the emergency channel is maintained until reception is made possible.

4. When the CH9 to CH19 switch is turned OFF, the preceding channels are resumed while a beep tone control signal is output (50 milliseconds).

5. CH9 has higher priority to CH19 (i.e. if CH9 and CH19 are turned ON simultaneously, only CH19 is ON).

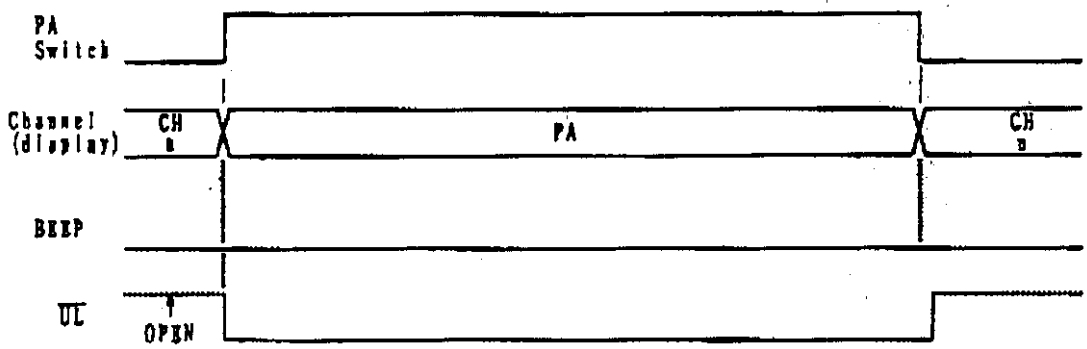
6. The unlock detection signal is output at low level over 25 milliseconds every time the CH9 or CH19 switch is turned ON/OFF.

7. The channel display "9" or "19" blinks.



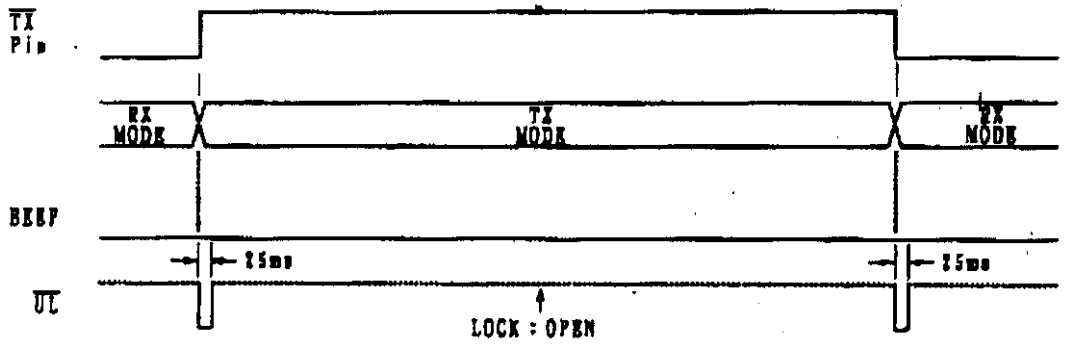
(3) Public Announcement (PA) Mode

1. Tuning ON the PA switch enters PA mode while the preceding channels are stored in the memeory (see below).
2. When the PA switch is turned ON, operation is imposaible even if one of the switches or keys ($\overline{TX}$, CH9/CH19, UP/DN, ME, or M1 to M5) is pressed.
3. Causes "PA" to be displayed
4. Turning OFF the PA enters CH mode and returns to the preceding channels.
5. The unlock detection signal is output at low level while the PA switch is turned ON.



(4) Transmit/Receive selection

1. Setting the $\overline{TX}$ terminal to LOW level enters TX mode.
2. Turning ON the PA switch in TX mode enters PA mode. If one of the switches (UP/DN, ME, M1 to M5, CH9, or CH19) is pressed in TX mode, operation is impossible.
3. The unlock detection signal is output every time transmit/receive selection is switched.



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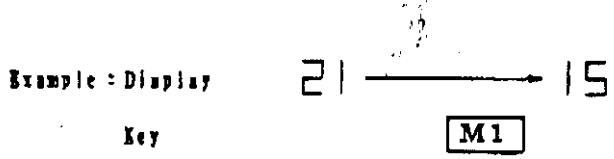
LC7185-8750

(5) Station memeory function

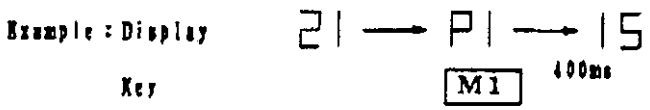
1. Five channels can be preset.
   - All the channels are set to CH33 during initial reset (i.e.when the initial power is supplied)

2. Memory read
   - Pressing one of the M1 to M5 keys permits the preset channels to be read.
   - Channel display can be selected according to the evidence of the key matrix diode.

MODE1 (Without diode)
Pressing one of the M1 to M5 keys displays the read channels.



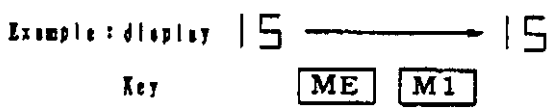
MODE2 (With diode)
When one of the M1 to M5 keys is pressed, the display "P1 to P5" appears during the subsequent 400 milliseconds, and then the read channels are displayed.



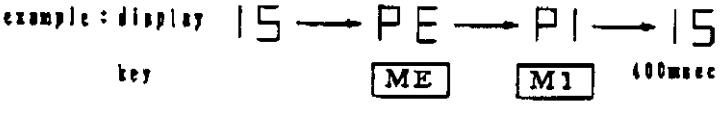
3. Memory write
   - When a desired key of the M1 to M5 keys is pressed after the ME key has been pressed, the currently received channels are written in the memory. The memory write enable status is released in one of the following cases:
     - When the memory write status is ON after one of the M1 to M5 keys has been pressed.
     - Emergency channels H9 or CH19 are currently selected.
     - During the transmission status
     - The PA switch is turned on
     - Hold mode

     If the above key operation is not performed, the memory write enable status is released automatically in 9 seconds.
   - Channel display can be selected as follows according to the evidence of the key matrix diode.

MODE1 (Without diode)
The currently received channel is displayed.



MODE2 (With diode)
When the ME keys is pressed, the "PE" lamp lights indicating memory write enable. When one of the M1 to M5 keys is pressed, the "P1" to "P5" is displays during the subsequent 400 milliseconds. The received channel display status is then resumed.



- If the M1 to M5 keys are pressed simultaneously, M1 has the highest priority. The priority is determined in advance in ascending order.

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(6) BEEP pin

Beep-tone control output

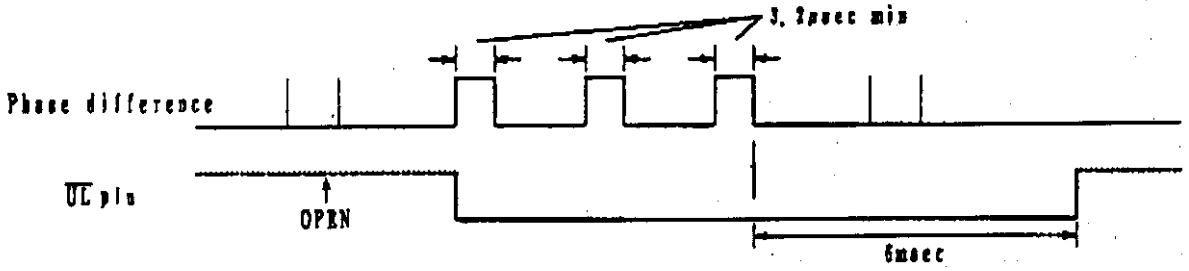
- A reset (e.g battery replacement) ($\overline{INIT}$= 0)
- Any key press associated with the channel memory
- Any emergency channel switch activation
- A new channel is selected
- Leaving hold mode

In one of the above cases, the channel is opened during 50 millisecond.

(7) $\overline{UL}$ pin

Unlock detected output

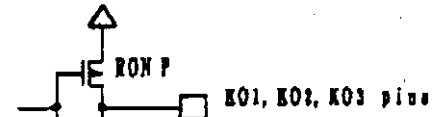
- The output is performed at the extended pulse width of 6 milliseconds if a differential phase of 3.2μ seconds or more of PLL is detected.



- A 25 millisecond pulse is output when opetation and transmit/receive switch are performed with a change of channel.
- While the PA switch is turned on.
- Open during PLL LOCK (differential phase of less than 3.2μ seconds).

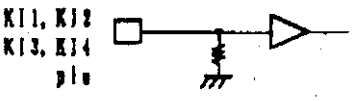
(8) Key matorix configulation

- It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines.
  But KO1, KO2, and KO3 lines need diodes.



RON P, RON N : on impedance

	MIN	TYP	MAX [kΩ]
RON P	0.5	1.0	2.0
RON N	30	50	70



RpdN	30	50	70

RpdN : pull-down resistor

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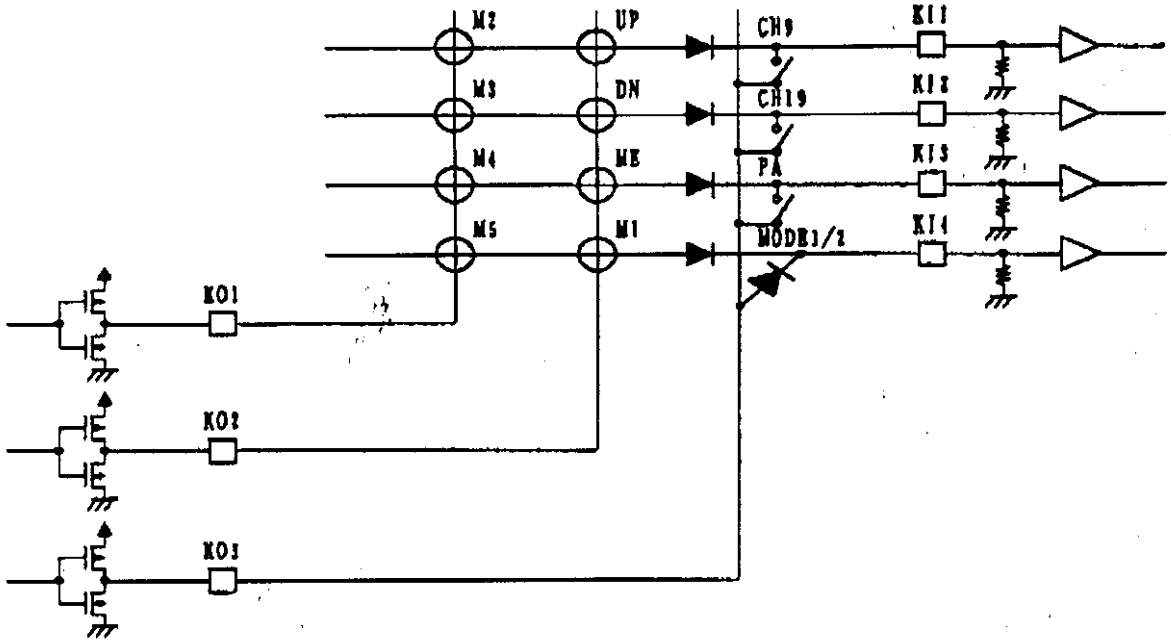


1 0. Description of Power ON/OFF and HOLD Mode

(1) Operation during HOLD mode

Operation other than initial reset of the $\overline{INIT}$ terminal is impossible during HOLD ($\overline{HOLD}$=0) mode. During this mode, the station memory is mainly maintained.

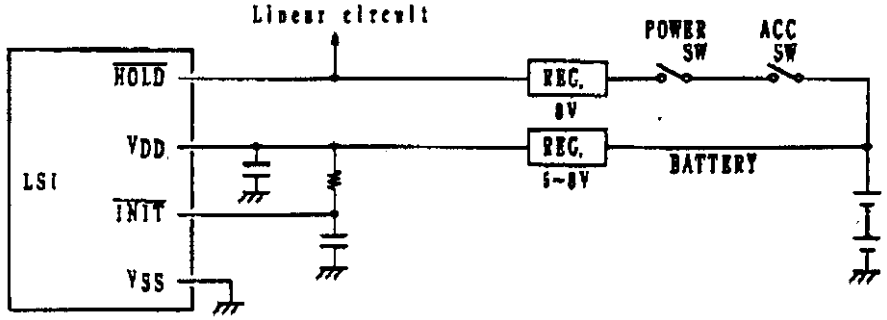
- The programmable divider and crystal oscillator circuit or the reference divider section are stopped. The PD terminal (charge pump output) becomes high impedance. The $\overline{UL}$ terminal becomes VSS.
- The channel display terminals D1 to D2 become high impedance.
- BEEP pin : VSS
- The key scan signal outputs (KO1 to KO3) become VSS. When the LC7185 leaves hold mode, the previously selected channel is reopened.

When the LC7185 leaves hold mode, the previously selected channel is reopened.

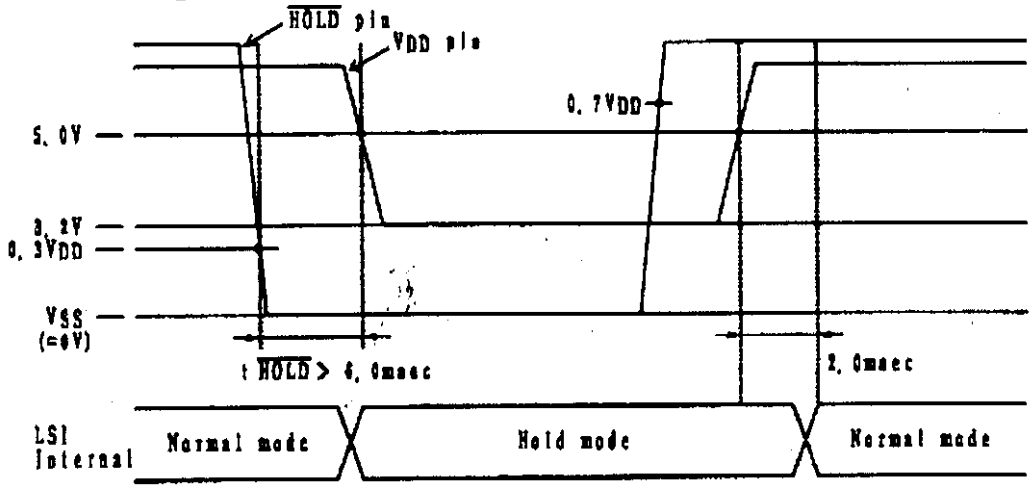
(2) Initial status setting

Initial reset is performed when $\overline{INIT}$ =0, such as in battery replacement. The initial status changed by initial reset.

- CH9 is selected.
- station memeory keys are all set to CH33.



(3) Hold mode timing

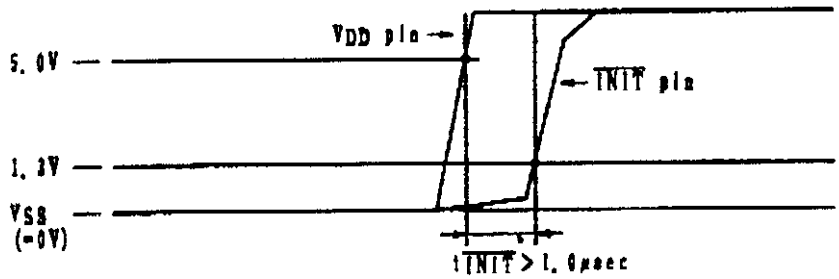


When $\overline{HOLD}$ terminal=0(<0.3VDD)or, during 6.0 subsequent milliseconds (t $\overline{HOLD}$), the VDD terminal must hold the crystal oscillator circuit and oscillation guarantee voltage (5.0V). Subsequenty, it can be reduced to the station memory hold voltage (>3.2V)

When $\overline{HOLD}$ mode is returned to NORMAL mode, timing of $\overline{HOLD}$ and VDD terminal is not limited. When the HOLD terminal is at a high level (>7.0 VDD) or when VDD terminal is at more than 5.0V within 2.0 milliseconds after the $\overline{HOLD}$ terminal has been at a high level, NORMAL mode is resumed within the subsequent 2.0 milliseconds.

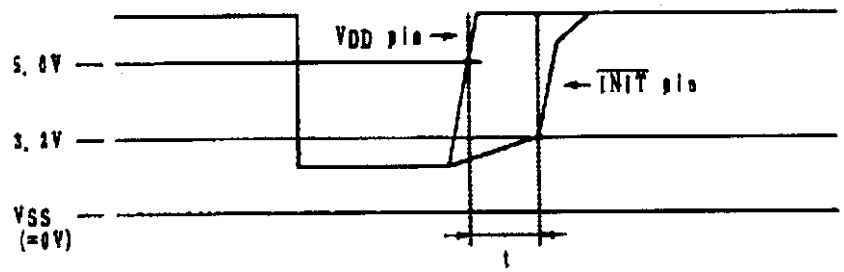
(4) Initial reset timing.

①Initial reset when the initial status is set, such as in battery replacement



Note : t $\overline{INIT}$ should be greater than 1.0 μsec

② Reset caused by a sudden voltage (VDD) drop



If VDD drops momentarily down to less than 3.0V and rises up to more than 5.0V (t >1.0μsec), a reset may be generated.

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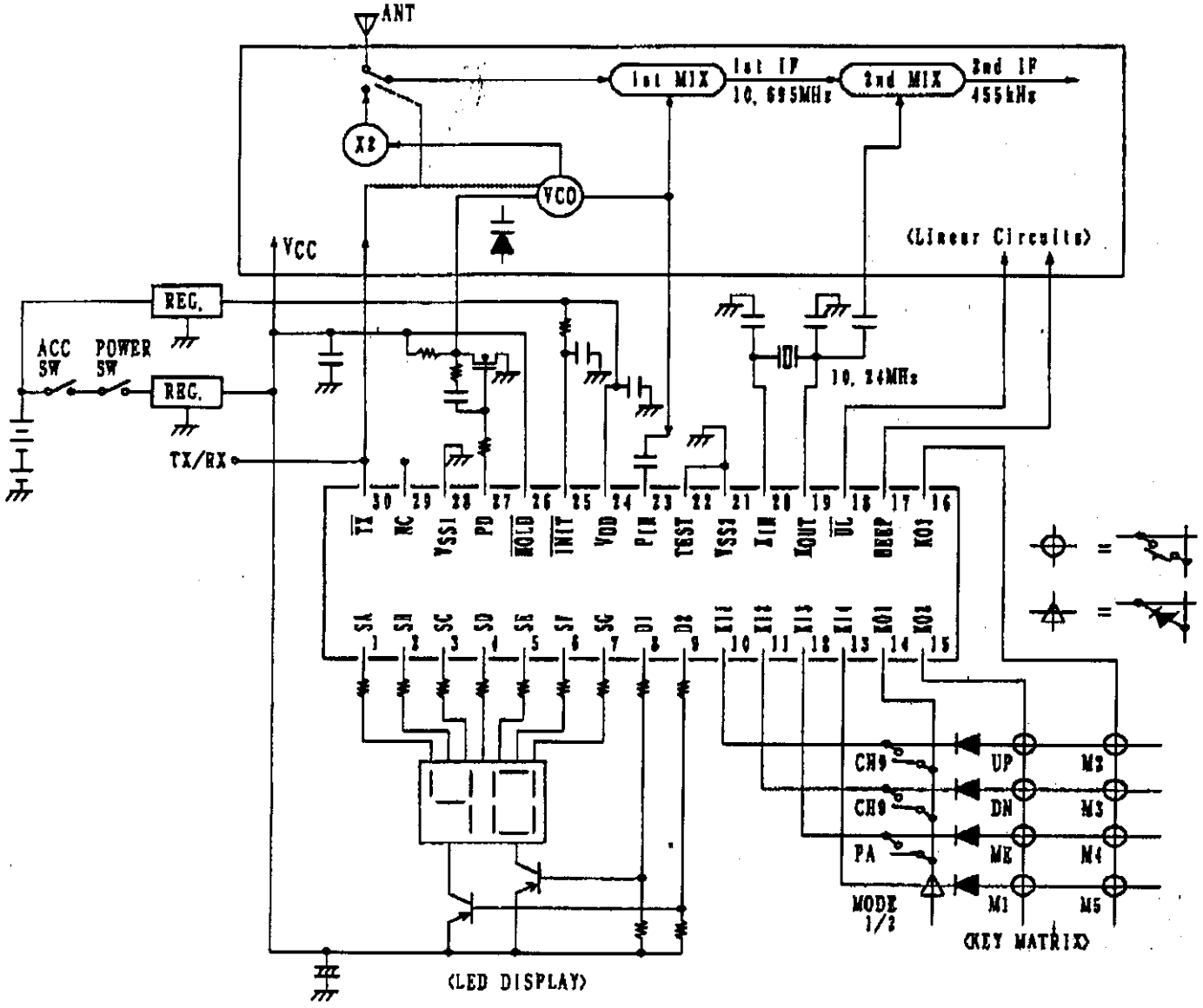
Example Application circuit



11. FREQUENCY TABLE (USA; LC7815-8750)

CHANNEL	FREQENCY (MHz)	RX ($\overline{TX}$ = 1)		TX ($\overline{TX}$ = 0)	
		N	FVCO	N	FVCO
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

VCO (TX) = RF ÷ 2

VCO (RX) = RF − 10.695MHz (IF)

CH1 : VCO (TX) = 26.965 ÷ 2 = 13.4825
VCO (RX) = 26.965 − 10.965 = 16.27

FEDERAL COMMUNICATIONS COMMISSION
Equipment Authorization Division
7435 Oakland Mills Road
Columbia, MD 21046
June 23, 1998

RadioShack A Division of Tandy Corporation
100 Throckmorton St, Suite 1300
Fort Worth, TX 76102-2802

Attention: Dwayne Campbell

Re: Application(s) dated May 22, 1998 and received May 27, 1998
Equipment Class: TNB-Non-Broadcast Transmitter
FCC ID: AAO21-1703

Gentlemen:

Please forward a production or near production sample of the above referenced equipment to the FCC Laboratory for the purpose of pregrant sample testing. Failure to provide a production or near production sample will result in retesting before processing can be completed on your pending application. This request is made under the authority of Section 2.943 or 2.965 of the Commission's Rules.

You will have a period of 60 days from the date of this letter to supply the requested sample or your application will be dismissed without action and the filing fee forfeited. We are convinced that 60 days is a reasonable time limit in which to supply the requested sample. Requests for extension of this time will be accepted in writing only and must provide an explanation of the circumstances which necessitate an extension. Most requests for an extension are not honored due to the fact that the present time limit has been considered overly reasonable.

The sample and, in the case of a personal computer, all related accessories including connecting cables used to generate the test report should be submitted. ALL samples and accessories must be properly labeled with the IDENTICAL identification in the reference.

The sample MUST be shipped with charges PREPAID. To avoid delays in testing, and return of the equipment after testing is complete, a copy of this letter and the completed "Return Shipment Form" MUST accompany your shipment. Please address the shipping container to the attention of the undersigned.

Replies to this letter MUST contain the Reference Number: 1431

Sincerely,

Bill Inglis
Electronics Engineer
Applications Processing Branch

FEDERAL COMMUNICATIONS COMMISSION
Equipment Authorization Division
7435 Oakland Mills Road
Columbia, MD 21046
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Sincerely,

Bill Inglis
Electronics Engineer
Applications Processing Branch

To: ~~Bill Inglis~~ D C

Date: 6/23/98 15:24:42

Subject: Sample request

Message:

We will need a copy of the specification sheets for the PLL and a description of how the unit protects against out-of-band operation. Please verify the synthesizer block diagram and explain the operation of the circuitry it represents. Please note that we have not yet reviewed the test report.

Replies to this letter MUST contain the Reference Number: 1434

To: ~~Bill Inglis~~

Date: 6/23/98 15:24:42

Subject: **Sample request**

Message:

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Replies to this letter MUST contain the Reference Number: 1434