NEC
NEC America, Inc.
Wireless Communications Division

NEC CDMA Hand Held Phones

SPECIFICATIONS

Frequency Range Transmitter Receiver	 824.01 –848.97MHz 869.01 – 893.97 MHz
Number of Channels AMPS CDMA	 832 53248 Code Channels
Vocoder	8kbps QCELP 13kbps QCELP EVRC
RF Power Output AMPS CDMA	 600mW Maximum ERP (Class III) 6.3mW minimum ERP 6 different power levels in 4 dB steps. 200mWatts minimal at maximum ERP(Class III) 1 Watt maximal at maximum ERP (Class III) 0.00002mWatts minimum ERP 146 different power level in 0.5 dB steps
Receiver Sensitivity AMPS CDMA	 -116 dBm/ 30kHz -104 dBm /1.23MHz
Receiver IM Free Dynamic Range AMPS CDMA	 86 dB 79 dB
Channel Spacing AMPS CDMA	 30 kHz 1.23MHz
Operating Voltage	3.6 V (Internal Battery) Up to 5.5V (Battery terminals)
Modulation Analog Digital	 FM OQPSK
Modulation Data Rate	1.2288MHz
Data Structure	CDMA

Description of RF Transceiver of the Handheld Cellular Phone

The equipment under test is a dual mode, full duplex handheld cellular phone (HHP) designed to meet or exceed the TIA/EIA interim standard IS-95-A, and the IS-98-A. The EUT is capable of communicating in either analog mode (FM) or digital mode (CDMA).

The technical descriptions included in this section cover the RX, TX, frequency synthesizer and antenna sections of the HHP. The technical descriptions are intended to describe the RF hardware circuits only. The base band processing circuit and control circuit, as well as the firmware and protocol issues are not included in this description.

Antenna and Duplexer

The retractable bottom helical antenna system, consisting of a helical element and a retractable whip through the helical element, is designed to transmit and receive signals in both the extended and retracted positions. For hand free mode operation the RF signals from/to the transceiver are routed to the micro-switch connector located at the upper back cover of the HHP. The duplexer antenna port will be switched to external antenna when the external antenna is plugged in the micro-switch connector. In either case the duplexer provides a full duplex operation required by the standard.

RF Receive (RX) Path Description

The receiver section is designed to receive FM and CDMA signals in 869 MHz to 894 MHz frequency band. The receive (RX) signal from the duplexer RX port is routed to an adjustable attenuator (U1) and a low noise amplifier (LNA,U2). After the LNA, the signal with appropriate power level passes through a band pass filter (BPF1). The band pass filter provide an out band noise suppression for the following frequency down conversion. The frequency down conversion is accomplished at mixer (U11). Local frequency signal is provided to down-converter through a band pass filter (BPF2). The down-converted immediate frequency (IF) signal is delivered to a 1.3MHz band pass filter (BPF3) for digital mode (CDMA) operation, or a 30kHz band pass filter (BPF4) for analog mode (AMPS) operation. The filtered signal is routed to the RX AGC device (U4) for further signal level adjustment. Therefore the IF signal on desired power level is inputted to the base band signal processing unit (U18).

The baseband processor (BBA2, U18) demodulates the RX IF signal centered at 85.38 MHz into I and Q base band components by mixing with a 85.38 MHz signal generated by an on-chip voltage controlled oscillator (VCO). For both the CDMA and FM base band signals the low pass filtering and analog-to-digital conversion (ADC) are provided on the same chip U18. The clock is derived from the voltage-controlled temperature compensated crystal oscillator (VC-TCXO) U17 that will be discussed separately. The I and Q data stream is routed to the logic unit of the HHP for further processing.

RF Transmitter (TX) Path Description

The HHP is capable of transmitting FM (30 kHz bandwidth) and CDMA (1.23 MHz bandwidth) signal in the 824 MHz to 849 MHz cellular frequency band.

FM and CDMA modulation functions are achieved in the baseband processor (BBA2, U18). In digital mode (CDMA), the incoming I and Q data from the logic unit are multiplexed over an 8-bit input port into the BBA CDMA digital-to-analog converters (DACs). Each DAS is followed by an anti-alising low-pass filter with a bandwidth of 630 kHz that reduces unwanted frequency components. The I and Q base band components from the anti-aliasing filter are mixed in quadrature with the unmodulated I and Q signals at 130.38 MHz to generate the TX IF signal centered at 130.38 MHz. The unmodulated I and Q signals are generated from the on chip frequency synthesizer. Similar to the RX circuit, the reference frequency and clock are derived from the VC-TCXO. In analog mode (FM) only the Q channel DAC is used. The FM modulation is carried out in an off chip circuit, which will be described separately.

The TX IF signal from U18 is route to the TX AGC stage U9. The TX AGC unit provides an 80-dB dynamic power control range to meet the power control requirement. The IF signal then passes through a band pass filter, BPF8 centered at 130.38 MHz and then enters the mixer, U8, for frequency up conversion. Aftèr the up converter, a band pass filter BPF7, a gain adjustable driver amplifier U7, and a band pass filter BPF6 boost the RF signal with desired spectrum to a desired power level for the power amplifier (PA) input. Between the duplexer and PA, an isolator is used to protect the PA and power detecting circuit

Frequency Synthesizer

The system crystal oscillator U17 supplies the 19.68 MHz reference frequency to the baseband processor U18 and dual frequency synthesizer U3. U3 generates the LO frequency for the receive section by means of a phase lock loop (PLL) implementation. The reference frequency of the PLL is from the crystal oscillator. The frequency synthesizer also generates the LO frequency for the TX up converter and the RX down converter. The TX tank circuit and the RX tank circuit are designed for the transmit and receive VCOs in the baseband processor U18. In analog mode, the FM modulation is achieved in the TX tank circuit. Depending on the TX output requirement, the frequency of the transmit VCO is modulated with either voice, SAT, ST or wide band data.

Hardware Logic Section Description

Introduction

Scope

This document describes the hardware functional specification of the AMPs/CDMA Digital Subsystem developed by NEC America, Inc. for use in a AMPs/CDMA handheld cellular phone (SYNERGY HHP).

Acronyms and Abbreviations

The acronyms used most frequently in this document are listed and described below:

AF	Audio Frequency
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
CDMA	Code Division Multiple Access
CPU	Central Processing Unit
DSP	Digital Signal Processor
DTMF	Dual-Tone Multifrequency
FET	Field-Effect Transistor
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
EVRC	Enhanced Variable Rate Coder
GPIO	General Purpose Input Output
HHP	Handheld Portable Phone
I	In-phase
IC	Integrated Circuit
I/O	Input/Output
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least significant bit
MSB	Most significant bit
Ni-Cd	Nickel-Cadmium rechargeable battery
Ni-MH	Nickel-Metal Hydride rechargeable battery
NOTIS	NEC Open Telephone Interface Specification
PCM	Pulse Code Modulation

Q	Quadrature
RC	Resistor-Capacitor
RF	Radio Frequency
ROM	Read Only Memory
RX	Receive
SCI	Serial Communication Interface
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TRX	Transmit/Receive Module
TX	Transmit
VOCOD	Voice Coding and Decoding

References

The following references are used in support of this document.

1. EIA/TIA-553 STANDARD, "*Mobile Station - Land Station Compatibility Specification*", September 1989
2. IS-95, "*CDMA Digital Common Air Interface Standard, Cellular System Dual-Mode Mobile Station - Base Station Compatibility Standard*", October 1990

DSS Features

The Code Division Multiple Access (CDMA) Digital Subsystem has the following features:

- ASIC for complete digital signal processor implementation of a mobile station spread spectrum digital cellular system, CodeBook Excited Linear Prediction (QCELP) variable rate voice processing VOCODER and compatible microprocessor.
- CODEC Provides A-to-D and D-to-A function
- Audio Amplifier Circuit Sounder
- Power ON Reset Reset
- Flash ROM Read Only Memory (ROM)
- SRAM Static Random Access Memory (SRAM)
- Power supply (Regulators, Switcher)
- Keypad 3-key (horizontal), 4-key (horizontal), 12-key matrix (3-key (horizontal) by 4-key (vertical))
- Display 10-character by 4-lines, including Display Driver
- NOTIS interface Reconfigurable between NEC Open Telephone Interface Specification (NOTIS)
- RF Interface Other part of sub-system
- Real-Time Clock With two alarm capability
- Battery A/D interface

DSS Functional Description
Hardware Block Diagram
The CDMA Digital Subsystem consists of:

- CDMA Application Specific Integrated Circuit (ASIC)
- Field Programmable Gate Array (FPGA)
- CODEC circuit
- Audio amplifier
- NOTIS bus interface
- RF bus interface
- Reset control
- Power supply
- Display

Mobile Station Modem

- The CDMA ASIC implements the majority of the baseband digital signal processing.

It is the digital signal-processing core of a full-duplex spread spectrum modem. It is optimized for processing the CDMA waveform as specified in the CDMA Digital Common Air Interface (CAI) Standard. This chip performs all real-time waveform-processing functions in hardware under software control using a microprocessor.
The microprocessor receives and transmits data as follows:

In the receive mode (Rx), digitized baseband in-phase (I) and quadrature (Q) samples are input to the chip, demodulated, despread, deinterleaved, and decoded. This data is made available to the processor.
In the transmit mode (Tx), the processor presents data packets to the chip for encoding, interleaving, spreading, and filtering. Digitized I and Q samples are then available for appropriate processing.
The ASIC interfaces with the following:

- RF module
- CODEC
- FPGA memory
- General-purpose data ports

The Radio Frequency (RF) interface allows ASIC to communicate with the external RF circuitry. It controls the power amplifier, the local oscillator and the Automatic Gain Control (AGC) feedback on the transmit and receive sides.
The Baseband Analog interface consists of:

(1) CDMA Rx interface Receives the incoming forward link symbols when in CDMA mode
(2) Serial FM Rx interface Receives the incoming forward link symbols when in Frequency Modulation (FM) mode