Shenzhen Yiqifei Technology Co., Ltd

YQF-6012-00

Technical Specification for Radar Module

2025-02-10

Table to Contents

1. Device overview

1.1. Features

- Integrated PLL, Transmitter, Receiver, Baseband and ADCs
- Operating Frequency: 57 to 64GHz
- 2-Transmit, 2-Receive Channels
- Ultra-Accurate Chirp (Timing) Engine Based on Fractional-N PLL
- Tx Power @ Single Channel: 12dBm
- 57 to 65GHz Phase Noise@1MHz offset: -91dBc/Hz
- Rx Noise Figure: 11dB
- RF Built-in self-test (BIST) module, Self-calibrated System Across Frequency and Temperature
- ARM® Cortex®-M3 Core
- Built-in Digital Signal Process, including FIR, FFT and etc.
- Built-in FMCW Chirp generation
- Available IOs:
  --- 1 SPI Channels
  --- 1 CAN2.0/CAN-FD
  --- 3 UARTs
  --- 1 I2Cs
  --- Interface for analog IF output
- Power management with low power mode.
- Digital I/O voltage 3.3V
- Clock Source
  --- 50.0MHz Oscillator or Crystal
  --- Support external 32.768KHz crystal.
  --- Internal RC Oscillator, 32KHz +/-20%
- Easy hardware design with 0.5mm pitch, 125-pin and 6.75mm x 6.75mm x 0.49mm fanout BGA package for small formfactor size

1.2. Applications

- Respiratory rate monitoring
- Human persistence monitoring
- Gesture recognition
- Low power carpark monitoring

1.3. Description

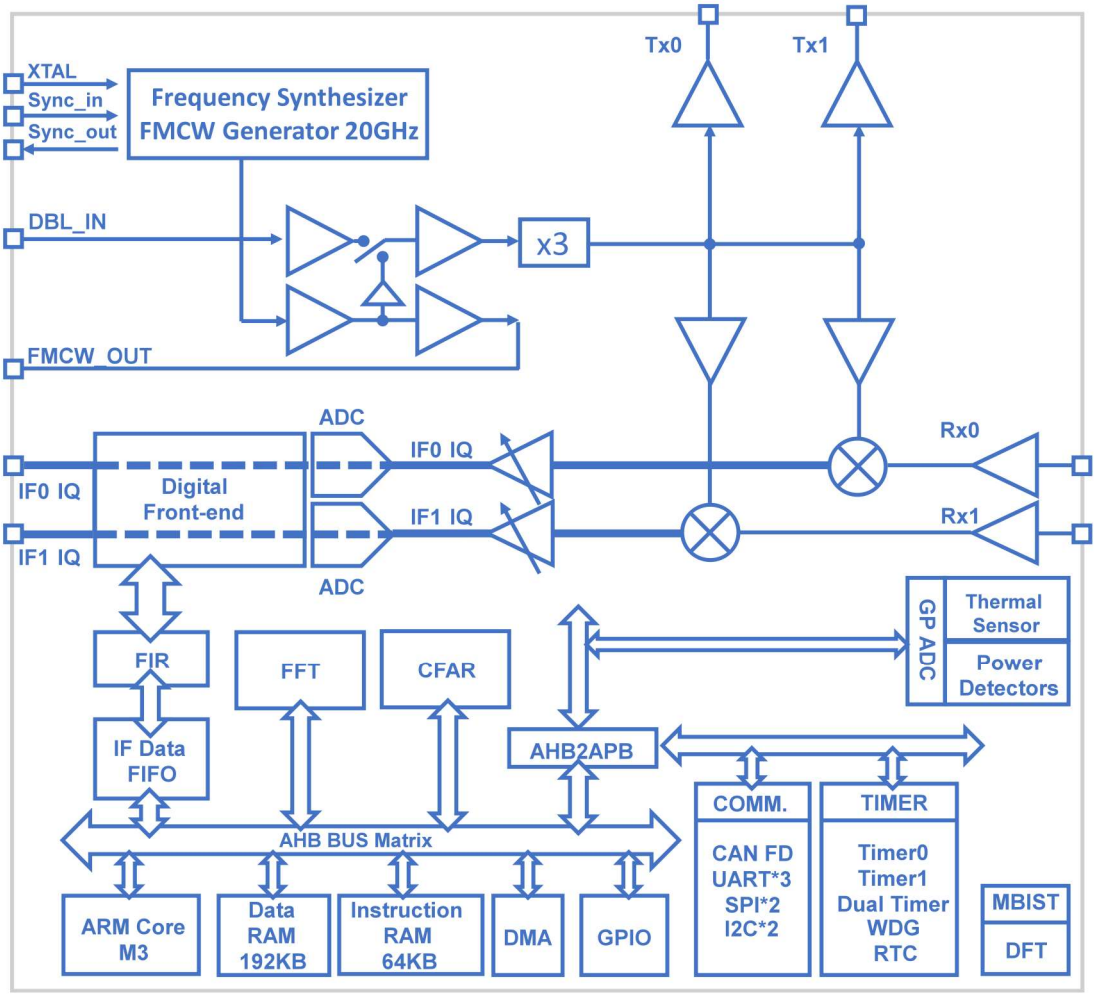
The ADT6101 device has integrated 2 transmit and 2 receive channels, IQ down-conversion mixers, a RF VCO, a Fractional-N PLL, frequency tripler, built-in digital signal processing units, including FIR, FFT and other radar signal processing function blocks. The device includes an ARM® Cortex®-M3 Core based processor subsystem, which is responsible for radio chip configuration, control, calibration and data communications. The device is provided with a complete platform including

reference design, software drivers, API guides and user documentations. The device also supports cascade-mode operation for applications that need higher accuracy and long range.

1.4. System Block Diagram

The detail system block diagram is shown in Fig. 1.1

Fig. 1.1 ADT6101 System Block Diagram



2. Specifications

2.1. Absolute maximum ratings [1]

Table 2.1 Absolute Maximum Ratings

Signal Name	Signal description	Max Ratings		Unit
		Min	Max	
VDD_RF	RF power	0	1.45	V
VDD	Digital 1.2V supply	0	1.4	V
VDD12	Internal 1.2V LDO output	0	1.4	V
AVDD18_PLL	Internal PLL Power supply	0	2.75	V
AVDD18_PLL_VCO	Internal VCO Power	0	2.75	V

AVDD18_BB1	Internal Baseband1 Power	0	2	V
AVDD18_BB2	Internal Baseband2 Power	0	2	V
VDD33	Analog 3.3V Power	0	3.63	V
DVDD33	Digital 3.3V Power	0	3.63	V
CLKP, CLKN	Input ports for reference crystal	-0.5	2	V
Clamp current	Limit clamp current through the internal diode protection of the I/O	-20	20	mA
T_J	Operating junction temperature range	-40	125	°c
T_{STG}	Storage temperature range after soldered onto PC board	-55	150	°c

(1)Stress beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Exposure to any Absolute Maximum Rating condition for extended periods of time may affect device reliability and lifetime

2.2. ESD ratings

Table 2.2 ESD Ratings

Signal description		Value	Unit
V(ESD)	Human-body model, HBM	±2000	V
	Charged-device model, CDM	±500	

2.3. Recommended operating conditions

Table 2.3 Recommended Operating Conditions

Signal Name	Signal description	Max Ratings			Unit
		Min	Nom	Max	
VDD_RF	RF power supply	1.15	1.35	1.45	V
VDD	Digital 1.2V Power	1.08	1.2	1.32	V
VDD12	Internal output 1.2V Power	1.08	1.2	1.32	V
AVDD18_PLL	Internal PLL Power Supply	2	2.5	2.75	V
AVDD18_PLL_VCO	Internal VCO Power Supply	1.7	1.8	1.9	V
AVDD18_BB1	Internal Baseband1 Power	1.7	1.8	1.9	V
AVDD18_BB2	Internal Baseband2 Power	1.7	1.8	1.9	V
DVDD33	3.3V, for GPIO interface	3	3.3	3.6	V
AVDD33	3.3V, for analog PLL, ADC	3	3.3	3.6	V
Analog module VIH	Voltage Input High (1.2V mode)	1.1			V
	Voltage Input High (3.3V mode)	2.5			
Analog module VIL	Voltage Input Low (1.2V mode)	0.3			V
	Voltage Input Low (3.3V mode)	0.8			

CLKP, CLKN	Voltage Input High	1.2	V
	Voltage Input Low	0.2	
MCU	Voltage Input High (3.3V mode)	2.5	V
	Voltage Input Low (3.3V mode)	0.6	V

2.4. Power supply specifications

Table 2.4 Power Supply SPEC

Voltage Define	1.35V	1.8V	3.3V
Supply SPEC	RF	Analog	GPIO, analog and digital part

2.5. Power consumption summary [(2)]

Table 2.5 Power Consumption Summary

Signal Name	Signal description	Max Ratings			Unit
		Min	Nom	Max	
VDD_RF	1.35V, power for 60GHz RF			600	mA
VDD	1.2V, for Digital Core		15		
DVDD33	3.3V, for GPIO interface		40		
AVDD33	3.3V, for analog circuits		210	250	

(2)The data is based on IC test data (10 pcs) under maximum output power on TX mode and RX mode at the same time

2.6. RF & IF specification

Table 2.6 RF Specifications

Parameter		Min	Nom	Max	Unit
SYS	Rx Baseband Frequency	0.1		4	MHz
	RF Frequency range	57	60	65	GHz
RF TX	Output Power		12		dBm
	In-band spur suppression		-50		dBc
	RF Phase Noise@1MHz		-91		dBc/Hz
RF RX	Reflection coefficient		-10		dB
	Receive Noise Figure		11		dB
	In- band spur suppression		-50		dBc

RX IF	TIA dynamic range (6dB/step)	0		18	dB
	High Pass Filter Conner Frequency	100		300	KHz
	Low Pass Filter Conner Frequency	2	4	10	MHz
	ADC sampling rate (real)			7.14	MSps
	ADC sampling rate (complex)			7.14	MSps
	ADC resolution		12		Bits
	Single end IF signal to ADC	0		800	mVpp
	VGA dynamic range (2dB/step)	0		40	dB
Local Oscillator	Frequency range	19		21.7	GHz
	Ramp rate		50		MHz/μs
	Input Local Oscillator Power	-15	-10	0	dBm
	Output Local Oscillator Power	0	2	4	dBm

2.7. MCU specification

Table 2.7 CPU Specifications

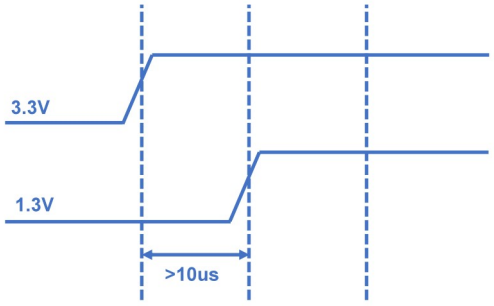
Parameter		Min	Mid	Max	Unit
ARM® Cortex®-M3 Core	Clock Speed		50	100	MHz
	ROM			32	KB
	Instruction RAM			64	KB
	Data RAM			192	KB

2.8. Timing and switching characteristics

2.8.1 Power supply sequencing

The ADT6101 device expects the power on sequence as shown in Fig. 2.8.1.

Fig. 2.8.1 Power ON sequence



2.8.2 Input clock source specifications

A 50MHz crystal or external oscillator is used as the clock source.

Fig. 2.8.2 shows the crystal implementation. Table 2.8.2.1 lists the electrical characteristics of the required crystal.

Table 2.8.2.1 Crystal Electrical Characteristics

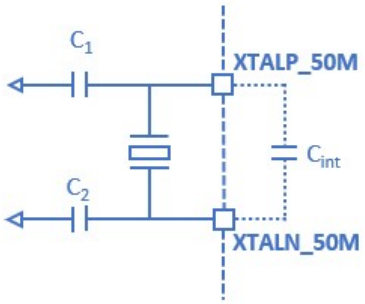
Name	Description	Min	Mid	Max	Unit
Reference Frequency	Crystal frequency		50		MHz
Temperature range	Operation temperature range	-40		125	℃
Frequency tolerance	Note (1)	-200		200	ppm
Load capacitance	Crystal load capacitance		8	12	pF
ESR	Effective Resistance			50	Ω

(1) Includes frequency tolerance, frequency stability over operating temperature range, aging and frequency pulling due to incorrect load capacitance of the crystal.

The load capacitors, C_1 and C_2 should be determined based on Equation 2.8.2, where C_L is the load capacitance in crystal specification provided by the manufacturer. C_{1p} and C_{2p} are the parasitic capacitances on the PCB traces. The crystal and load capacitors should be placed as close as possible to the oscillator pins, i.e. XTALP_50M and XTALN_50M. C_{int} is the on-chip capacitance between XTALP and XTALN, and it is 5.5pF under the typical condition using default register setting.

$$C_L = \frac{(C_1 + C_{1p}) \times (C_2 + C_{2p})}{(C_1 + C_{1p}) + (C_2 + C_{2p})} + C_{int} \qquad \text{Equation (2.8.2)}$$

Fig. 2.8.2 Crystal Implementation



If an external oscillator is used as the input clock source, the signal must be fed to the XTALP_50M pin only, and XTALN_50M is grounded. Table2.8.2.2 lists the electrical characteristics of the external

clock signal. For better performance of the FMCW synthesizer, oscillator frequency of at least 100MHz is highly recommended if an external oscillator is used.

Table 2.8.2 External Clock Specifications

Name	Description	Min	Mid	Max	Unit
Frequency		50	100		MHz
AC Amplitude	AC-coupled	0.5		1.8	Vpp
Phase Noise at 1kHz	Phase Noise referred to 50MHz			-132	dBc/Hz
Phase Noise at 10kHz				-143	
Phase Noise at 100kHz				-152	
Phase Noise at 1MHz				-153	
Phase Noise at 10MHz				-153	
Frequency Tolerance		-50		50	ppm

2.8.3 Serial communication interface (SCI)

Two external pins: RS232_RX and RS232_TX

Table 2.8.3 Electrical Characteristics

	Min	Mid	Max	Unit
f(baud) Supported baud rate at 20 pF		115.200		KHz

2.8.4 Serial peripheral interface specifications

The related parameters about SPI mainly define the SPI timing sequence and communication logic, are shown as Table 2.8.4

Table 2.8.4 SPI Timing Conditions

Input conditions	Min	Mid	Max	Unit
Input rise time	1		3	ns
Input fall time	1		3	ns
Output conditions	**Min**	**Mid**	**Max**	**Unit**
Output load capacitance	2		12	pF

2.8.5 SWD interface specifications

Compatible with the general SWD interface, this interface is used as a debug port.

3、YQF-6012-00 Module Block

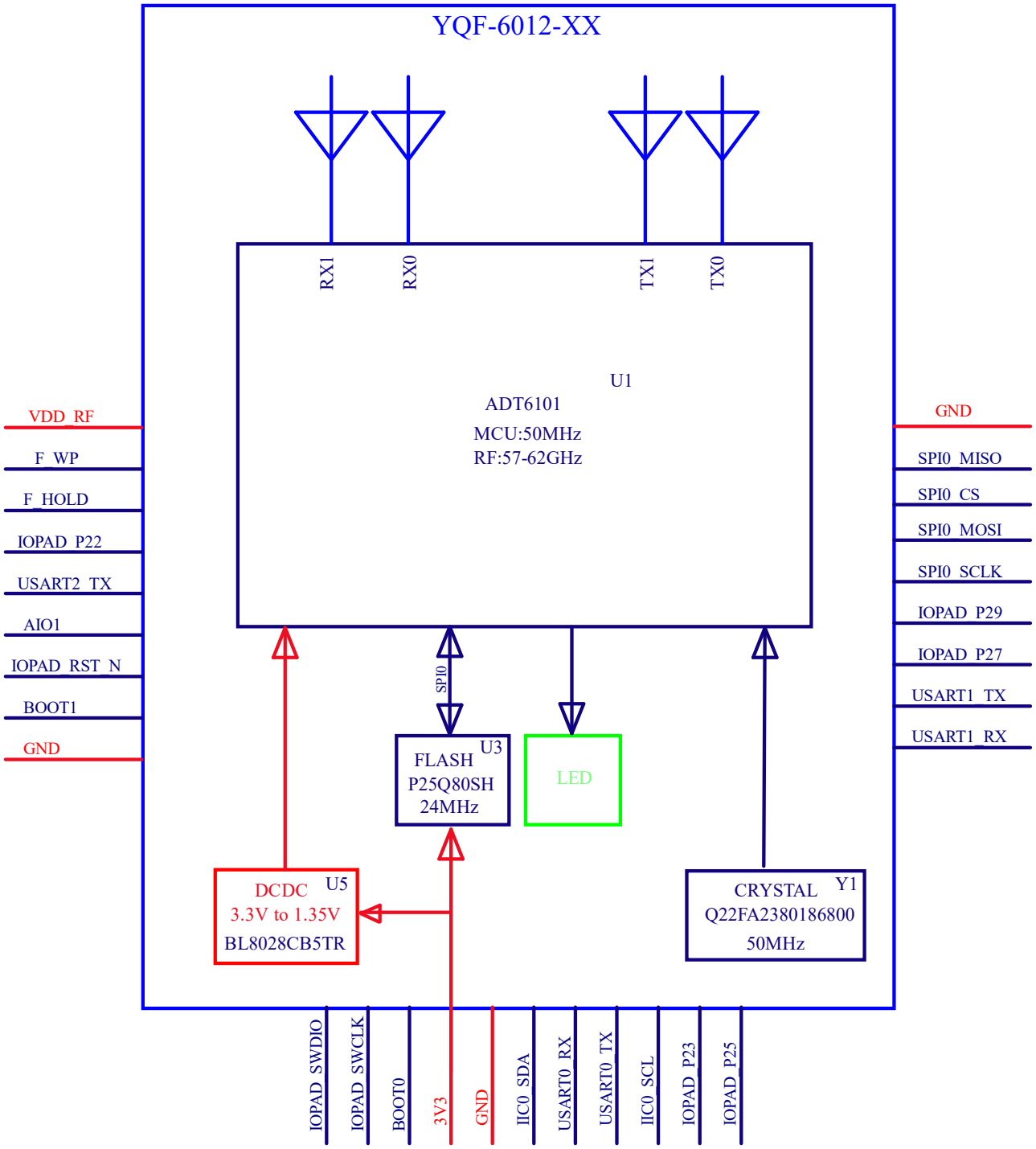


Figure 3-1 YQF-6012-00 module block.

4、YQF-6012-00 Module size

4.1、Top size

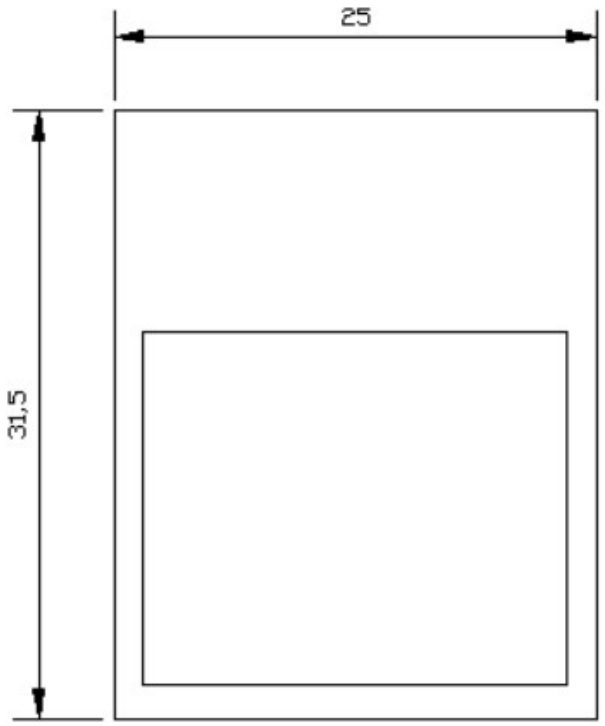


Figure 4-1 YQF-6012-00 module size(unit: mm).

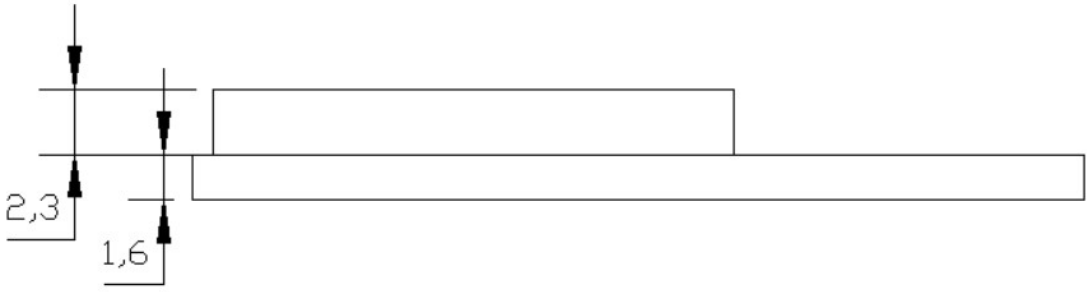


Figure 4-2 YQF-6012-00 module thickness(unit: mm).

4.2、Footprint size

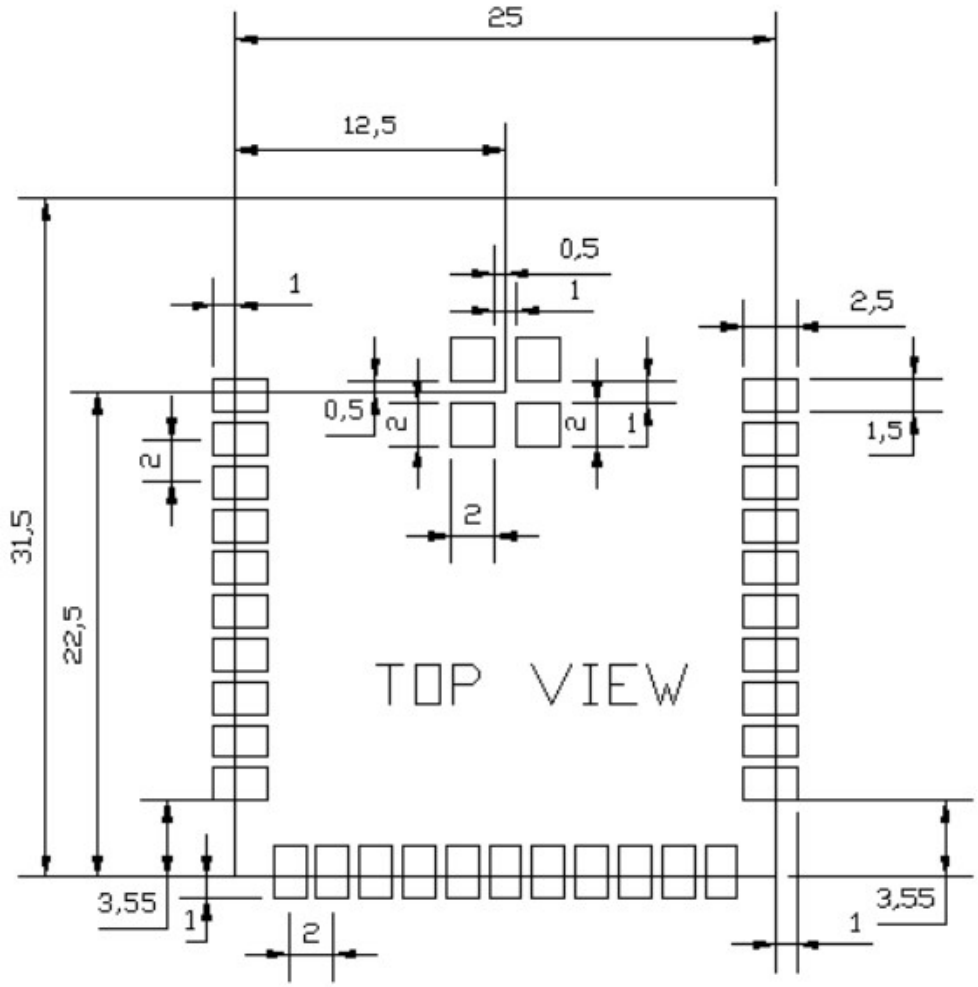


Figure 4-3 YQF-6012-00 module SMT footprint(unit: mm)

(TOP VIEW)

5、YQF-6012-00 Module external interface

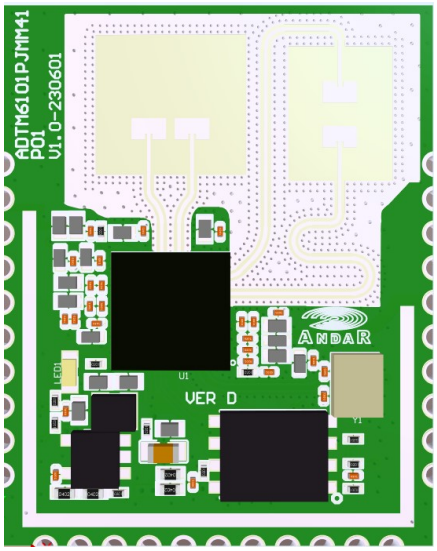


Figure 5.1 package design for 1patch (TOP VIEW)

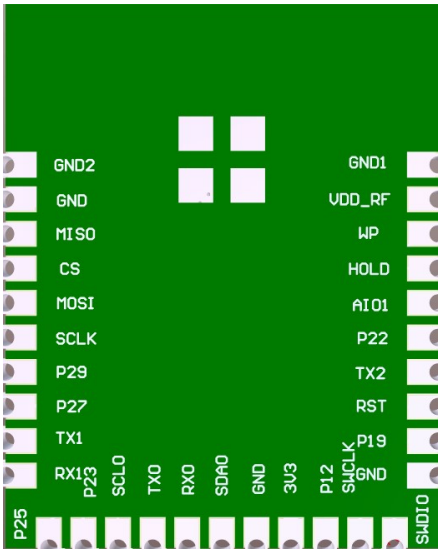


Figure 5.2 package design for 1patch (BOT VIEW)

Table 5.1. 9-Pin of left (TOP VIEW)

Pin No	Pin name	Description	Notes
GND1	GND	GND	
1	VDDRF	External RF Power/1.35V	
2	WP	Write protection active low	
3	HOLD	To pause the device without deselecting the device	
4	AIO1	Temperature index test interface	
5	P22	interfaceGPIO_P22/LDO_EXT_EN_H	
6	TX2	GPIO_P20/uart2 txd	
7	RST	Reset Signal input	
8	P19	GPIO_P19/boot1	Boot
9	GND0	GND	

Table 5.2. 11-Pin of down (TOP VIEW)

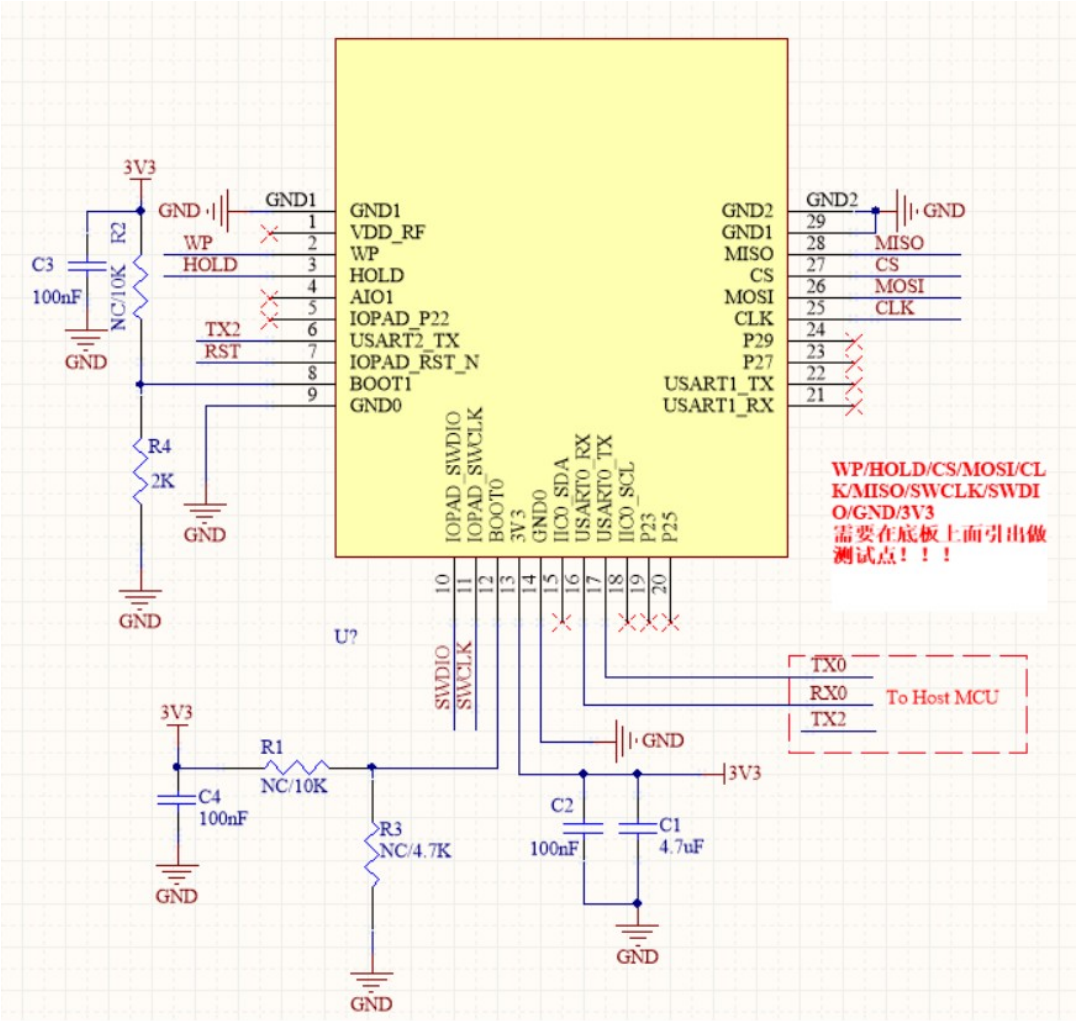
Pin No	Pin name	Description	Notes
10	SWDIO	SWD Debug Signal	
11	SWCLK	SWD Debug Clock	
12	P12	GPIO_P12/boot0	
13	3.3V	POWER INPUT 3.3V	
14	GND	GND	
15	SDA	GPIO_P08/IIC0_SDA	
16	RX0	GPIO_P01/uart0 _txd	
17	TX0	GPIO_P00/uart0 _txd	
18	SCL	GPIO_P07/IIC0_SCL	
19	P23	IOPAD_P23	
20	P25	IOPAD_P25	

Table 5.3. 9-Pin of right (TOP VIEW)

Pin No	Pin name	Description	Notes
21	RX1	GPIO_P11/uart1 rxd	
22	TX1	GPIO_P10/uart1 txd	
23	P27	IOPAD_P27	
24	P29	IOPAD_P29	
25	SCLK	IOPAD_P03/SPI0_SCLK	
26	MOSI	IOPAD_P06/SPI0_MOSI	
27	CS	IOPAD_P04/SPI0_CS	
28	MISO	IOPAD_P05/SPI0_MISO	
29	GND1	GND	
GND2	GND2	GND	

6、YQF-6012-00 Module Reference Schematic

Figure 6-1 YQF-6012-00 Module Reference Schematic.



FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC Part 15 Subpart C has been investigated. It is applicable to the modular transmitter

2.3 Specific Operational Use Conditions - Antenna Placement Within the Host Platform

The module is tested for standalone mobile RF exposure use condition.

- The antenna must be installed such that 20cm is maintained between the antenna and users,
- The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.4 Limited Module Procedures

Not applicable

2.5 Trace Antenna Designs

Not applicable

2.6 RF Exposure Considerations

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antenna Type and Gain

The module only used patch antenna and maximum antenna gain is y6.00dBi.
Only antennas of the same type with equal or lower gain may also be used with this module. Other types of antennas and/or higher gain antennas may require the additional authorization for operation.

2.8 End Product Labelling Compliance Information

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: **2BOAI-YQF-6012-00**”. The FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on Test Modes and Additional Testing Requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) class II permissive change re-evaluation or new FCC authorization.
Host manufacturer installed this modular with single modular approval should perform the test of radiated emission and spurious emission according to FCC part 15C, 15.209, 15.207 requirement, only if the test result comply with FCC part 15C, 15.209, 15.207 requirement, then the host can be sold legally.

2.10 Additional testing, Part 15 Subpart B Disclaimer

This transmitter modular us tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B rules requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rules requirements if applicable.
As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this modular installed.

2.11 Manual Information to The End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The host integrator must follow the integration instructions provided in this document and ensure that the composite system end product complies with the requirements by a technical assessment or evaluation to the rules and to KDB Publication 996369.
The host integrator installing this module into their product must ensure that the final composite product complies with the requirements by a technical assessment or evaluation to the rules, including the transmitter operation and should refer to guidance in KDB Publication 996369.

OEM/Host Manufacturer Responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and RF Exposure essential requirements of the FCC rules.

2.12 How to Make Changes - Important Note

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.