I491 Series

Hardware Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Description
-	2025-04-07	Creation of the document
1.0	2025-04-09	First official release

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1 Introduction

This document defines the I491 series module and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of I491 series module. With application note and user guide, you can use I491 series module to design and set up mobile applications easily.

2 Product Overview

2.1. Frequency Bands and Functions

I491 series module is an embedded 4G wireless communication module with receive diversity. It supports LTE/WCDMA wireless communication, and provides data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA networks. It can also provide voice functionality [1] to meet your specific application demands.

The following table shows the frequency bands and functions of the module.

Table 1: Frequency Bands and Functions

Module	LTE Band (with Rx-diversity)	WCDMA Band (with Rx-diversity)	GNSS [2]
I491-NAX	FDD: B2/B4/B5/B12/B13/B25/B26	B2/B4/B5	GPS, GLONASS, BDS, Galileo, QZSS
I491-NAXD	FDD: B2/B4/B5/B12/B13/B25/B26	B2/B4/B5	

It is an SMD-type module designed for integration into applications using its 106 LGA pins. With its compact size of 29.0 mm × 25.0 mm × 2.45 mm, the module is well-suited for most M2M and IoT applications.

The module comes with built-in Internet service protocols like TCP, UDP, and PPP. It also includes extended AT commands, making it easy to use these protocols.

[1] I491-NAX is **Data + Voice** version while I491-NAXD is **Data-only** version. Data + Voice version supports voice and data functions, while Data-only version only supports data function.
[2] GNSS function is optional.

2.2. Key Features

The table provides detailed information about the features of the module.

Table 2: Key Features

Feature	Details
Power Supply	● Operating voltage range: 3.3–4.3 V ● Nominal supply voltage: 3.8 V
Transmitting Power	● WCDMA bands: Class 3 (23 dBm ±2 dB) ● LTE-FDD bands: Class 3 (23 dBm ±2 dB)
LTE Features	● Support up to non-CA Cat 1 FDD ● RF bandwidths: 1.4/3/5/10/15/20 MHz ● DL modulations: QPSK,16QAM and 64QAM ● UL modulations: QPSK and 16QAM ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● DL modulations: QPSK, 16QAM and 64QAM ● UL modulation: QPSK ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/MMS/SMTP/SSL/MQTT/FILE/CMUX/SMTPS protocols ● Support PAP and CHAP protocols for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	● Support 1.8 V and 3.0 V (U)SIM cards ● Support Dual SIM Single Standby
Audio Features	● Support one digital audio interface: PCM interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
PCM Interface	● Support audio with an external codec ● 16-bit linear data format ● Long and short frame synchronization ● Master and slave modes (must be master for long frame sync)
USB Interface	● USB 2.0 compliant (slave mode, up to 480 Mbps) ● Used for AT command communication, data transmission, GNSS NMEA

	sentence output, software debugging, firmware upgrade and voice over USB ● Support USB serial drivers for: Windows 10/11, Linux 2.6–6.7, Android 4.x–14.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate up to 921600 bps (default: 115200 bps) ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
SPI	● Support duplex, synchronous serial communication with peripheral devices ● Designed for direct one-to-one connections without the need for chip selection ● 1.8 V operation voltage with clock rate up to 50 MHz
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features (Optional)	● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default ● Support AGNSS. For more details, see ***document [1]***
AT Commands	● Compliant with *3GPP TS 27.007* and *3GPP TS 27.005* ● Eagle enhanced AT commands
Network Indication	NETLIGHT pin for network activity status indication
Antenna Interfaces	● Main antenna interface: ANT_MAIN ● Rx-diversity antenna interface: ANT_DIV ● GNSS antenna interface: ANT_GNSS [3]
Physical Characteristics	● Size: (29.0 ±0.15) mm × (25.0 ±0.15) mm × (2.45 ±0.2) mm ● Package: LGA ● Weight: approx. 4.2 g
Temperature Ranges	● Operating temperature range [4]: -35 °C to +75 °C ● Extended temperature range [5]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[3] GNSS function is optional.

[4] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[5] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -35 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. EVB Kit

Eagle supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document [2]***.

3 Application Interfaces

3.1. General Description

The module includes 106 LGA pins for connection to a cellular application platform. The following chapters will provide detailed explanations of its interfaces/functions.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SPI
- Indication signals
- ADC interface
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment.

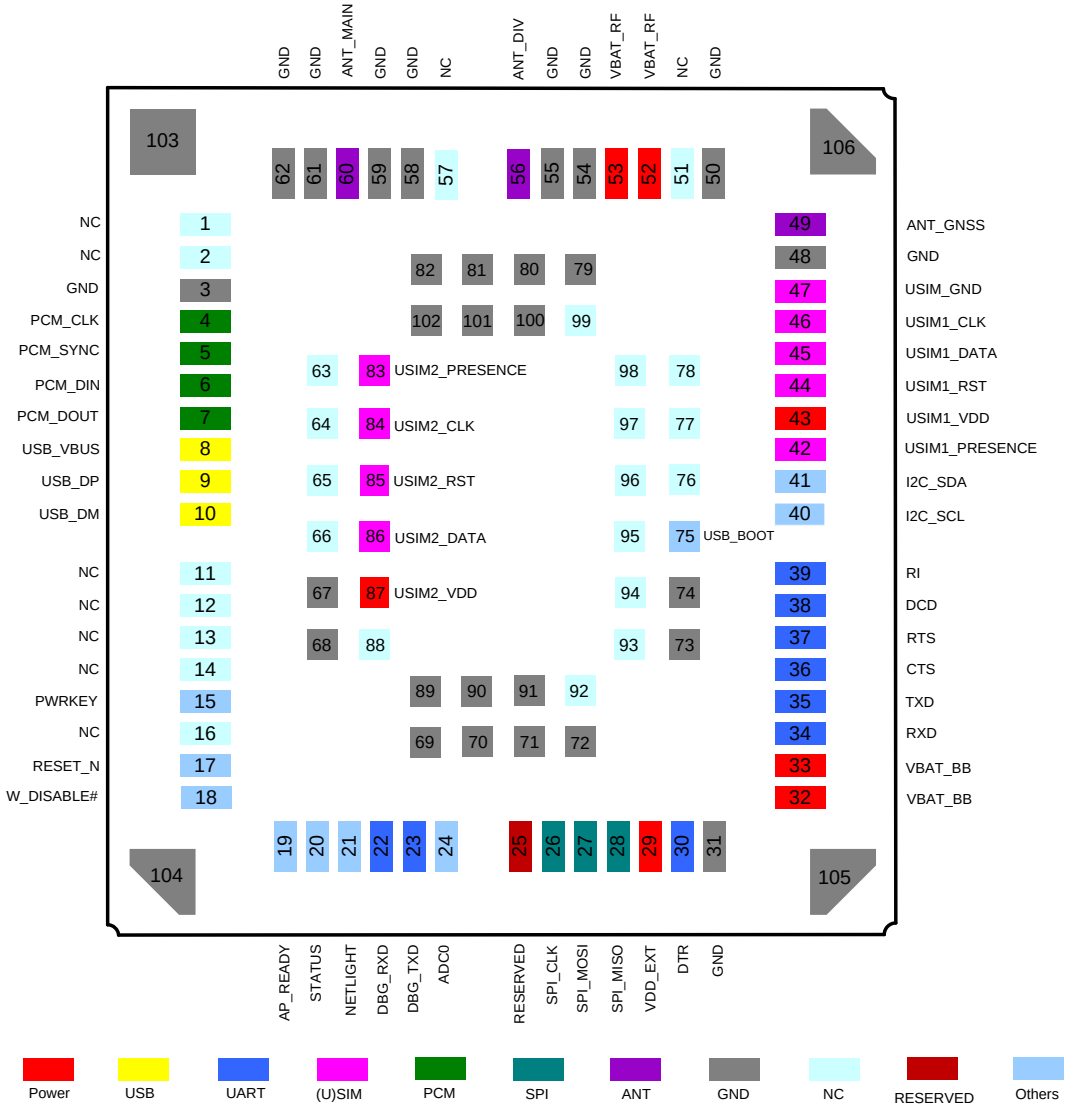


Figure 1: Pin Assignment (Top View)

NOTE

1. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Eagle Technical Support.
2. Due to the diode drop in the baseband chipset, the output voltage PWRKEY is 0.8 V.
3. Keep all RESERVED, NC and unused pins unconnected.
4. Connect GND pins to ground.

3.3. Pin Description

The following tables show the pin definition.

Table 3: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 1.3 A in a burst transmission. A test point is recommended to be

					reserved.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull up circuits. If unused, keep it open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106				Connect them to ground.
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Require pull-up resistor to 1.8 V internally. Active low. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicate the module's operating status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep them open.
NETLIGHT	21	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Require differential

USB_DM	10	AIO	USB differential data (-)		impedance of 90 Ω. Test points must be reserved.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_GND	47	-	Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_ PRESENCE	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.

				Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	
USIM2_DATA	86	DIO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST	85	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_ PRESENCE	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	39	DO	Ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DCD	38	DO	Data carrier detect		
CTS	36	DO	Clear to send signal from the module		1.8 V power domain. Connect to MCU's CTS.

					If unused, keep it open.
RTS	37	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control		1.8 V power domain. Pulled up by default. When it remains at low level, it can wake up the module. If unused, keep it open.
TXD	35	DO	Transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
RXD	34	DI	Receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Test points must be reserved.
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_SYNC	5	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM_CLK	4	DIO	PCM clock		

I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock (for external codec)		Require an external pull-up to 1.8 V If unused, keep them open.
I2C_SDA	41	OD	I2C serial data (for external codec)		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Input voltage range: 0.3 V to VBAT_BB	If unused, keep it open.
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
SPI_MOSI	27	DO	SPI master-out slave-in		
SPI_MISO	28	DI	SPI master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep them open.
ANT_DIV	56	AI	Diversity antenna interface		
ANT_MAIN	60	AIO	Main antenna Interface		50 Ω characteristic impedance.
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. Pulled up by default. When this pin is at low

				V_{IH}max = 2.0 V	level, the module will enter airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready		1.8 V power domain. If unused, keep it open.
USB_BOOT	75	DI	Force the module to enter download mode		1.8 V power domain. Active high. A test point is recommended to be reserved.

NC and RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
NC	1, 2, 11–14, 16, 51, 57, 63–66, 76–78, 88, 92–99	Keep them unconnected.
RESERVED	25	

NOTE

1. To reduce the probability of module damage and extend module service life, do not power up and down frequently.
2. Do not pull up the USB_BOOT pin and BOOT_CONFIG pins (SPI_CLK, PCM_CLK and PCM_SYNC) before startup.

3.4. Operating Modes

The table highlights the operating modes that will be detailed in the following sections.

Table 5: Overview of Operating Modes

Mode	**Details**	
Full Functionality Mode	Idle	Software is active. The module has registered on network, and it is ready to send and receive data.
	Voice/Data	Network is connected. In this mode, the power consumption is decided by network setting and data transmission rate.
Airplane Mode	**AT+CFUN=4** or pulling down W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.	
Minimum	**AT+CFUN=0** can set the module to a minimum functionality mode without	

Functionality Mode	removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Sleep Mode	In this mode, the power consumption of the module will be reduced to an ultra-low level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

For details of the above AT command, see ***document [3]***.

3.5. Power Saving

3.5.1. Sleep Mode

The module minimizes power consumption to an ultra-low level in sleep mode.

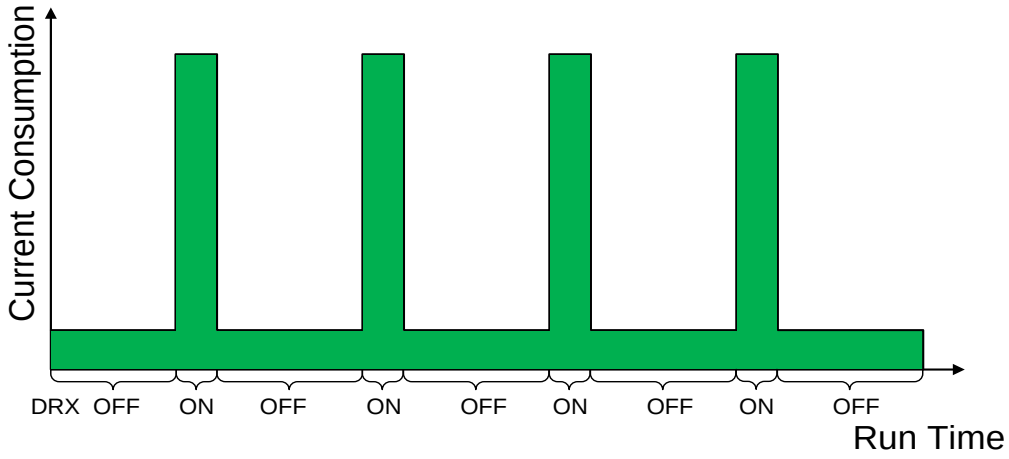


Figure 2: Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.5.1.1. UART Application Scenario

If the MCU communicates with the module via UART interface, the following preconditions can make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the MCU.

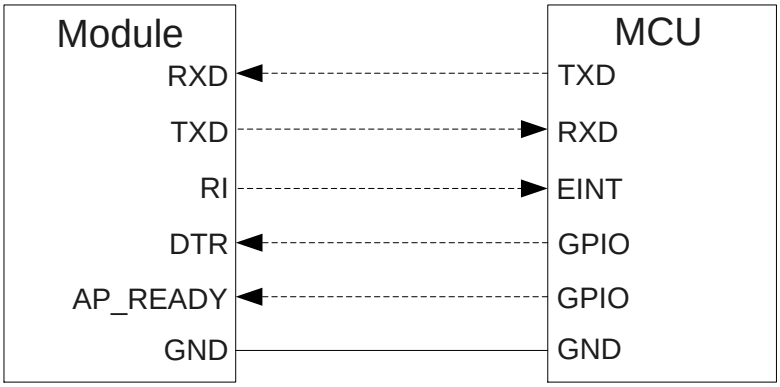


Figure 3: Sleep Mode Application via UART

- Driving the module's DTR to low level will wake up the module.
- When the module has a URC to report, RI signal will wake up the MCU. See ***Chapter 3.15.3*** for details about RI behaviors.
- AP_READY will detect the sleep state of MCU (This pin can be configured to high-level or low-level detection). See **AT+QCFG="apready"** in ***document [4]*** for details.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Ensure the host's USB bus, connected to the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

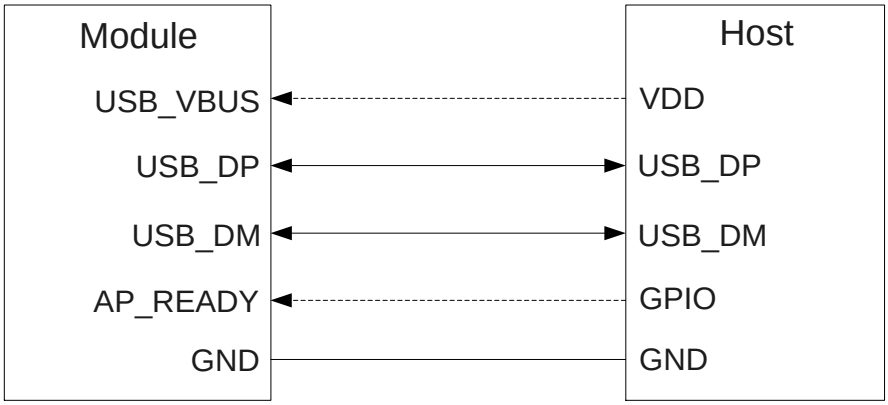


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data via USB wakes up the module.
- When the module has a URC to report, it will send remote wakeup signals via USB bus to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB Suspend/Resume but not remote wakeup, the RI signal wakes up the host. Three conditions are needed for the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Ensure the host's USB bus, connected to the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

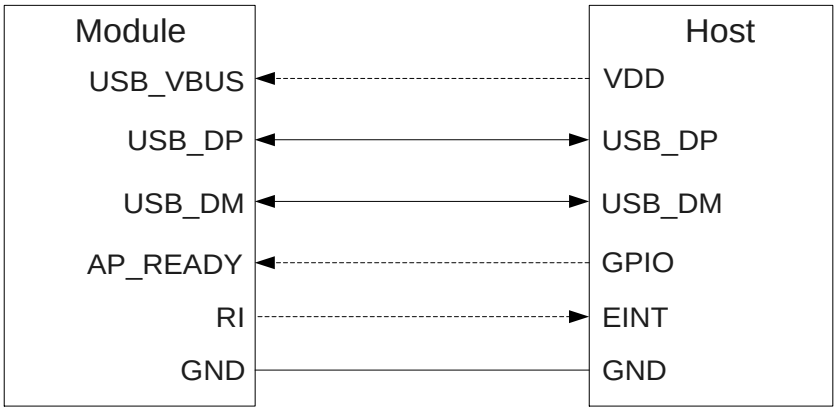


Figure 5: Sleep Mode Application with RI

- Sending data via USB wakes up the module.
- When the module has a URC to report, RI signal will wake up the host.

3.5.1.4. USB Application Without USB Suspend Function

If the host does not support USB Suspend function, an additional control circuit should disconnect USB_VBUS to allow the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

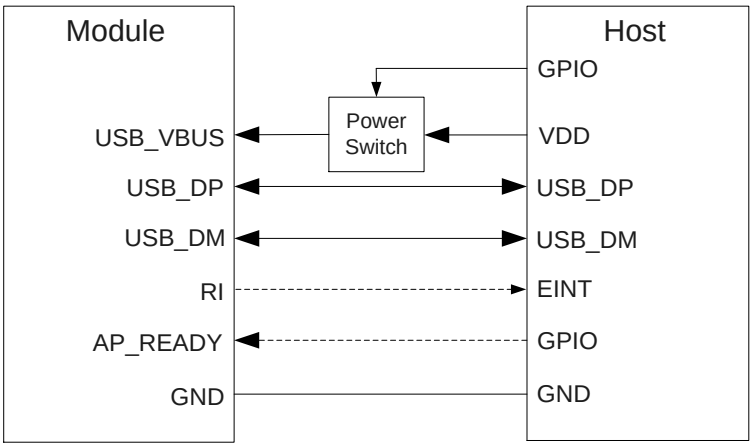


Figure 6: Sleep Mode Application Without Suspend Function

Resuming the power supply to USB_VBUS will wake up the module.

NOTE

1. Ensure proper level matching between the module and the host, as indicated by the dotted line.
2. For more details about on module power management application, see ***document [5]***.
3. For details of **AT+QSCLK**, see ***document [3]***.
4. For details of **AT+QCFG**, see ***document [4]***.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level activates airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** as 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled).

NOTE

1. The W_DISABLE# control function is disabled by default in firmware. It can be enabled by **AT+QCFG="airplanecontrol"**. See ***document [4]*** for more details.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

The module provides four VBAT pins for connecting to an external power supply, divided into two separate voltage domains.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's BB part.

The following table shows the details of VBAT and ground pins.

Table 6: Pin Definition of VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for the module's BB part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–106					

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure that the input voltage will never drop below 3.3 V.

To reduce voltage drop, use a 100 µF filter capacitor with low ESR (0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to its ultra-low ESR for VBAT_BB and VBAT_RF. For the MLCC array, it is recommended to use three ceramic capacitors: 100 nF, 33 pF, and 100 pF for VBAT_BB, and 100 nF, 33 pF, and 10 pF for VBAT_RF. Place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from the external application should be a single voltage source, split into two sub-paths using a star structure. The VBAT_BB trace width should be at least 1 mm, and the VBAT_RF trace width at least 2 mm. As a general rule, longer VBAT traces should be made wider.

To prevent damage from electrical surges and ESD, it is recommended to use a TVS component with a low reverse stand-off voltage (VRWM) of 4.5 V, low clamping voltage (VC), and high reverse peak pulse current (IPP).

The following figure shows the star structure of the power supply.

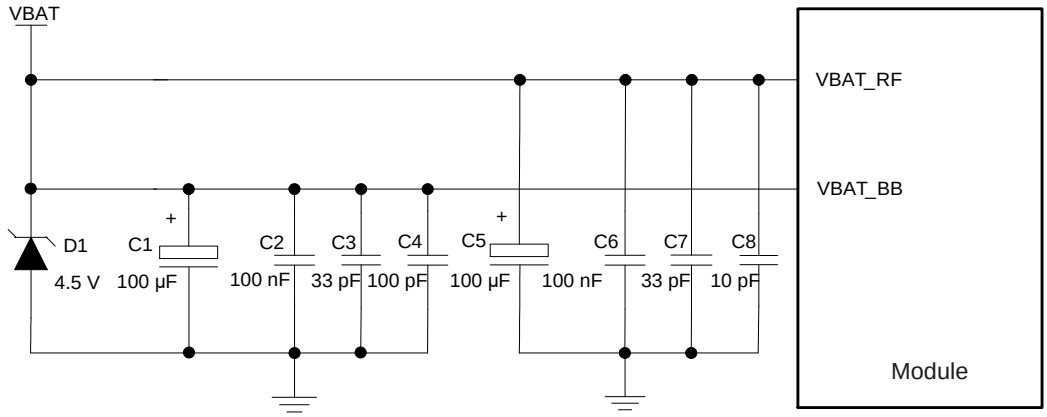


Figure 7: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

The performance of the module heavily relies on the power source. The power supply must provide a minimum current of 1.5 A. If the voltage drop between the input and output is minimal, using an LDO is recommended for powering the module. However, if there is a large voltage difference between the input source and the required output (VBAT), a buck converter is the preferred option for the power supply.

The following figure shows a reference design for a +5.0 V input power source. The power supply provides a typical output of around 3.8 V with a maximum load current of 3.0 A.

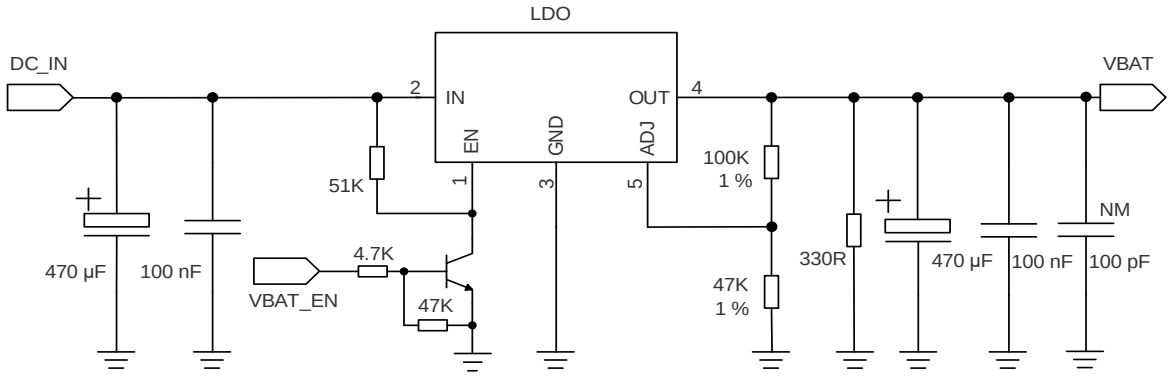


Figure 8: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

3.6.4. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [3]***.

3.7. Turn On

3.7.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	Description	Comment
PWRKEY	15	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.

To turn on the module from power-down mode, drive the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY and release it once the STATUS pin outputs a low level. The STATUS pin acts as an indicator to show that the module has been

turned on normally.

The reference circuit is illustrated in the following figure.

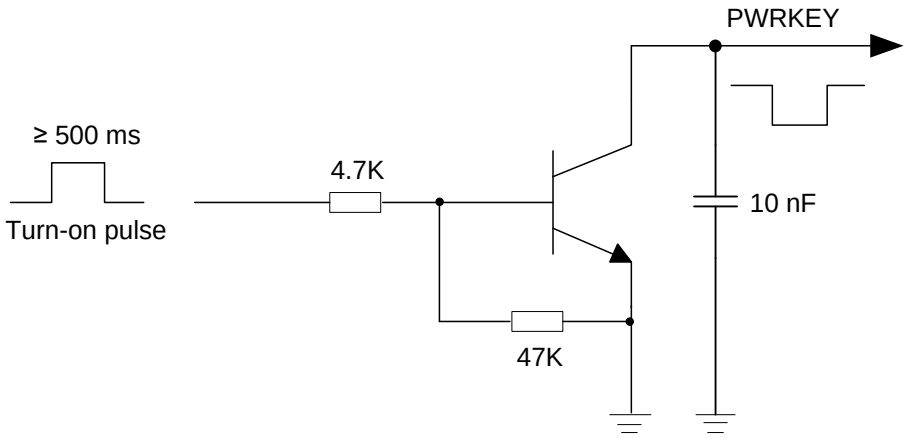


Figure 9: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is by using a button directly. Since pressing the button may generate electrostatic discharge (ESD) from fingers, it is essential to place a TVS component near the button for ESD protection.

A reference circuit is shown in the following figure.

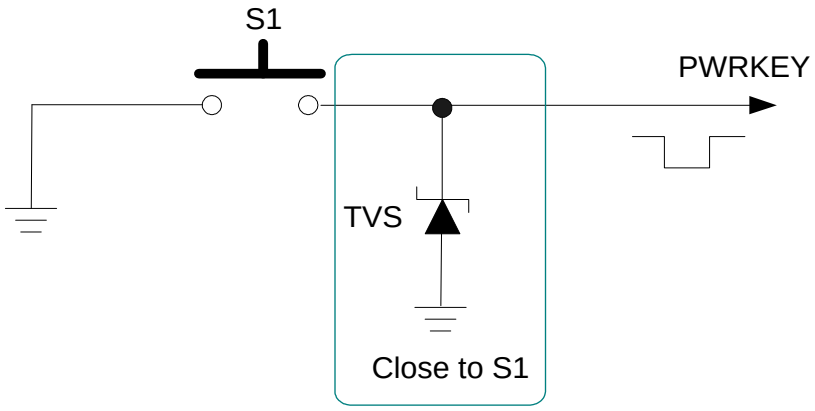


Figure 10: Turn On the Module Using a Button

The turn-on timing is illustrated in the following figure.

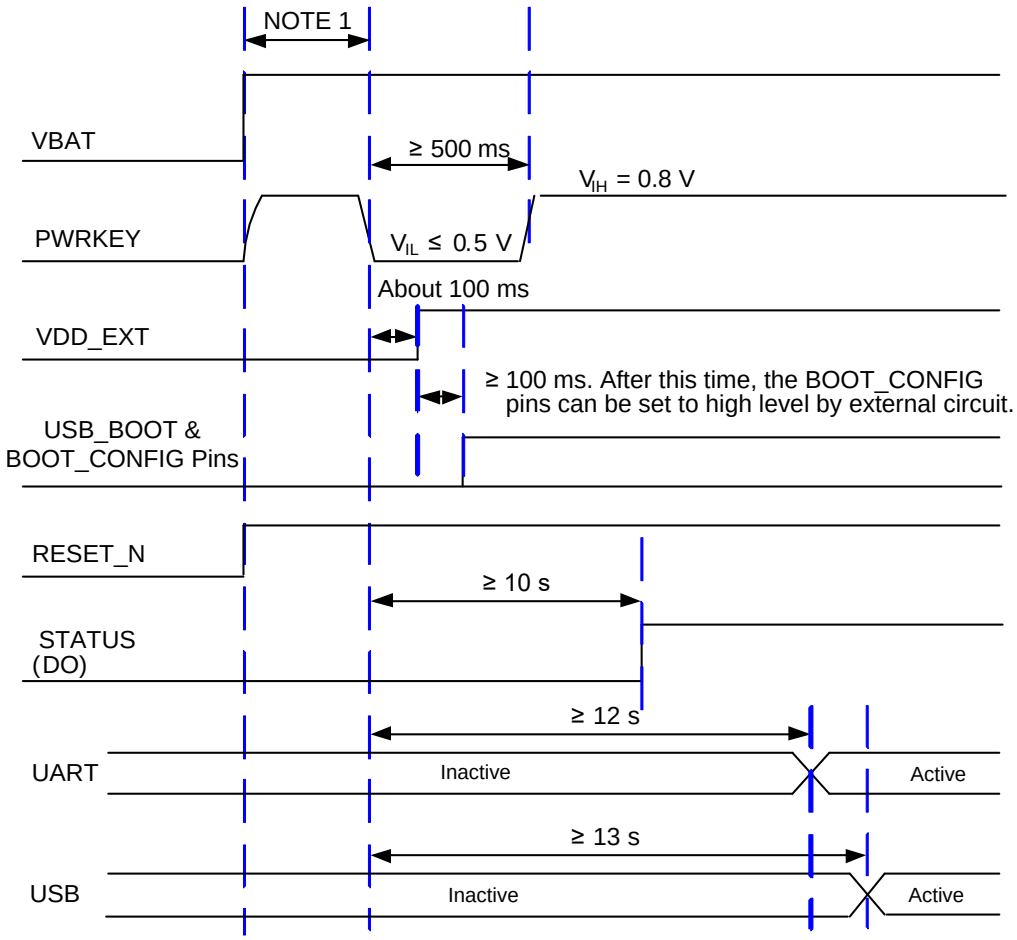


Figure 11: Turn-on Timing

NOTE

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to wait at least 30 ms after powering up VBAT before pulling down the PWRKEY pin.
2. For automatic module startup without requiring a turn-off, connect PWRKEY directly to GND with a recommended 10 kΩ resistor.
3. Do not pull up the USB_BOOT pin and BOOT_CONFIG pins (SPI_CLK, PCM_CLK and PCM_SYNC) before startup.

3.8. Turn Off

Either of the following methods can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD**

3.8.1. Turn Off with PWRKEY

To power down the module, drive the PWRKEY pin to a low level for at least 650 ms. The module will begin the power-down process once the PWRKEY pin is released. The turn-off timing is shown in the following figure.

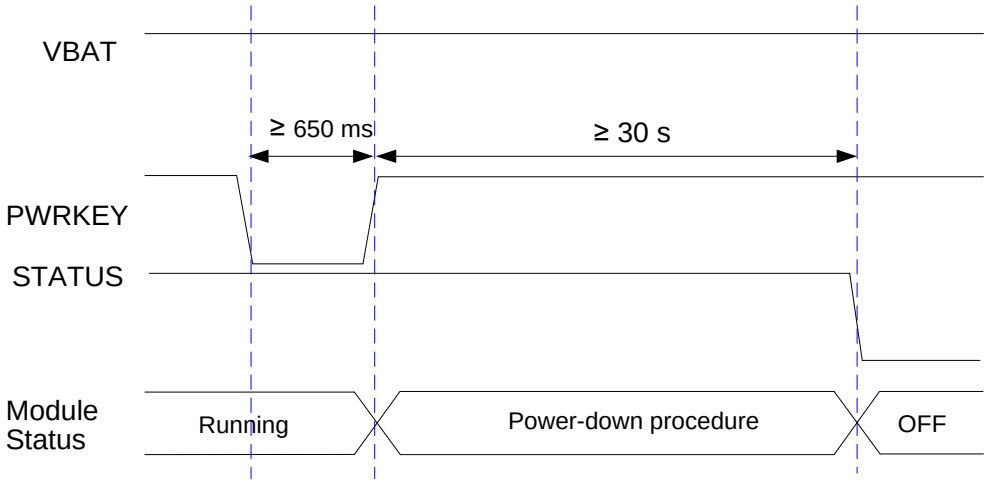


Figure 12: Turn-off Timing

3.8.2. Turn Off with AT Command

Using the **AT+QPOWD** command is another safe method to turn off the module, similar to turning it off via the PWRKEY pin. See ***document [3]*** for details about the **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after the module is turned off by PWRKEY or AT command can the power supply be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after a successful turn-off.

3.9. Reset

The module can be reset by driving RESET_N low for 150–460 ms.

Table 8: Pin Definition of RESET_N

Pin Name	Pin No.	Description	Comment
RESET_N	17	Reset the module	Require pull-up resistor to 1.8 V internally. Active low. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

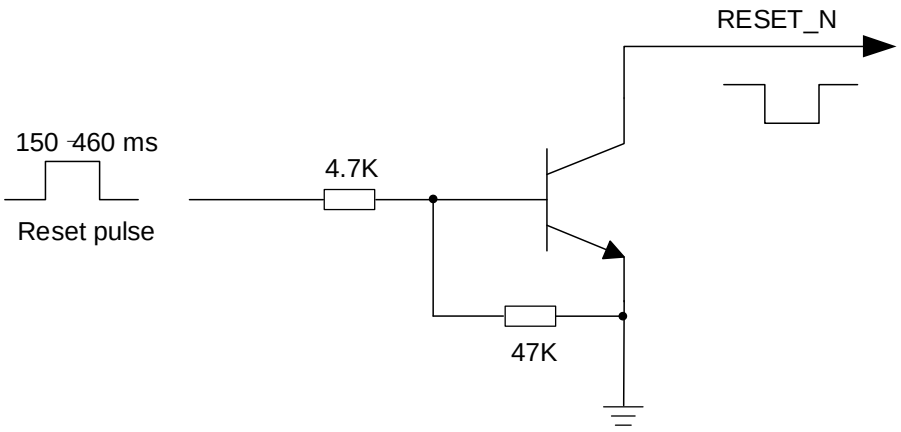


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

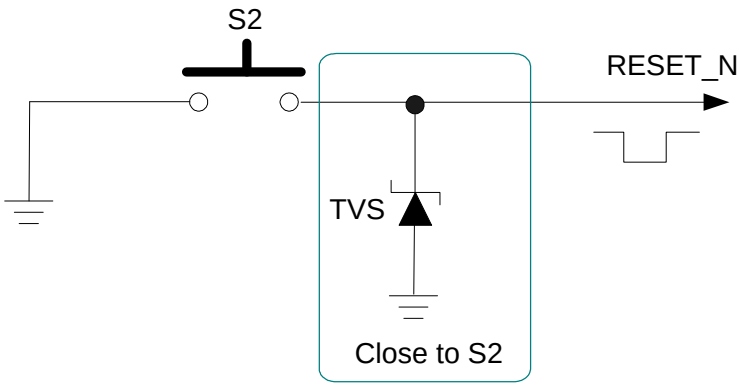


Figure 14: Reference Circuit of RESET_N by Using a Button

The reset timing is illustrated in the following figure.

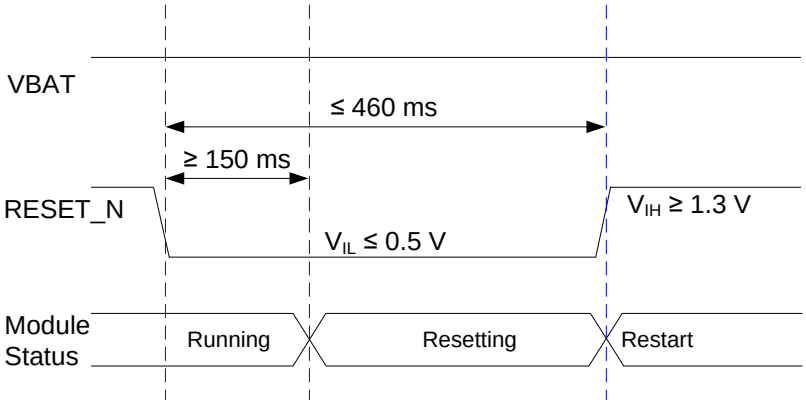


Figure 15: Reset Timing

NOTE

1. Use the RESET_N pin only if the module cannot be turned off using the **AT+QPOWD** command or the PWRKEY pin.
2. Ensure there are no large capacitors connected to the PWRKEY and RESET_N pins.

3.10. (U)SIM Interfaces

The module provides two (U)SIM interfaces, and only one (U)SIM card can work at a time. The (U)SIM1 and (U)SIM2 cards can be switched by **AT+QDSIM**. For more details, see ***document [6]***.

The (U)SIM interface of the module complies with ETSI and IMT-2000 standards, supporting both 1.8 V and 3.0 V (U)SIM cards.

Table 9: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM_GND	47	-	Specified ground for (U)SIM card	Connect to ground of (U)SIM card connector.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	

USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_PRESENCE	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM2_DATA	86	DIO	(U)SIM2 card data	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_PRESENCE	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports hot-plugging of (U)SIM cards through the USIM_PRESENCE pin, with options for low-level and high-level detection. This feature is disabled by default but can be enabled using the **AT+QSIMDET** command. See ***document [3]*** for more details about **AT+QSIMDET**.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

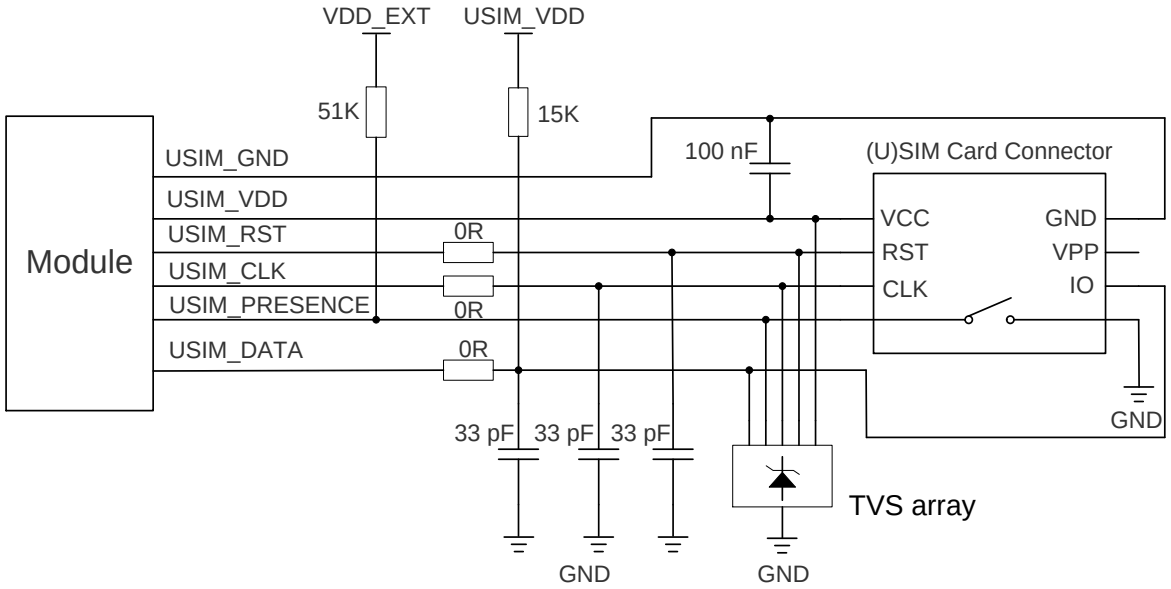


Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_PRESENCE unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

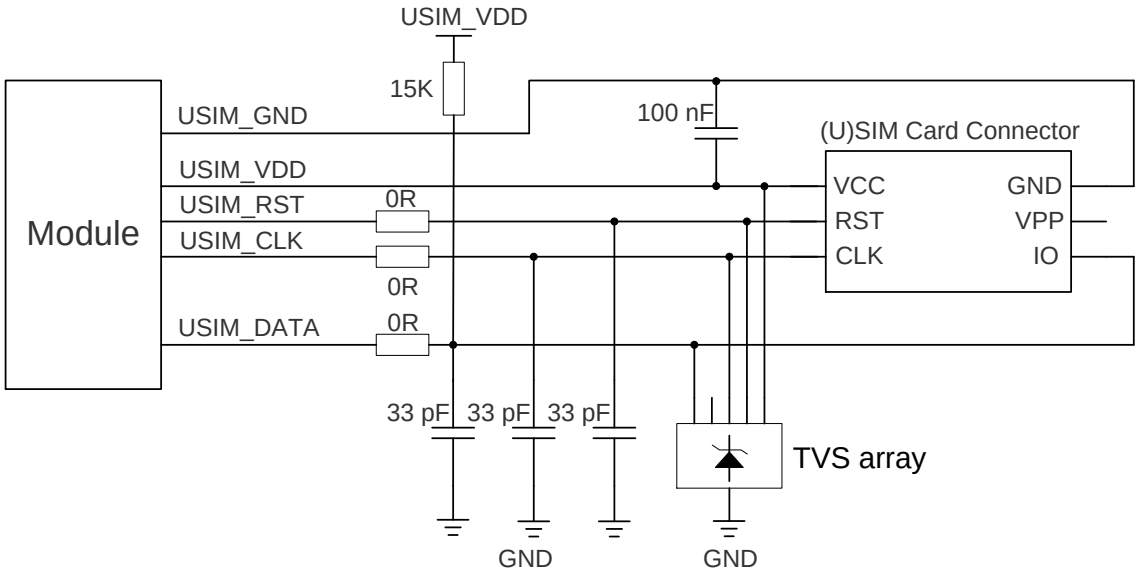


Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To improve the reliability and performance of the (U)SIM card in your applications, follow these guidelines when designing the (U)SIM circuit:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, add a TVS array with parasitic capacitance not exceeding 15 pF. Include 0 Ω resistors in series between the module and the (U)SIM card for easier debugging. Use 33 pF capacitors to filter RF interference. Ensure the (U)SIM circuit is located close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.11. USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification, supporting both high-speed (480 Mbps) and full-speed (12 Mbps) modes. This interface operates only as a slave device.

The interface can be used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

The following table shows the pin definition of USB interface.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	
USB_VBUS	8	AI	USB connection detect	Typical: 5.0 V A test point must be reserved.
GND	3	-	Ground	

For more details about USB 2.0 specifications, visit http://www.usb.org/home.

The test points are recommended to be reserved for firmware upgrade and software debugging in your design. The following figure shows a reference circuit of USB interface.

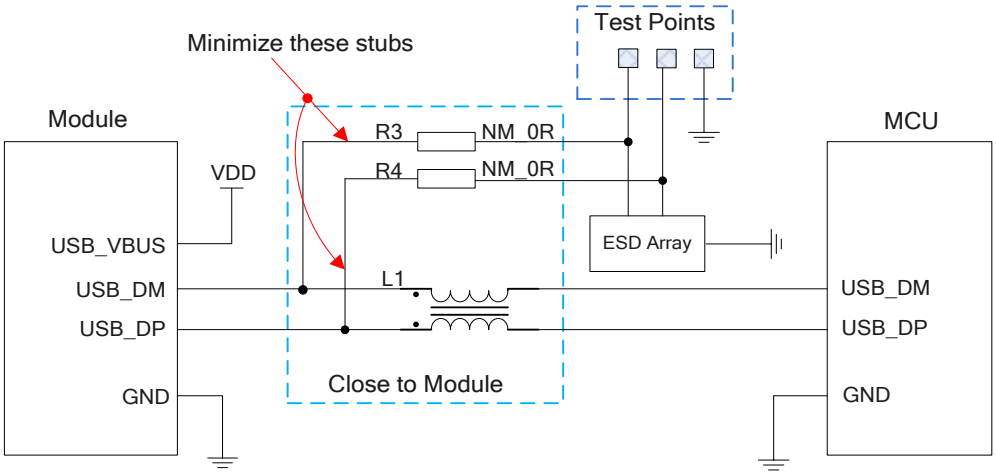


Figure 18: Reference Circuit of USB Interface

A common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R3 and R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To ensure compliance with the USB 2.0 specification when designing the USB interface, follow these guidelines:

- Route the USB signal traces as differential pairs surrounded by ground. The impedance of the USB differential traces should be 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components as close to the USB connector as possible.

3.12. UART Interfaces

The module provides two UART interfaces: the main UART and the debug UART. The following shows their features.

- Main UART interface supports baud rates of 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps and 921600 bps. It also supports RTS and CTS hardware flow control, and can be used for AT command communication and data transmission.

- Debug UART interface supports 115200 bps baud rate and is used for Linux console and log output.

The following tables show the pin definition of the two UART interfaces.

Table 11: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	39	DO	Ring indication	1.8 V power domain. If unused, keep them open.
DCD	38	DO	Data carrier detect	
CTS	36	DO	Clear to send signal from the module	1.8 V power domain. Connect to MCU's CTS. If unused, keep it open.
RTS	37	DI	Request to send signal to the module	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
DTR	30	DI	Data terminal ready. Sleep mode control	1.8 V power domain. Pulled up by default.

				When it remains at low level, it can wake up the module. If unused, keep it open.
TXD	35	DO	Transmit	1.8 V power domain. If unused, keep them open.
RXD	34	DI	Receive	

Table 12: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved.
DBG_RXD	22	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

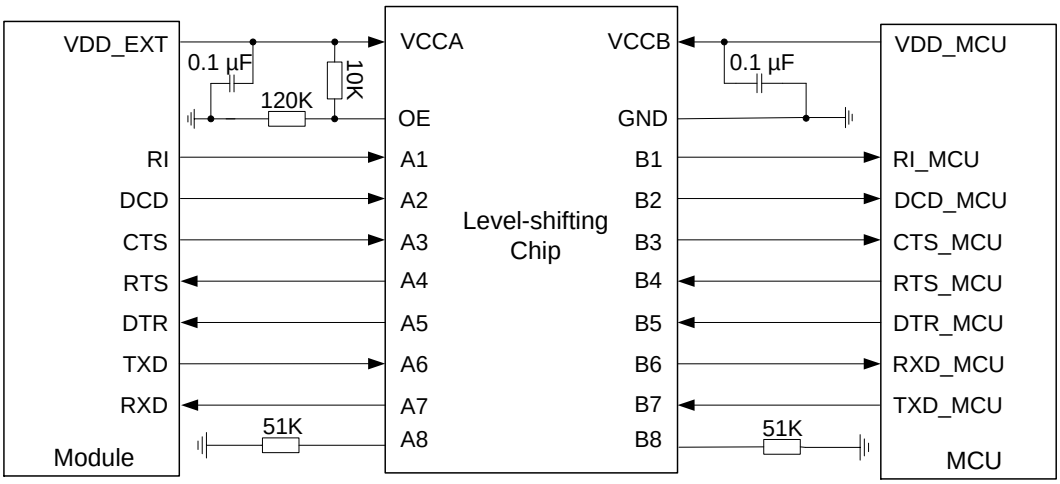


Figure 19: Reference Circuit with Level-shifting Chip

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

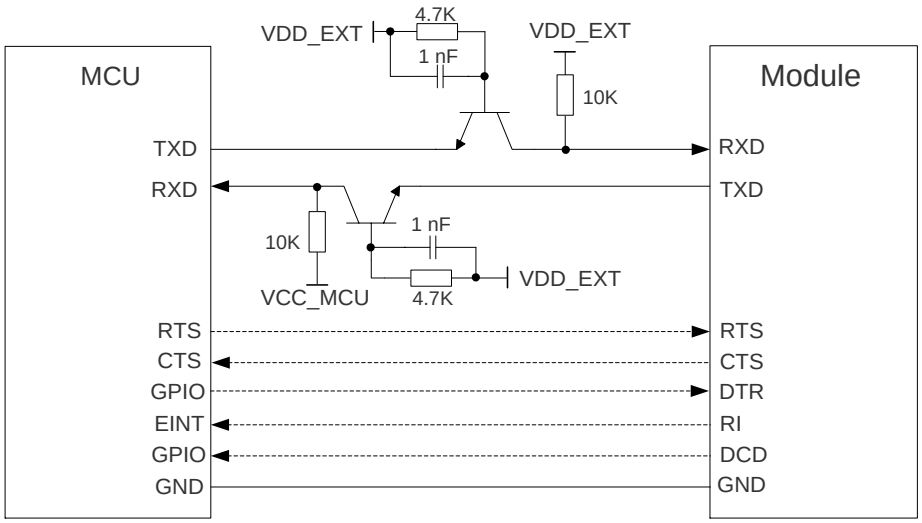


Figure 20: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

3.13. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design which supports the following modes, and provides one I2C interface:

- Short frame synchronization: The module works as both the master and slave devices.
- Long frame synchronization: The module only works as the master device.

In short frame sync mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on its rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In long frame sync mode, the data is also sampled on the falling edge of the PCM_CLK and transmitted on its rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC.

The module supports a 16-bit linear data format. The following figures show the short frame sync mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the long frame sync mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

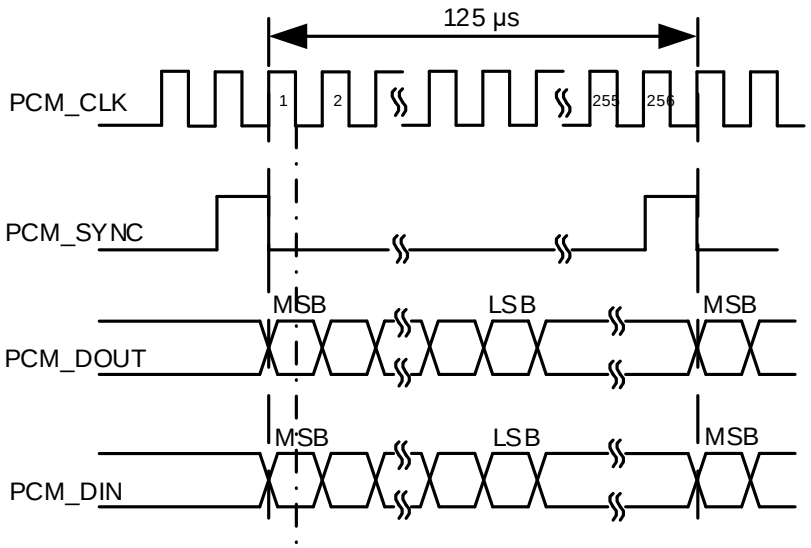


Figure 21: Short Frame Sync Mode Timing

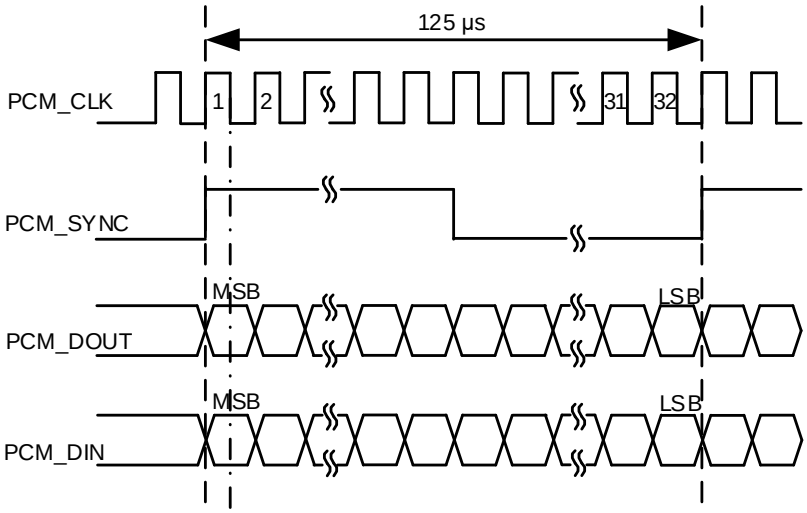


Figure 22: Log Frame Sync Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 13: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DIO	PCM data frame sync	1.8 V power domain. In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM_CLK	4	DIO	PCM data clock	
I2C_SCL	40	OD	I2C serial clock (for external codec)	Require an external pull-up to 1.8 V If unused, keep them open.
I2C_SDA	41	OD	I2C serial data (for external codec)	

The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [3]*** about **AT+QDAI** for details.

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

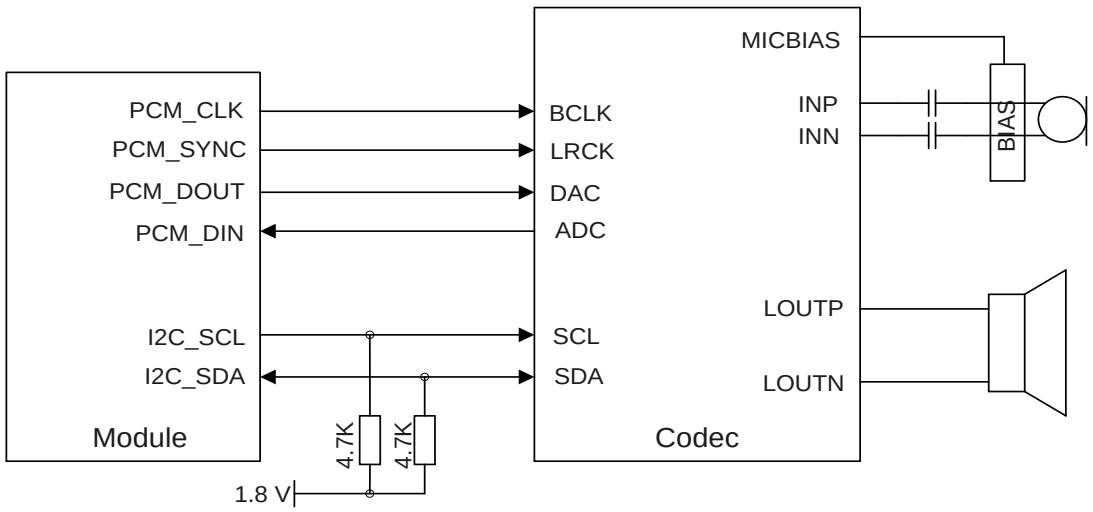


Figure 23: Reference Circuit of PCM Application with Audio Codec

NOTE

1. Reserve RC circuits (R = 22 Ω, C = 22 pF) to the PCM traces, especially PCM_CLK, close to codec.
2. The module only works as a master device pertaining to I2C interface.

3.14. SPI

SPI functions only as a master device, providing a duplex, synchronous serial communication link with peripheral devices. It is designed for a one-to-one connection without the need for chip selection. It operates at 1.8 V with clock rates up to 50 MHz.

The following table shows the pin definition of SPI

Table 14: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. If unused, keep them open.
SPI_MOSI	27	DO	SPI master-out slave-in	
SPI_MISO	28	DI	SPI master-in slave-out	

The following figure shows a reference design of SPI with a peripheral.

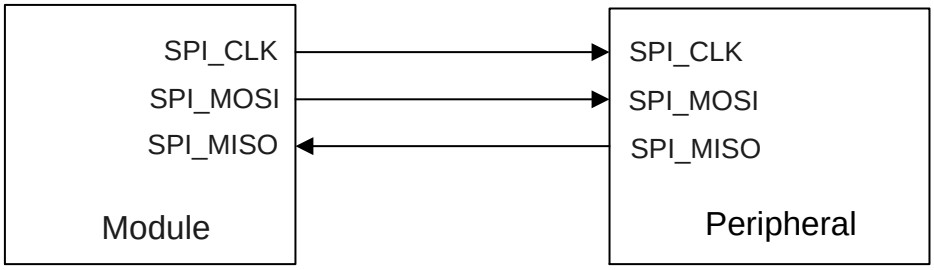


Figure 24: Reference Circuit of SPI with Peripheral

NOTE

The module supports 1.8 V SPI. If your application uses a 3.3 V processor or device interface, a voltage-level translator should be added between the module and the peripheral.

3.15. Indication Signals

3.15.1. Network Status Indication

The module provides a network indication pin, NETLIGHT, which controls the LED status. The tables below show the pin definition and logic level changes of NETLIGHT for different network status.

Table 15: Pin Definition of Network Status Indication

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.

Table 16: Working State of Network Status Indication

Pin Name	Logic Level Change	Network Status
NETLIGHT	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

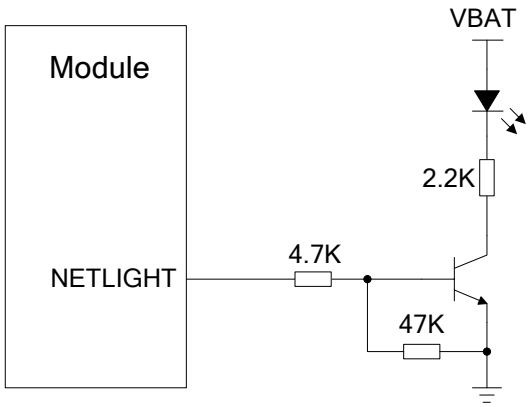


Figure 25: Reference Circuit of Network Status Indication

3.15.2. STATUS

The STATUS pin is set as the module's operating status indicator. It will output high level when the module is turned on normally. The following table describes the pin definition of STATUS.

Table 17: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operating status	1.8 V power domain. If unused, keep it open.

The following figure shows the reference circuit of STATUS.

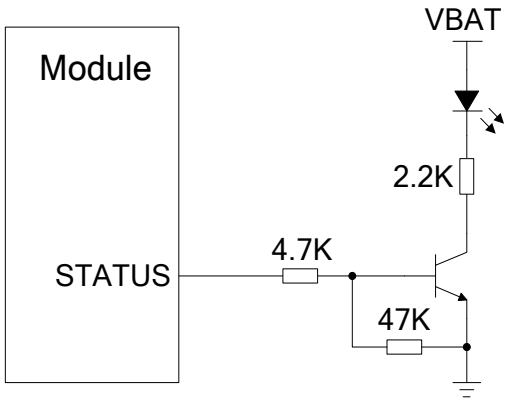


Figure 26: Reference Circuit of STATUS

3.15.3. RI

AT+QCFG="risignaltype","physical" can be used to configure RI behaviors. See ***document [4]*** for details.

No matter on which port (UART port, USB AT port or USB modem port) a URC is presented, URC will trigger the behaviors of RI pin.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. See ***document [3]*** for details.

The default behaviors of the RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document [4]*** for details.

Table 18: Default Behaviors of RI

Status	Response
Idle	RI keeps at high level.
URC	RI outputs 120 ms low pulse when a new URC returns.

3.16. ADC Interface

The module provides one analog-to-digital converter (ADC) interface. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. For more details about the command, see ***document [3]*** .

To improve the accuracy of ADC input voltage values, the trace of ADC should be surrounded by ground.

Table 19: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep it open.

The following table describes the characteristics of ADC interface.

Table 20: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTE

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pin when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.17. USB_BOOT Interface

The module provides a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 21: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter download mode	1.8 V power domain. Active high. A test point is recommended to be reserved.

The following figures show the reference circuit of the USB_BOOT interface and the timing of entering forced download mode.

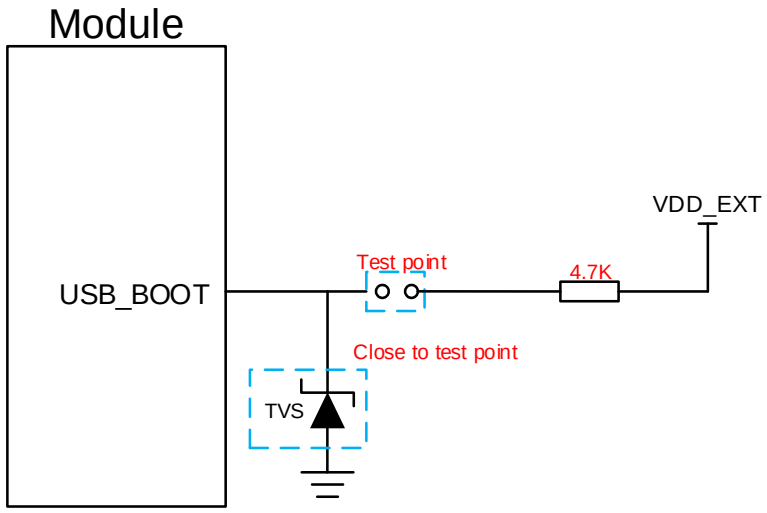


Figure 27: Reference Circuit of USB_BOOT Interface

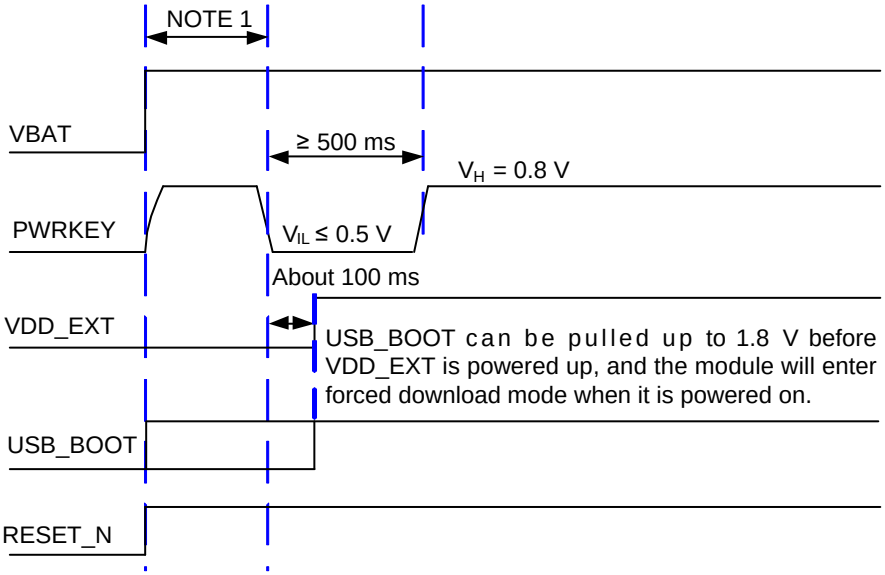


Figure 28: Timing of Entering Forced Download Mode

NOTE

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to wait at least 30 ms after powering up VBAT before pulling down the PWRKEY pin.
2. Follow the above timing when using MCU to control the module to enter the forced download mode. Do not pull up USB_BOOT to 1.8 V before powering up VBAT.
3. If you need to manually force the module to enter forced download mode, directly connect the test points shown in ***Figure 27***.

4 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The impedance of the antenna port is 50 Ω. The antenna interfaces of the module are shown as follow:

- One main antenna interface
- One diversity antenna interface (designed to minimize signal loss caused by high-speed movement and multipath effects)
- One GNSS antenna interface

4.1. Cellular Network

4.1.1. Antenna Interfaces & Frequency Bands

The pin definition of main antenna and diversity antenna interfaces is shown below.

Table 22: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DIV	56	AI	Diversity antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 23: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz

WCDMA B5	824–849	869–894	MHz
LTE FDD B2	1850–1910	1930–1990	MHz
LTE FDD B4	1710–1755	2110–2155	MHz
LTE FDD B5	824–849	869–894	MHz
LTE FDD B12	699–716	729–746	MHz
LTE FDD B13	777–787	746–756	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz

4.1.2. Tx Power

The following table shows the Tx power.

Table 24: Tx Power

Frequency Band	Max. Tx Power	Min. Tx Power
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE-FDD bands	23 dBm ±2 dB	< -39 dBm

4.1.3. Receiver Sensitivity

The following tables show the conducted RF receiver sensitivity.

4.1.3.1. I491-NAX Conducted RF Receiver Sensitivity

Table 25: I491-NAX Conducted RF Receiver Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm

WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

4.1.3.2. I491-NAXD Conducted RF Receiver Sensitivity

Table 26: I491-NAXD Conducted RF Receiver Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
WCDMA B2	-110 dBm	-110 dBm	-112.5 dBm	-104.7 dBm
WCDMA B4	-110 dBm	-110 dBm	-112.5 dBm	-106.7 dBm
WCDMA B5	-111 dBm	-111 dBm	-113 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98 dBm	-99 dBm	-102.2 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.8 dBm	-99.5 dBm	-102.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.4 dBm	-100 dBm	-102.7 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-99.2 dBm	-100 dBm	-102.5 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-97.6 dBm	-99 dBm	-102.2 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-99.1 dBm	-99.9 dBm	-102.7 dBm	-93.8 dBm

4.1.4. Reference Design

A reference design of ANT_MAIN and ANT_DIV antennas is shown as below. A dual L-type circuit should be reserved for better RF performance. The capacitors C1–C4 are not mounted by default.

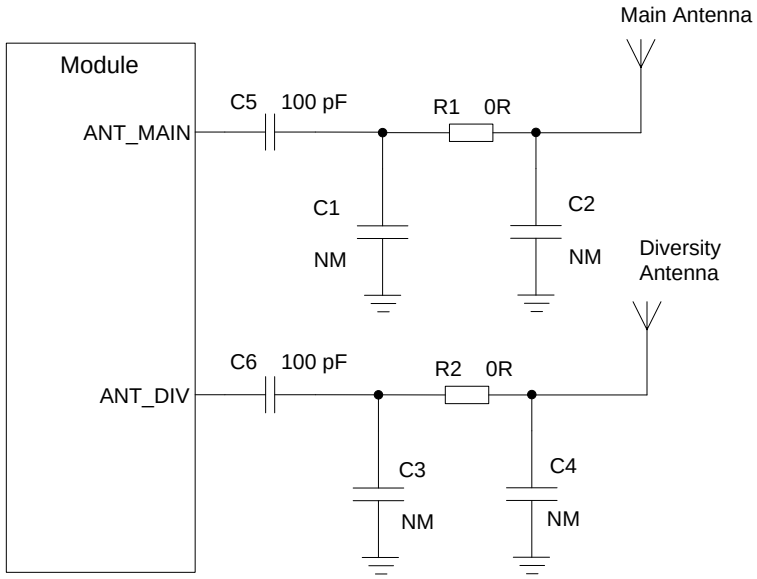


Figure 29: Reference Circuit of RF Antenna Interfaces

NOTE

1. Keep a proper distance between the main antenna and the diversity antenna to improve the receiver sensitivity.
2. For the operation of ANT_MAIN and ANT_DIV, see **AT+QCFG="divctl"** in ***document [4]*** for more details.
3. Place the dual L-type components (R1/C1/C2, R2/C3/C4, C5/C6) as close to the antenna as possible.
4. Notes on C5 and C6:
   1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C5 and C6.
      b) If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.

4.2. GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

It supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz update rate via USB interface by default.

The GNSS engine is disabled by default and can be enabled via AT command. For more details about GNSS engine technology and configurations, see ***document [1]***.

4.2.1. Antenna Interface & Frequency Bands

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 27: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 28: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1601.7 ±4.2	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

4.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 29: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	34.6	s
		AGNSS start	11.57	s
	Warm start @ open sky	Autonomous	26.09	s
		XGNSS start	3.7	s
	Hot start @ open sky	Autonomous	1.8	s
		AGNSS start	3.4	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.2.3. Reference Design

It is generally recommended to use a passive antenna for the module. However, if your application requires an active antenna, it is advised to reserve a π-type attenuation circuit and ensure the power system design uses a high-performance LDO.

A reference design of GNSS antenna is shown as below.

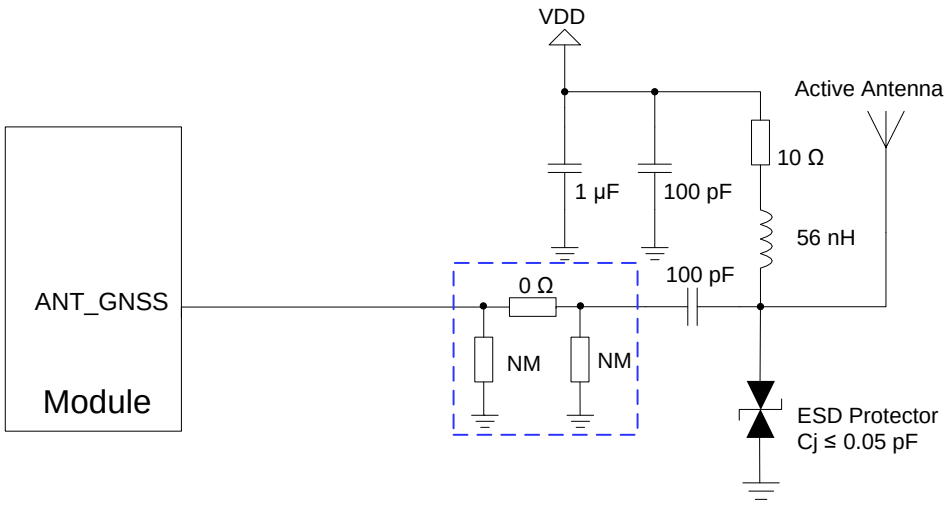


Figure 30: Reference Circuit of GNSS Antenna

NOTE

1. Use an external LDO to supply power if required by the active antenna.
2. If a passive antenna is used, the VDD circuit is not needed.
3. It is recommended to reserve an ESD protection component D1 and the junction capacitance should not exceed 0.05 pF.
4. It is recommended to use a passive antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

4.2.4. Layout Guidelines

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50 Ω.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic

impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

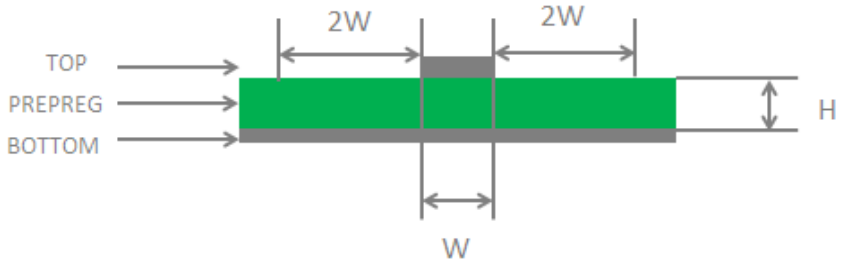


Figure 31: Microstrip Design on a 2-layer PCB

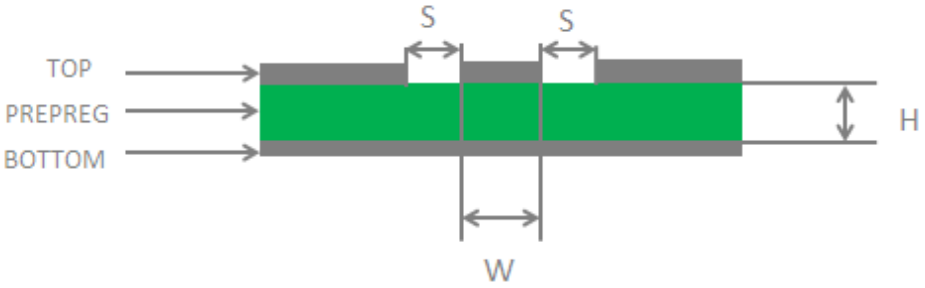


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

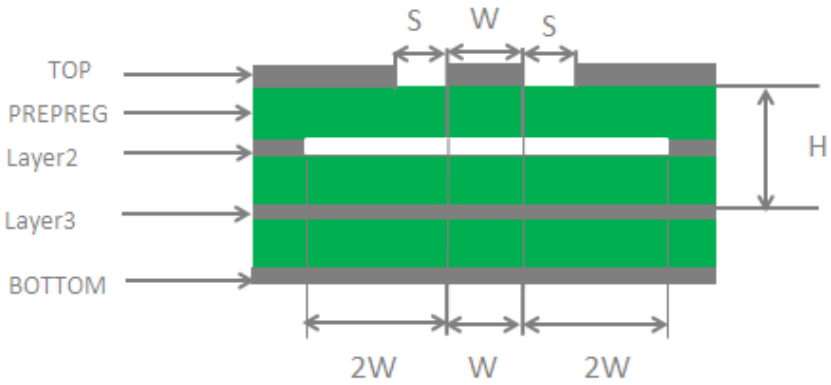


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

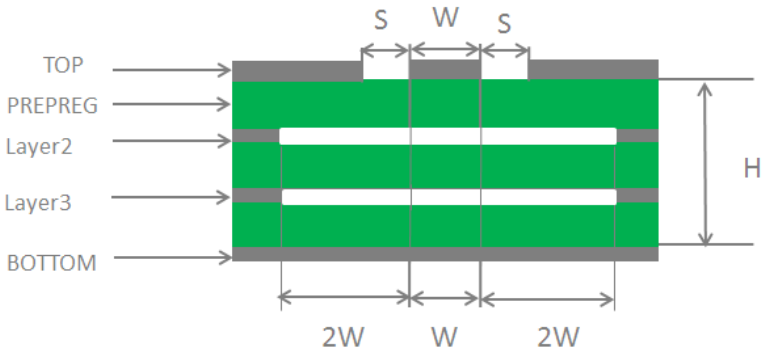


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, refer to ***document [7]***.

4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 30: Antenna Requirements

Type	Requirements
GNSS (Optional)	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)

	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: ● Active antenna noise figure: < 1.5 dB ● Active antenna embedded LNA gain: < 17 dB
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max. input power: 50 W ● Input impedance: 50 Ω ● Vertical polarization ● Cable insertion loss: – **< 1 dB:** LB (<1 GHz) – **< 1.5 dB:** MB (1–2.3 GHz)

4.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

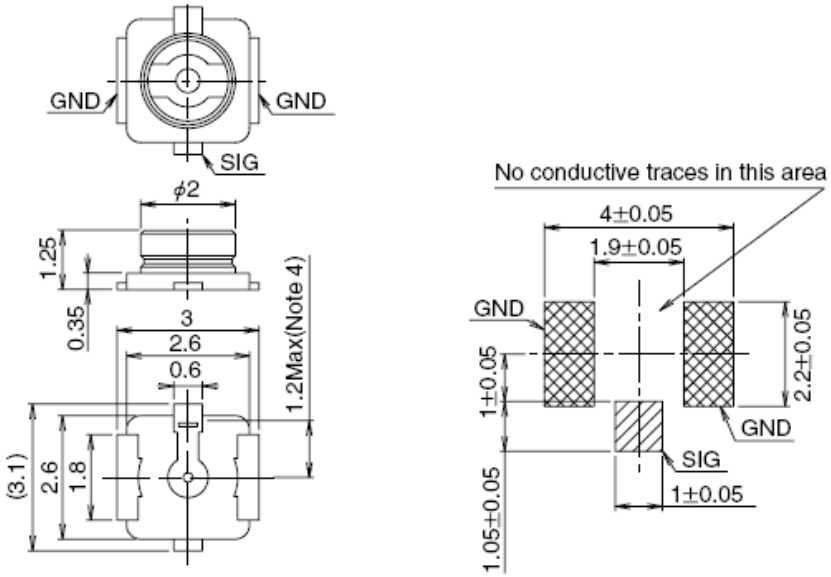


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

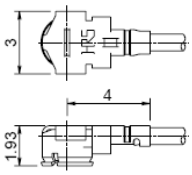
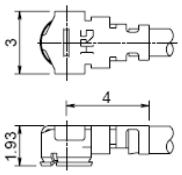
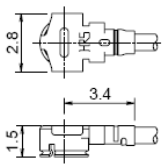
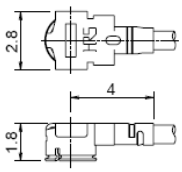
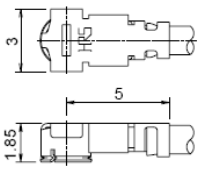
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

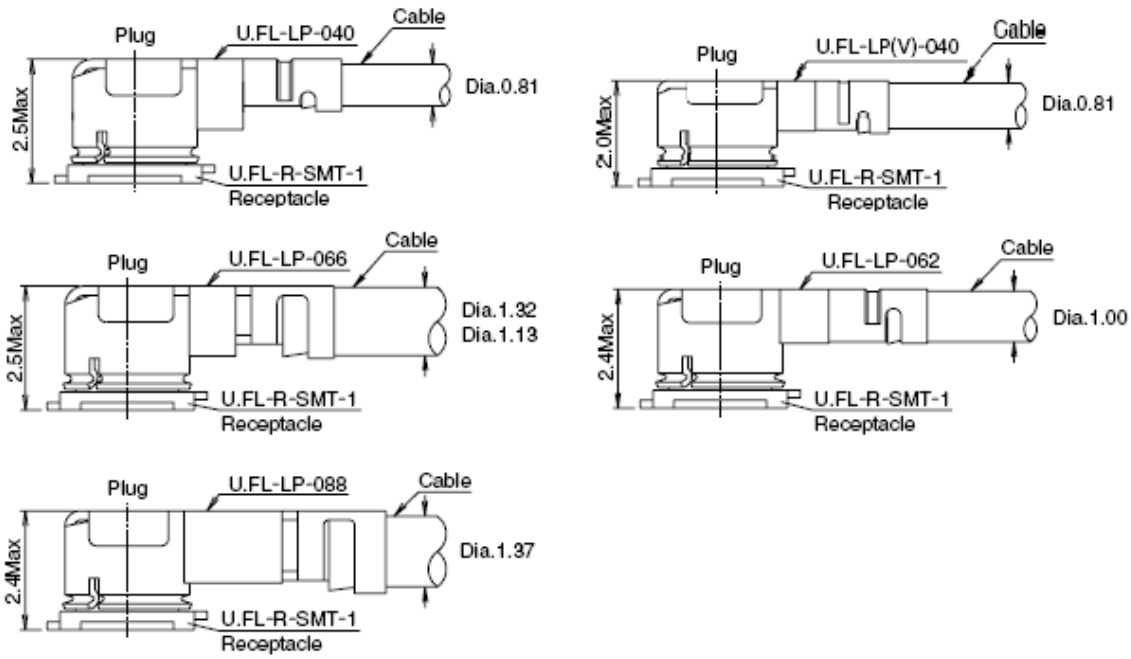


Figure 37: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.3	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

5.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak supply current	At maximum power control level	-	-	1.5	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 33: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [6]	-35	+25	+75	ºC
Extended Temperature Range [7]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[6] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[7] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -35 °C or 75 to 85 °C, the module remains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

5.4. Power Consumption

5.4.1. I491-NAX Power Consumption

Table 34: I491-NAX Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	9	μA
Sleep	**AT+CFUN=0** (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.1	mA
	WCDMA PF = 64 (USB Suspend)	2.2	mA
	WCDMA PF = 512 (USB disconnected)	1.6	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB Suspend)	2.7	mA
	LTE-FDD PF = 256 (USB disconnected)	1.8	mA
Idle	WCDMA PF = 64 (USB disconnected)	16.7	mA
	WCDMA PF = 64 (USB connected)	32.2	mA
	LTE-FDD PF = 64 (USB disconnected)	14.0	mA
	LTE-FDD PF = 64 (USB connected)	32.6	mA
WCDMA data transmission	WCDMA B2 HSDPA @ 21.74 dBm	528	mA
	WCDMA B2 HSUPA @ 21.47 dBm	536	mA
	WCDMA B4 HSDPA @ 22.67 dBm	542	mA
	WCDMA B4 HSUPA @ 22.30 dBm	550	mA
	WCDMA B5 HSDPA @ 22.63 dBm	523	mA
	WCDMA B5 HSUPA @ 22.31 dBm	523	mA
LTE data transmission	LTE-FDD B2 @ 23.08 dBm	694	mA
	LTE-FDD B4 @ 23.31 dBm	691	mA

	LTE-FDD B5 @ 23.23 dBm	586	mA
	LTE-FDD B12 @ 23.03 dBm	613	mA
	LTE-FDD B13 @ 23.13 dBm	626	mA
	LTE-FDD B25 @ 22.96 dBm	689	mA
	LTE-FDD B26 @ 23.11 dBm	636	mA
WCDMA voice call	WCDMA B2 @ 23.08 dBm	581	mA
	WCDMA B4 @ 23.21 dBm	557	mA
	WCDMA B5 @ 23.29 dBm	534	mA

5.4.2. I491-NAXD Power Consumption

Table 35: I491-NAXD Power Consumption

Test Item	Condition	Typ.	Unit
Turn-off	Turn off	9	μA
Sleep	**AT+CFUN=0** (USB disconnected)	1.1	mA
	WCDMA PF = 64 (USB disconnected)	2.1	mA
	WCDMA PF = 64 (USB Suspend)	2.2	mA
	WCDMA PF = 512 (USB disconnected)	1.6	mA
	LTE-FDD PF = 64 (USB disconnected)	2.6	mA
	LTE-FDD PF = 64 (USB Suspend)	2.7	mA
	LTE-FDD PF = 256 (USB disconnected)	1.8	mA
Idle	WCDMA PF = 64 (USB disconnected)	16.7	mA
	WCDMA PF = 64 (USB connected)	32.2	mA
	LTE-FDD PF = 64 (USB disconnected)	14.0	mA
	LTE-FDD PF = 64 (USB connected)	32.6	mA
WCDMA data transmission	WCDMA B2 HSDPA @ 21.74 dBm	528	mA

	WCDMA B2 HSUPA @ 21.47 dBm	536	mA
	WCDMA B4 HSDPA @ 22.67 dBm	542	mA
	WCDMA B4 HSUPA @ 22.30 dBm	550	mA
	WCDMA B5 HSDPA @ 22.63 dBm	523	mA
	WCDMA B5 HSUPA @ 22.31 dBm	523	mA
LTE data transmission	LTE-FDD B2 @ 23.08 dBm	694	mA
	LTE-FDD B4 @ 23.31 dBm	691	mA
	LTE-FDD B5 @ 23.23 dBm	586	mA
	LTE-FDD B12 @ 23.03 dBm	613	mA
	LTE-FDD B13 @ 23.13 dBm	626	mA
	LTE-FDD B25 @ 22.96 dBm	689	mA
	LTE-FDD B26 @ 23.11 dBm	636	mA

5.4.3. GNSS Power Consumption

Table 36: GNSS Power Consumption

Description	Condition	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Passive antenna	54	mA
	Hot start @ Passive antenna	54	mA
	Lost state @ Passive antenna	53	mA
Tracking (**AT+CFUN=0**)	Open sky @ Passive antenna	32	mA

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 37: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.6. Thermal Dissipation

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On your PCB design, please keep placement of the module away from heating sources, especially high-power components such as ARM processor, audio power amplifier and power supply.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to your application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.

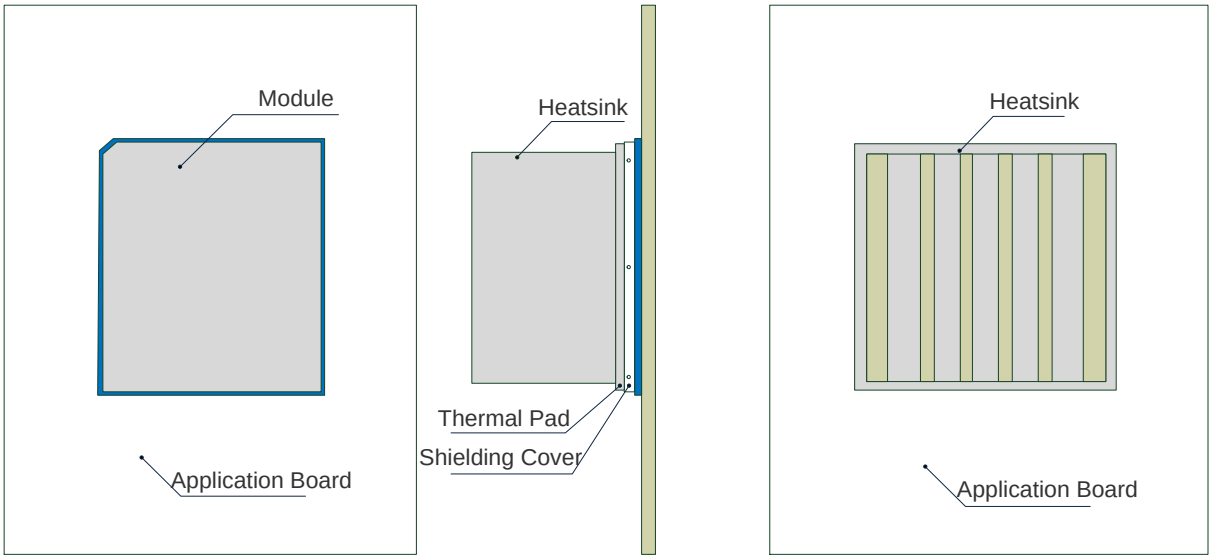


Figure 38: Referenced Heatsink Design (Heatsink at the Top of the Module)

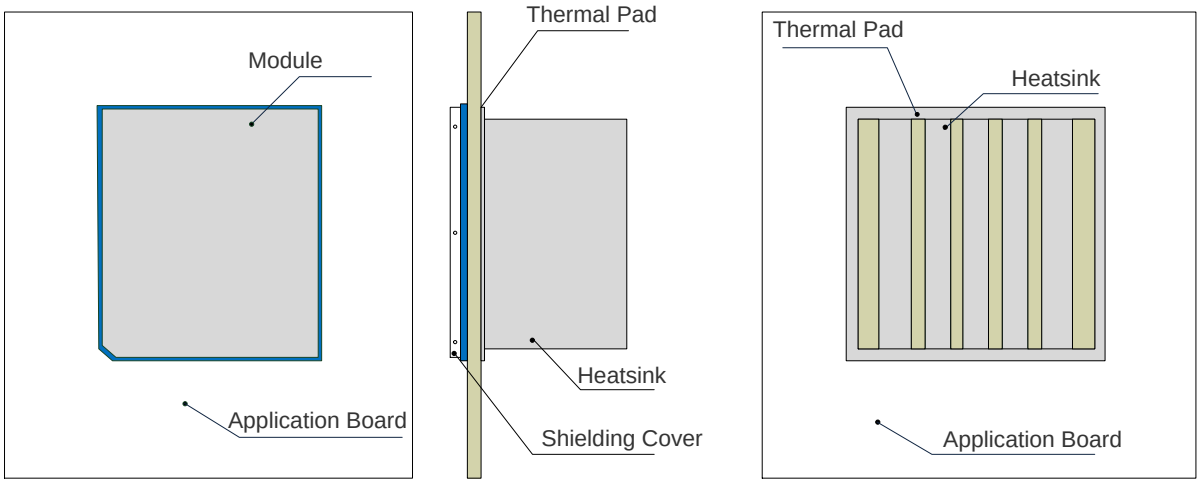


Figure 39: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTE

The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power and data rate). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. You can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value. For more details, see ***document [8]***.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

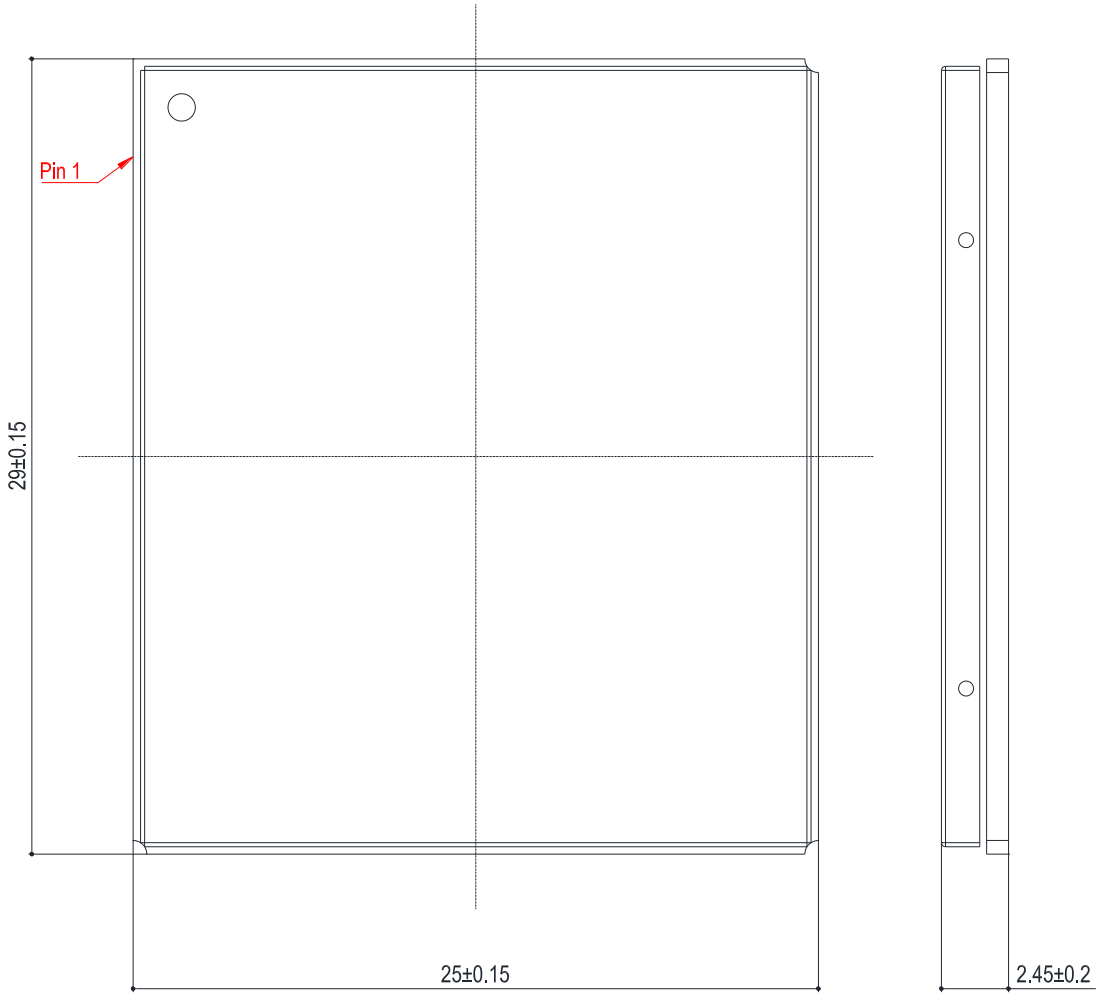


Figure 40: Top and Side Dimensions

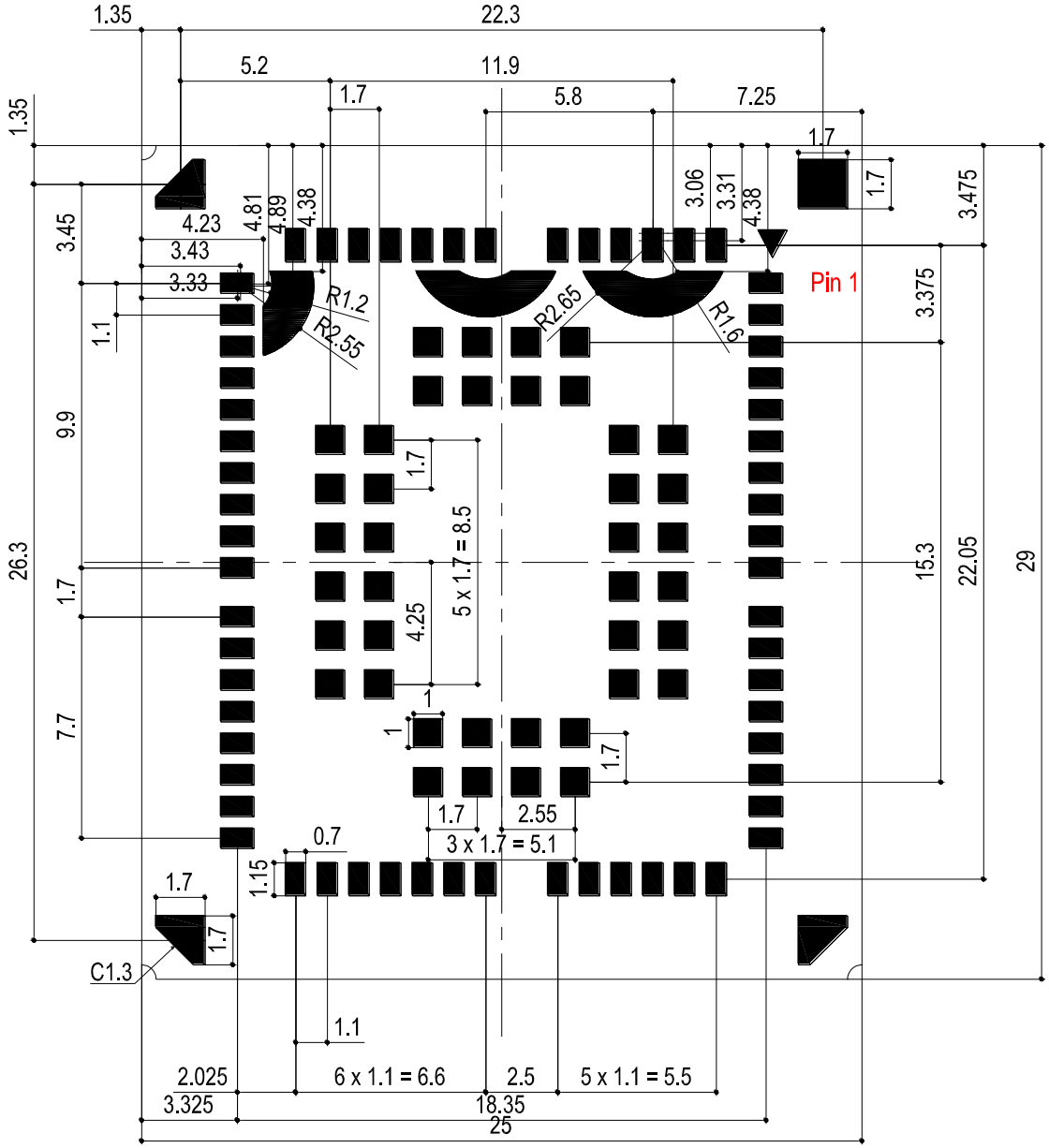


Figure 41: Bottom Dimensions (Bottom View)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

6.2. Recommended Footprint

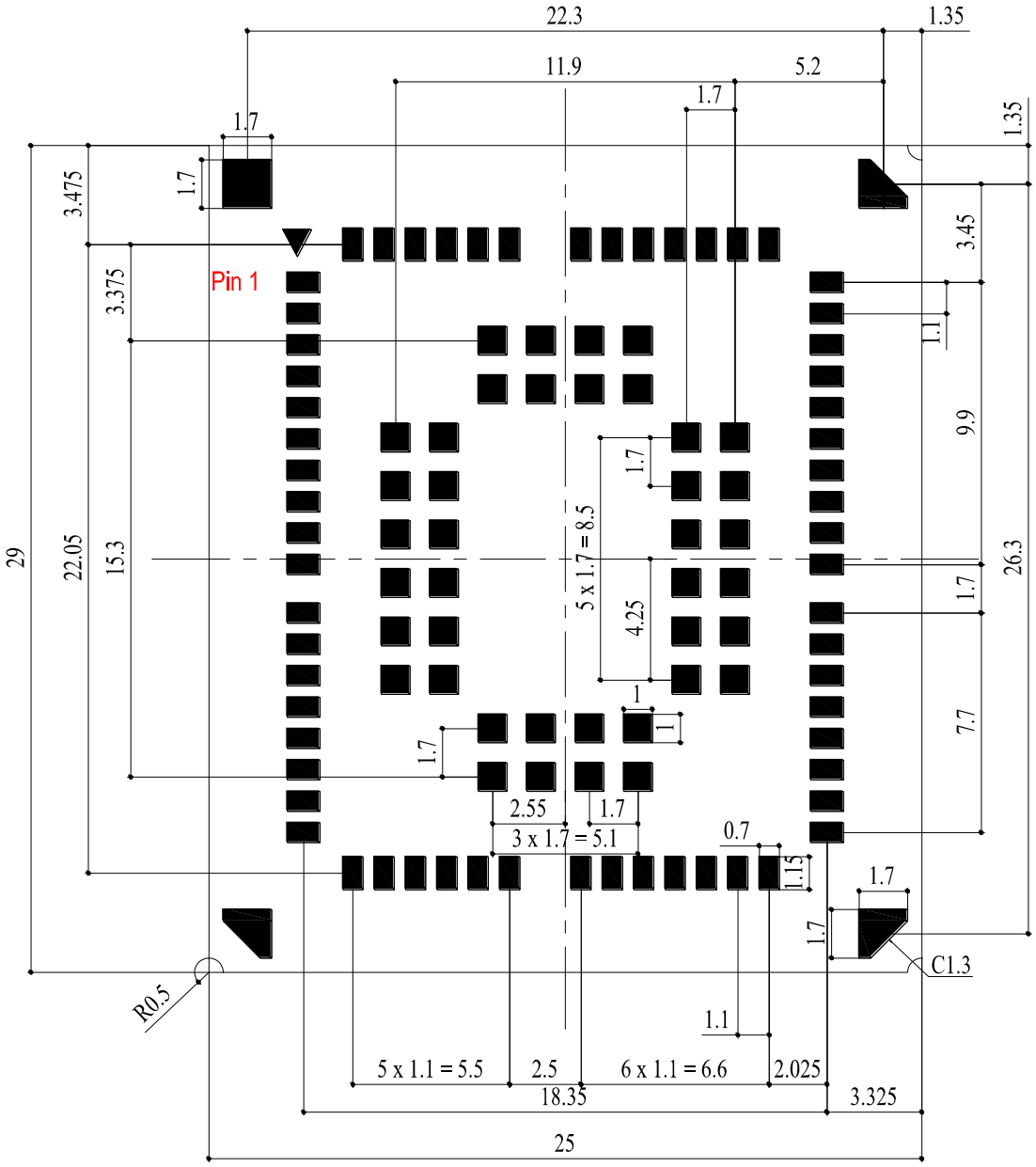


Figure 42: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

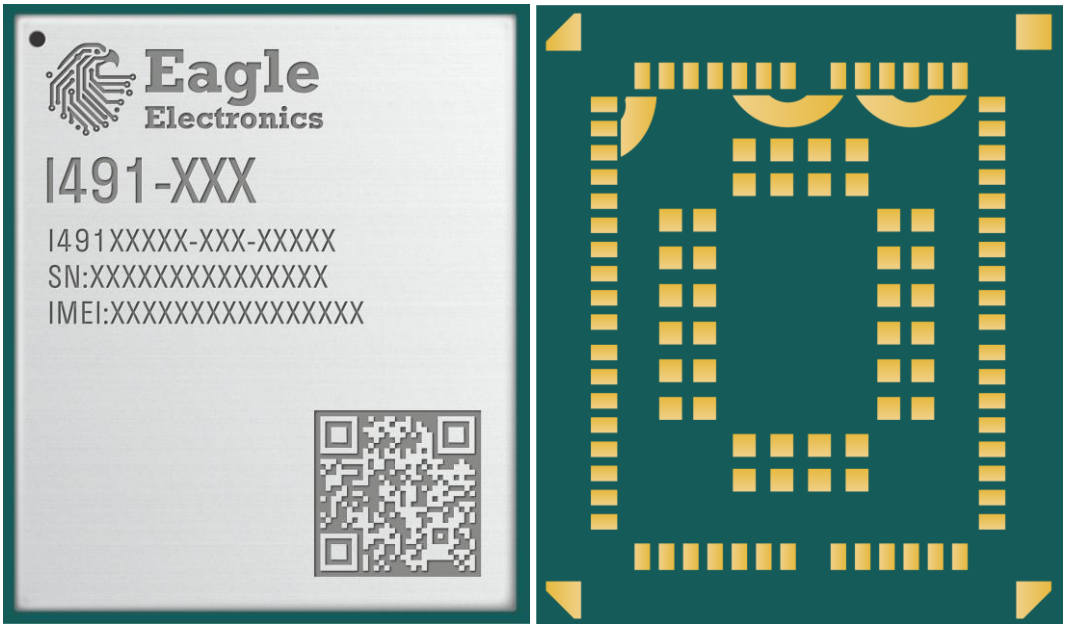


Figure 43: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Eagle.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [8] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see ***document [9]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

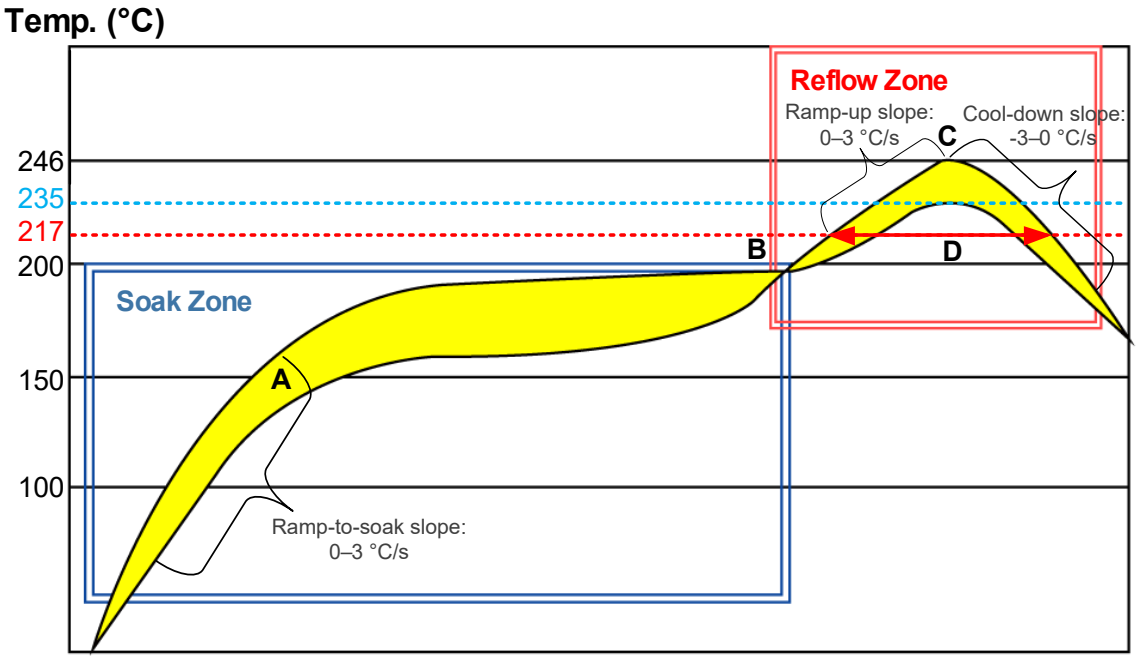


Figure 44: Recommended Reflow Soldering Thermal Profile

Table 38: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max. Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
6. Due to the complexity of the SMT process, please contact Eagle Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [10]***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

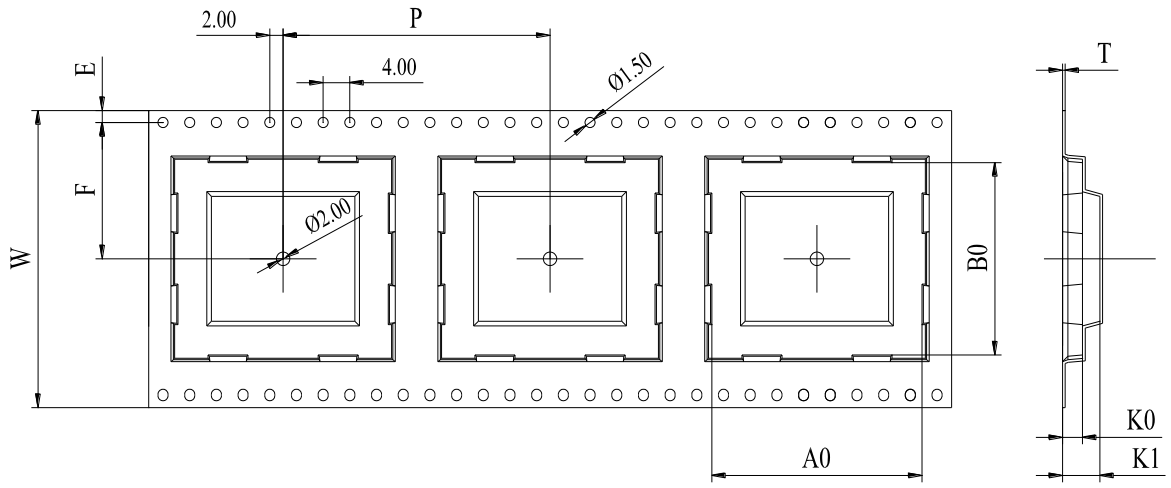


Figure 45: Carrier Tape Dimension Drawing (Unit: mm)

Table 39: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

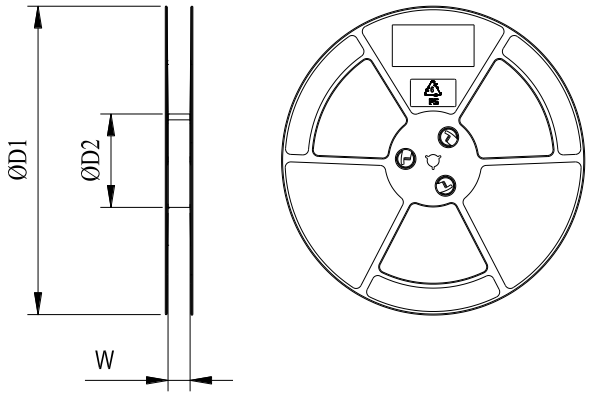


Figure 46: Plastic Reel Dimension Drawing

Table 40: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

7.3.3. Mounting Direction

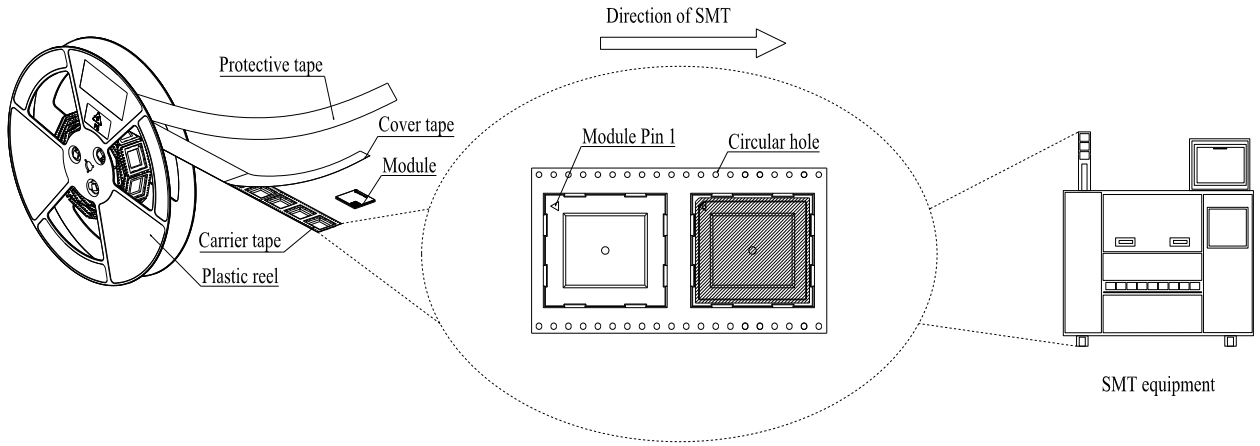
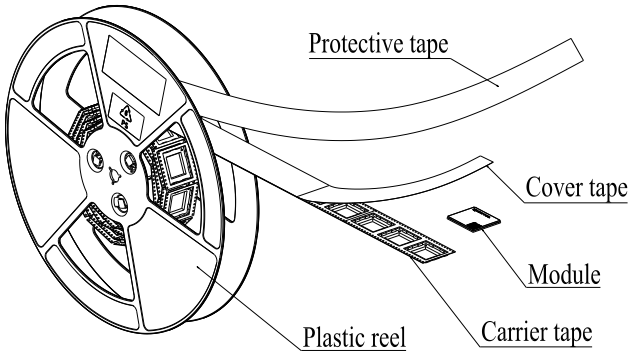


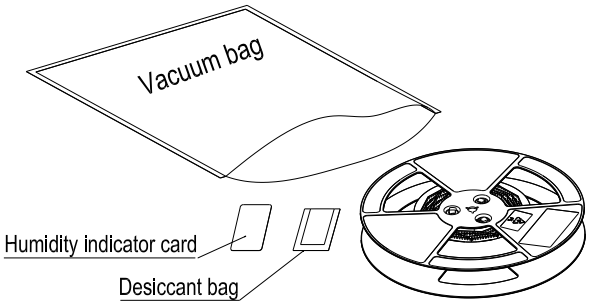
Figure 47: Mounting Direction

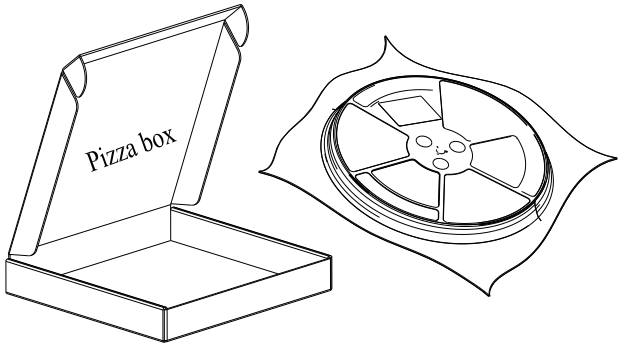
7.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

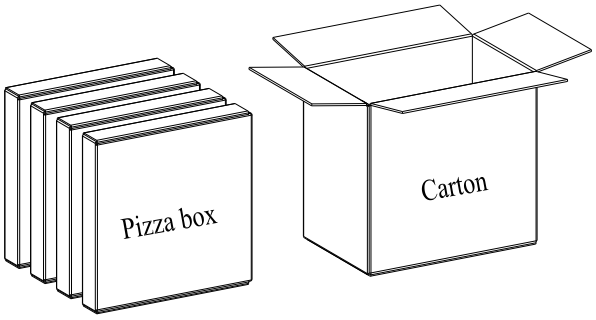


Figure 48: Packaging Process

8 Appendix References

Table 41: Related Documents

Document Name
[1] Eagle_I421&I425&I491_Series_GNSS_Application_Note
[2] Eagle_UMTS&LTE_EVB_User_Guide
[3] Eagle_I421&I425&I491_Series_AT_Commands_Manual
[4] Eagle_I421&I425&I491_Series_QCFG_AT_Commands_Manual
[5] Eagle_I421&I425&I491_Series_Low_Power_Mode_Application_Note
[6] Eagle_I421&I425&I491_Series_AT+QDSIM_Command_Manual
[7] Eagle_RF_Layout_Application_Note
[8] Eagle_I421&I425&I491_Series_Software_Thermal_Management_Guide
[9] Eagle_Module_Stencil_Design_Requirements
[10] Eagle_Module_SMT_Application_Note

Table 42: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AGNSS	Assisted GNSS (Global Navigation Satellite System)
AMR	Adaptive Multi-rate
BDS	BeiDou Navigation Satellite System

bps	bits per second
CHAP	Challenge Handshake Authentication Protocol
Cj	Junction Capacitance
CMUX	Connection Multiplexing
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DC-HSPA+	Dual-carrier High Speed Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access

HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
Inom	Nominal Current
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long Term Evolution
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MS	Mobile Station (GSM engine)
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
NAND	Non-volatile Memory Device
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAM	Pulse-Amplitude Modulation

PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
Rx	Receive
SAW	Surface Acoustic Wave
SMD	Surface Mount Device
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SMS	Short Message Service
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter

UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USB	Universal Serial Bus
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

FCC ID: 2BNX7I491NAXDA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Eagle that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: 2BNX7I491NAXDA”
“Contains IC: 33571-I491NAXDA”
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Antenna Type	Max Gain	
External Antenna	WCDMA II: 1.59dBi WCDMA IV: 2.00dBi WCDMA V: 2.13dBi LTE Band 2:1.59dBi LTE Band 4: 2.00dBi LTE Band 5: 2.13dBi	LTE Band 12: 3.26dBi LTE Band 13: 4.45dBi LTE Band 25: 1.59dBi LTE Band 26(814-824MHz):2.53dBi LTE Band 26(824-849MHz):2.13dBi

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27 and part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC: 33571-I491NAXDA

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne

seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 33571-I491NAXDA ”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 33571-I491NAXDA ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.