HonqTech

HQ308
Hardware Design

LTE Module

Shenzhen Honq Technology Co., Ltd
203, No.10, gongyehou street,
Songgang street, Bao'an District, Shenzhen P.R. China
Tel: 86-0755-27901357
support@honqtech.com
www.honqtech.com

Document Title:	HQ308 Hardware Design
Version:	V1.00
Date:	2025-02-17
Status:	Released

GENERAL NOTES

honqtech OFFERS THIS INFORMATION AS A SERVICE TO ITS CUSTOMERS, TO SUPPORT APPLICATION AND ENGINEERING EFFORTS THAT USE THE PRODUCTS DESIGNED BY honqtech. THE INFORMATION PROVIDED IS BASED UPON REQUIREMENTS SPECIFICALLY PROVIDED TO honqtech BY THE CUSTOMERS. honqtech HAS NOT UNDERTAKEN ANY INDEPENDENT SEARCH FOR ADDITIONAL RELEVANT INFORMATION, INCLUDING ANY INFORMATION THAT MAY BE IN THE CUSTOMER'S POSSESSION. FURTHERMORE, SYSTEM VALIDATION OF THIS PRODUCT DESIGNED BY honqtech WITHIN A LARGER ELECTRONIC SYSTEM REMAINS THE RESPONSIBILITY OF THE CUSTOMER OR THE CUSTOMER'S SYSTEM INTEGRATOR. ALL SPECIFICATIONS SUPPLIED HEREIN ARE SUBJECT TO CHANGE.

COPYRIGHT

honqtech Wireless Solutions Limited
honqtech Headquarters Building, Building 3, No. 289 Linhong Road, Changning District, Shanghai P.R. China
Tel: +86 755 27901357
Email: honqtech@honqtech.com

For more information, please visit:
https://www.honqtech.com/technical_files.html

For technical support, or to report documentation errors, please visit:
https://www.honqtech.com/online_questions.html or email to: support@honqtech.com

Version History

Date	Version	Description of Change	Author
2025-02-17	1.00	Initial	

Contents

Table Index

Figure Index

1. Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics, and test results of the module. With the help of this document, customers can quickly understand the module.

Referring to other software application notes and user guides, customers can use the module to design and develop applications easily. Honqtech provides a set of evaluation boards to test easily and develop the module. The evaluation board tools include an EVB board, a USB cable, an antenna and other peripherals.

1.1. Documentation Overview

The documents listed in Table 1 primarily cover the module's technical information. To thoroughly understand the device and its application, it is necessary to study all relevant documents.

Table 1: Documents Overview

No.	Document	Description
1	HQ308_Hardware_Design (This document)	Mainly introducing interface functions, recommend circuit, PCB layout guidelines, packaging and other hardware components, as well as the use of AT commands
2	HQ308_Reference_Design	Reference circuit applications
3	MOD_HQ308_109	Reference Package (Pads)

NOTE

This current revision is an early release to support initial product developers. The content is subject to change without advance notice.

1.2. Product Overview

The module supports LTE-FDD. The supported radio frequency bands are described in the following table.

Table 2: Module Frequency Bands

Standard	Frequency	HQ308
LTE-FDD	LTE-FDD B2	✓
	LTE-FDD B4	✓
	LTE-FDD B5	✓
	LTE-FDD B12	✓
	LTE-FDD B13	✓
	LTE-FDD B66	✓
Category	CAT1	

Table 3: Overview of Module Functionality

Function	HQ308
USIM	✓
VoLTE	✓
SMS	✓
Analog audio input	✓
Analog audio output	✓
Wi-Fi Scan	✓
FOTA	✓

With a small physical dimension of 15.7*17.6*2.4mm, the module can meet almost any space requirement in customers' applications, such as telematics, surveillance devices, industrial routers remote diagnostics, etc.
The module provides 109 pins, including 48 LGA pins in the outer ring and 61 LGA pins in the inner ring. This document will introduce all the functional pins.

NOTE

The functions supported by the module depend on the actual hardware model and software version.

1.3. Hardware Interface Overview

The interfaces are described in detail in the following chapters, including:

- Power supply
- USB 2.0 interface
- Three UART interfaces, one full function serial port, one ordinary serial port and one debug serial port
- Two USIM interfaces
- I2C interface
- ADC interface
- PCM interface
- General input and output interfaces (GPIOs)
- USB boot download and guidance interface
- Two audio interfaces, one MIC port and one Receiver port
- Module operation status indication interface
- Network status indication interface
- GRFC interface
- LTE Antenna interface

1.4. Hardware Block Diagram

The block diagram of the module is shown in the figure below.

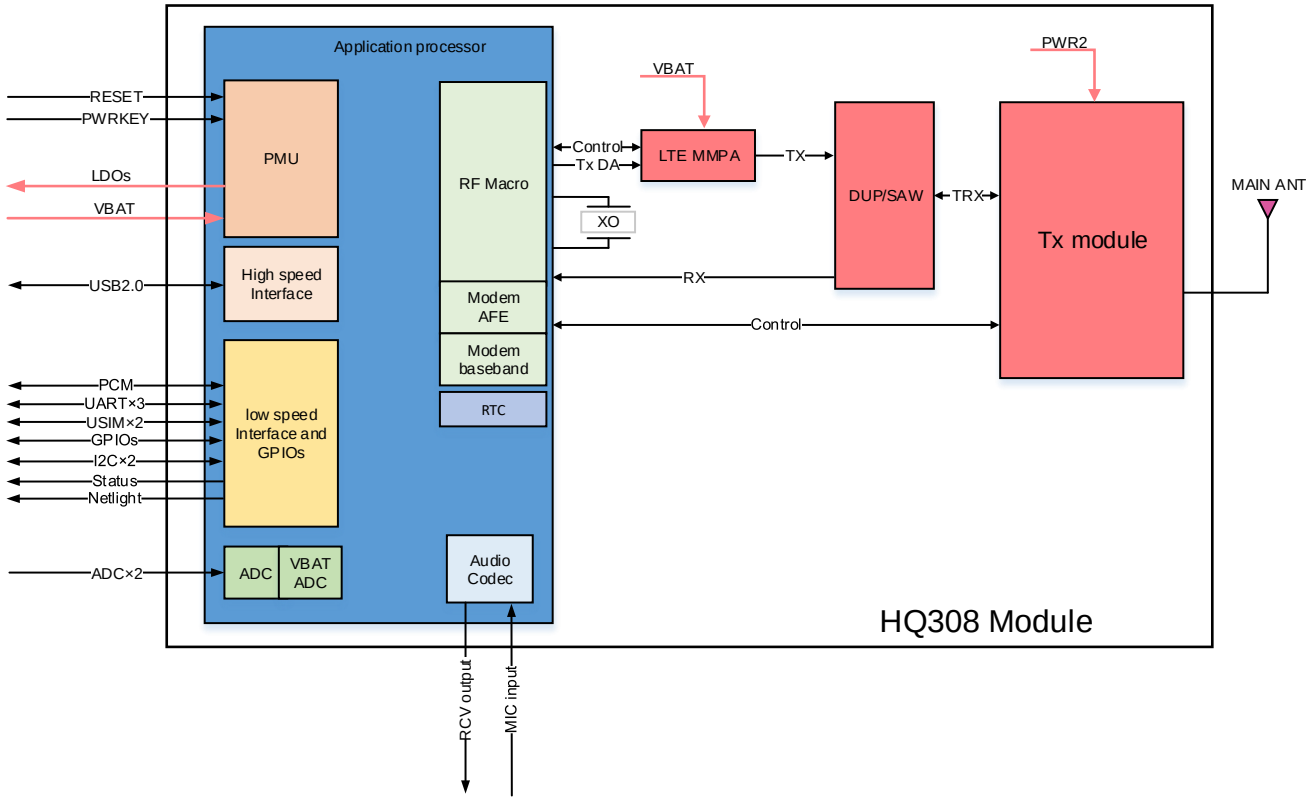


Figure 1: The Block Diagram

1.5. Functional Overview

Table 4: General Features

Feature	Implementation
Power supply	VBAT: 3.4V~4.2V, Recommended VBAT: 3.8V
Power saving	Current in Sleep mode@DRX=0.32S typical: 1.8mA Current in Sleep mode@DRX=0.64S typical: 1.4mA Current in Sleep mode@DRX=1.28S typical: 1.2mA Current in Sleep mode@DRX=2.56S typical: 1mA

	Current in PSM mode typical: 120uA Please refer to the table 58
Radio frequency bands	Please refer to the table 2
Transmitting power	LTE power level: 3 (23dBm±2.7dB)
Data Transmission Throughput	TDD/FDD-LTE category 1 : 10 Mbps (DL), 5 Mbps (UL)
Antenna	LTE antenna interface
SMS	● MT, MO, CB, Text, PDU mode ● Short Message (SMS) storage device: USIM Card, CB does not support saving in SIM Card ● Support CS and PS domain SMS
USIM interface	Support identity card: 1.8V/ 3V
USIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: SM/FD/ON/AP/SDN
Audio feature	● Support analog audio input/output interface ● Support PCM interface
I2C interface	Support I2C interface Comply with I2C bus protocol specification Multi host mode not supported
UART interface	● Full function serial port Baud rate support from 300bps to 3686400bps AT command and data can be sent through serial port Support RTS/CTS hardware flow control Support serial port multiplexing function conforming to GSM 07.10 protocol ● Debug serial port Support debug function, the baud rate is 115200bps ● AUX_UART serial port Auxiliary serial port, the baud rate is 115200bps
USB	Compliant with USB 2.0 specification and supports slave mode but not master mode. This interface can be used for AT command sending, data transmission, software debugging and upgrading.
Firmware upgrade	Firmware upgrade via USB/FOTA
Physical characteristics	Size: (15.7±0.15)*(17.6±0.15)*(2.4±0.20)mm Weight: 1.38g (Typical)
Temperature range	Normal operation temperature: -30°C to +75°C Extended operation temperature: -40°C to +85°C* Storage temperature: -45°C to +90°C

NOTE

When the module is within the extended operation temperature range, module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

2. Package Information

2.1. Pin Assignment Overview

The following figure is a top view of the pin assignment of the module.

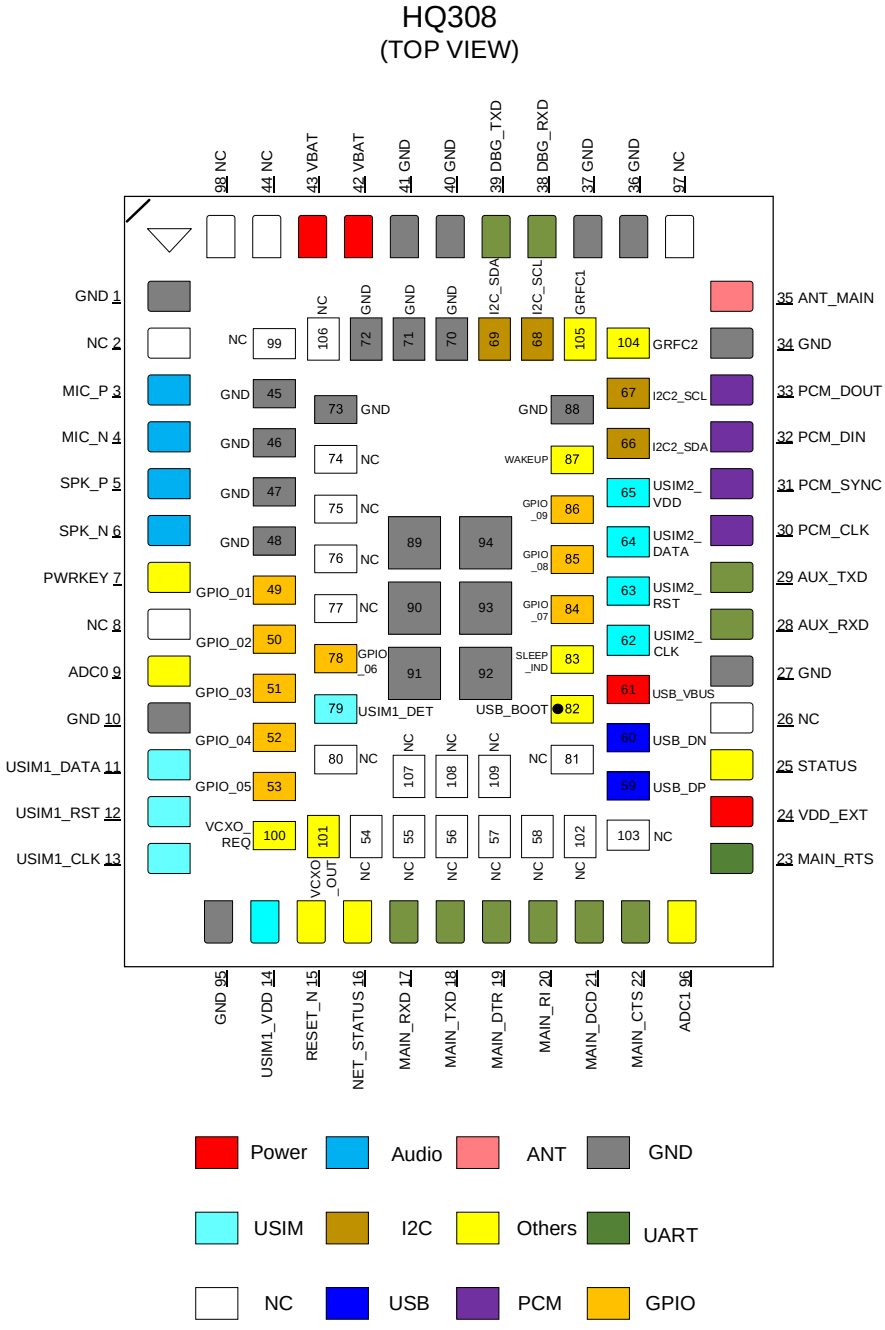


Figure 2: Pin Assignment Overview

Table 5: Pin Description

PIN NO	PIN NAME	PIN NO	PIN NAME
1	GND	2	NC
3	MIC_P	4	MIC_N
5	SPK_P	6	SPK_N
7	PWRKEY	8	NC
9	ADC0	10	GND
11	USIM1_DATA	12	USIM1_RST
13	USIM1_CLK	14	USIM1_VDD
15	RESET_N	16	NET_STATUS
17	MAIN_RXD	18	MAIN_TXD
19	MAIN_DTR	20	MAIN_RI
21	MAIN_DCD	22	MAIN_CTS
23	MAIN_RTS	24	VDD_EXT
25	STATUS	26	NC
27	GND	28	AUX_RXD
29	AUX_TXD	30	PCM_CLK
31	PCM_SYNC	32	PCM_DIN
33	PCM_DOUT	34	GND
35	ANT_MAIN	36	GND
37	GND	38	DBG_RXD
39	DBG_TXD	40	GND
41	GND	42	VBAT
43	VBAT	44	NC
45	GND	46	GND
47	GND	48	GND
49	GPIO_01	50	GPIO_02
51	GPIO_03	52	GPIO_04
53	GPIO_05	54	NC
55	NC	56	NC
57	NC	58	NC
59	USB_DP	60	USB_DN
61	USB_VBUS	62	USIM2_CLK
63	USIM2_RST	64	USIM2_DATA
65	USIM2_VDD	66	I2C2_SDA
67	I2C2_SCL	68	I2C_SCL
69	I2C_SDA	70	GND
71	GND	72	GND
73	GND	74	NC

75	NC	76	NC
77	NC	78	GPIO_06
79	USIM1_DET	80	NC
81	NC	82	●USB_BOOT
83	SLEEP_IND	84	GPIO_07
85	GPIO_08	86	GPIO_09
87	WAKEUP	88	GND
89	GND	90	GND
91	GND	92	GND
93	GND	94	GND
95	GND	96	ADC1
97	NC	98	NC
99	NC	100	VCXO_REQ
101	VCXO_OUT	102	NC
103	NC	104	GRFC2
105	GRFC1	106	NC
107	NC	108	NC
109	NC		

NOTE

'●' Indicates that the pin cannot be pulled down before the module powered on. Otherwise, it will affect the normal start-up of the module.
NC: NOT CONNECT. Do not connect them to GND.

2.2. Pin Description

Table 6: Pin Parameter Abbreviation

Pin Type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input

DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down
OD	Open Drain

Table 7: 1.8V IO Parameters Definition

Power Domain	Parameter	Description	Min	Typ.	Max
1.8V	V_{IH}	High level input	VCC * 0.7	1.8V	VCC+0.2
	V_{IL}	Low level input	-0.3V	0V	VCC *0.3
	R_{PU}	Pull up resistor	55KΩ	79KΩ	121KΩ
	R_{PD}	Pull down resistor	51KΩ	87KΩ	169 KΩ
	I_{IL}	Input leakage current	-	-	10uA
	V_{OH}	High level output range	VCC-0.2	-	-
	V_{OL}	Low level output range	-	-	0.2V
	I_{OL}	Maximum current driving capacity at low level output V_{pad}=0.2V I_{OL} DCS[1:0]= 00 01 10 11		 13 mA 25 mA 37 mA 49 mA	
	I_{OH}	Maximum current driving capacity at high level output V_{pad}=VCC-0.2V I_{OH} DCS[1:0]= 00 01 10 11		 11 mA 21 mA 32 mA 42 mA	

Table 8: 3.0V IO Parameters Definition

Power Domain	Parameter	Description	Min.	Typ.	Max.
	V_{IH}	High level input	2V	-	VCC+0.3
	V_{IL}	Low level input	-0.3V	0V	0.8V
	R_{PU}	Pull up resistor	26KΩ	47KΩ	72KΩ

3.0V	R_{PD}	Pull down resistor	27KΩ	54KΩ	267KΩ
	I_{IL}	Input leakage current	-	-	10uA
	V_{OH}	High level output range	2.4V	-	-
	V_{OL}	Low level output range	-	-	0.4V
	I_{OL}	Maximum current driving capacity at low level output V_{pad}=0.4V I_{OL} DS[2:0]= 000 001 010 011 100 101 110 111		7 mA 10 mA 14 mA 18 mA 21 mA 24 mA 28 mA 31 mA	
	I_{OH}	Maximum current driving capacity at high level output V_{pad}=VCC-0.5V I_{OH} DS[2:0]= 000 001 010 011 100 101 110 111		7 mA 10 mA 13 mA 16 mA 19 mA 23 mA 26 mA 29 mA	

Table 9: Pin Description

Pin Name	Pin No.	Pin Parameter		Description	Note
		Power Domain	Type		
Power Supply					
VBAT	42,43	-	PI	Module power input	Module input voltage ranges from 3.4V to 4.2V, typical value is 3.8V, and the external power supply must provide 1A

					continuous current.
VDD_EXT	24	-	PO	Internal power output	$V_{(nom)}$=1.8V $I_{o(max)}$=50mA
GND	1,10,27,34, 36,37,40, 41,45,46, 47,48,70, 71,72,73, 88,89,90, 91,92,93, 94,95	-	-	Ground	
System Control					
PWRKEY	7	-	DI,PU	System power on/off control input, active low.	Default high V_{IH}=0.7*VBAT V_{IL}=0.3*VBAT It has been internally pulled up to the VBAT with 50K (Typical).
RESET_N	15	-	DI,PU	System reset control input, active low.	Default high V_{nom}=1.6V V_{IL}=0.5V
USIM Interface					
USIM1_DET	79	1.8V	DI	USIM1 card insert detect.	It can be set to high/low active with the AT command。
USIM1_DATA	11	1.8/3.0V	DIO	USIM1 data signal.	This pin has been pull-up with 4.7KΩ resistor to USIM1_VDD internally.
USIM1_RST	12	1.8/3.0V	DO	USIM1 reset signal.	
USIM1_CLK	13	1.8/3.0V	DO	USIM1 clock signal.	
USIM1_VDD	14	1.8/3.0V	PO	USIM1 card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.
USIM2_CLK	62	1.8/3.0V	DO	USIM2 clock signal.	

USIM2_RST	63	1.8/3.0V	DO	USIM2 reset signal.	
USIM2_DATA	64	1.8/3.0V	DIO	USIM2 data signal.	This pin has been pull-up with 4.7KΩ resistor to USIM2_VDD internally.
USIM2_VDD	65	1.8/3.0V	PO	USIM2 card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.
USB Interface					
USB_VBUS	61	-	PI	Valid USB detection input. Active high, V_{min}=3.0V, V_{max}=5.2V, V_{nom}=5V.	
USB_DN	60	-	AIO	Negative electrode of the differential, bi-directional USB signal.	
USB_DP	59	-	AIO	Positive electrode of the differential, bi-directional USB signal.	
Main UART Interface					
MAIN_RXD	17	1.8V	DI	Data input	If unused, keep it open.
MAIN_TXD	18	1.8V	DO	Data output	
MAIN_DTR	19	1.8V	DI	DTE Ready	
MAIN_RI	20	1.8V	DO	Ringing indicator	
MAIN_DCD	21	1.8V	DO	Carrier detection	
MAIN_CTS	22	1.8V	DO	DTE clears sending	
MAIN_RTS	23	1.8V	DI	DTE request sent	
Debug UART Interface					
DBG_RXD	38	1.8V	DI	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DBG_TXD	39	1.8V	DOH		
Auxiliary UART Interface					
AUX_TXD	29	1.8V	DO	Data output	If unused, keep it open.
AUX_RXD	28	1.8V	DI	Data input	
PCM Interface					

PCM_CLK	30	1.8V	DO	PCM clock	If unused, keep it open.
PCM_SYNC	31	1.8V	DO	PCM data frame sync	
PCM_DIN	32	1.8V	DI	PCM data input	
PCM_DOUT	33	1.8V	DO	PCM data output	
I2C Interface					
I2C_SCL	68	1.8V	OD	I2C clock output	If unused, keep it open. Need pull up to VDD_EXT.
I2C_SDA	69	1.8V	OD	I2C data I/O	
I2C2_SDA	66	1.8V	OD	I2C2 data I/O	
I2C2_SCL	67	1.8V	OD	I2C2 clock output	
Analog Audio Interface					
MIC_P	3	-	AI	MIC input positive	If unused, keep it open.
MIC_N	4	-	AI	MIC input negative	
SPK_P	5	-	AO	Audio receiver output positive	
SPK_N	6	-	AO	Audio receiver output negative	
GPIO Interface					
GPIO_01	49	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO_02	50	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO_03	51	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO_04	52	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
GPIO_05	53	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
GPIO_06	78	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO_07	84	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
GPIO_08	85	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
GPIO_09	86	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
ANT Interface					
ANT_MAIN	35	-	AIO	Main antenna	
Other Interface					
ADC0	38	-	AI	General Purpose ADC	Voltage input range 0-1.8V.
ADC1	96	-	AI	General Purpose ADC	Voltage input range 0-1.8V.

NET_STATUS	16	1.8V	DO	Network registration status indicator(LED).	If unused, keep it open.
STATUS	25	1.8V	DO	Module status indicator (LED).	If unused, keep it open.
USB_BOOT●	82	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	It is recommended to place a test point for easy debugging and upgrade. Do not pull down before normal boot.
SLEEP_IND	83	1.8V	DO	Sleep mode indicator	If unused, keep it open.
WAKEUP	87	1.8V	DI	Pulling it up can wake up the module.	If unused, keep it open.
GRFC2	104	1.8V	DO	RF switch IO	If unused, keep it open.
GRFC1	105	1.8V	DO	RF switch IO	If unused, keep it open.
VCXO_REQ	100	1.8V	DI	26Mhz clock request	If unused, keep it open.
VCXO_OUT	101	-	AO	26Mhz clock output	If unused, keep it open.

NOTE

1. Please reserve a test point for USB_BOOT, GND, DBG_TXD and VDD_EXT. If there is no USB connector, please also reserve a test point for USB_VBUS, USB_DP, and USB_DN for firmware upgrading.
2. '●' Indicates that the pin cannot be pulled down before the module powered on. Otherwise, it will affect the normal start-up of the module.

2.3. Mechanical Information

The following figure shows the package outline drawing of the module.

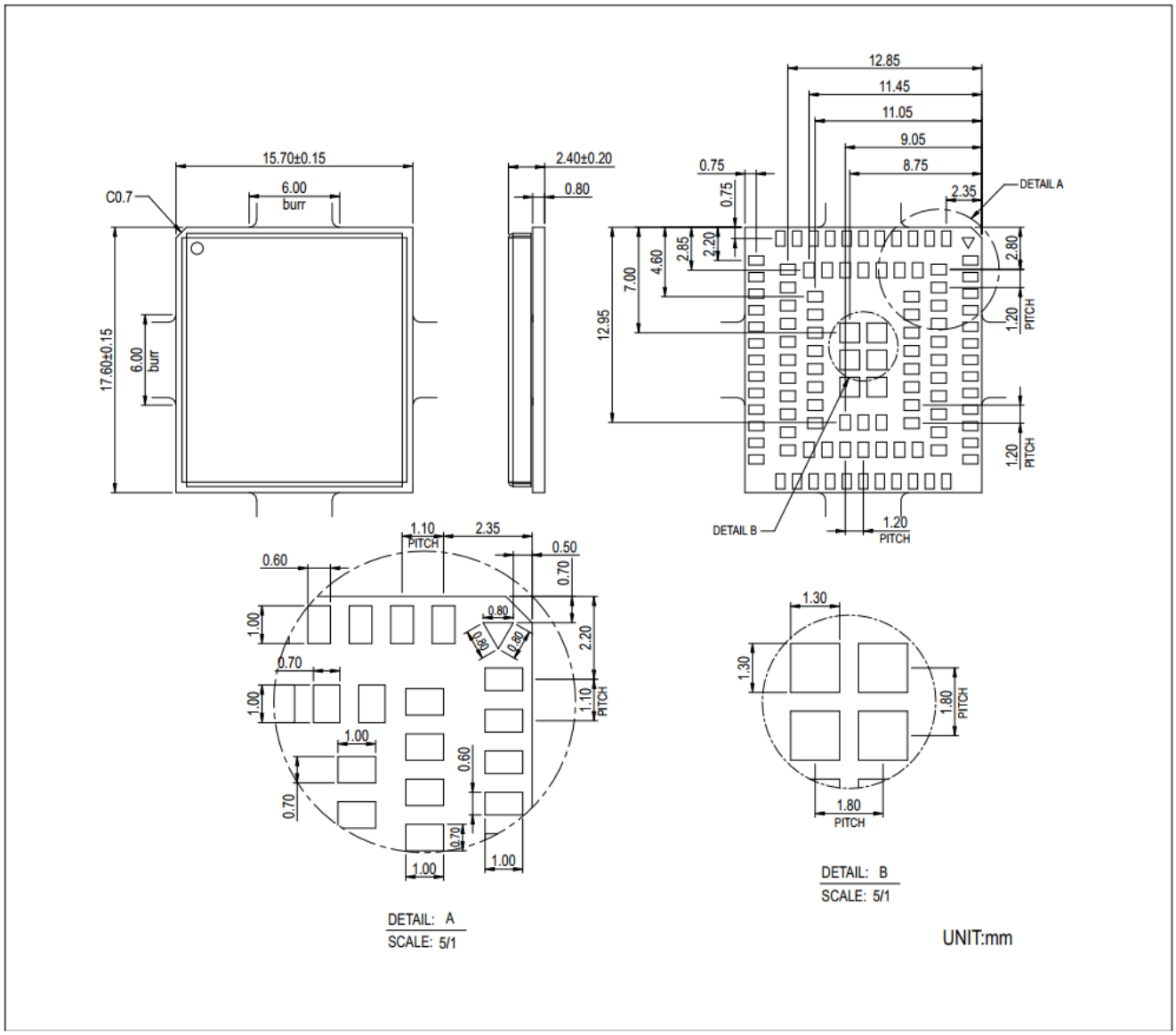


Figure 3: Dimensions (Unit: mm)

NOTE

The side length dimension is 15.70*17.60±0.15mm excluding the burr area.

3. Interface Application

3.1. Power Supply

The module offers 2 power supply pins (42, 43) as VBAT power input pin. The module supplies power to the internal RF and baseband circuits through these two pins.

When the module is transmitting at maximum power in LTE mode, the peak current will reach up to 700mA, please ensure that the external power supply capacity is no less than 1A.

Table 10: Power Interface Pins Definition

Pin Name	Pin No.	Type	Description	Note
VBAT	42,43	PI	Module power input	The input voltage range is 3.4V~4.2V, and the external power supply needs to provide a current carrying capacity of 1A.
GND	1,10,27,34,36,37,40,41,45,46,47,48,70,71,72,73,88,89,90,91,92,93,94,95			

Table 11: VBAT Pins Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Module supply voltage	3.4	3.8	4.2	V
$I_{VBAT (peak)}$	Module consumption peak current	-	-	700	mA
$I_{VBAT (IDLE)}$	Module average consumption current (IDLE mode)	-	11	-	mA
$I_{VBAT (sleep)}$	Current in Sleep mode@DRX=0.32S	-	1.8	-	mA
	Current in Sleep mode@DRX=0.64S	-	1.4	-	mA
	Current in Sleep mode@DRX=1.28S	-	1.2	-	mA
	Current in Sleep mode@DRX=2.56S	-	1	-	mA
$I_{VBAT (PSM)}$	Current in PSM mode	-	120	-	uA
$I_{VBAT (power-off)}$	Module average consumption current (off leakage current)	-	13	-	uA

NOTE

Test condition: VBAT power supply 3.8V, the module is tested on EVB board, and the power input has a 200uF tantalum capacitor.

3.1.1. Power Supply Design Guide

In the customer's design, special attention must be paid to the design of the power supply. If the voltage drops below 3.4V, the RF performance of the module will be affected, the module will shut down if the voltage is too low. It is recommended to select an LDO or DC-DC chip with an enable pin, and the enable pin is controlled by the MCU.

NOTE

When the power supply can provide a continuous current of 1A, the total capacity of the external power supply capacitor is recommended to be no less than 200uF.

It is recommended to place four 10pF/33pF/0.1uF/1uF ceramic capacitors near VBAT to improve RF performance and system stability. At the same time, it is recommended that the VBAT layout routing width from the power supply on the PCB to the module be at least 2mm.The recommended reference design is as follows:

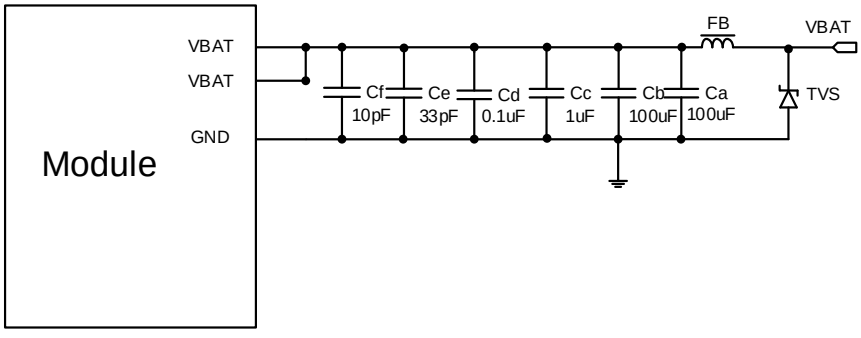


Figure 4: Power Supply Application Circuit

If the VBAT input contains high-frequency interference, it is recommended to add magnetic beads for filtering. The recommended types of magnetic beads are BLM21PG300SN1D and MPZ2012S221A.

In addition, in order to prevent the damage of the module caused by surge and overvoltage, it is recommended to parallel one TVS on the VBAT pin of the module.

Table 12: Recommended TVS Diodes for VBAT

Manufacturer	Part Number	V_{RWM}	V_C(Max)	P_{PP}(Max)	C_J(Max)	Package
WILL	ESD56301D05-2/TR	5V	9.5V	1500W	700pF	DFN1610-2L
WILL	ESD56301D04-2/TR	4.85V	11V	2000W	480pF	DFN1610-2L
WAYON	WS2057KP	5V	12V	2040W	700pF	DFN1610-2L
WAYON	WS4.5DPHXM	4.85V	11V	2255W	700pF	DFN1610-2L

NOTE

When selecting TVS by customers, it is necessary to pay attention to the clamping voltage in the case of surge protection. The clamping voltage should not be higher than 10V when 100V surge input.

3.1.2. Recommended Power Supply Circuit

In order to avoid damaging the module, please do not cut off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

It is suggested that customer's design should have the ability to cut off the power supply for module in abnormal state, and then switch on the power supply to restart the module.

When the input power is greater than 5V, it is recommended to use DCDC chip. When the input is less than 5V, use the LDO power supply. If the OPEN LINUX secondary development function of the module is used, since there is no MCU, a low-cost MCU can be added to play the role of the hardware watchdog that can pull PWRKEY to start up and power off.

It is recommended that a switching mode power supply is used. The following figure shows the DC-DC regulator reference circuit:

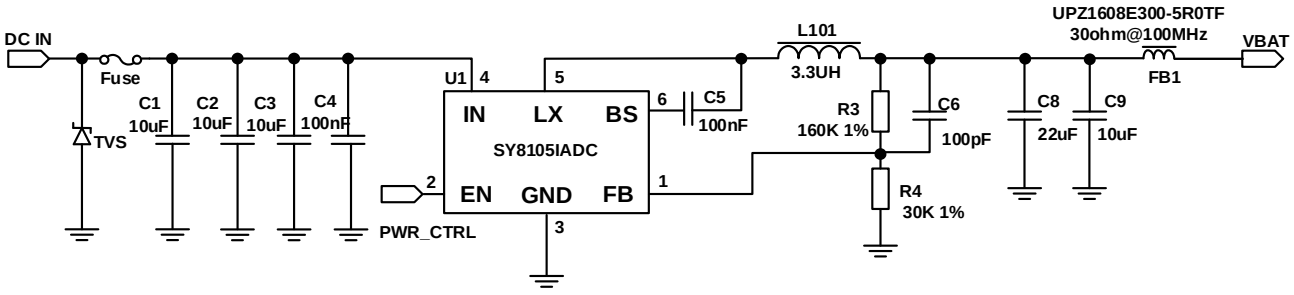


Figure 5: Power Supply Reference Circuit

When the VBAT power is turned off, the voltage should decrease rapidly within 50ms. To avoid voltage anomalies, when the VBAT is lower than the minimum value, the system must power on the VBAT at a voltage which lower than 100mV for at least 2 second to restart the system.

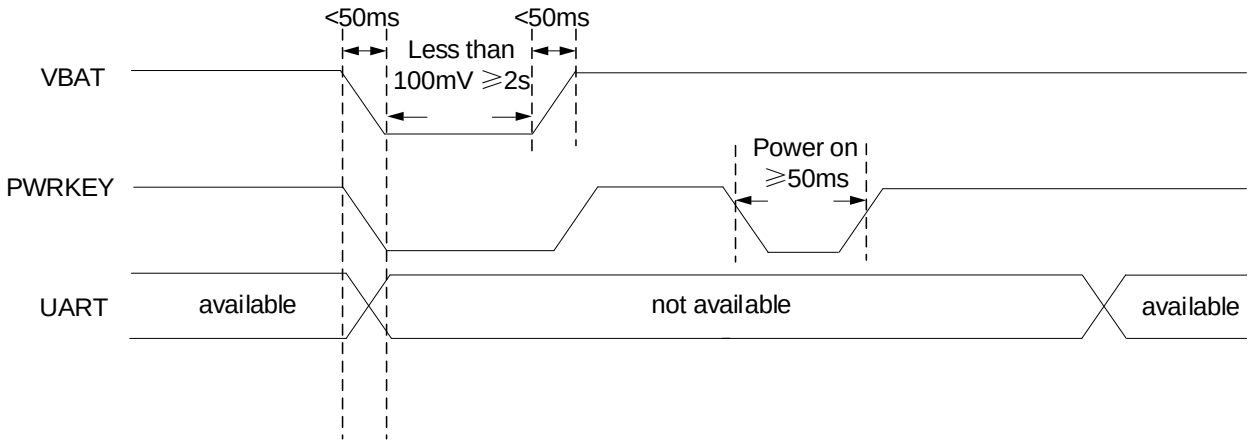


Figure 6: Power-Off and Power-On Restart Sequence

3.1.3. Voltage Monitor

AT command ‘AT+CBC’ can be used to monitor VBAT voltage.

AT command ‘AT+CVALARM’ can be used to set high/low voltage alarm, when the actual voltage exceeds the preset range, a warning message will be reported through the AT port.

AT command ‘AT+CPMVT’ can be used to set high/low voltage power off, when the actual voltage exceeds the preset range, the module will shut down automatically.

NOTE

Overvoltage alarm and overvoltage shutdown are off by default.

3.2. Power On/ Off and Reset

3.2.1. Power on

Table 13: PWRKEY Interface Pin Definition

Pin name	Pin No.	Type	Description	Note
PWRKEY	7	DI,PU	System power on/off control input, active low.	It has been internally pulled up to the VBAT with 50K (Typical).

Customers can power on the module by pulling down the PWRKEY pin. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is as follows:

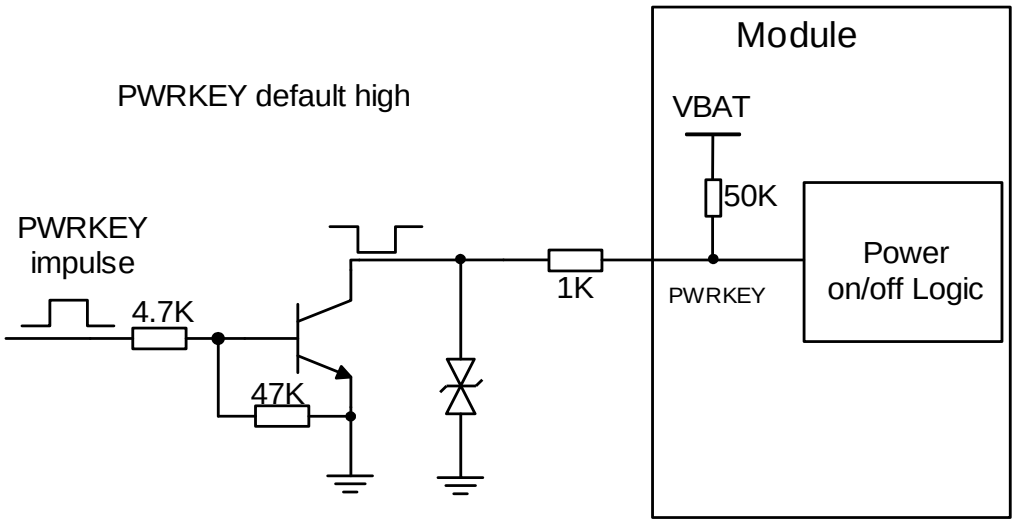


Figure 7: Power On/Off Reference Circuit

NOTE

1. It is forbidden to pull down both RESET_N and PWRKEY to power on the module at the same time.
2. If the customer does not need to start the PWRKEY automatically, do not connect capacitors larger than 10pF on the PWRKEY. Otherwise, the module will start automatically if the low level is detected during the power-on.

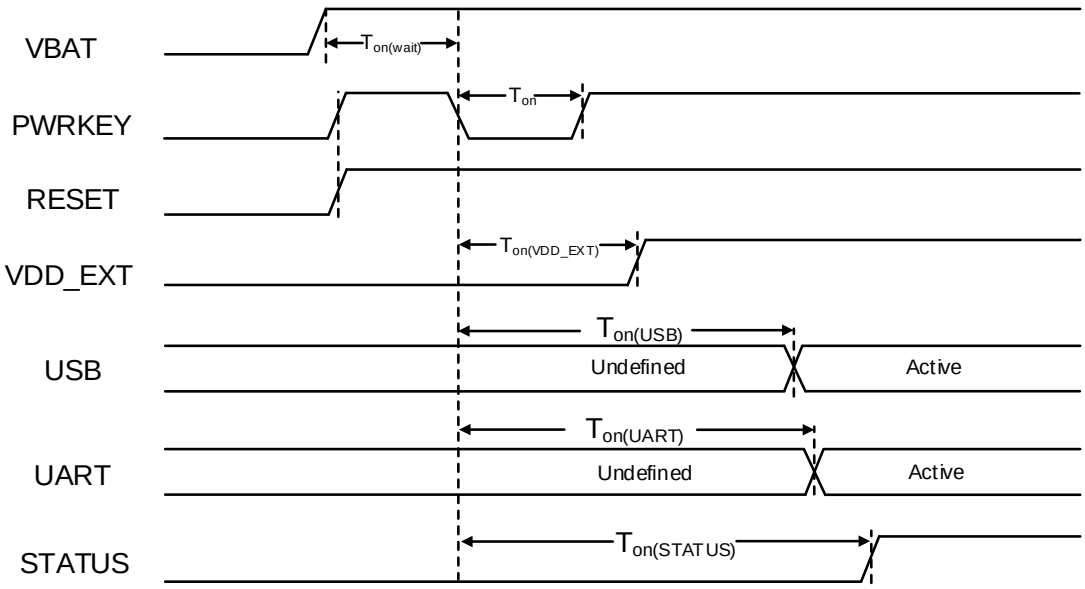


Figure 8: Power on Sequence

Table 14: Power on Timing and Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{on(wait)}$	The time from VBAT power-on stabilization to PWRKEY pin pull-down validity	40	-	-	ms
T_{on}	The time of active low-level impulse of PWRKEY pin to power on module	50	-	-	ms
$T_{on(VDD\_EXT)}$	Output time of VDD_EXT	-	11	-	ms
$T_{on(USB)}$	The time from power-on issue to USB port ready	-	-	5	s
$T_{on(UART)}$	The time from power-on issue to UART port ready	-	-	6	s
$T_{on(STATUS)}$	The time from power-on issue to STATUS pin output high level (indicating power up ready)	-	-	7	s
V_{IH}	Input high level voltage on PWRKEY pin	0.7*VBAT	-	VBAT	V
V_{IL}	Input low level voltage on PWRKEY pin	0	0	0.3*VBAT	V

3.2.2. Power off

The following methods can be used to power off the module.

- Power off by pulling the PWRKEY pin down to a low level for 2.5s.
- Power off Module by AT command ‘AT+CPOF’.
- Over-voltage or under-voltage automatic power off, the voltage range can be set by ‘AT+CPMVT’.
- Over-temperature or under-temperature automatic power off.

It is strongly recommended that the customer use PWRKEY or ‘AT+CPOF’ to shut down, and then cut off VBAT (especially when the module does not need to work). In addition, the customer cannot shut down VBAT by disconnecting it, which may cause damage to flash.

NOTE

When the temperature exceeds the range of - 30 ~ + 75 ℃, the module will report warning information through AT port. When the temperature exceeds the range of - 40 ~ + 85 ℃, the module will shut down automatically.

PWRKEY can be used to power off the module. For power off sequence, please see the following figure:

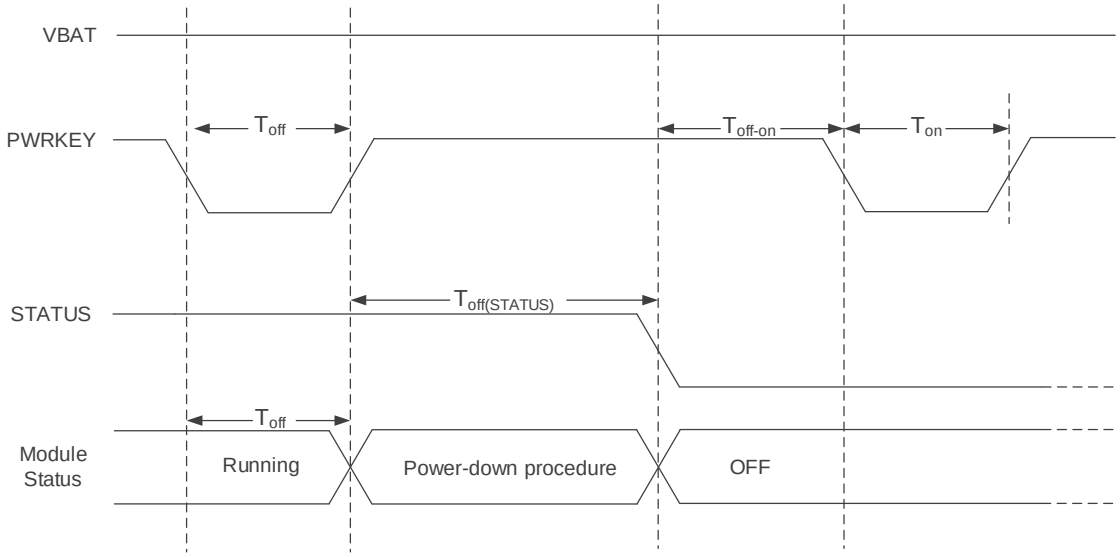


Figure 9: Power off Timing Sequence

Table 15: Power off Sequence Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{off}	Power off low level pulse width	2.5	-	-	s
$T_{off(VDD\_EXT)}$	VDD_EXT shutdown time	-	-	4	s
$T_{off(STATUS)}$	Power off time (according to status interface)	-	-	4	s

NOTE

The status pin can be used to judge whether the module is powered on or not. When the module is powered on and initialization is completed, the status outputs a high level. Otherwise, the low level will be maintained all the time.

3.2.3. Reset Function

Table 16: RESET_N Interface Pin Definition

Pin Name	Pin No.	Type	Description	Note
RESET_N	15	DI,PU	System reset control input, active low.	Default high V_{nom}: 1.6V V_{IL}: 0.5V

The module can be reset by pulling down the RESET_N pin to a low level. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is shown as follows:

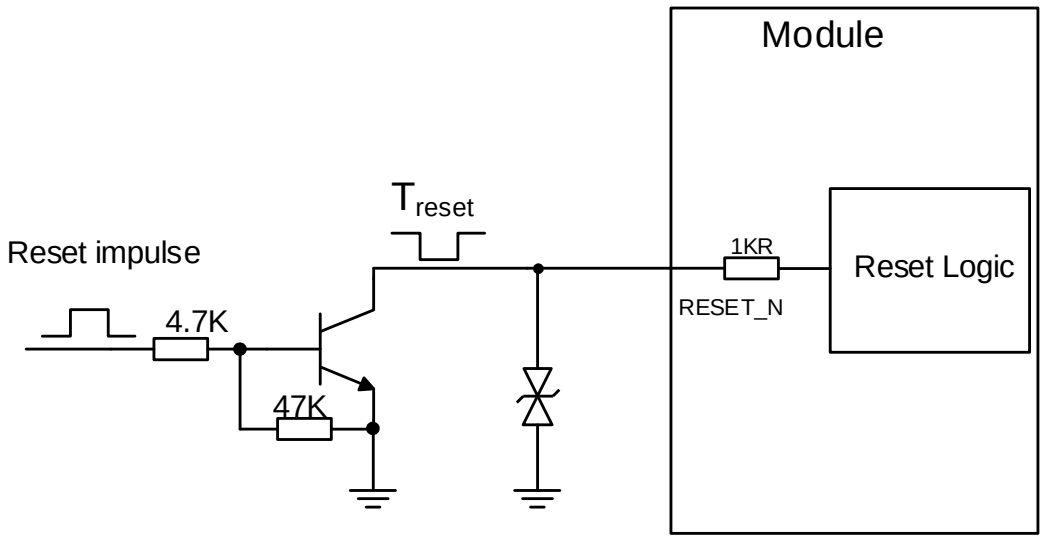


Figure 10: Reset Reference Circuit

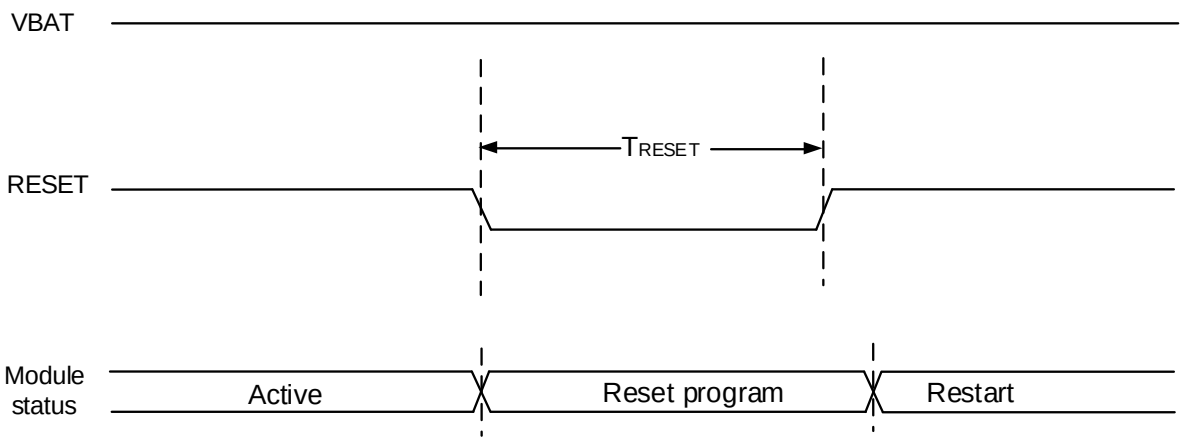


Figure 11: Reset Timing Sequence

Table 17: RESET_N Pin Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RESET_N}	The active low level time impulse on RESET_N pin to reset module	2	2.5	-	s
V_{IH}	Input high level voltage	0.7*VBAT	-	VBAT	V
V_{IL}	Input low level voltage	0	0	0.3*VBAT	V

NOTE

1. It is recommended to use the reset pin only in case of emergency, such as the module is not responding. The reset time is recommended to be 2.5s.
2. Do not connect capacitors larger than 10pF on the PWRKEY and RESET_N.

3.3. UART Interface

The module provides three serial ports, one main communication serial port (UART1), one auxiliary serial port (UART3), and one debug serial port (DEBUG_UART) dedicate to print log.

Table 18: UART Information

Interface	Support Baud Rate (bps)	Default Baud Rate (bps)	Function Description
Full function UART	300 600 1200 2400 4800 9600 19200 38400 57600 115200 230400 460800 921600 1842000 and 3686400	115200	Data transmission and AT command transmission.
Debug UART	115200	115200	Module partial log output.
Auxiliary UART	115200	115200	Used to communicate with peripherals

Table 19: UART Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
Main UART interface					
MAIN_RXD	17	1.8V	DI	Data input	If unused, keep it open
MAIN_TXD	18	1.8V	DOH	Data output	

MAIN_DTR	19	1.8V	DI	DTE Ready	
MAIN_RI	20	1.8V	DO	Ringing indicator	
MAIN_DCD	21	1.8V	DO	Carrier detection	
MAIN_CTS	22	1.8V	DO	DTE clears sending	Connect to the CTS of DTE. If unused, keep it open
MAIN_RTS	23	1.8V	DI	DTE request sent	Connect to the RTS of DTE. If unused, keep it open.
Debug UART					
DBG_TXD	39	1.8V	DOH	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DBG_RXD	38	1.8V	DI		
Auxiliary UART					
AUX_TXD	29	1.8V	DOH	Data output	Used to communicate with peripherals
AUX_RXD	28	1.8V	DI	Data input	

NOTE

In order to ensure the stability of UART data transmission, it is recommended that the baud rate of the serial port should not exceed 38400bps when the continuous transmission is set (without inserting delay) and the flow control function is not enabled. When the baud rate does not exceed 460800bps, it is recommended to insert 50ms delay for every 256 bytes sent, and whether to add flow control can be decided according to requirements. When the baud rate is greater than or equal to 921600bps, it is recommended to insert 50ms delay for every 256 bytes sent, and adopt UART hardware flow control design.

3.3.1. UART Design Guide

When customer uses full-function serial port, please refer to the following connection mode:

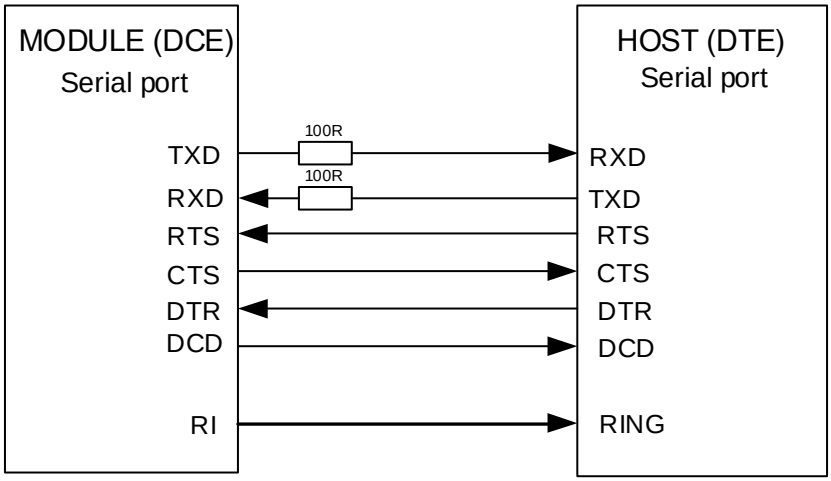


Figure 12: Serial Port Connection Diagram (Full-function Mode)

When using 2-wire serial port, please refer to the following connection mode:

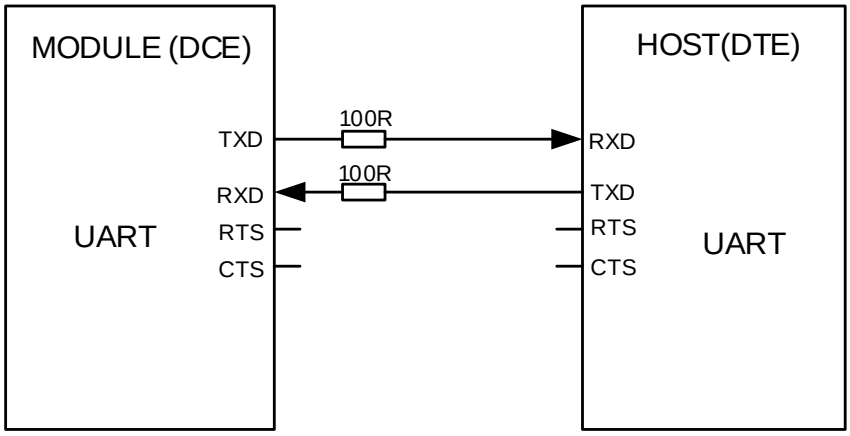


Figure 13: Serial Port Connection Diagram (NULL Mode)

When the level translator chip is used to connect the module and the host (the interface level does not match), the reference design is shown as followed.

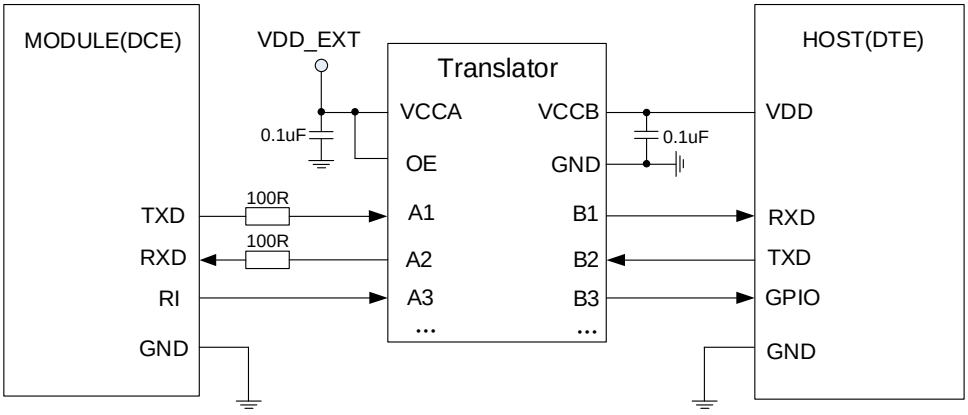


Figure 14: The Reference Design of Level Translator

The following figure shows the use of triode for level shifter circuits. Please pay special attention to the direction of signal. The recommended triode model is MMBT3904.

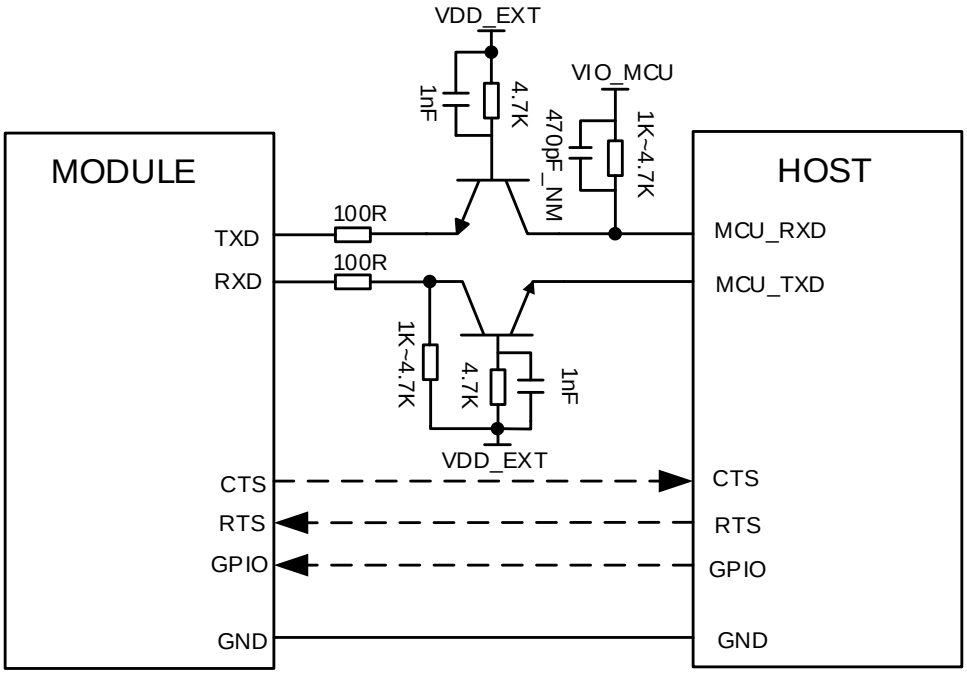


Figure 15: Triode Level Conversion Circuit

NOTE

1. The parasitic capacitance of the transistor will affect the edge of the high-speed digital signal. It is not recommended to use this circuit when the signal speed is higher than 115200bps.
2. It is recommended that the TXD and RXD are connected with 100R resistors in series on the module end to prevent damage to module pins caused by static electricity or surge.

3.3.2. RI Function Description

RI usually keeps high level output. When receiving a short message or URC report, RI outputs a low level for 120ms (short message)/60ms (URC), and then returns to a high-level state.
RI will continues to output a 5.9s (low level)/100ms (high level), when receiving a phone call as the called party. Until the host accepts the call with the "ATA" command, or the caller stops the call, the RI will resume holding the high output after the next 100ms high level.

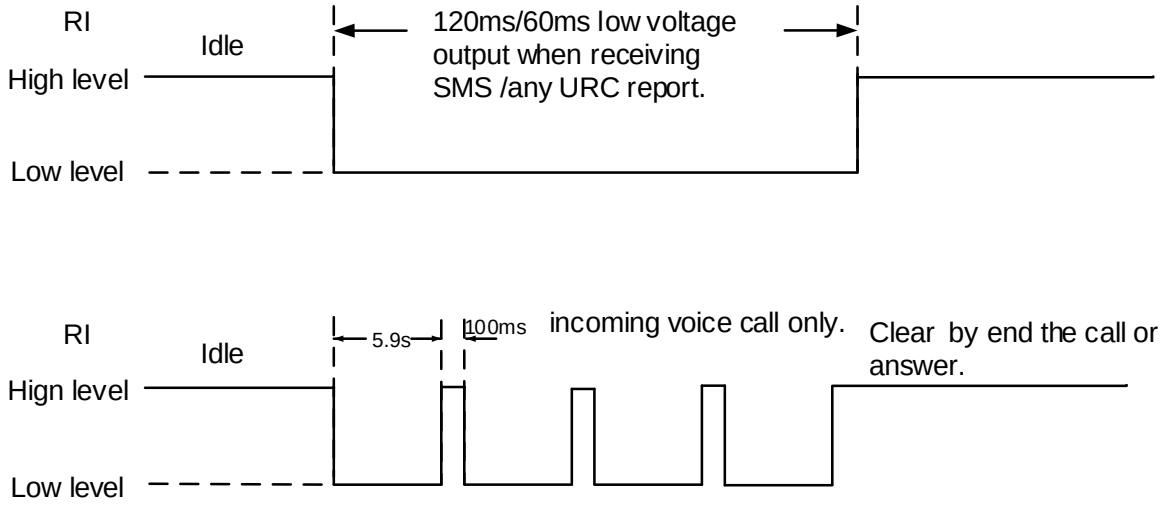


Figure 16: RI Behaviour (SMS and URC Report)

3.3.3. DTR Function Description

The DTR can be used as the sleep-wake pin of the module. After the module enters sleep mode, pull down the DTR to wake up the module. DTR defaults to high level.

When the customers set "AT+CSCLK=1", the module will automatically enter sleep mode. After entering sleep mode, the serial port function cannot communicate normally, and external pulling down the DTR can wake up the module.

After setting the AT command “AT+CSCLK=0”, pulling the DTR pin to a high level will not have any effect, and the normal communication of the serial port function will not be affected.

3.4. USB Interface

The module provides one USB interface, which complies with the USB2.0 specification as a peripheral, but does not support USB charging function and USB HOST mode.

USB supports high speed mode (480Mbps) and full speed mode (12Mbps), it is used for AT command communication, data transmission, firmware upgrade and software debugging.

Table 20: USB Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
USB_VBUS	61	-	PI	Valid USB detection input. Active high,	

				V_{min}=3.0V, V_{max}=5.2V, V_{norm}=5.0V.	
USB_DP	59	-	AIO	Positive electrode of the differential, bi-directional USB signal.	
USB_DN	60	-	AIO	Negative electrode of the differential, bi-directional USB signal.	

3.4.1. USB Reference Design

USB is the main debugging port and software upgrade interface. It is recommended that customers reserve USB test points for debugging during design. If a main control chip is connected, 0R resistors must be reserved for switching external test points during design. The recommended reference design is as follows:

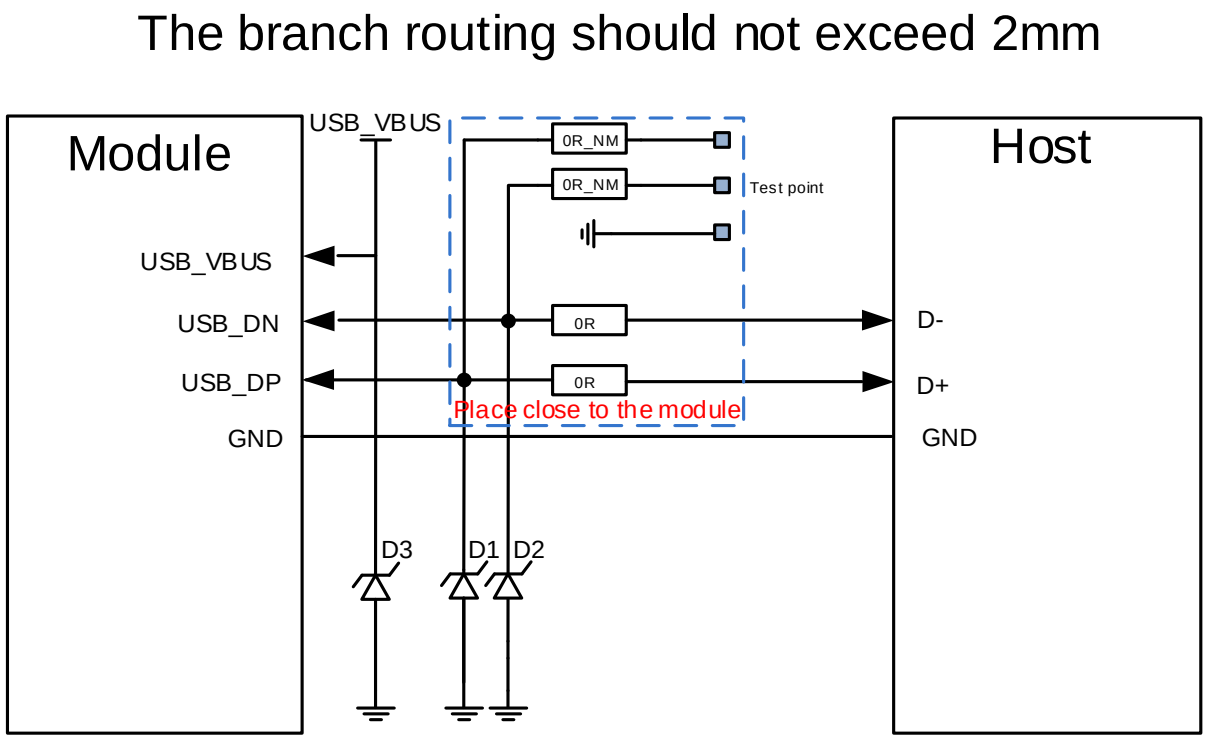


Figure 17: USB Reference Circuit

The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF. The recommended models of D1 and D2 are listed in Table 21.

When in use, attention should be paid to the selection of D3 devices. It is recommended to choose anti-static and surge protection TVS devices. The recommended models of D3 are listed in Table 22.

USB_VBUS is the USB detection pin for module, it's active high and the available identification voltage is 3.0V~5.2V, generally recommend to connect to the VBUS signal of external USB connector or of MCU, it also can be connected to other power supplies, such as the VBAT. If the USB_VBUS pin is connected to the power supply, it's recommended to reserve a switch circuit to ensure that the power supply can be turned off then turn it on, that make USB enumerating afresh.

Table 21: Recommended TVS Diodes for USB_DP and USB_DN

Manufacturer	Part Number	V_{RWM}	V_C(Max)	C_J(Max)	Package
WILL	ESD73131CZ-2/TR	5V	6.5V	0.45pF	DWN0603-2L
ON	ESD9L5.0ST5G	5V	9.8V	0.9pF	SOD-923
LRC	LESD9L5.0T5G	5V	9.8V	0.9pF	SOD-923

Table 22: Recommended TVS Diodes for VBUS

Manufacturer	Part Number	V_{RWM}	V_C(Max)	C_J(Max)	Package
WAYON	WS07DP	7V	20V	1000pF	DFN1610-2L
PRISEMI	PTVSHC2EN7VU	7V	24V	750pF	DFN1610-2L
BILLSEMI	BLE7V065B6U	7V	16V	500pF	DFN1610-2L
LRC	LTVS16H7.0T5G	7V	15V	750pF	DFN1610

NOTE

1. The USB data cable must be strictly routed in 90Ω differential. The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF. TVS should be placed near USB connectors or test points.
2. Route away from other sensitive signals (RF, audio, and XO).
3. The USB 2.0 speed detection is automatically determined through the USB protocol. Customer does not need to additionally pull up the DP. Otherwise, it may affect the USB enumeration of the module.

3.4.2. USB_BOOT Interface

The module provides one forced download boot interface ‘USB_BOOT’.

Table 23: USB_BOOT Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
USB_BOOT	82	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	Please reserve 2 test points for debug. Do not pull down USB_BOOT during normal power on!

If the module fails to boot, customers can force upgrade through the USB_BOOT port.

Before the module is powered on, pull down the USB_BOOT pin to GND, then apply VBAT power to the module, and press PWRKEY to enter the download mode. After entering the download mode, release USB_BOOT and remove the pull-down.

It is recommended to place TVS protection devices to prevent external static electricity from damaging the module.

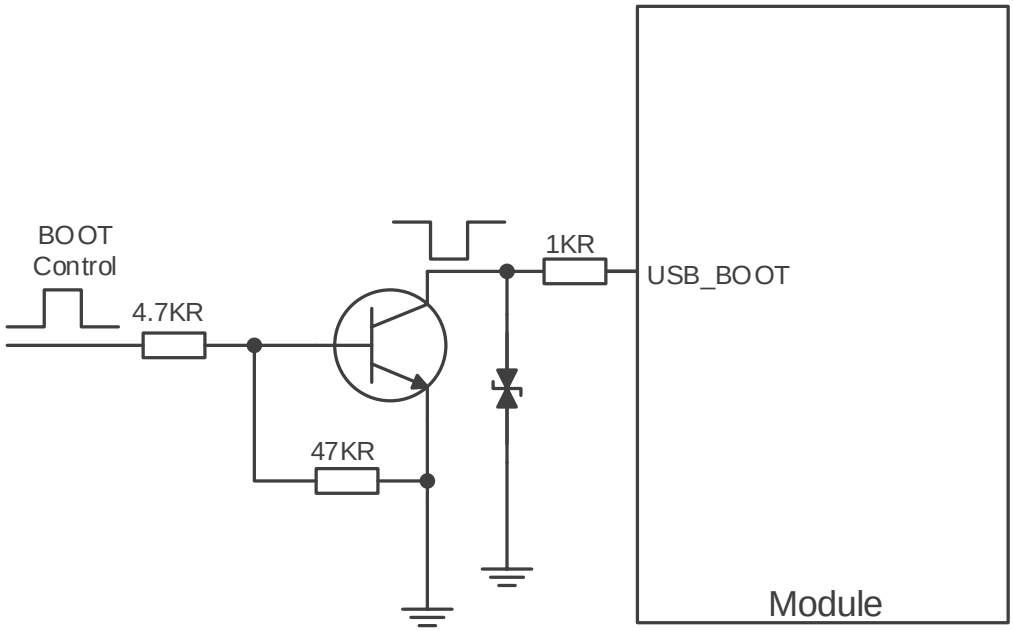
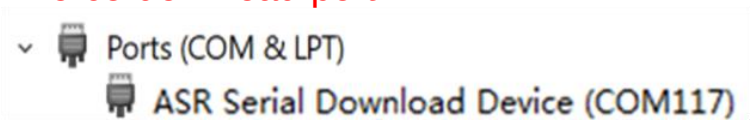


Figure 18: USB_BOOT Reference Circuit

Customers will see the download port in the device manager port of the windows system.

Force-download port:



The port after powering on normally:

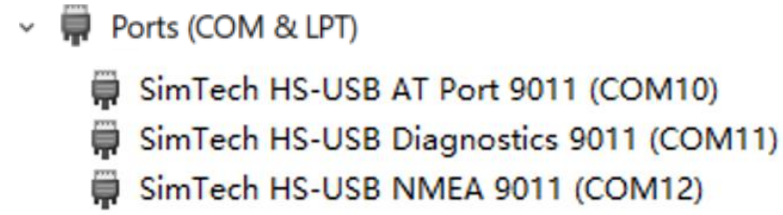


Figure 19: The USB Port

NOTE

1. USB_BOOT is the download control pin, this pin cannot be pulled down before the normal power on. Otherwise, it will enter the download mode.
2. If the customer's design includes an MCU, USB_BOOT must be connected to the MCU. So that the MCU can still perform firmware upgrades on the module in the event of unexpected file damage.
3. If the customer's design do not include an MCU, please reserve a test point for USB_BOOT.
4. USB_BOOT is the USB download boot port, and firmware needs to be loaded from the USB port. Please ensure that the USB is also connected to the MCU or reserve test points for USB.

3.5. USIM Interface

The module supports both 1.8V and 3.0V USIM cards. The interface power of the USIM card is provided by the voltage regulator inside the module.

Table 24: USIM Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
USIM1_DET	79	1.8V	DI	USIM1 card insert detect.	It can be set to high/low active with the AT command.
USIM1_DATA	11	1.8/3.0V	DIO	USIM1 data signal.	This pin has been pulled up with 4.7KΩ resistor to USIM1_VDD internally.
USIM1_RST	12	1.8/3.0V	DO	USIM1 reset signal.	
USIM1_CLK	13	1.8/3.0V	DO	USIM1 clock signal.	
USIM1_VDD	14	1.8/3.0V	PO	USIM1 card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.
USIM2_CLK	62	1.8/3.0V	DO	USIM2 clock signal.	
USIM2_RST	63	1.8/3.0V	DO	USIM2 reset signal.	

USIM2_DATA	64	1.8/3.0V	DIO	USIM2 data signal.	This pin has been pull-up with 4.7KΩ resistor to USIM2_VDD internally.
USIM2_VDD	65	1.8/3.0V	PO	USIM2 card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.

Table 25: USIM Electrical Characteristic in 1.8V Mode (V_{USIM_VDD}=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{USIM_VDD}	LDO power output voltage	1.62	1.8	1.98	V
V_{IH}	High-level input voltage	0.7*V_{USIM_VDD}	-	V_{USIM_VDD}+0.4	V
V_{IL}	Low-level input voltage	-0.4	0	0.25*V_{USIM_VDD}	V
V_{OH}	High-level output voltage	V_{USIM_VDD}-0.4	-	V_{USIM_VDD}	V
V_{OL}	Low-level output voltage	-	0	0.2	V

Table 26: USIM Electrical Characteristic in 3.0V Mode (V_{USIM_VDD}=3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{USIM_VDD}	LDO power output voltage	2.7	3	3.3	V
V_{IH}	High-level input voltage	0.7*V_{USIM_VDD}	-	V_{USIM_VDD}+0.4	V
V_{IL}	Low-level input voltage	-0.4	0	0.25*V_{USIM_VDD}	V
V_{OH}	High-level output voltage	V_{USIM_VDD}-0.45	-	V_{USIM_VDD}	V
V_{OL}	Low-level output voltage	-	0	0.3	V

NOTE

The USIM card functions supported by the module depend on the actual hardware and software versions.

3.5.1. USIM Hot Swap Function

The (U)SIM card supports the hot swap function. You can use AT+UIMHOTSWAPON=1 to turn on the hot swap detection function.

If the (U)SIM card holder is normally open, the AT command “AT+UIMHOTSWAPLEVEL=0” can be sent to set the detection level to a low level, when USIM1_DET is pulled down, the (U)SIM card is considered inserted.

If the (U)SIM card holder is normally closed, the AT command “AT+UIMHOTSWAPLEVEL=1” can be sent to set the detection level to a high level, when USIM1_ DET is pulled up, it is considered that the (U)SIM card is inserted.

If the (U)SIM card hot swap function is not used, the customer can maintain the USIM1_DET pin is disconnected.

3.5.2. USIM Application Guide

It is recommended to use ESD protection component. Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

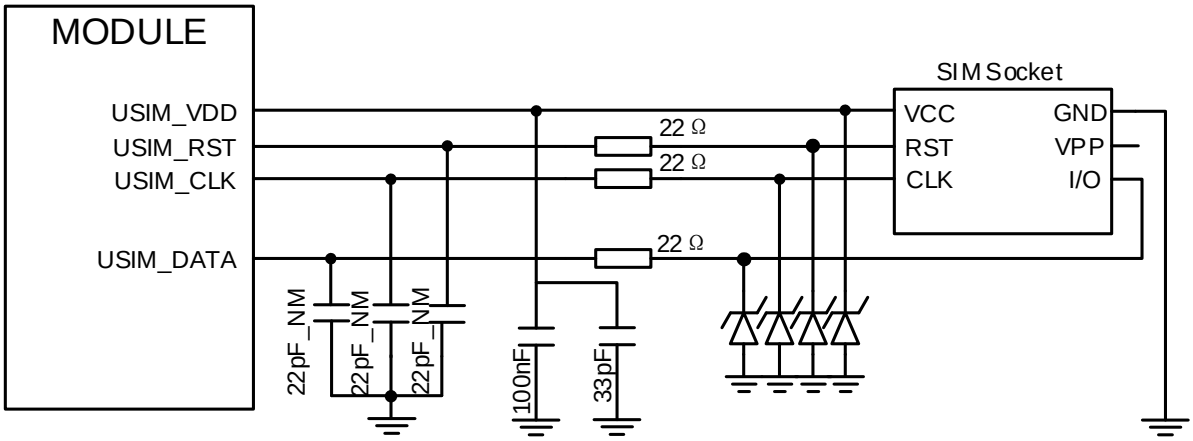


Figure 20: USIM Interface Reference Circuit

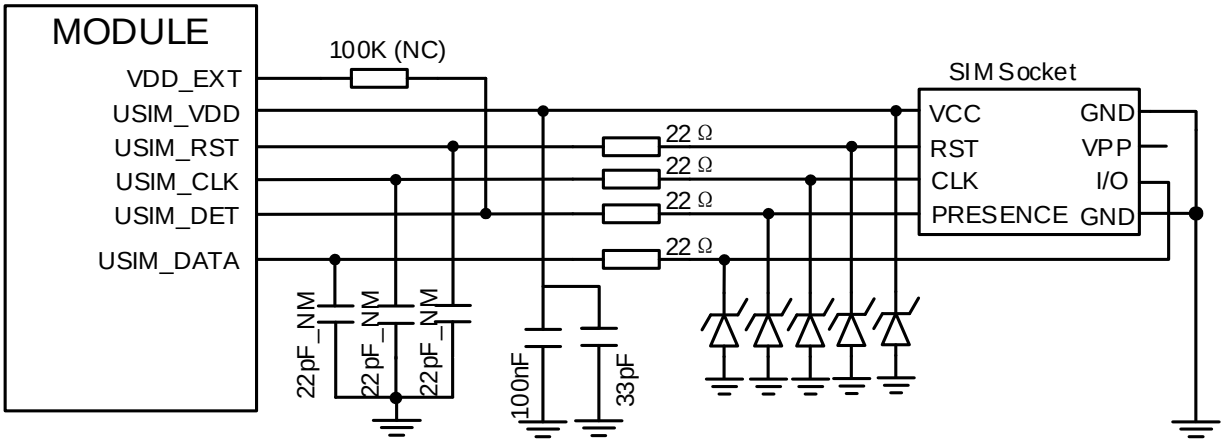


Figure 21: USIM Interface Reference Circuit (8PIN)

NOTE

1. The USIM1_DATA has been pulled up with a 4.7KΩ resistor to USIM1_VDD in module, and the USIM2_DATA also has been pulled up with a 4.7KΩ resistor to USIM2_VDD in module.
2. A 100nF capacitor on USIM_VDD is used to reduce interference.

The circuit of the USIM card is easy to be interfered with, resulting in the failure to recognize or drop the card, etc. so please follow the following principles during the design:

- Be sure to keep the USIM socket away from the main antenna during the PCB layout phase.
- USIM card traces should be away from RF, VBAT and high speed signals, at the same time the USIM card traces should be as short as possible.
- Keep the USIM socket's GND pin directly connected to the main ground.
- To prevent USIM_CLK from other signal interference, it is recommended to protect USIM_CLK separately by surrounding it with ground.
- Place TVS near the USIM socket, and the parasitic capacitance of TVS should not be greater than 15pF, such as WS03DTUMS-B.
- Connect 22 Ω resistors in series between USIM socket and module can enhance ESD protection performance.
- The rise/fall time of USIM_CLK should not exceed 40ns.

Table 27: Recommended TVS Diodes for USIM Socket

Manufacturer	Part Number	V_{RWM}	V_C(Max)	P_{PP}(Max)	C_J(Max)	Package
WAYON	WS03DTUMS-B	3.3V	8V	35W	0.7pF	DFN0603-2L
WILL	ESD9X5VU-2/TR	5V	8V	72W	0.9pF	DFN1006-2L

3.6. PCM Interface

The module provides one PCM interface, it can be connected to an external audio codec chip.

Table 28: PCM Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
PCM_CLK	30	1.8V	DO	PCM clock	If unused, keep it open.
PCM_SYNC	31	1.8V	DO	PCM data frame sync	
PCM_DIN	32	1.8V	DI	PCM data input	
PCM_DOUT	33	1.8V	DO	PCM data output	

Table 29: PCM Characteristic

Characteristic	Description
Encoding-Format	Linear
Data bits	16bits
Master-slave mode	Master/slaver
PCM sample rate	8KHz/16KHz
PCM frame synchronization	Short frame/long frame
Data format	MSB

3.6.1. PCM Sequence

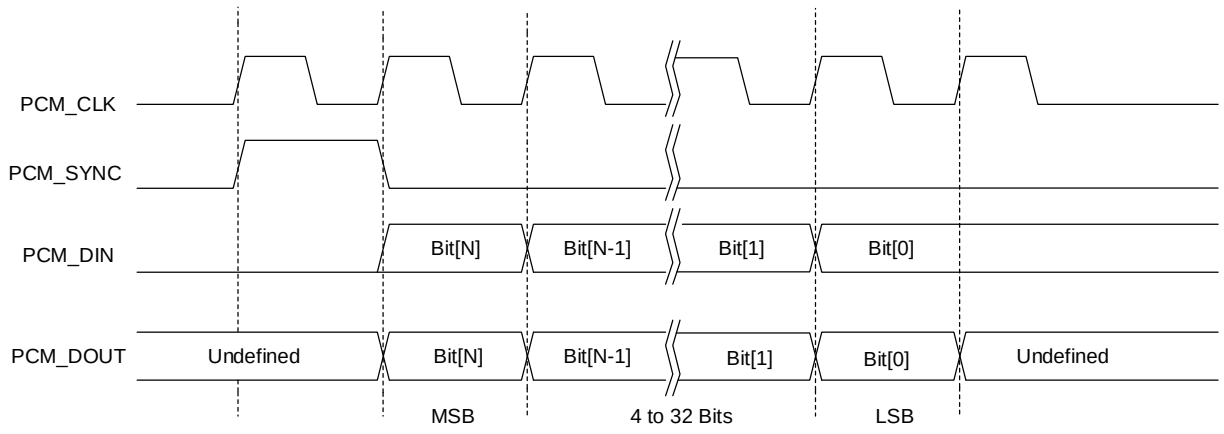


Figure 22: PCM Sequence

3.6.2. PCM Reference Design

The recommended reference design is as follows:

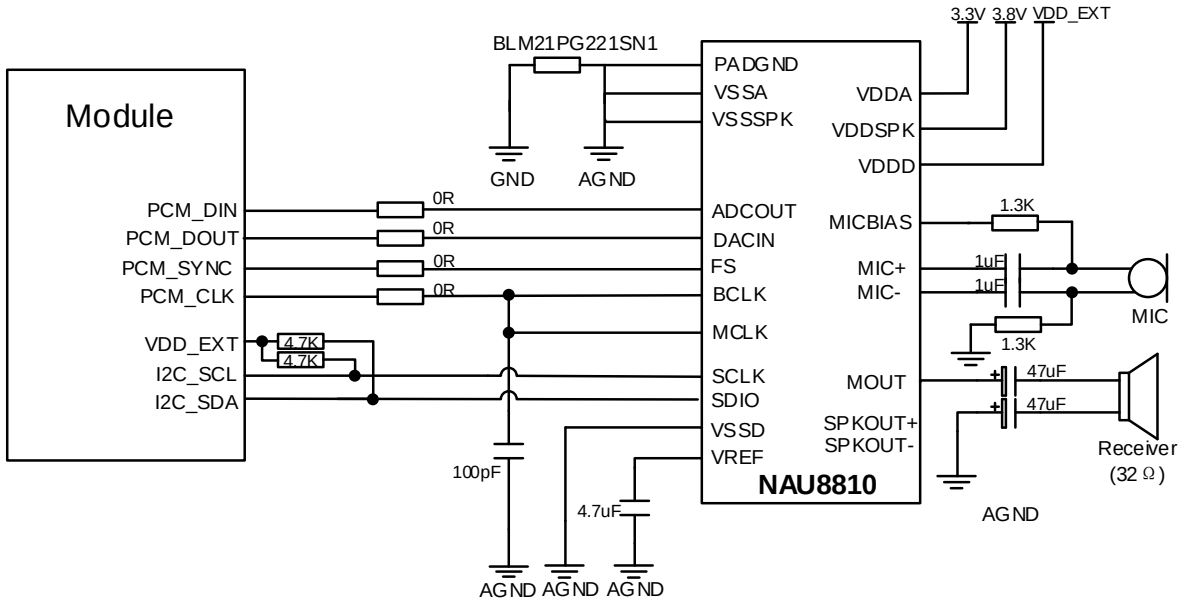


Figure 23: PCM Reference Circuit

3.7. Analog Audio Interface

3.7.1. Analog Audio Input Interface

The module provides an analog audio MIC input interface, which can be connected to an external handle for voice calls.

Table 30: Analog Audio MIC Interface Definition

Pin Name	No.	Power Domain	Type	Description	Note
MIC_P	3	-	AI	Microphone input channel (+)	If unused, keep it open.
MIC_N	4	-	AI	Microphone input channel (-)	

3.7.2. Analog Audio Output Interface

The module provides an analog audio output interface, which can be connected to an external Receiver/Speaker for voice calls or multimedia playback.

Table 31: Analog Audio Output Interface Definition

Pin Name	No.	Power Domain	Type	Description	Note
SPK_P	5	-	AO	Handset differential output channel (+)	If unused, keep it open.
SPK_N	6	-	AO	Handset differential output channel (-)	

3.7.3. Analog Audio Electrical Characteristics

The module Integrates High quality audio codec and audio front-end. The main features are as follows.
ADC: 90dB SNR@20~20kHz
DAC: 95dB SNR@20~20kHz
(Class-AB): THD<-85dB@32-ohm loading

Table 32: Analog Audio Output (AVDD_AUD=1.8V,T=25℃)

Feature	Details	DR (Typ)	THD+N (Typ)	Max Power(1%THD)
DAC	RL=10K	101dBA	-96dB(@vout -2dBv)	1.59Vp
Class-AB	Mono,32Ω, Differential	100dBA	-90dB (0.00316%) (@20mW output)	37mW

3.7.4. Analog Audio Reference Design

The recommended reference design is as follows:

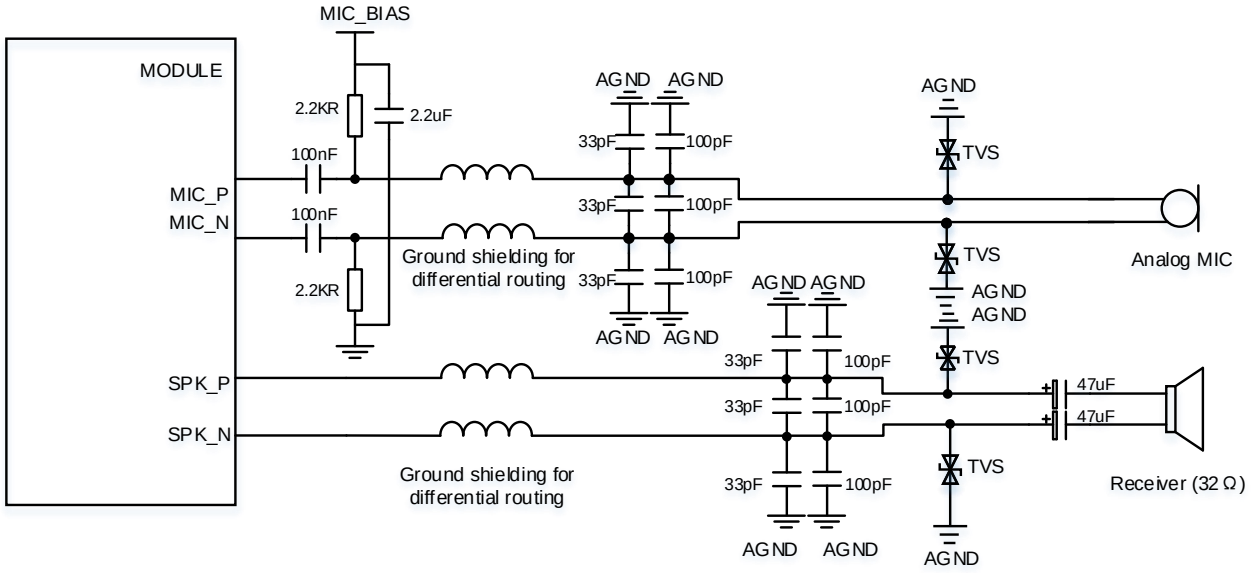


Figure 24: Analog Audio Interface Reference Circuit

3.8. I2C Interface

The module provides two I2C interfaces, which supports standard speed clock frequency 100Kbps and high speed clock frequency 400Kbps. Its operation voltage is 1.8V.

Table 33: I2C Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
I2C2_SDA	66	1.8V	OD	I2C2 data I/O	If unused, keep it open. Need to pull up to VDD_EXT.
I2C2_SCL	67	1.8V	OD	I2C2 clock output	
I2C_SCL	68	1.8V	OD	I2C clock output	
I2C_SDA	69	1.8V	OD	I2C data I/O	

The recommended reference design is as follows:

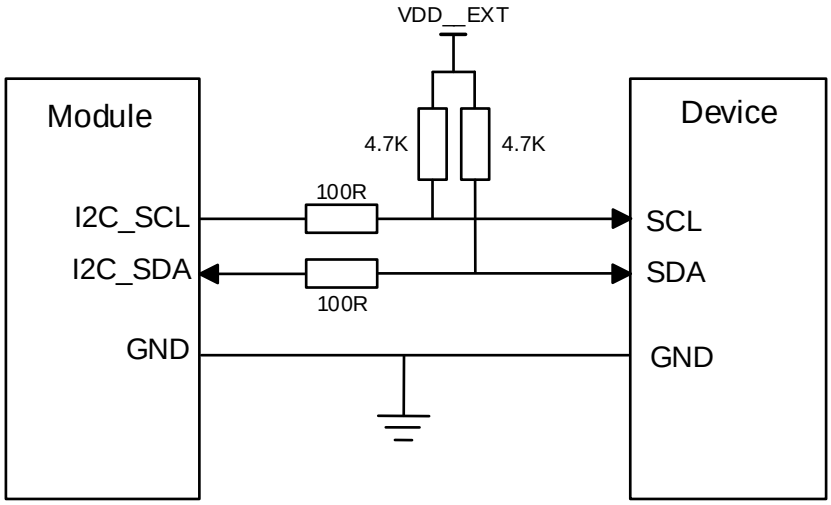


Figure 25: I2C Reference Circuit

NOTE

1. The I2C_SCL and I2C_SDA pins require pull-up resistors, and the pull-up power supply must be VDD_EXT of the module output.
2. Connecting a 100R resistor in series with the I2C signal line close to the module terminal is recommended to reduce overshoot on the signal line.

3.9. GPIO Interface

The module provides multiple GPIOs.

Table 34: Standard GPIO Resources of the Module

Pin No.	Pin Name	AT Command Operation GPIO Number	Pin Typ.	Power Domain	Default Function	Pad Edge Wakeup
49	GPIO_01	GPIO1	IO,PU	1.8V	GPIO	YES
50	GPIO_02	GPIO2	IO,PU	1.8V	GPIO	YES
51	GPIO_03	GPIO3	IO,PU	1.8V	GPIO	YES
52	GPIO_04	GPIO4	IO,PD	1.8V	GPIO	YES
53	GPIO_05	GPIO5	IO,PD	1.8V	GPIO	YES
78	GPIO_06	GPIO6	IO,PU	1.8V	GPIO	YES

84	GPIO_07	GPIO7	IO,PD	1.8V	GPIO	YES
85	GPIO_08	GPIO8	IO,PD	1.8V	GPIO	YES
86	GPIO_09	GPIO9	IO,PD	1.8V	GPIO	YES

3.10. STATUS Interface

The STATUS pin can be used to determine whether the module is powered on or not. When the module is powered on and initialization is complete, the status output is high. Otherwise, it will remain low.

Table 35: STATUS Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
STATUS	25	1.8V	DO	Module operation status indication	If unused, keep it open.

The recommended reference design is as follows:

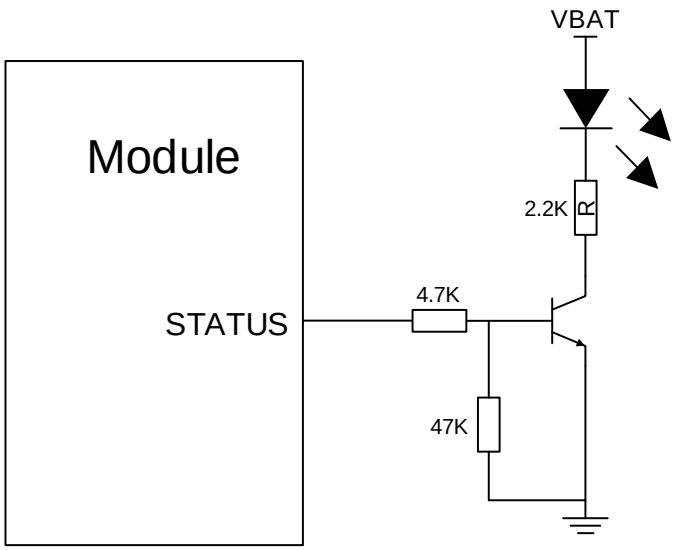


Figure 26: STATUS Reference Circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

3.11. NET_STATUS Interface

NET_STATUS can indicate the current network status. It is usually used to drive the LED light indicating the network status.

Table 36: NET_STATUS Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
NET_STATUS	16	1.8V	DO	Network registration status indicator (LED).	

The recommended reference design is as follows:

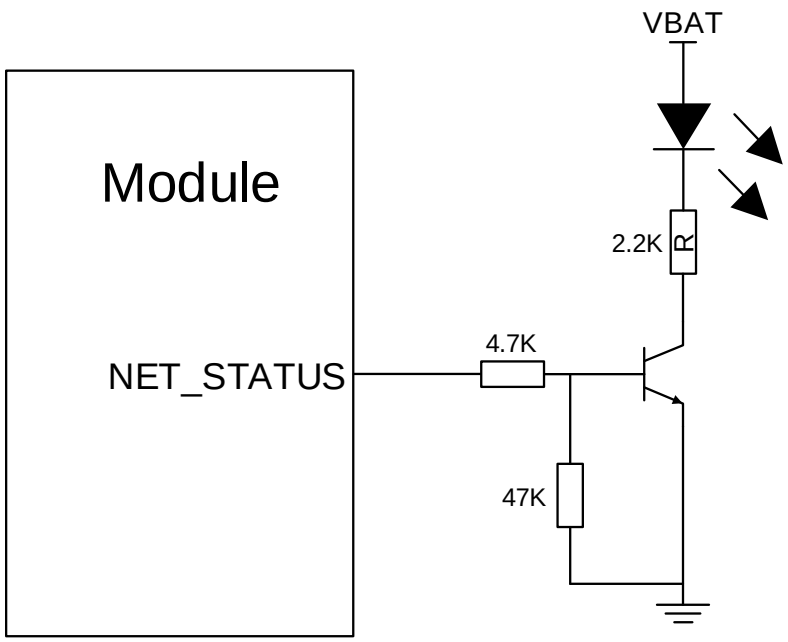


Figure 27: NET_STATUS Reference Circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

The NET_STATUS signal is used to control the LED light that indicates the status of the network. The working status of this pin is shown in the table below.

Table 37: LTE Mode NET_STATUS Pin Status

NETLIGHT Pin Status	Module Status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit/Registered
OFF	Power off / Sleep

3.12. Other Interface

3.12.1. ADC

The module provides two general-purpose ADC pins and a built-in VBAT ADC interface.

Table 38: ADC Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
ADC0	9	0V-1.8V	AI	General Purpose ADC	If unused, keep it open.
ADC1	96	0V-1.8V	AI	General Purpose ADC	If unused, keep it open.

The electrical characteristics are as follows:

Table 39: General ADC Electronic Characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	-	12	-	Bits
Input Range	0	-	1.8	V
Input Resistance		Hi-Z		

NOTE

1. “AT+CADC=2” can be used to read the voltage of the ADC0 pin.
2. “AT+CADC2=2” can be used to read the voltage of the ADC1 pin.
3. “AT+CBC” can be used to read the voltage of the VBAT.

3.12.2. VDD_EXT

The module provides 1 LDO outputs: VDD_EXT.
VDD_EXT can only provide a current capacity of 50mA. It cannot be used as a high current drive source.

Table 40: VDD_EXT Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
VDD_EXT	24	-	PO	1.8V power output, output current up to 50 mA.	Default on. If unused, keep it open.

Table 41: VDD_EXT Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{VDD_EXT}	Output voltage	-	1.8	-	V
I_O	Output current	-	-	50	mA

The recommended reference design is as follows:

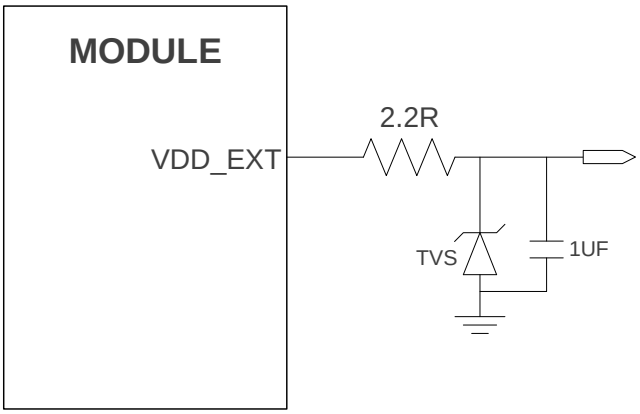


Figure 28: VDD_EXT Reference Circuit

NOTE

VDD_EXT is the module power supply. If the damage will affect the system startup, it is recommended that customers add TVS protection. The recommended model is ESD56051N.

Table 42: TVS for VDD_EXT Part Number List

Manufacturer	Part Number	V_{RWM}	V_C(Max)	C_J(Max)	Package
AMAZING	AZ3103-01F	3.3V	9V	720W	550pF
Prisemi	PTVSHC2EN3V3U	3.3V	13V	1500W	400pF

3.12.3. VCXO_OUT and VCXO_REQ

The module provides 26MHz clock for other peripherals (GNSS and Bluetooth, etc.).

When pull up the VCXO_REQ, the VCXO_OUT will output 26MHz clock.

Table 43: VCXO_OUT and VCXO_REQ Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
VCXO_REQ	100	1.8V	DI	26Mhz clock request	If unused, keep it open.
VCXO_OUT	101	-	AO	26Mhz clock output	If unused, keep it open.

NOTE

VCXO_OUT can be controlled with VCXO_REQ or software.

3.12.4. SLEEP_IND and WAKEUP

The module provides a SLEEP_IND interface and a WAKEUP interface.

Table 44: SLEEP_IND and WAKEUP Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
SLEEP_IND	83	1.8V	DO	Sleep mode indicator	If unused, keep it open.
WAKEUP	87	1.8V	DO	It can wake up the module from sleep mode.	Wake up the module by pulling up it. If unused, keep it open.

NOTE

SLEEP_IND and WAKEUP only take effect when the module enters sleep mode by sending "AT+CSCLK=3".

3.12.5. GRFC

The module provides a set of LTE antenna GRFC dedicated signals lines. It can be used to control the antenna tuner to improve antenna performance. For circuit design, please refer to Section 4.3.

Table 45: GRFC Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
GRFC2	104	1.8V	DO	RF switch IO	If unused, keep it open.
GRFC1	105	1.8V	DO	RF switch IO	

4. RF Specifications

4.1. LTE Specifications

Table 46: Conducted Transmission Power

Frequency	Power	Min.
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm
LTE-FDD B13	23dBm +/-2.7dB	<-40dBm
LTE-FDD B66	23dBm +/-2.7dB	<-40dBm

Table 47: E-UTRA Operating Bands

E-UTRA	UL Freq.	DL Freq.	Duplex Mode
2	1850~1909.9 MHz	1930~1989.9 MHz	FDD
4	1710~1754.9 MHz	2110~2154.9 MHz	FDD
5	824～848.9 MHz	869～893.9MHz	FDD
12	699~715.9MHz	729~745.9MHz	FDD
13	777~786.9 MHz	746~755.9 MHz	FDD
66	1710~1779.9MHz	2110~2179.9MHz	FDD

Table 48: Conducted Receive Sensitivity

Frequency	Receive Sensitivity(Typical)	Receive Sensitivity(MAX)
LTE FDD/TDD	Refer to the table 49	3GPP

Table 49: Reference Sensitivity (QPSK)

E-UTRA Band	3GPP TS36.521-1						Actual	Duplex Mode
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz	10 MHz	
2	-102	-99	-97.3	-94.3	-92.5	-91.3	-98.5	FDD
4	-104	-101	-99.3	-96.3	-94.5	-93.3	-99.5	FDD

5	-102	-99	-97.3	-94.3	-	-	-98	FDD
12	-101	-98	-96.3	-93.3	~	~	-99	FDD
13	~	~	-96.3	-93.3	-	-	-97.5	FDD
66	-103.5	-100.5	-98.8	-95.8	-94	-92.8	-98.5	FDD

4.2. LTE Antenna Requirements

For better overall performance, it is recommended that the antenna design should refer to the index requirements in the following table.

Table 50: LTE Antenna Requirements

Passive	Recommended Standard
Operating band	Please refer to the table 46 and table 47
Direction	Omnidirectional
Gain	> -3dBi (Avg)
Input impedance	50 ohm
Efficiency	> 50 %
Maximum input power	50W
VSWR	< 2
Isolation	>20dB
PCB insertion loss(<1GHz)	<0.5dB
PCB insertion loss(1GHz~2.2GHz)	<1dB
PCB insertion loss(2.3GHz~2.7GHz)	<1.5dB

4.3. Antenna Reference Design

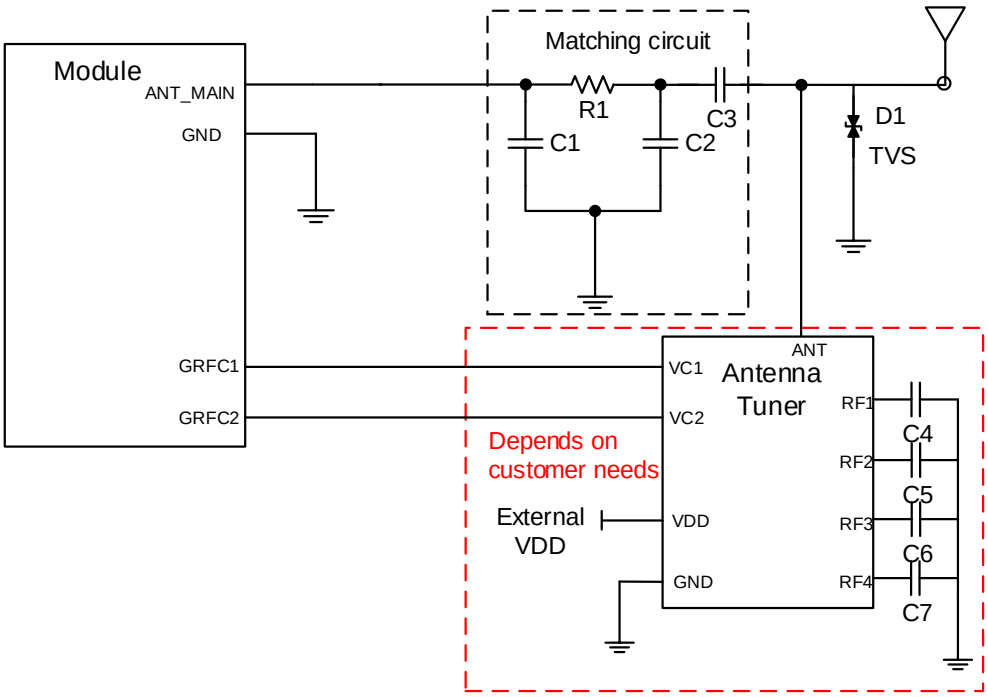


Figure 29: Passive Antenna Reference

The matching circuit R1 is labeled 0Ω by default, and C1 and C2 are reserved by default, and the specific value is determined by the antenna optimization, usually provided by the antenna manufacturer.

The Pins 104 and 105 are reserved for the LTE Antenna tuner, which is dependent on the specific requirements of the customer.

The antenna port is easy to introduce static electricity, to avoid the internal components of the module being damaged by static electricity, C3 is pasted with a 100pF capacitor by default to enhance ESD protection capability.

It is recommended that D1 choose a suitable two-way TVS protection device placed close to the antenna. It especially needs to pay attention to the influence of TVS junction capacitance value on RF signals. Recommended TVS models are as follows:

Table 51: TVS for RF Main Antenna Part Number List

Manufacturer	Part Number	V_{RWM}	V_C(Max)	C_J(Typ)	Package
BILLSEMI	BLE5V0CR05UB	5V	40V	0.05pF	DFN1006-2L

4.4. PCB Layout

When routing the PCB, users should pay attention to the impedance design of the trace from the module's ANT port to the antenna connector on the PCB, controlling the impedance at 50Ω. The trace length is recommended to be kept within 20mm and should stay away from interference signals such as power supply and clock signals.

If using an IPEX connector, ensure impedance control by leaving the projection area hollow and using a reference layer.

If using an SMA connector, ensure impedance control by keeping the distance between the RF signal pad edge and the GND copper foil sufficiently far, at least 1.2mm

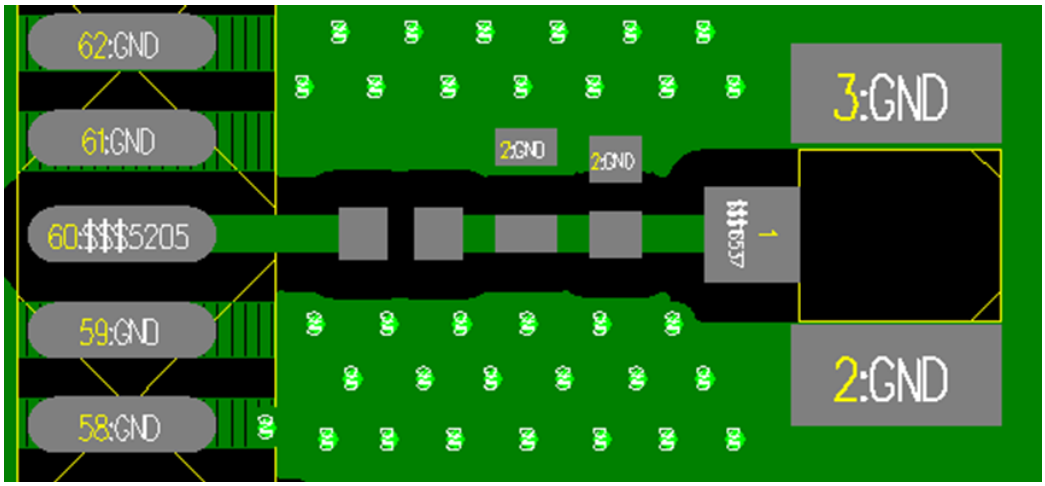


Figure 30: Reference PCB Layout for IPEX Connector

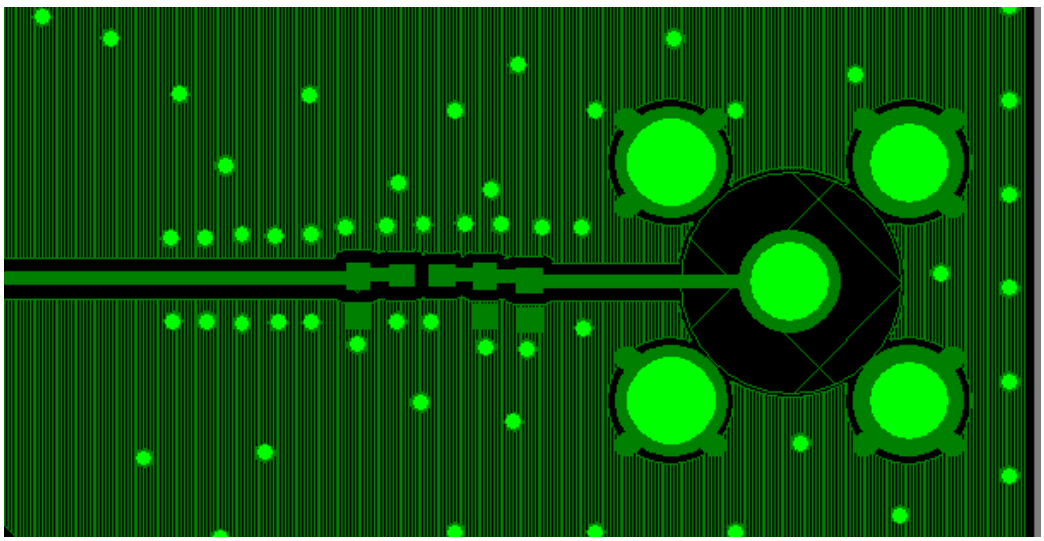


Figure 31: Reference PCB Layout for SMA Connector

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of the module are listed in the following table, exceeding these limits may cause permanent damage to the module.

Table 52: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage on VBAT	-0.5	-	4.8	V
Voltage on USB_VBUS	-0.5	-	5.4	V
Voltage at digital pins (GPIO, I2C, UART, PCM, RESET_N)	-0.3	-	2.0	V
Voltage at I/O pins	-0.3	-	2.0	V
(USIM)	-0.3	-	3.9	V
Voltage at PWRKEY	-0.3	-	4.8	V

5.2. Operating Conditions

Table 53: Recommended Operating Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	3.4	3.8	4.2	V
Voltage at USB_VBUS	3.0	5.0	5.2	V

Table 54: 1.8V Digital I/O Characteristics*

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	VCC*0.7	1.8	VCC+0.2	V
V_{IL}	Low-level input voltage	-0.3	0	VCC*0.3	V

V_{OH}	High-level output voltage	VCC-0.2	-	-	V
V_{OL}	Low-level output voltage	0	-	0.2	V
I_{OH}	High-level output current (no pull down resistor)	-	-	42	mA
I_{OL}	Low-level output current (no pull up resistor)	-	-	49	mA
I_{IH}	Input high leakage current (no pull-down resistor)	-	-	10	uA
I_{IL}	Input low leakage current (no pull up resistor)	-10	-	-	uA

NOTE

These parameters are for digital interface pins, such as GPIO, I2C and UART.

The operating temperature of the module is listed in the following table.

Table 55: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	75	℃
Extended operation temperature*	-40	-	85	℃
Storage temperature	-45	-	90	℃

NOTE

When Module is within the extended operation temperature range, Module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

5.3. Operating Mode

5.3.1. Operating Mode Definition

The table below summarizes the various operating modes of the module.

Table 56: Operating Mode Definition

Mode		Function
Normal operation	LTE Sleep	AT command “AT+CSCLK=1” can be used to set the module to sleep mode. In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message and SMS.
	LTE Idle	Software is active. The module is registered to the network, and the module is ready to communicate.
	LTE Talk	Two customers are connected. In this case, the power consumption of the module depends on the network and module configuration.
	LTE Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g., power control level); uplink/downlink data rates (e.g., multi-slot configuration), etc.
Minimum functionality mode		AT command ‘AT+CFUN=0’, ‘AT+CSCLK=1’ can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work and the USIM card will not be accessible, and the UART does not work properly. The power consumption in this mode is lower than normal mode.
Flight mode		AT command ‘AT+CFUN=4’ can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
PSM mode		The module can be set to PSM mode by AT command without removing the power supply. In this mode, the CPU is powered off, only the clock circuit inside the module works, the network is not connected, and the serial port and USB are unavailable. In this case, the power consumption of the module is reduced to the minimum.

Power off	Module will go into power off mode by sending the AT command 'AT+CPOF' or pull down the PWRKEY pin, normally. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are not accessible.

5.3.2. Sleep Mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message and SMS.

Both hardware and software should meet several conditions simultaneously so that the module will enter into sleep mode:

- The peripherals (GNSS and Bluetooth, etc.) of the module stop working.
- Set sleep mode and the source of waking up the module by "AT+CSCLK=<n>".
- Disconnect the USB_VBUS power supply.

If the software support sleep mode configuration and the module's peripherals stop working, after sending "AT+CSCLK=<n>" by MAIN_UART or USB and disconnect the USB_VBUS power supply, the module will enter sleep mode.

NOTE

1. If the module enters sleep mode by sending "AT+CSCLK=1", pulling down the MAIN_DTR can wake up the module.
2. If the module enters sleep mode by sending "AT+CSCLK=2", sending data to the MAIN_RXD can wake up the module.
3. If the module enters sleep mode by sending "AT+CSCLK=3", pulling up the WAKEUP can wake up the module.

5.3.3. Minimum Functionality Mode and Flight Mode

Minimum power consumption mode ceases a majority function of Module, to enable the module enter the minimum power consumption mode, the following hardware and software conditions must be followed:

(1) Module is in normal mode.
(2) Send AT command "AT+CFUN=0".
(3) Send AT command "AT+CSCLK=1".
(4) DTR pin pulled to high level and USB_ VBUS pulled to low level.

This mode is set by the AT command which provides a choice of the functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If the module has been set to minimum functionality mode, the RF function and SIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and SIM card will be unavailable.

If the module has been set to flight mode, the RF function will be closed. In this case, the serial port and USB are still accessible, but RF function will be unavailable.

When the module is in minimum functionality or flight mode, it can return to full functionality by the AT command “AT+CFUN=1”.

5.3.4. PSM Mode

The PSM mode can be set by “AT+CPSMS”, and it can minimize the current consumption.

The module is initially in the RRC connect state, and it will enter idle mode after disconnecting RRC Connect by “end call”, while the timer T3324/T3412 starts timing. After the timer T3324 expires, the module enters the PSM mode. The module will wake up automatically after the timer T3412 expiring, and it will enter TAU mode.
The AT command for entering the PSM mode are as follows:
AT*COMCFG=1,,,,,254//Enable the 1bis
AT+CFUN=0
AT+CPSMS=1,,,"01100101","00000101"//Open the PSM
AT+MEDCR=0,103,1
AT+MEDCR=0,71,2//Set the wake-up time to 2 minutes
AT+CFUN=1

After entering the PSM mode, the module will terminate the network connection, and unable to respond to requests. Customers can send AT command when the timer T3412 expiring or pull down the PWRKEY to wake up the module. The module will exit the PSM mode by “AT+CPSMS=0”.

5.3.5. RTC Mode

Module supports RTC mode for alarm clock, timer, auto power-on by alarm clock or other functions, it can track or record the current date and time by sending "AT+CCLK?". There is no independent 32K crystal oscillator and RTC backup power supply for RTC clock inside the module, and the RTC logic requires VBAT power supply to PMU to generate the RTC clock, so the power supply for VBAT should not be turned off.

Module can enter the RTC mode even in shutdown or sleep mode as long as the correct power supply connected to VBAT.
RTC clock is generated by the divider, and LDO is always on for power supply to 26M XO, so LDO will occur some current consumption. The RTC block diagram is shown as follow.

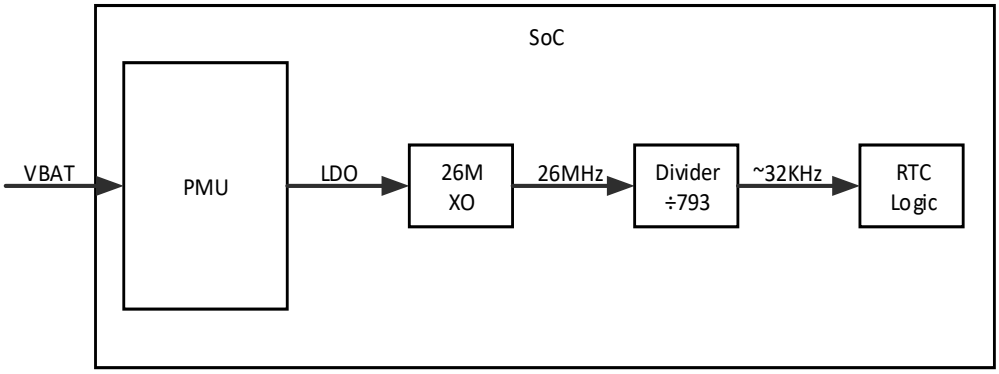


Figure 32: RTC Block Diagram

Table 57: RTC Characteristics

Operating Conditions	RTC Time Accuracy	VBAT Current Consumption
VBAT=3.8V Module shutdown	+/- 1 s within 24H(Typical)	110uA (Typical)

NOTE

For current software version, LDO will be turned off by default after module turned off, so RTC function is not supported; If need to keep LDO always on after module turned off, please contact honqtech FAE to get customized software version.

5.4. Current Consumption of LTE Operation

The current consumption is listed in the table below.

Table 58: Current Consumption on VBAT Pins (VBAT=3.8V)

PSM Mode	
PSM supply current	Typical: 120uA

LTE sleep/Idle Mode	
LTE supply current (Without USB connection)	Idle mode Typical: 11mA Sleep mode@DRX=0.32S typical: 1.8mA Sleep mode@DRX=0.64S typical: 1.4mA Sleep mode@DRX=1.28S typical: 1.2mA Sleep mode@DRX=2.56S typical: 1mA
Minimum Functionality Mode	
AT+CFUN=0, AT+CSCLK=1	Typical: 0.84mA (With simcard) Typical: 0.86mA (Without simcard)
LTE Cat1	
LTE-FDD B2	@5MHz 23dBm Typical :548mA
LTE-FDD B4	@5MHz 23dBm Typical :594mA
LTE-FDD B5	@5MHz 23dBm Typical :596mA
LTE-FDD B12	@5MHz 23dBm Typical :526mA
LTE-FDD B13	@5MHz 23dBm Typical :521mA
LTE-FDD B66	@5MHz 23dBm Typical :575mA

5.5. ESD Notes

The module is sensitive to ESD in the process of storage, transporting, and assembling. When the module is mounted on the customers' mother board, the ESD components should be placed beside the connectors which human body may touch, such as SIM card holder, audio jacks, switches, keys, etc. The following table shows the ESD measurement performance.

Table 59: The ESD Performance Measurement Table (Temperature: 25℃, Humidity: 45%)

Part	Contact Discharge	Air Discharge
VBAT, GND	±4KV	±8KV
Antenna port	±4KV	±8KV
Other PADs	±0.5KV	±1KV

6. SMT Production Guide

6.1. Top and Bottom View of the Module

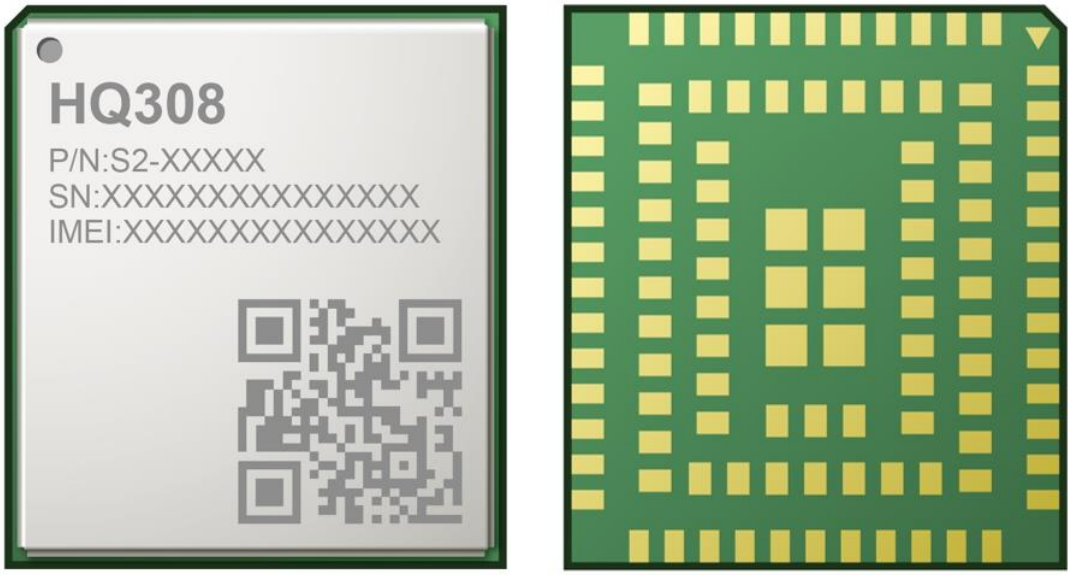


Figure 33: Top and Bottom View of the Module

NOTE

The above is the design effect diagram of the module for reference. The actual appearance is subject to the actual product.

6.2. Label Information

Figure 34: Label Description of the Module

Table 60: The Description of Label Information

No.	Description
A	Project name
B	Part number
C	Serial number
D	IMEI number
E	QR code

6.3. Recommended PCB Footprint

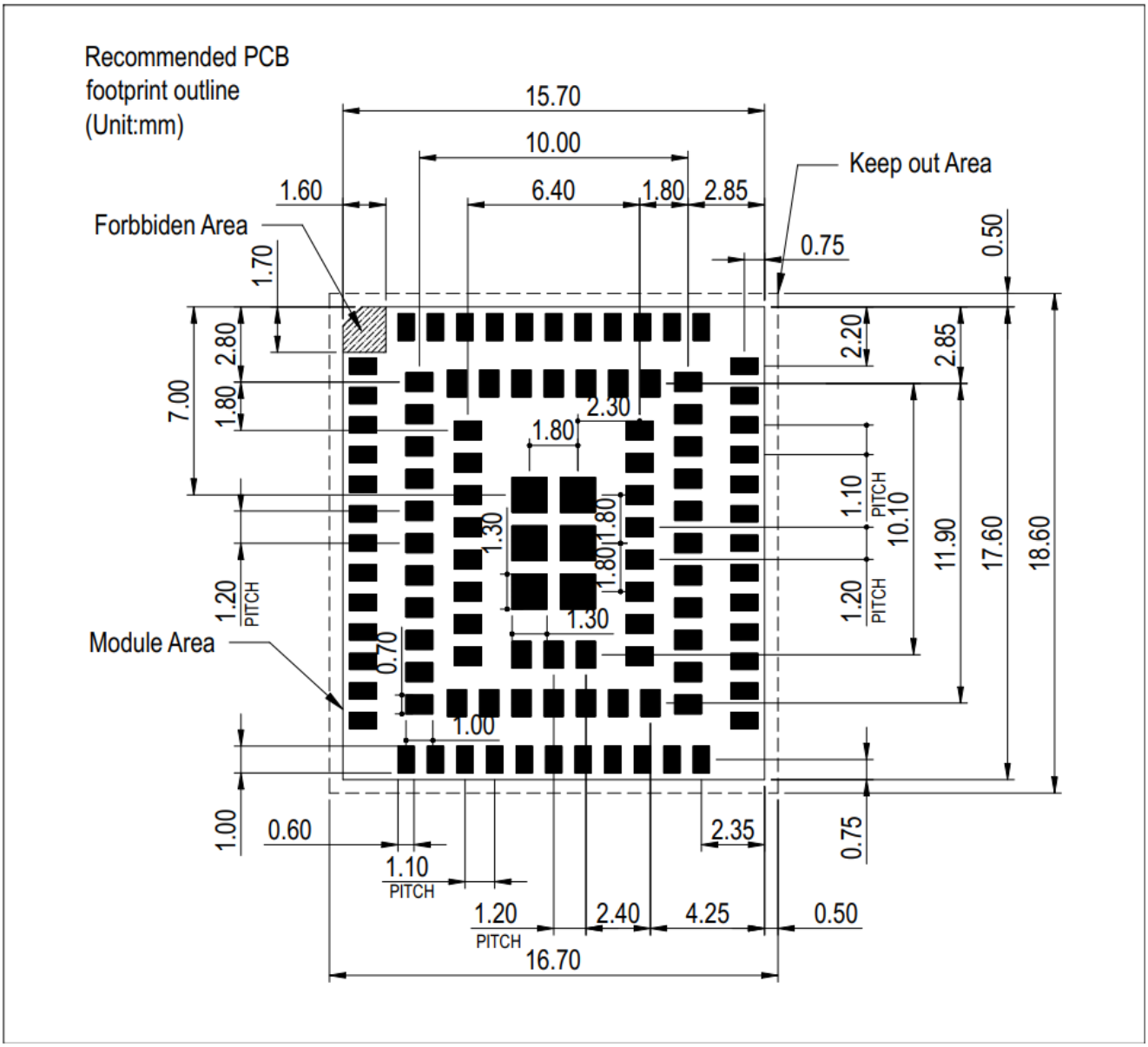


Figure 35: Footprint Recommendation (Unit: mm)

6.4. Recommended SMT Stencil

The recommend stencil thickness is 0.15mm.The following figure shows the SMT stencil of the module.

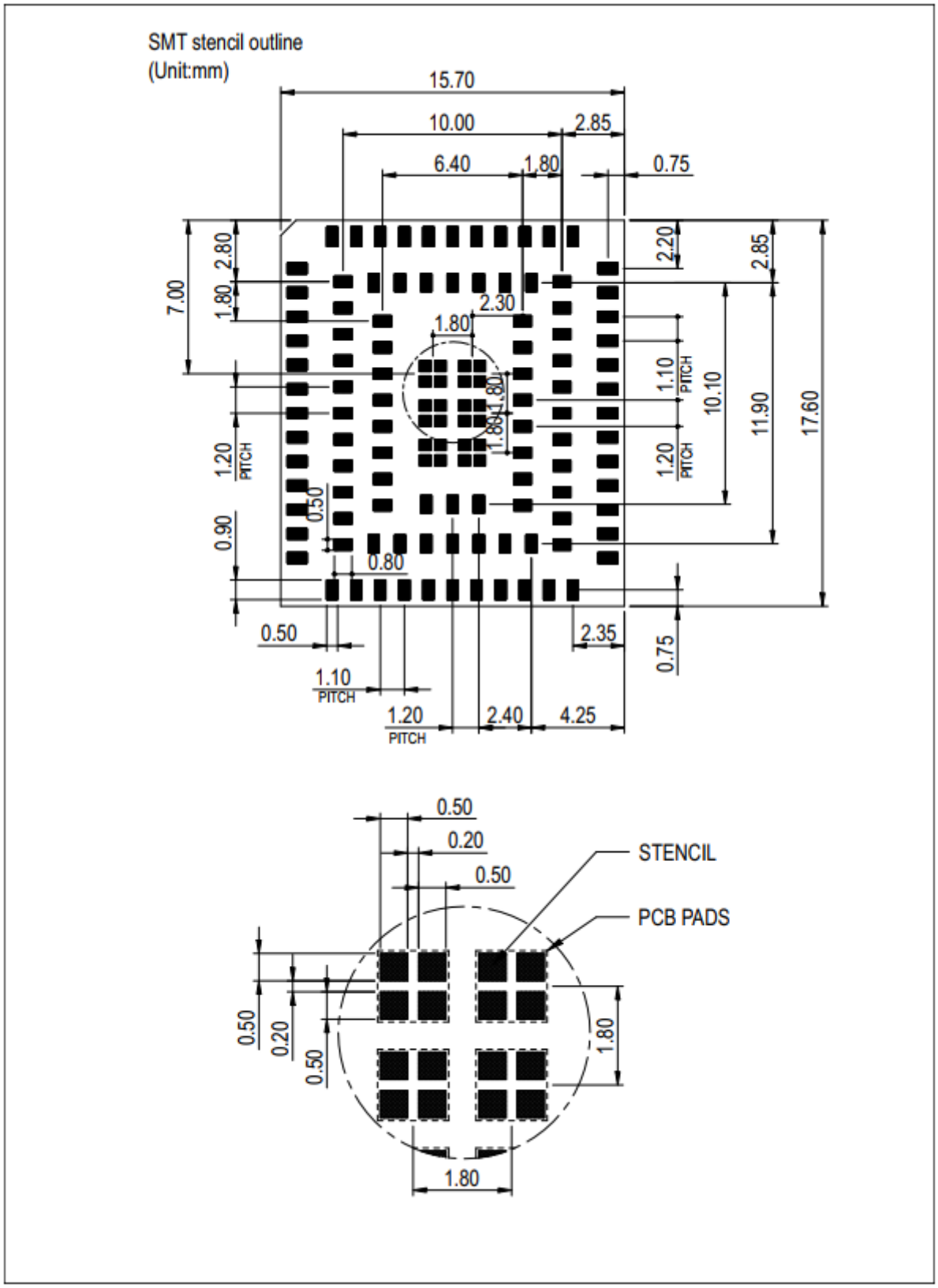


Figure 36: Recommended SMT Stencil (Unit: mm)

6.5. Recommended Reflow Furnace Temperature Curve

It is recommended to lead free.
During the furnace temperature test, the thermocouple test point should be connected to the module position to ensure that the module position reaches the required temperature. Recommended furnace temperature profile (lead-free SMT reflow) is as follows:

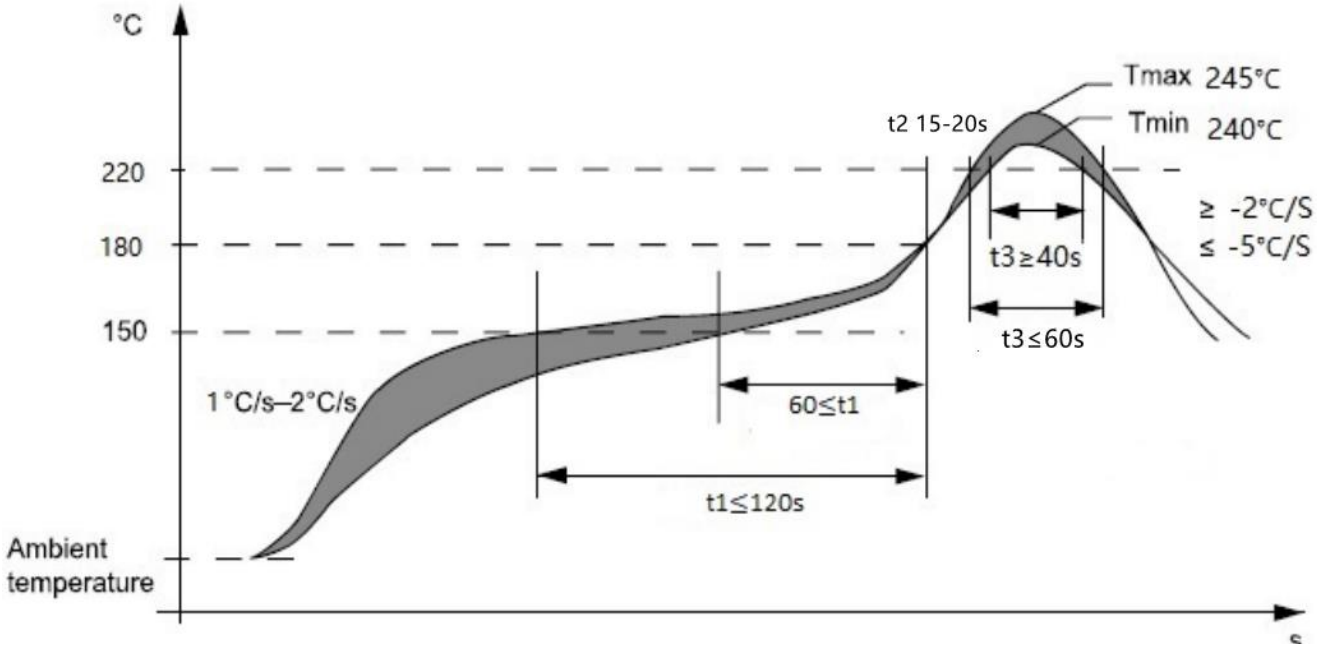


Figure 37: Recommended Reflow Furnace Temperature Curve (lead-free)

Table 61: The Main Board Reflux Temperature Curve Requirements (lead-free)

Temperature Range	Time	Critical Parameter
Preheating zone (Room temperature~150 ℃)	NA	Temperature rise slope 1~2℃/s
T1(150~180℃)	60-120s	/
T2(180-220℃)	15-20s	/
T3(≥220℃)	40-60s	Peak temperature 240~245℃
Cooling Zone	NA	Cooling slope -2~-5℃/s

NOTE

- The maximum times of refluxes for the module is once.
- Recommended lead-free process.
- In the table above, the temperature testing location includes the solder mask of the module MCU pins, bottom LGA pins, and external LCC pins.
- The actual welding temperature is affected by other external factors, such as the presence of furnace carriers, solder paste, size and thickness of the substrate, and component resistance. Thermal requirements and panel design, etc. Please confirm with our engineering and technical personnel in time if the recommended parameters cannot be reached. Otherwise, the module may be damaged.
- For boards with thickness less than 1.2mm, it is recommended to use board supported by furnace carrier or materials with high Tg to prevent warping when heated. Deformation, thus affecting module welding. For modules larger than 35.0 mm *35.0 mm and 5G products, it is recommended to use the furnace carrier to pass through the furnace to reduce the cause of the bottom plate and mold. Due to the difference of Tg value of block, the phenomenon of unbalanced thermal stress appears in the process of high temperature welding reflow, resulting in the defect rate of virtual welding and little tin.
- After the module is welded, X-ray and optical inspection methods shall be used to check the welding quality. For specific standards, please refer to relevant standards of IPC-A-610H.
- Due to the complexity of the SMT process, in case of uncertainty or processes not mentioned in this document (such as selective wave soldering, ultrasonic welding), please contact honqtech support team before SMT process starts.

6.6. Moisture Sensitivity Level (MSL)

The modules are shipped in vacuum-sealed aluminum foil bag bags, vacuum packaging according to IPC/JEDEC standard J-STD-020C specification.

- Recommended storage conditions: temperature 23℃± 5℃, and relative humidity 35%~60%.
- Storage period: 12 months (Under recommended storage conditions and in sealed vacuum packaging).

The module meets the humidity sensitivity level 3 (MSL-3), and the storage period after unpacking is shown in table below.

The out-of-bag floor life of the module with MSL-3 is 168 hours. If the workshop temperature is 23℃±5℃ and the relative humidity is less than 60%, the module needs to be unpacked within 168 hours of reflux production or other high temperature operations. Otherwise, the module shall be stored in an environment with relative humidity less than 10% (for example, a moisture-proof cabinet) to keep the product dry.

Table 62: Moisture Sensitivity Level

MSL	Out-of-bag Floor Life	Comment
1	Unlimited	≤+30℃/85% RH
2	1 year	≤+30℃/60% RH
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	

Before using, it is necessary to confirm whether the package is in good condition. After unpacking, check the status of humidity indicator card in vacuum bag (Figure 38). The module needs to be baked before use if any of the following conditions occur.

- Explanation Humidity indicator card: 30%, 40%, and 50% of any indicator circle has discolouring.
- The module has been un-packed and the module exceeds the humidity sensitivity level corresponding to the exposed workshop time. For example, MSL=3 is 168.
- Packed, but the Shelf Life exceeds 12 months.
- Exceeds the Floor Life.
- Unable to track and determine the status of the module.

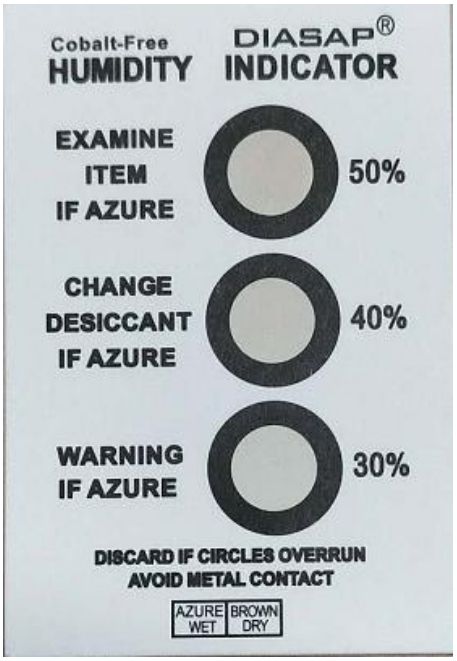


Figure 38: Humidity Card

The following conditions also need to be pre-baked.

- The storage temperature and humidity do not meet the recommended storage conditions.
- Vacuum sealed bag leak, bulk materials.
- Before repairing the module.
- After unpacking, the module failed to complete production or storage under the control of humidity sensitive level 3.

6.7. Baking Requirements

If baking is required, proceed according to the requirements in the table below. Preferentially choose a nitrogen-filled oven.

Table 63: Module Baking Requirements

Baking Conditions	Baking Time	Comment
120℃±5℃, <5% RH	8 hours	Not applicable to original packaging pallets

NOTE

- In order to prevent and reduce the occurrence of poor welding caused by moisture, such as foaming and delamination, the module should be strictly controlled. It is not recommended to expose the module to air for a long time after unpacking the vacuum package.
- Before baking, it is necessary to remove the module from the package and place the bare module on the high temperature resistant device to avoid high temperature damage to the plastic tray or coil. The modules for secondary baking must be welded within 24 hours after baking. Otherwise, they need to be stored in vacuum packaging or in a drying oven.
- Please pay attention to ESD protection when unpacking and placing modules, such as wearing anti-static gloves.

7. Packaging

7.1. Tray Packaging

The module support tray packaging.

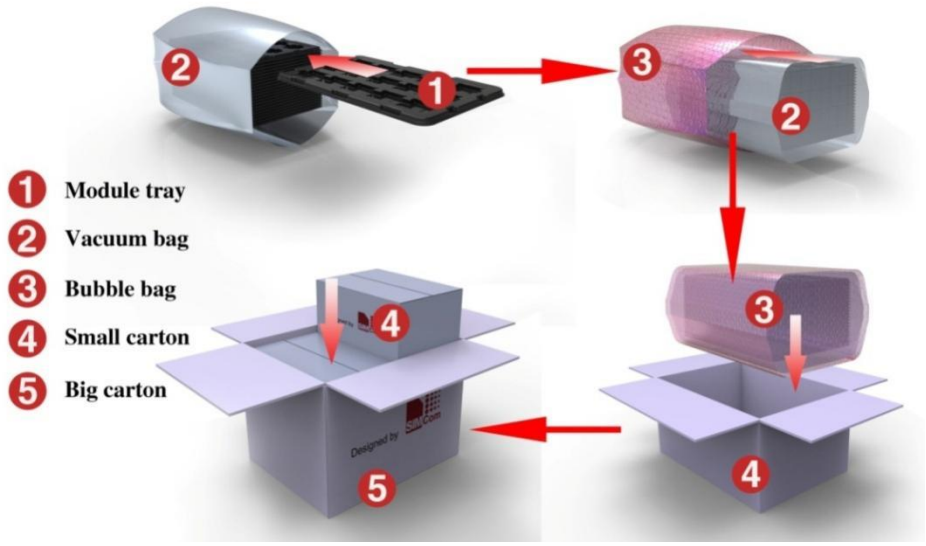


Figure 39: Tray Packaging Diagram

Module tray drawing:

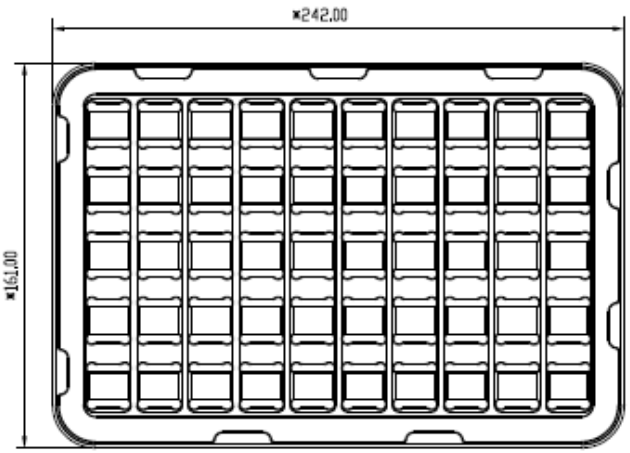


Figure 40: Tray Drawing

Table 64: Tray Size

Length (±3mm)	Width (±3mm)	Module Number
242.0	161.0	50

Small carton drawing:

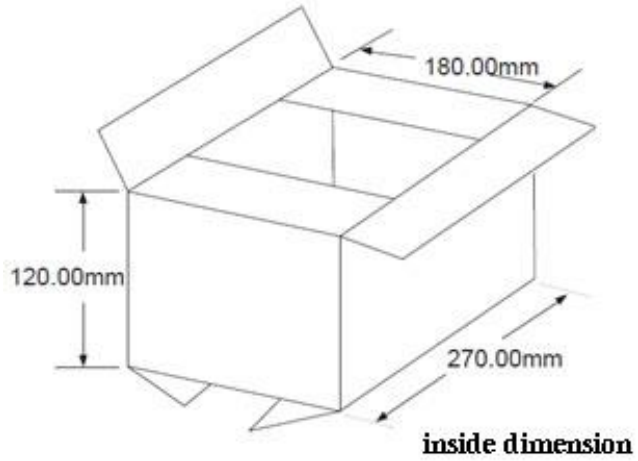


Figure 41: Small Carton Drawing

Table 65: Small Carton Size

Length (±10mm)	Width (±10mm)	Height (±10mm)	Module Number
270	180	120	50*20=1000

Big carton drawing:

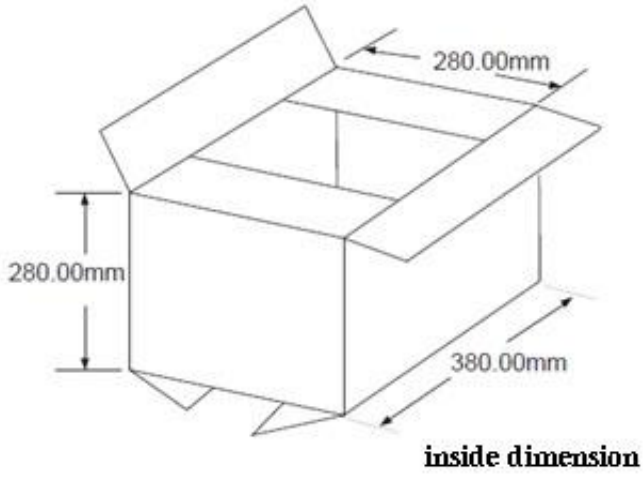


Figure 42: Big Carton Drawing

Table 66: Big Carton Size

Length (±10mm)	Width (±10mm)	Height (±10mm)	Module Number
380	280	280	1000*4=4000

7.2. Reel Packaging

Module support reel packaging.

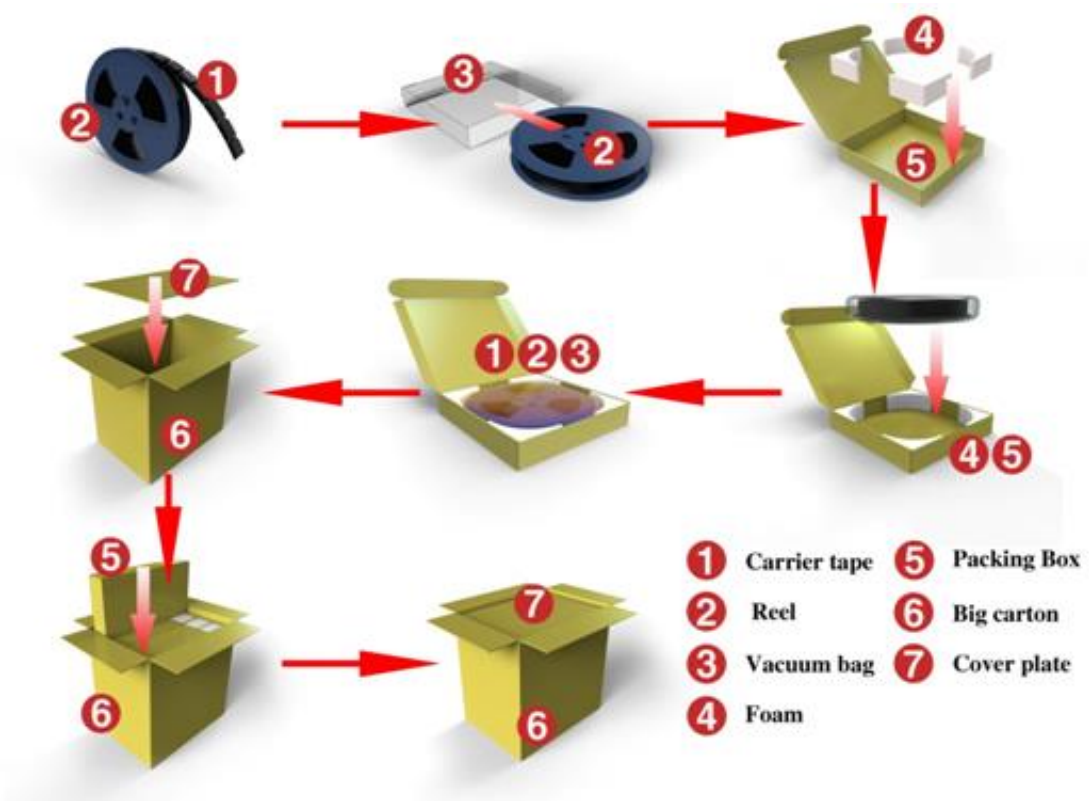


Figure 43: Reel Packaging Diagram

Carrier tape drawing：

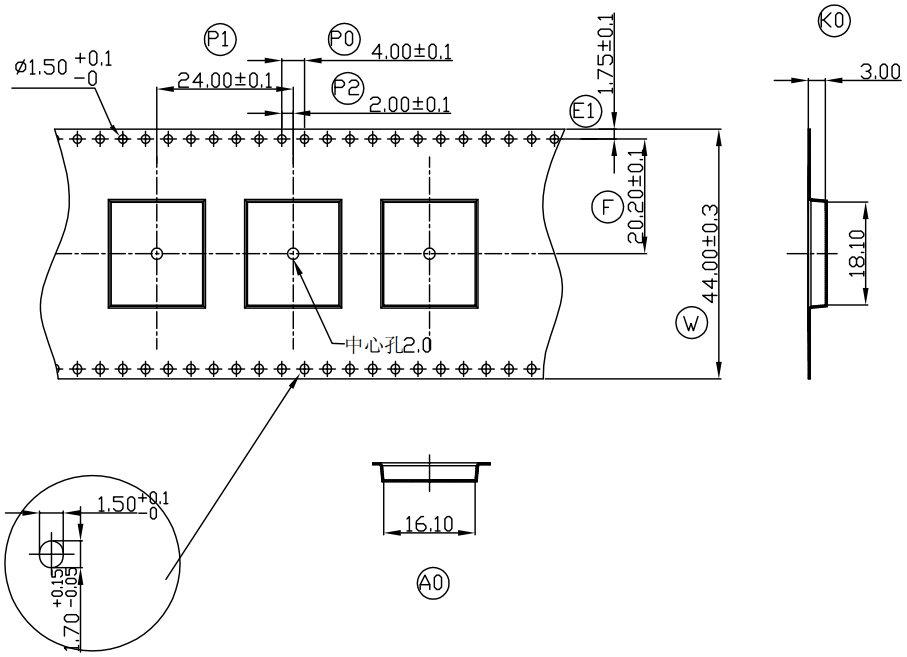


Figure 44: Carrier Tape Drawing

Table 67: Reel Size

External Diameter (mm)	Width (mm)	Inside Diameter(mm)	Module Number
330.0	44.0	180.0	500

Packing box drawing:

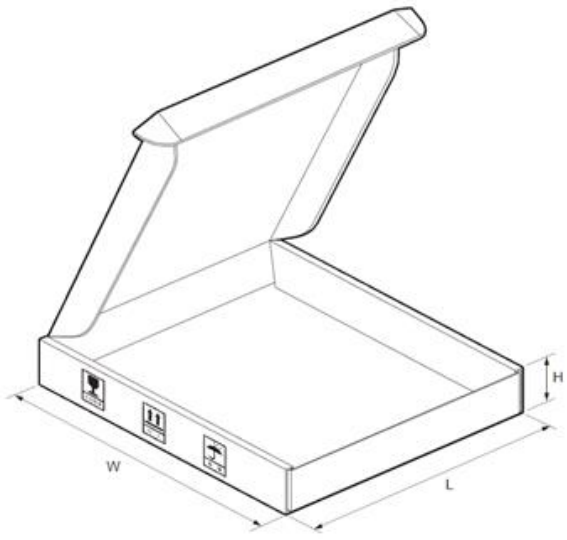


Figure 45: Packing Box Drawing

Table 68: Packing Box Size

Length(±10mm)	Width(±10mm)	Height(±10mm)	Module Number
345	340	60	500

Big carton drawing:

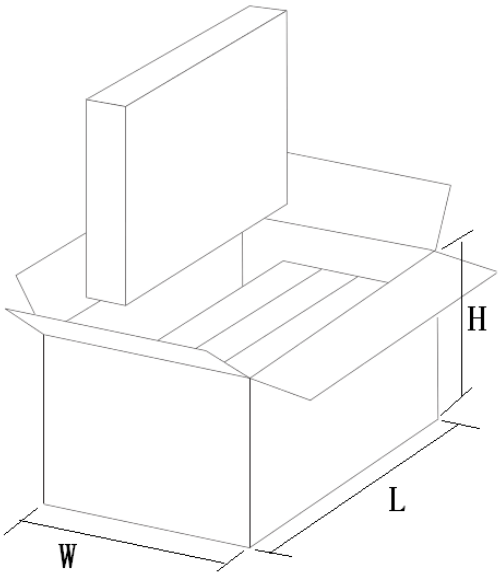


Figure 46: Big Carton Drawing

Table 69: Big Carton Size

Length(±10mm)	Width(±10mm)	Height(±10mm)	Module Number
380	275	380	500*4=2000

8. Appendix

8.1. Coding Schemes and Maximum Net Data Rates over Air Interface

Table 70: Coding Schemes and Maximum Net Data Rates over Air Interface

LTE-FDD Device Category (Downlink)	Max Data Rate (peak)	Modulation Type
Category 1	10Mbps	QPSK/16QAM/64QAM
LTE-FDD Device Category (Uplink)	**Max Data Rate (peak)**	**Modulation Type**
Category 1	5Mbps	QPSK/16QAM

8.2. Related Documents

Table 71: Related Documents

NO.	Title	Description
[1]	ITU-T Draft new recommendationV.25ter	Serial asynchronous automatic dialing and control
[2]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[3]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[4]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[6]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.

[7]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[8]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment.
[9]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[10]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[11]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[12]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

8.3. Terms and Abbreviations

Table 72: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ARP	Antenna Reference Point
BER	Bit Error Rate
BD	BeiDou
BTS	Base Transceiver Station

CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
DAM	Downloadable Application Module
DPO	Dynamic Power Optimization
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FCC	Federal Communications Commission (U.S.)
FD	SIM fix dialing phonebook
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Standard for Mobile Communications
HR	Half Rate
I2C	Inter-Integrated Circuit
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
NMEA	National Marine Electronics Association
PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PCS	Personal Communication System, also referred to as GSM 1900
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
SIM	Subscriber Identification Module
SMS	Short Message Service

SMPS	Switched-mode power supply
TDMA	Time Division Multiple Access
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
EDGE	Enhanced data rates for GSM evolution
ZIF	Zero intermediate frequency
WCDMA	Wideband Code Division Multiple Access
VCTCXO	Voltage control temperature-compensated crystal oscillator
USIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
PSM	Power saving mode
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

8.4. Safety Caution

Table 73: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operating over radio frequency signals and cellular networks cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.