DX-SMART

DX-LR01-900
Module Technical Manual

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1. Module Introduction

1.1. Overview

DX-LR01-900M is a low-power LoRa module, which is designed for intelligent wireless data transmission by Shenzhen Daxia Longque Technology Co., Ltd. It uses the domestic ASR6601 SOC chip, which integrates a SUb 1GHz RF transceiver, an Arm China STAR-MC1 microprocessor, built-in Flash storage, and SRAM. This module supports interfaces such as UART, I2C , and I2S , supports IO port control, ADC acquisition, and has the advantages of low power consumption, high performance, long distance, and networking. It is suitable for a variety of application scenarios in the IoT field, such as smart meters, smart logistics, smart buildings, smart cities, smart agriculture, and many other application scenarios.

1.2. Features

- ASR6601 SoC
- Arm China STAR-MC1 architecture
- 32-bit ARM STAR core, maximum frequency 48MHz
- High power PA, ultra-large output power: +22dBm
- Maximum receiving sensitivity: -138 dBm
- Support UART, I2C , I2S , LPUART , SSP , QSPI and other interfaces
- Support sleep mode
- External Antenna
- Operating voltage : 3V-3.7 V (typical value: 3.3V)
- Support operating frequency range: 150-960MHz
- The visible distance in an open space can reach 8km (for reference only, the actual distance is subject to actual measurement)
- The distance to the city can be up to 2.9km (for reference only, the actual distance is subject to actual measurement)

1.3. application

- Smart Meter
- Smart Logistics
- Smart Buildings
- Smart City

1.4. Functional Block Diagram

The figure below is a functional block diagram of the DX-LR01-900M module, which explains its main functions as follows:

- Power supply
- Baseband
- Memory
- RF Part
- Peripheral Interface

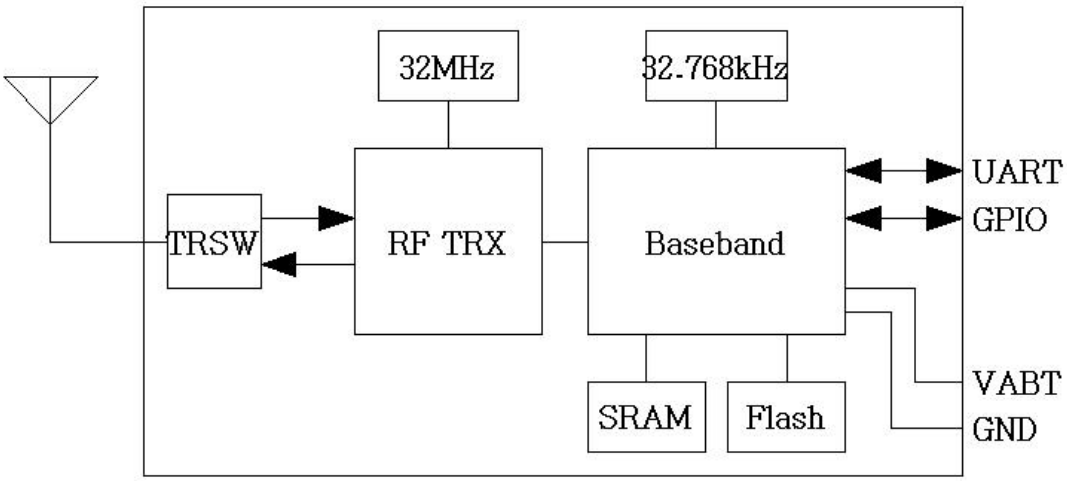


Figure 1 : Functional Block Diagram

1.5. Basic parameters

Table 1 : Basic parameter table

Parameter name	Details	Parameter name	Details
Chip Model	ASR6601	Module Model	DX-LR01-900M
Modulation	Spread spectrum modulation	Module size	19.0 (L) x 1 6.5 (W) x 2.4 (H) mm
Operating voltage	3 V-3.7 V	protocol	LoRa Protocol
Sensitivity	-138 dBm	Transmit power	0 ~ + 1 3 dBm
RF input impedance	50Ω	Frequency band	903-914.2MHz
Antenna interface	External Antenna	Hardware Interface	LPUART

1.6. Transmission method

- Transparent transmission : Data can be transmitted when the sending and receiving channels are the same

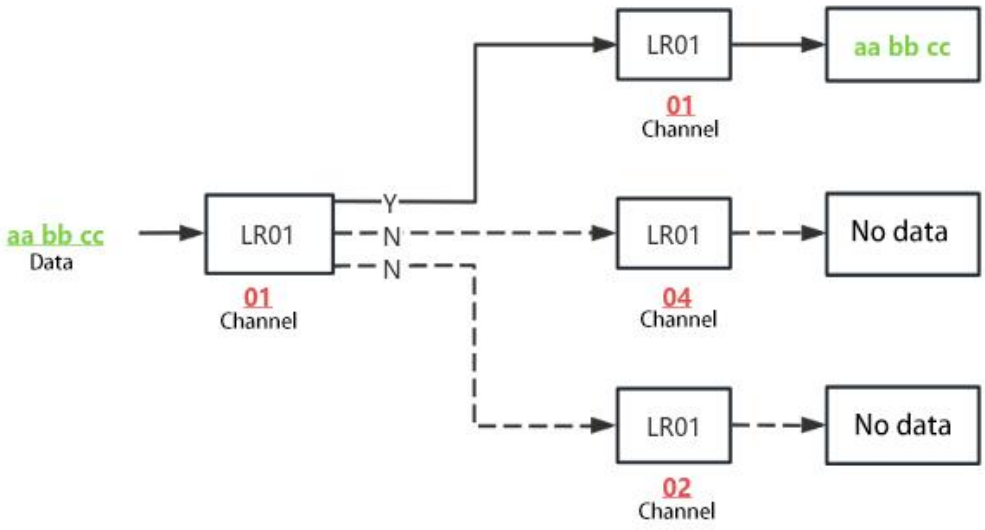


Figure 2 : Transparent transmission

- Fixed-point transmission: When the sender sends data, the target address and target channel contained in the data must be the same as the address and channel of the receiver.

Data format such as: target address (hexadecimal, two bytes) + target channel (hexadecimal, one byte) + data (hexadecimal)

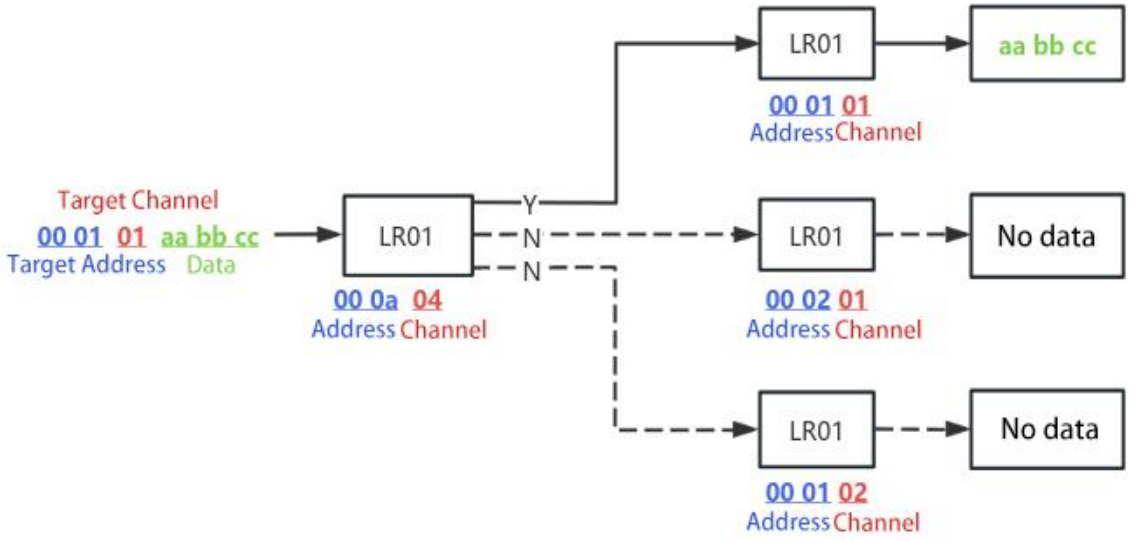


Figure 3 : Fixed-point transmission

- Broadcast transmission: When the sender sends data, the target channel in the data must be the same as the receiving channel.
  Data format such as: target channel (one byte, hexadecimal) + data (hexadecimal)

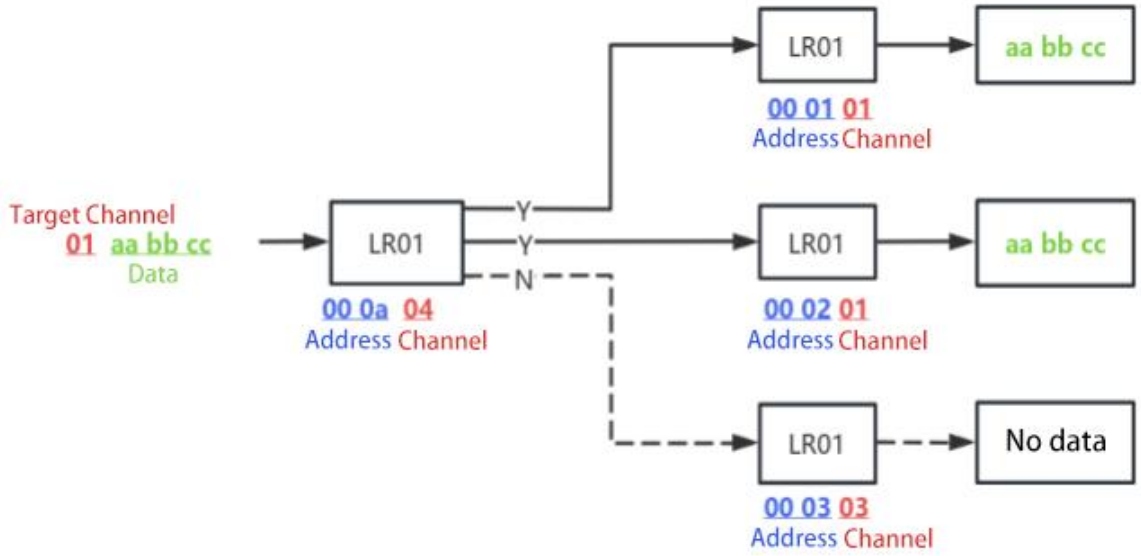


Figure 4 : Broadcast transmission

2. Application Interface

2.1. Module pin definition

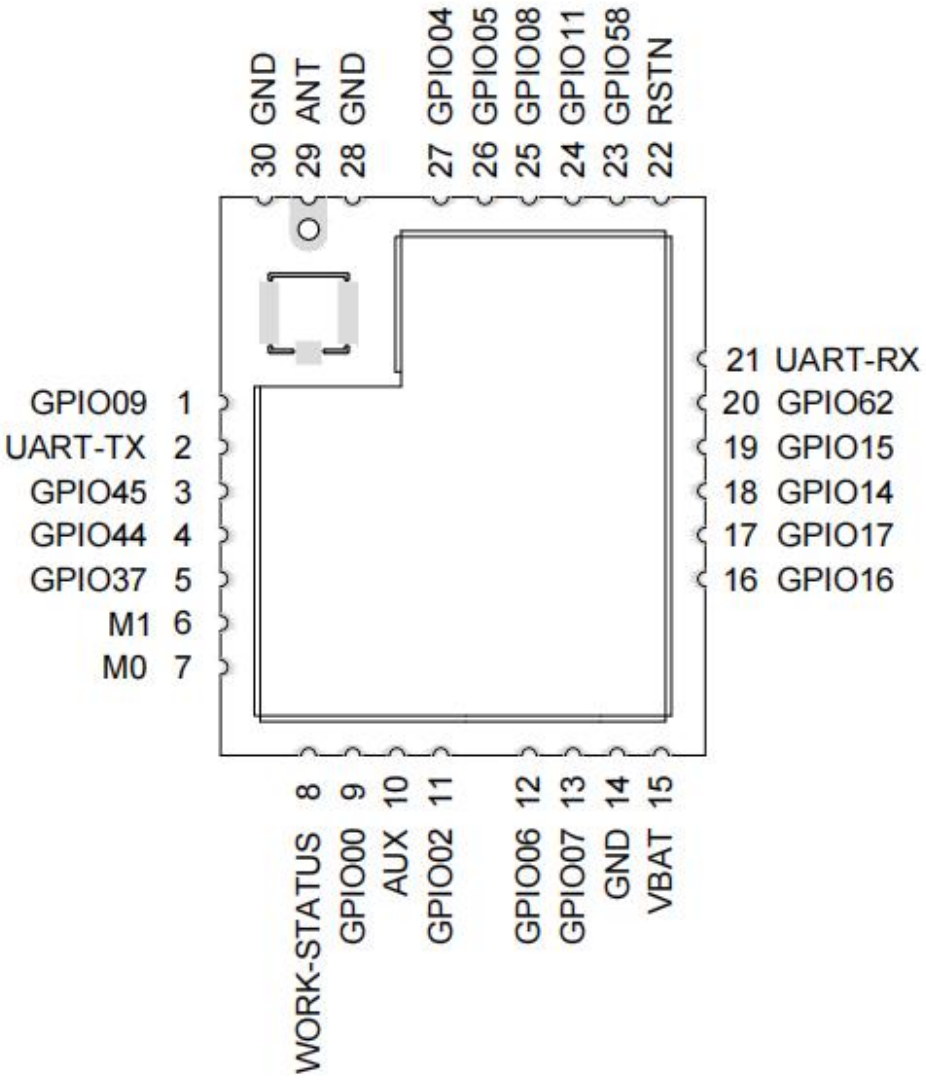


Figure 5 : Module pin definition

2.2. Pin Definition

Table 2 : Pin definition table

Pin number	Pin Name	Pin Function	illustrate
1,3,4,5,9,11,12,13,16,17, 18,19,20,23,24,25,26,27	GPIO09, GPIO45, GPIO44, GPIO37, GPIO00, GPIO02, GPIO06, GPIO07, GPIO16, GPIO17, GPIO14, GPIO15, GPIO62, GPIO58, GPIO11, GPIO08, GPIO05, GPIO04	IO	Programmable input/output pins
2	UART_TX	Serial data output	-
6	M1	Reserve	Customizable IO ports
7	M0	Reserve	Customizable IO ports
8	WORK-STATUS	Module working status output pin	1s high level 1s low level
10	AUX	Module RF status indicator pin	Please refer to 2.3.4 for details
14,28,30	GND	Power Ground	-
15	VBAT	Power input pin	3.3V (typical)
twenty one	UART_RX	Serial data input	-
twenty two	RSTN	Reset	Please refer to 2.3.3 for details
29	ANT	antenna	-

2.3. Power Design

2.3.1. Power interface

Table 3 : Power interface pin definition table

Pin Name	Pin Number	describe	Minimum	Typical Value	Maximum	unit
VBAT	15	Module power supply	3	3.3	3. 7	V
GND	14,28,30	land	-	0	-	V

2.3.2. Power stability requirements

The power supply range of DX-LR01-900M is 3 ~3.7 V , and it is necessary to ensure that the input voltage is not less than 3 V. The figure below shows the voltage drop of V VCC_3V3 during RF burst transmission .

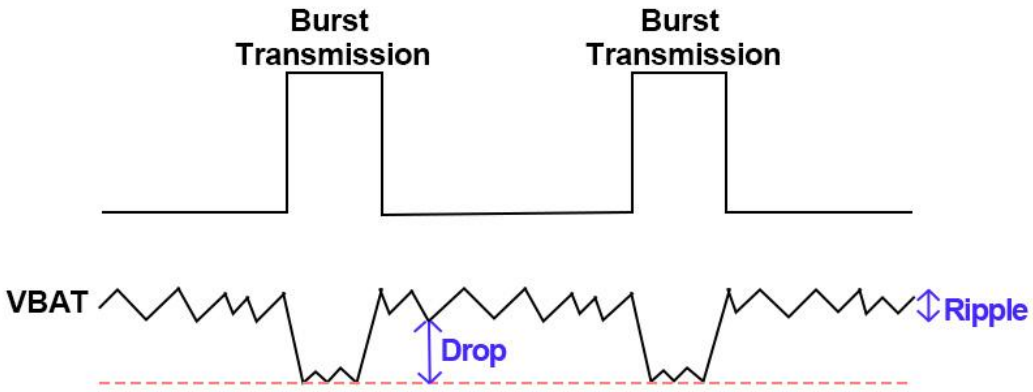


Figure 6 : Burst transmission power requirements

In order to reduce voltage drop, it is recommended to reserve two (100 uF, 0.1uF) chip multilayer ceramic capacitors (MLCC) with the best ESR performance for VBAT , and the capacitors should be placed close to the VBAT pin. The reference circuit is as follows:

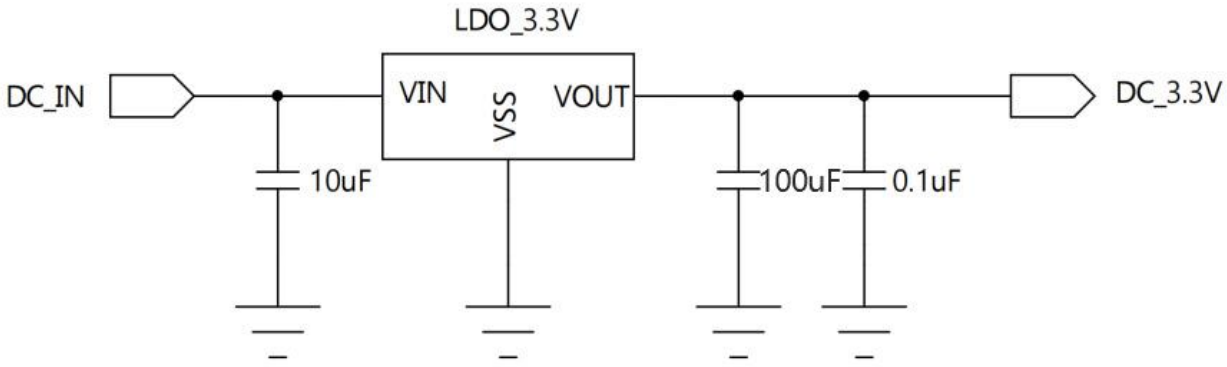


Figure 7 : Power supply reference circuit

2.3.3. RST reset pin description

Table 4 : RST pin definition table

Pin Name	Pin Number	describe	Remark
RSTN	twenty two	Module reset	250ms low level pulse

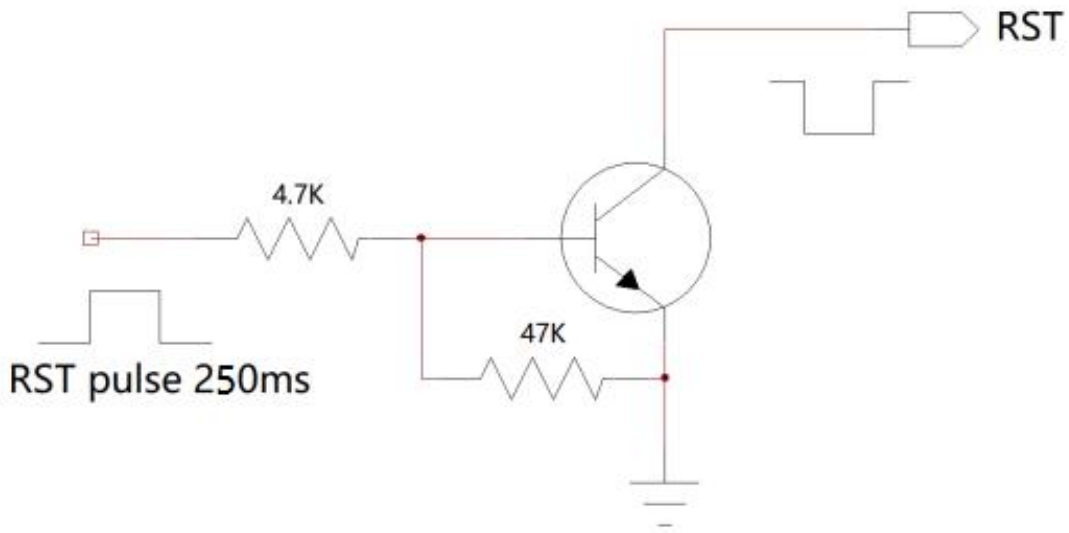


Figure 8 : Reset reference circuit

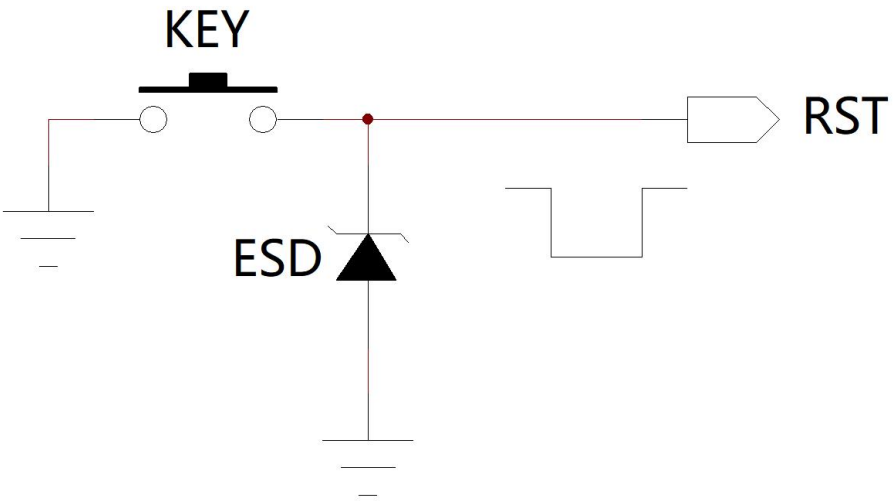


Figure 9 : Push button reset reference circuit

2.3.4. AUX module RF status indicator pin description

- Low level: The module is currently in the receiving idle state or data transmission idle state, and can send data, or is waiting for a response.
- High level: The module is currently in the data receiving or data sending accumulation state. Please wait for the pin to become low level.

2.4. Power consumption

- Sleep mode: In this mode, both the MCU and the RF enter sleep mode. Use the serial port to wake up, and you need to send 4 bytes to wake up. The mode is not written and saved, and you need to use instructions to enter each time.
- Air wake-up mode: In this mode, the module performs CAD detection in a four-second cycle (the overall sleep time is: 4s minus the CAD detection time). If the module detects data, it will enter the receiving mode. After receiving the data, it will automatically enter sleep mode. During sleep, the RF sleeps, but the MCU does not sleep. This mode can be written and saved.
- High-efficiency mode: In this mode, the module is always in the receiving state and can receive data from other devices at any time. When the module serial port receives data from the master control, it switches to the transmitting state and transmits the data. After the transmission is completed, it switches back to the receiving state.

Table 5 : Power consumption table

Working status	state	Current	Unit
Sleep Mode	Standby	56.39	uA
Air wake-up mode	Standby	4.25	mA
	receive	7.05	mA
High time efficiency mode	Standby	8.84	mA
	transmission	62.09	mA
	receive	8.86	mA

2.5. Hardware physical interface

2.5.1. General digital IO port

20 general-purpose digital IO ports are defined in the module . All of these IO ports can be configured by software to implement various functions, such as button control, LED drive or interrupt signal of the main controller. Keep them floating when not in use.

2.5.2. I2C Interface

ASR6601 includes an I2C master mode, supports standard rate mode (100Kbps) and fast mode (400Kbps), and supports multi-master and bus arbitration functions. SDA is the data transmission line and SCL is the reference clock line.

When the software starts to perform a read or write operation, I2C switches from the default slave receive mode to the master transmit mode. The Start condition is followed by a 7-bit slave address and a 1-bit R/nW. When an ACK is received, I2C enters one of the following two modes: Master Transmit Mode - Write Data, Master Receive Mode - Read Data.

The CPU writes the I2Cx_CR register to start a host transaction. The FIFO mode can only be used in the host mode. The FIFO mode can be used for sending and receiving to help reduce the I2Cx_DBR register empty interrupt and full interrupt. The FIFO allows reading and writing multiple bytes without interrupting the CPU after each byte operation.

Figure 10 shows the I2C timing diagram, which is the same as the I2C slave timing diagram.

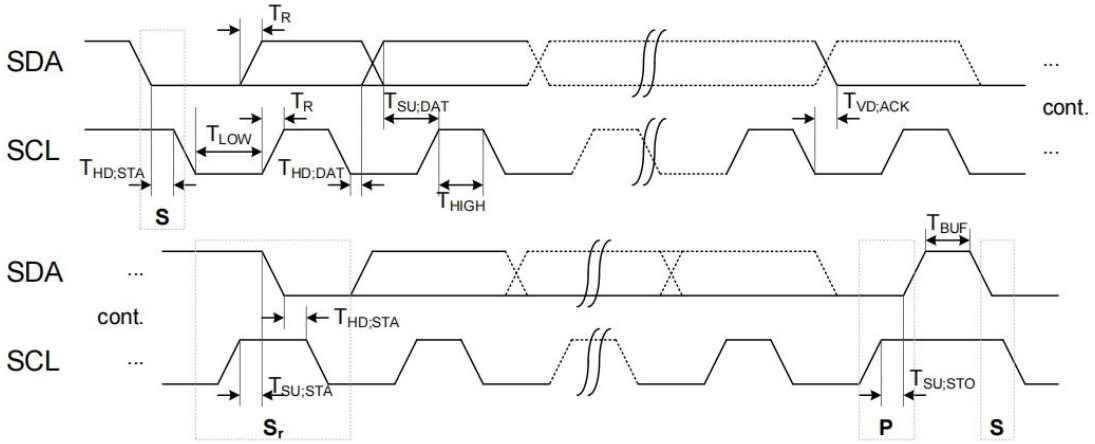


Figure 10 : IIC communication timing diagram

The ASR6601 also includes an I2C slave mode that supports both standard rate mode (100Kbps) and fast mode (400Kbps).

The slave reception is the default mode, I2Cx_CR{UE} must be set to 1, and I2C monitors the Start condition on the bus. If the Start condition is detected, the interface reads the first 8 bits of data and compares the first 7 bits with its own slave address. If they match, it responds to ACK. If the 8th bit (R/nW) of the first byte is low, then I2C remains in the slave reception mode and clears I2Cx_SR{SAD} to 0. If R/nW is high, I2C switches to the slave transmission mode and sets I2Cx_SR{SAD} to 1.

As a receiving slave, I2C pulls the SDA line low when SCL is high to generate ACK and sends it to the host.

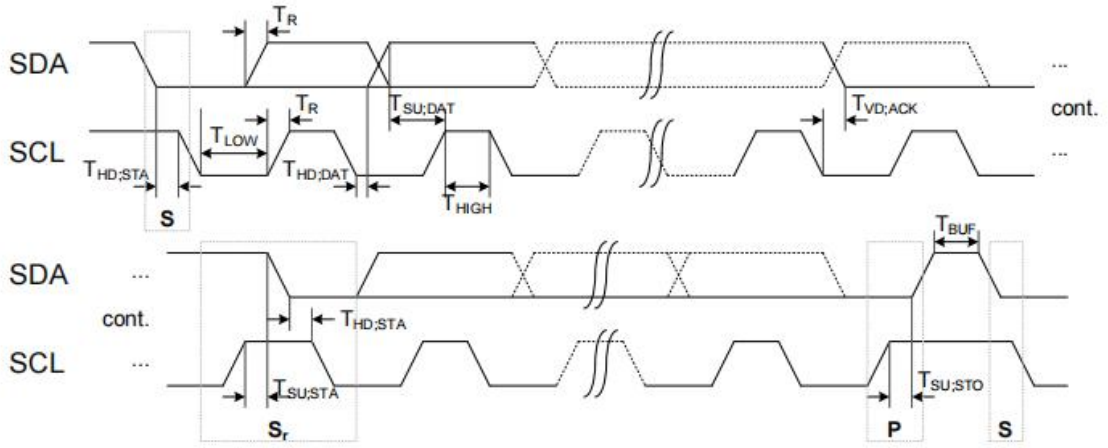


Figure 11 : I2C slave timing diagram

2.5.3. UART Interface

ASR6601 supports UART and IrDA modes. The transmit and receive FIFOs are independent, with 16-bit integer part of the baud rate divisor and 6-bit fractional part of the baud rate divisor. Standard asynchronous communication bits, support 5, 6, 7 and 8-bit data, support parity check, support 1 or 2 stop bits. Support DMA, support false start bit detection, support Line Break generation and detection, support hardware flow control. Each UART port can be uniquely identified through the ID register.

The frequency of UARTCLK must meet the requirements for baud rate generation: FUARTCLK(min)>=16 x baudrate(max), FUARTCLK(max)<=16 x 65535 x baudrate(min).

For example, to generate baud rates between 110 and 460800, the UARTCLK frequency must be between 7.3728MHz and 115.34MHz.

At the same time, UARTCLK cannot be greater than 5/3 times PCLK: FUARTCLK<=5/3 * FPCLK.

The transmit and receive FIFOs are independent and can be turned on or off by the line control register UARTx_LCR_H{FEN}. Transmit 16 x 8, receive 16 x 12, and receive FIFO has a 4-bit status code for each character. The FIFO water level can be configured to 1/8, 1/4, 1/2, 3/4, and 7/8 through the FIFO interrupt water level selection register UARTx_IFLS. When the FIFO is disabled, it is equivalent to a depth of 1. The FIFO status is obtained by querying the flag register UARTx_FR.

IrDA SIR ENDEC provides the function of converting between UART data stream and half-duplex serial SIR interface, encoding and decoding data from UART output and input to UART, with two modes:

In IrDA mode, the logic 0 level is converted to a high level pulse with a width of 3/16 of the nSIROUT baud rate bit period, and the logic 1 level is converted to a low level.

In Low-Power IrDA mode, the high-level pulse width sent is three times the internal IrLPBaud16 cycle (1.63us, assuming the nominal frequency is 1.842MHz). The IrDA SIR physical layer is a half-duplex communication link, and the switching between sending and receiving must maintain a delay of at least 10ms. This delay must be completed by software because the UART does not support automatic delay.

The following figure shows the effect of IrDA 3/16 data modulation:

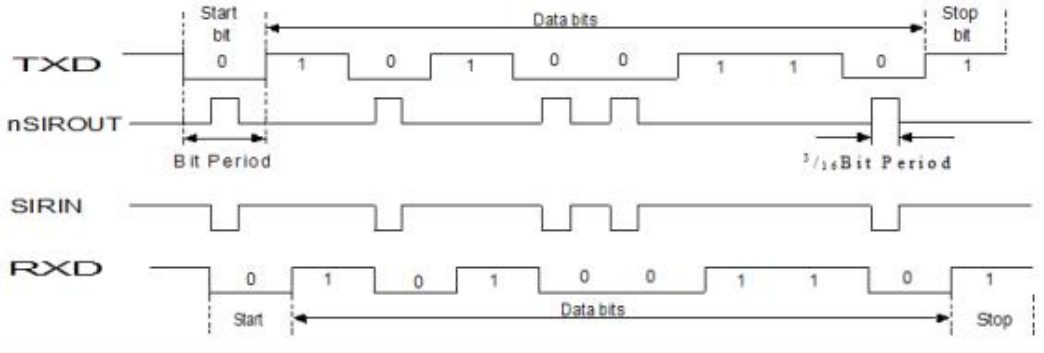


Figure 12 : IrDA data control

Enable UART through UARTx_CR{UARTEN} and configure parameters such as data bit, stop bit, parity check, etc. through the line control register UARTx_LCR_H.

When the receiver is idle, UARTRXD is pulled low, Baud16 enables the receive counter to start counting, and the UART mode starts sampling at the 8th counting cycle. The IrDA mode starts sampling at the 4th counting cycle to allow for shorter logic 0 pulses.

If UARTRXD remains low in the 8th counting cycle, then a valid start bit is detected, otherwise it is judged as a false start and is ignored.

If the start bit is valid, data sampling is performed every 16 Baud16 cycles, and the length is determined by UARTx_LCR_H{WLEN}. If parity check is enabled, the parity bit will be compared.

Finally, when UARTRXD goes high, a valid stop bit is recognized, otherwise a frame error occurs. The complete received character is stored in the receive FIFO along with the error bit.

2.5.4. SSP interface

ASR6601 supports SSP interface, which is a synchronous serial interface that supports MASTER and SLAVE modes. It supports multiple frame formats, and the data width and output rate can be configured as needed. It supports up to 16MHz output and supports 16-bit wide and 8-deep TX/RX FIFO.

SSP has 4 main pins: SSP_NSS, SSP_CLK, SSP_TX and SSP_RX.

- SSP_NSS : SSP chip select signal, low valid.
- SSP_CLK : SSP clock signal, which is the clock output for MASTER mode and the clock input for SLAVE mode.

- SSP_TX : SSP sends the signal, whether in MASTER mode or SLAVE mode, it is the sending pin.
- SSP_RX : SSP receive signal, whether in MASTER mode or SLAVE mode, it is the receive pin.

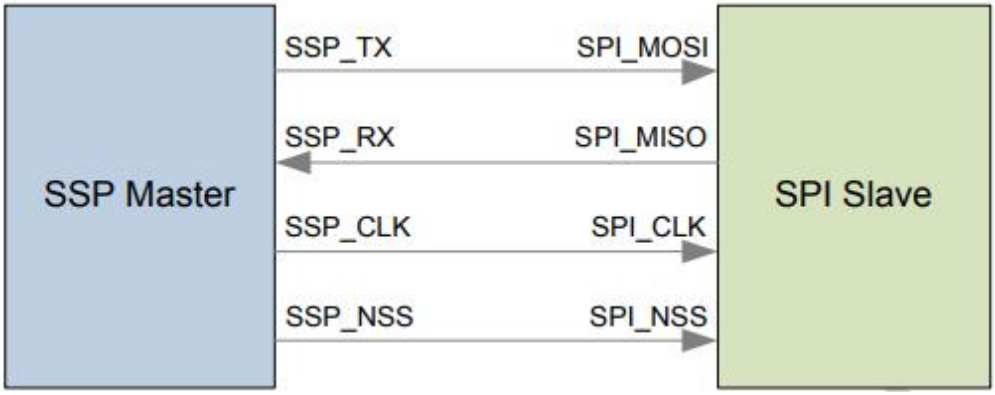


Figure 13 : Connection between SSP master and SPI slave

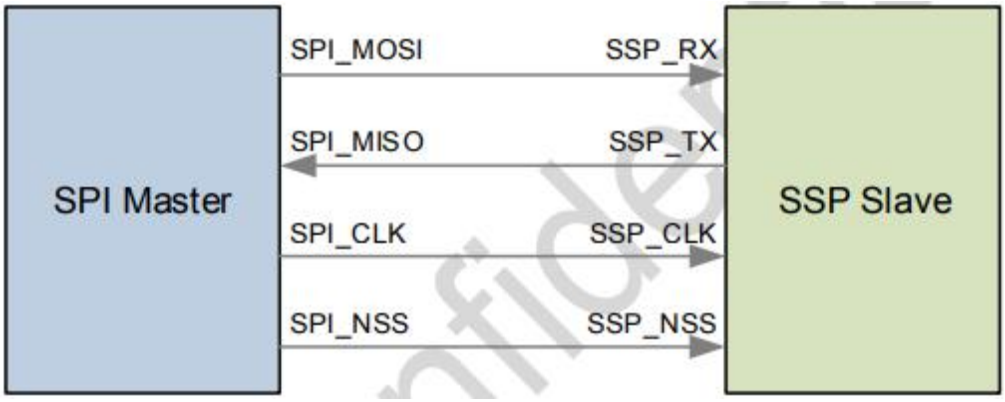


Figure 14 : Connection between SPI slave and SSP master

SSP clock constraints:

- The maximum supported output clock is 16MHz
- In MASTER mode, the maximum clock is 1/2 of PCLK
- In SLAVE mode, the maximum clock is 1/12 of PCLK

clock of SSP . SSPCLKOUT is the output clock of SSP. Taking the default 24MHz as an example , if you want to output a 1MHz clock, set CPSDVR to 2 and SCR to 11.

2.5.5. LPUART

ASR6601 includes LPUART interface, which is a low-power serial peripheral that supports baud rate up to 9600 at 32K clock. In ultra-low power mode, LPUART can also be awakened by received data. LPUART supports CTS/RTS flow control and DMA request.

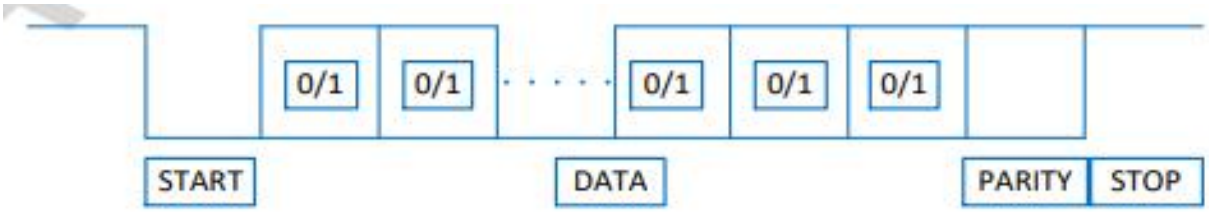


Figure 15 : LPUART data transfer format

When idle, the data line of LPUART should be kept at a high level. During data transmission, the start bit (START), data bit (DATA), parity bit (PARITY) and stop bit (STOP) are transmitted in sequence.

The meaning of each bit is as follows:

- Start bit: A 0 signal is sent first to indicate the start of data transmission.
- Data bits: Depending on the configuration, 5 to 8 bits are transmitted in sequence.
- Parity bit: After the data bit, a parity bit is transmitted, which can also be configured as no parity bit.
- Stop bit: A symbol that indicates the end of data transmission, which can be 1 or 2 bits.

The configuration of LPUART baud rate supports fractional division, which is mainly configured through two registers: LPUART_BAUD_RATE_INT and LPUART_ BAUD_RATE_FRA. Taking the LPUART interface clock frequency as 32.768KHz and the baud rate as 9600 as an example, the division coefficient is 32768/9600=3.413, then the register LPUART_BAUD_RATE_INT is configured as 3, and the register LPUART_BAUD_RATE_FRA is configured as 7 (0.413*16=6.608, rounded to 7).

The connection between the two LPUARTs is as follows:

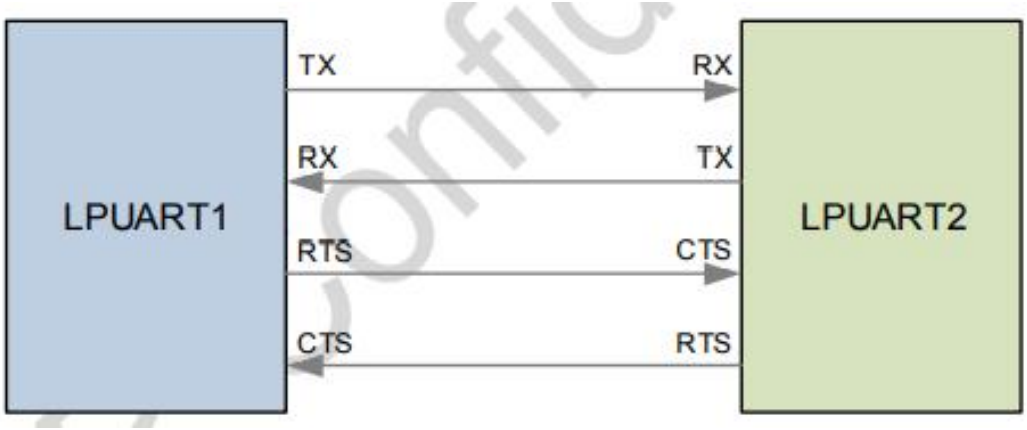


Figure 16 : Connection between two LPUART devices

RTS is an output signal, which indicates that the device is ready to receive data. Low level is effective, which means that the device can receive data. CTS is an input signal, which is used to determine whether data can be sent to the other party. Low level is effective, which means that the device can send data to the other party.

The low power wake-up of LPUART includes RX low level wake-up, valid START wake-up, and RX_DONE wake-up. The wake-up mode is enabled by configuring the LPUART_WAKEUP_EN bit of the LPUART_CR0 register.

2.5.6. Analog-to-digital converter (ADC)

ADC is a 12-bit analog-to-digital converter, which supports 8 external channels and 7 internal channels. The internal channels can collect VBAT/3 and support a maximum sampling rate of 1M. It supports single-ended and differential modes, with a single-ended range of 0.1V~1.1V and a differential range of -1.0~1.0V. It can configure 16 sampling sequences and support continuous, single, and non-continuous sampling modes. It supports software triggering and hardware triggering, and the trigger source can be configured. It supports DMA requests and interrupt requests.

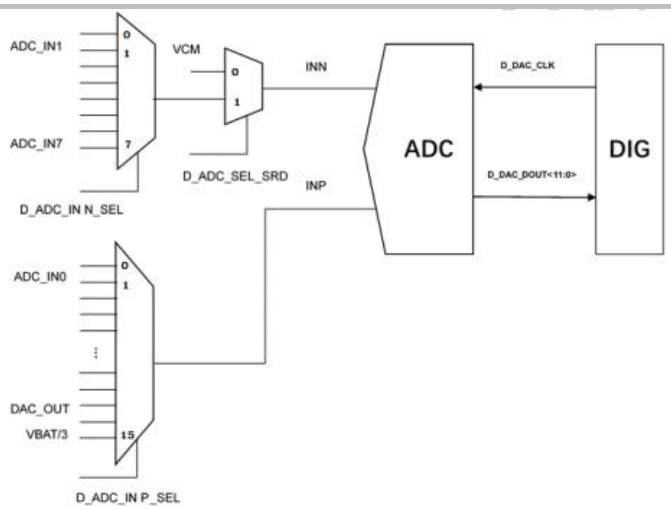


Figure 17 : ADC block diagram

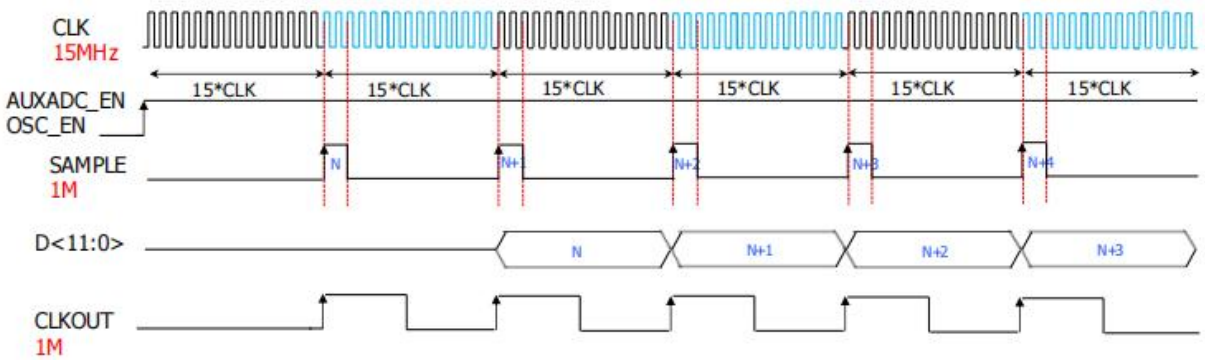


Figure 18 : 12-bit ADC timing diagram

Supports configuration in single-ended and differential modes. External channels support single-ended and differential modes, and internal channels only support single-ended mode. Differential is a fixed combination and does not support random pairing. Channels 0/1 are a group, channels 2/3 are a group, channels 4/5 are a group, and channels 6/7 are a group. Single-ended and differential are controlled differently only in the sampling phase, and there is no difference in the holding phase. In the final data, the highest bit of the differential input is the sign bit (11-bit data bit, 1 sign bit), and the single-ended input is 12-bit data bit without a sign bit. The input mode is configured through the sampling channel differential/single-ended selection register ADC_DIFFSEL.

Configure the sampling mode through ADC_CFGR{CONV_MODE}: Support sampling sequence configuration, the sampling sequence has a maximum of 16 channels, and both single-ended and differential channels can be configured. In differential mode, the sampling sequence only needs to configure the P end. The sampling channel can repeatedly configure the same channel to determine the channel to be sampled multiple times in each sequence. Configure the sampling sequence through the channel sampling sequence control registers

ADC_SEQR0 and ADC_SEQR1. Configure 1 sampling channel for every 4 bits. Two 32-bit registers have a total of 64 bits, and a maximum of 16 sampling channels can be configured.

- Continuous sampling: Once the trigger is valid, the selected input sequence will be continuously converted. After each cycle is completed, a new cycle will automatically start until the software is configured to stop.
- Single sampling: Each trigger executes a sampling sequence cycle, and the sampling ends automatically when it is completed.
- Non-continuous sampling: Each ADC conversion in the sequence requires a hardware or software trigger. If a sequence is completed, the next trigger starts from the beginning of the sequence; while in continuous and single modes, each trigger completes a complete sequence.

2.6. Reference connection circuit

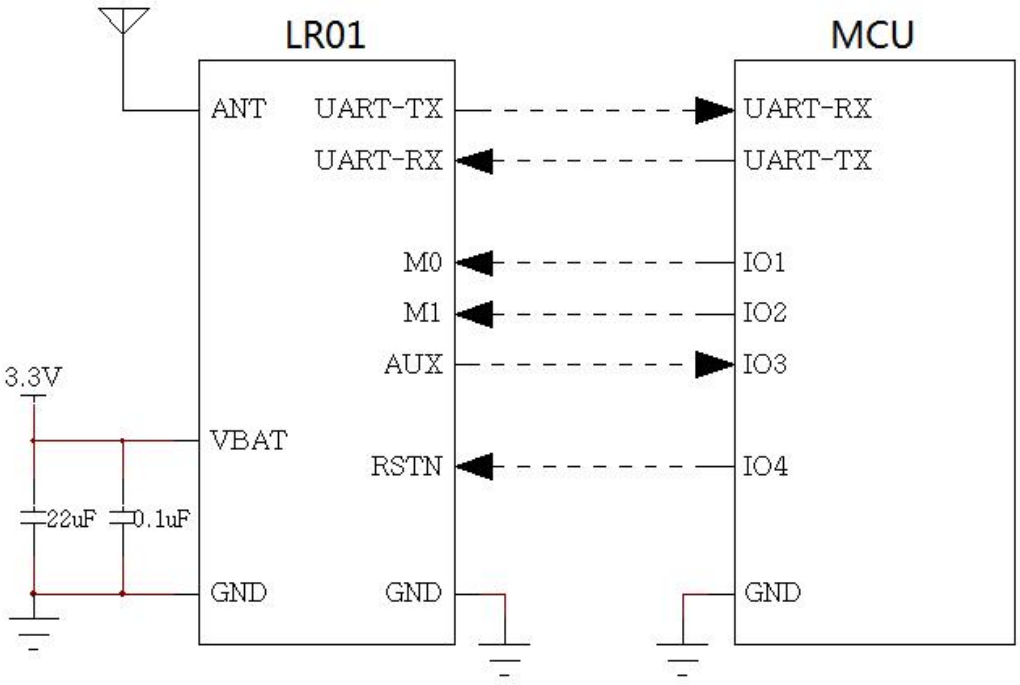


Figure 19 : Typical application circuit

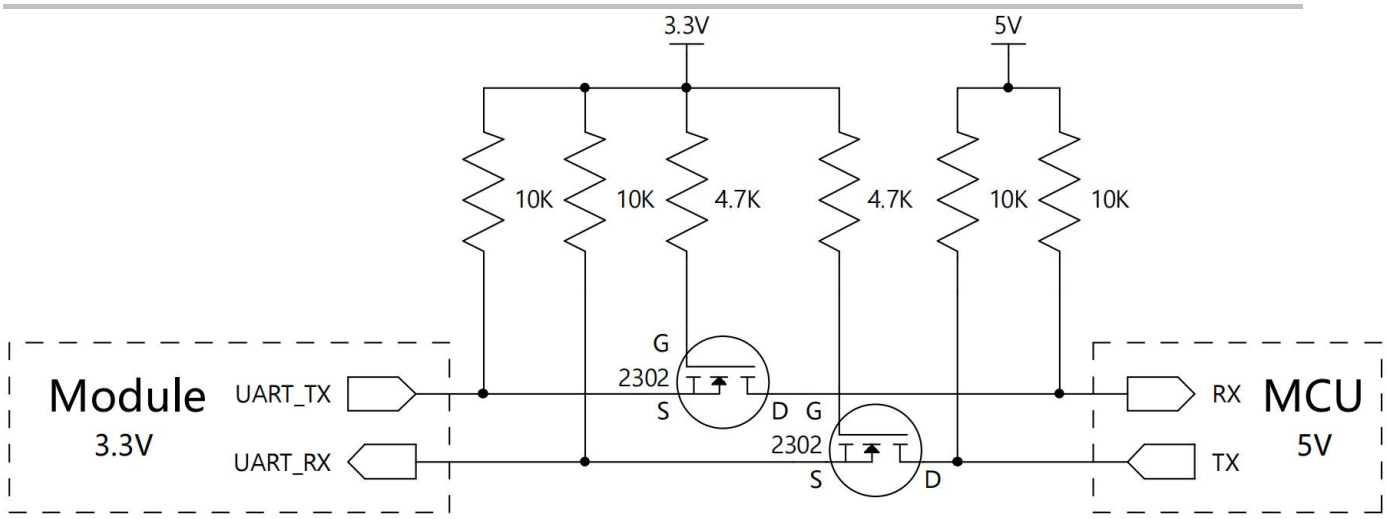


Figure 20 : Serial port level conversion reference circuit

3. Electrical characteristics , RF characteristics and reliability

3.1. Maximum Ratings

Stresses exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6 : Absolute Maximum Ratings Table

parameter	Minimum	Maximum	unit
VBAT	-0.2	3.7	V
I/O supply voltage (VDDIO)	-0.2	3.7	V
Storage temperature range	-40	+125	°C

Table 7 : Recommended operating conditions

parameter	Minimum	Typical Value	Maximum	unit
VBAT	3	3.3	3.7	V
I/O supply voltage (VDDIO)	3	3.3	3.7	V
Operating temperature range (TA)	-40	+25	+85	℃

3.2. Electrostatic protection

In module applications, static electricity generated by human static electricity, charged friction between microelectronics, etc., is discharged to the module through various channels, which may cause certain damage to the module. Therefore, ESD protection should be taken seriously. ESD protection measures should be taken during the R&D, production assembly and testing processes, especially in product design. For example, anti-static protection should be added at the interfaces of circuit design and points that are susceptible to damage or impact from electrostatic discharge, and anti-static gloves should be worn during production.

Table 8 : ESD withstand voltage of module pins

Test interface	Contact discharge	Air discharge	unit
VBAT and GND	+4	+8	kV
Main antenna interface	+2.5	+4	kV

4. Mechanical dimensions and layout recommendations

This section describes the mechanical dimensions of the module. All dimensions are in millimeters. For all dimensions without tolerance, the tolerance is ±0.3 mm.

4.1. Modular mechanical ruler

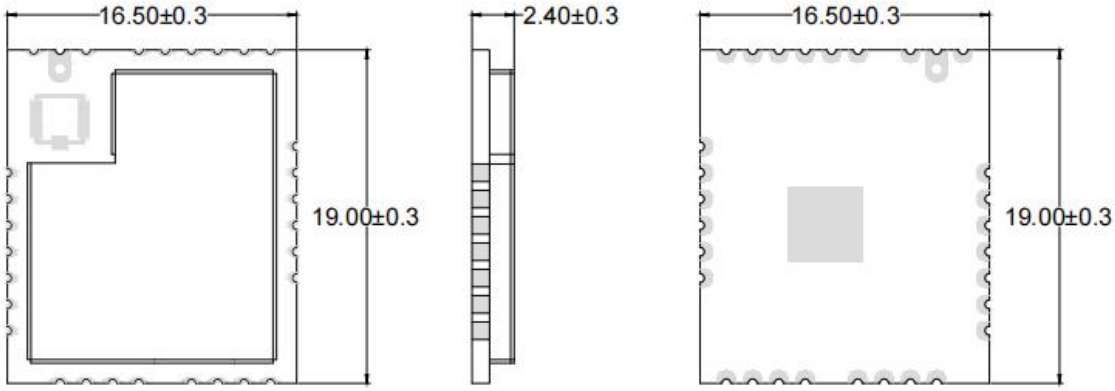


Figure 21 : Module top, side and bottom views

4.2. Recommended package

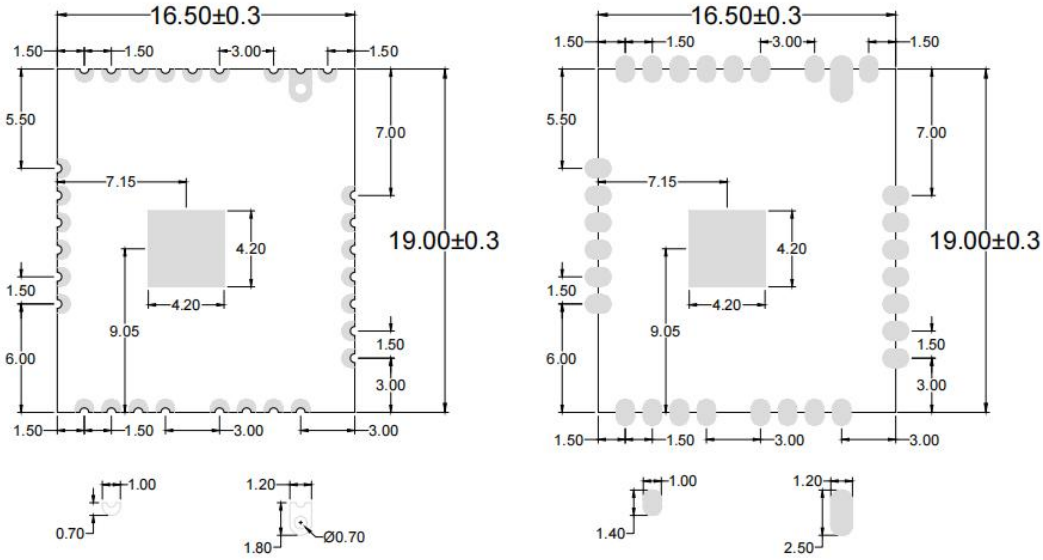


Figure 22 : Recommended package dimensions, top and bottom views

4.3. Module top view/bottom view

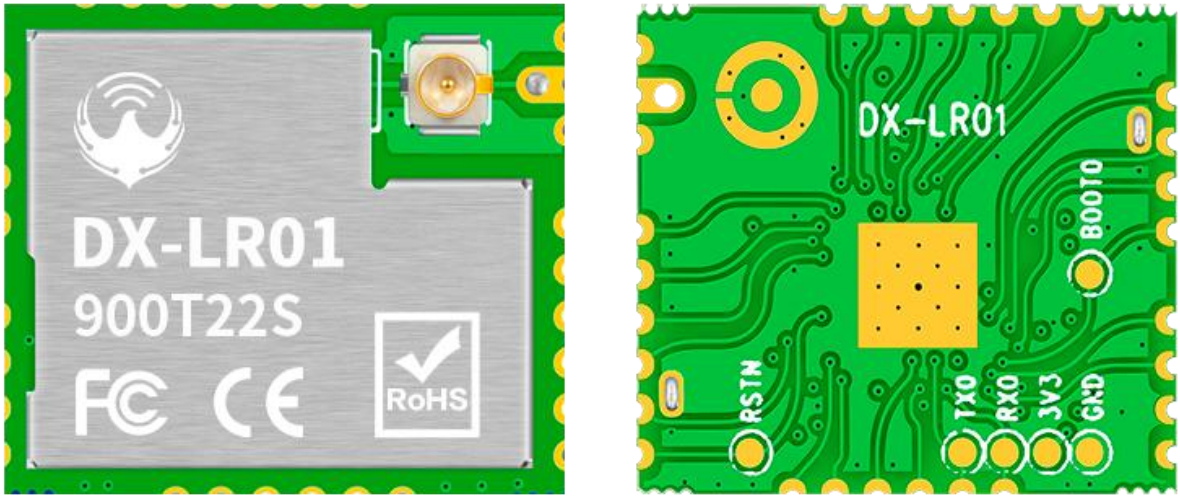


Figure 23 : Module top and bottom views

Remark

The above picture is for reference only. For the actual product appearance and label information, please refer to the actual module.

4.4. Hardware Design Layout Recommendations

The DX-LR01-900M module works in the SUB-G wireless frequency band and uses an external antenna. The VSWR and efficiency of the antenna depend on the patch position. Various factors that affect the wireless transceiver signal should be avoided as much as possible. Note the following points:

1. Avoid using metal for the product shell surrounding the LR01-900M. When using a partial metal shell, keep the module antenna away from the metal part as much as possible. The metal connecting wires or metal screws inside the product should be kept away from the module antenna as much as possible.

2. The module antenna should be placed close to the edge of the PCB or directly exposed from the PCB. Try not to place it in the middle of the board.

3. It is recommended to use insulating materials to isolate the module mounting position on the substrate, such as placing a whole piece of silk screen (TopOverLay) at this position.

5. Storage, production and packaging

5.1. Storage conditions

The module is shipped in a vacuum sealed bag. The module has a moisture sensitivity level of 3 (MSL 3) and its storage must comply with the following conditions:

1. Recommended storage conditions: temperature 23±5°C and relative humidity 35~60%.

2. Under recommended storage conditions, modules can be stored in vacuum sealed bags for 12 months.

3. Under workshop conditions of 23±5°C and relative humidity below 60%, the workshop life of the module after unpacking is 168 hours. Under this condition, the module can be directly subjected to reflow production or other high-temperature operations. Otherwise, the module needs to be stored in an environment with a relative humidity of less than 10% (for example, a moisture-proof cabinet) to keep the module dry.

4. If the module is in the following conditions, it is necessary to pre-bake the module to prevent the module from absorbing moisture and then causing PCB blistering, cracks and delamination after high-temperature soldering:

- The storage temperature and humidity do not meet the recommended storage conditions
- After the module is unpacked, it fails to complete production or storage according to the above clause 3
- Vacuum packaging leaks, bulk materials
- Before module repair

5.2. Module baking process

- It needs to be baked at 120±5°C for 8 hours
- 24 hours after baking , otherwise it still needs to be stored in a drying oven.

Remark

1. In order to prevent and reduce the occurrence of poor welding such as blistering and delamination of the module due to moisture, strict control should be exercised. It is not recommended to expose the module to the air for a long time after opening the vacuum packaging.
2. Before baking, the module needs to be taken out of the package and placed on a high temperature resistant device to prevent high temperature from damaging the plastic tray or reel; the module for secondary baking must be soldered within 24 hours after baking, otherwise it needs to be stored in a drying oven. Please pay attention to ESD protection when unpacking and placing the module, for example, wear anti-static gloves .

5.3. Reflow

Use a printing scraper to print solder paste on the stencil so that the solder paste leaks through the stencil opening onto the PCB. The strength of the printing scraper needs to be adjusted appropriately. To ensure the quality of the module printing paste, the recommended steel mesh thickness corresponding to the module pad part is 0.1~0.15mm.

The recommended reflow temperature is 235~250 ℃, and the maximum temperature should not exceed 250 ℃. To avoid damage to the module due to repeated heating, it is strongly recommended that customers mount the module after completing the reflow soldering of the first side of the PCB board. The recommended furnace temperature curve (lead-free SMT reflow soldering) and related parameters are shown in the following chart:

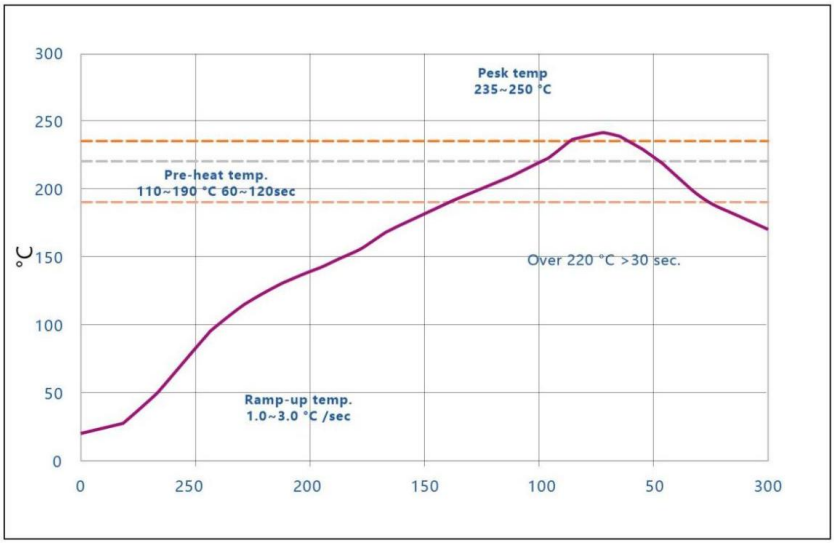


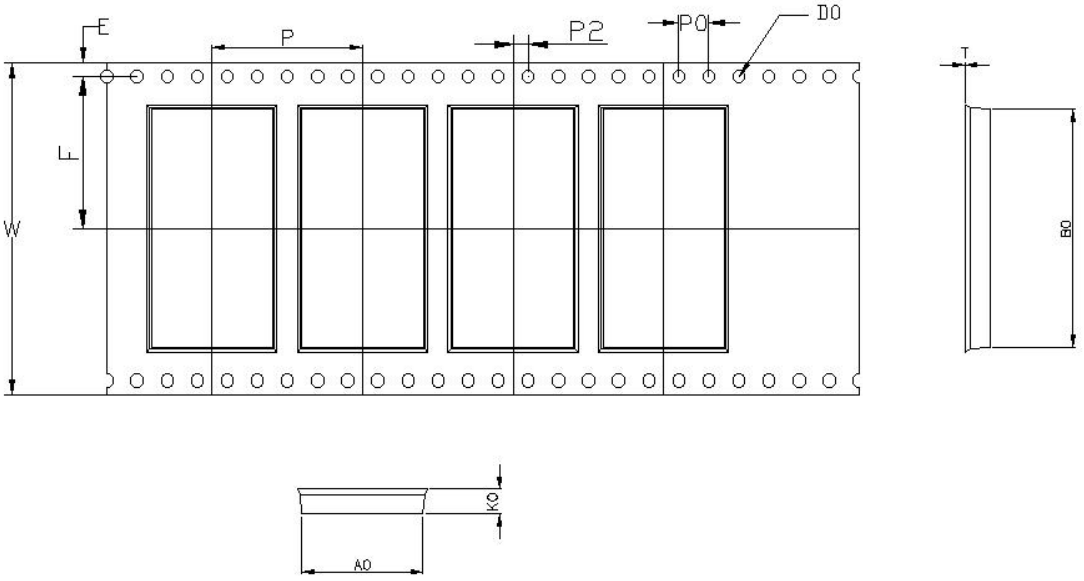
Figure 24 : Recommended reflow temperature profile

Table 9 : Recommended reflow temperature

Statistical name	Lower limit	Upper limit	unit
Slope 1 (target = 2.0) between 30.0 and 70.0	1	3	Degree/second
Slope 2 (target = 2.0) between 70.0 and 150.0	1	3	Degree/second
Slope 3 (target = -2.8) between 220.0 and 150.0	-5	-0.5	Degree/second
Constant temperature time 110-190℃	60	120	Second
@220℃ reflow time	30	65	Second
Peak temperature	235	250	Celsius
Total time @ 235℃	10	30	Second

5.4. Packing Specifications

The DX-LR01-900M modules are packaged in tape and reel and sealed in vacuum sealed bags with desiccant and humidity card. Each carrier is 20 meters long and contains 1000 modules. The reel diameter is 330 mm. The specific specifications are as follows:



W	44.00±0.30	P	20.00±0.10	A0	15.70±0.10	B0	31.20±0.10
S0	———	P0	4.00±0.10	A1		B1	
E	1.75±0.10	P2	2.00±0.10	A2		B2	
F	20.2±0.10	D0	ø1.50$^{+0.10}_{0}$	K0	3.40±0.10		
T	0.40±0.05	D1		K1			

Figure 25 : Carrier tape dimensions (unit: mm)

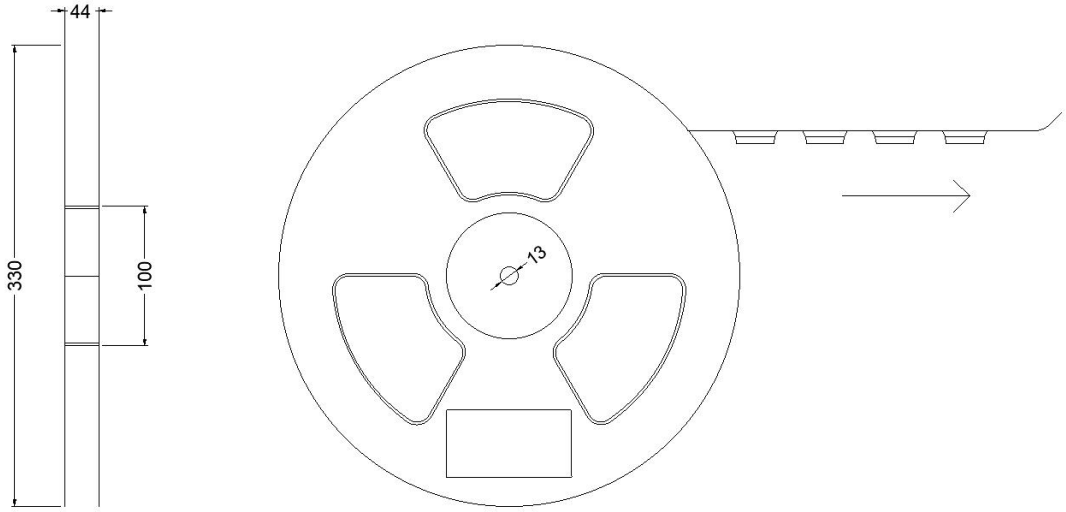


Figure 26 : Reel dimensions (unit: mm)

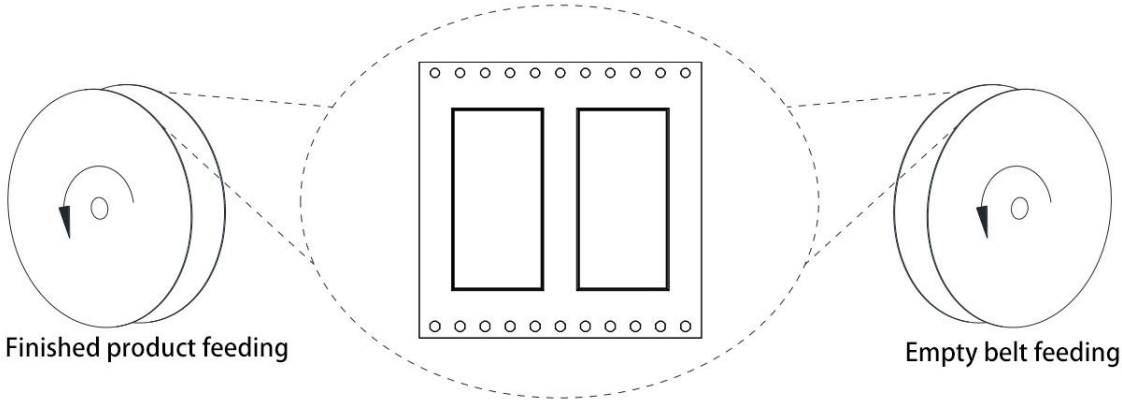


Figure 27 : Tape Direction

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This modular has been tested and found to comply with part 15 requirements for Modular Approval.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC Part 15 Subpart C and Subpart F has been investigated. It is applicable to the modular transmitter

2.3 Specific Operational Use Conditions - Antenna Placement Within the Host Platform

The module is tested for standalone mobile RF exposure use condition.
● The antenna must be installed such that 20cm is maintained between the antenna and users,
● The transmitter module may not be co-located with any other transmitter or antenna.
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.4 Limited Module Procedures

Not applicable

2.5 Trace Antenna Designs

Not applicable

2.6 RF Exposure Considerations

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antenna Type and Gain

The following antennas have been certified for use with this module.
Only antennas of the same type with equal or lower gain may also be used with this module.
Other types of antennas and/or higher gain antennas may require the additional authorization for operation.
Antenna Specification list below:

Antenna Type	Antenna Model No.	Maximum Antenna Gain (dBi)	Frequency Range
Spring Antenna	DX-LR01-900	0	903 – 914.2MHz

2.8 End Product Labelling Compliance Information

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily removed. If not, a second label must be placed on the outside of the final device that contains the following text: “ Contains FCC ID: 2BLPG-DX-LR01-900 ”. The FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on Test Modes and Additional Testing Requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) class II permissive change re-evaluation or new FCC authorization.
Host manufacturer installed this modular with single modular approval should perform the test of radiated emission and spurious emission according to FCC part 15C, 15.209, 15.207 requirement, only if the test result comply with FCC part 15C, 15. 209, 15.207 requirement, then the host can be sold legally.

2.10 Additional testing, Part 15 Subpart B Disclaimer

This transmitter modular us tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B rules requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rules requirements if applicable.
As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this modular installed.

2.11 Manual Information to The End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user ’ s manual of the end product which integrates this module.
The host integrator must follow the integration instructions provided in this document and ensure that the composite system end product complies with the requirements by a technical assessment or evaluation to the rules and to KDB Publication 996369.
The host integrator installing this module into their product must ensure that the final composite product complies with the requirements by a technical assessment or evaluation to the rules, including the transmitter operation and should refer to guidance in KDB Publication 996369.

OEM/Host Manufacturer Responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and RF Exposure essential requirements of the FCC rules.

2.12 How to Make Changes - Important Note

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.