RL78/G1D

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Design of a Reference Antenna

Introduction

This application note describes an example of the design of a pattern antenna and its characteristics when connected with the RL78/G1D.

Target Device

RL78/G1D (R5F11A)

Contents

Figures and Tables

1. Overview

This application note describes an example of the design of a pattern antenna.

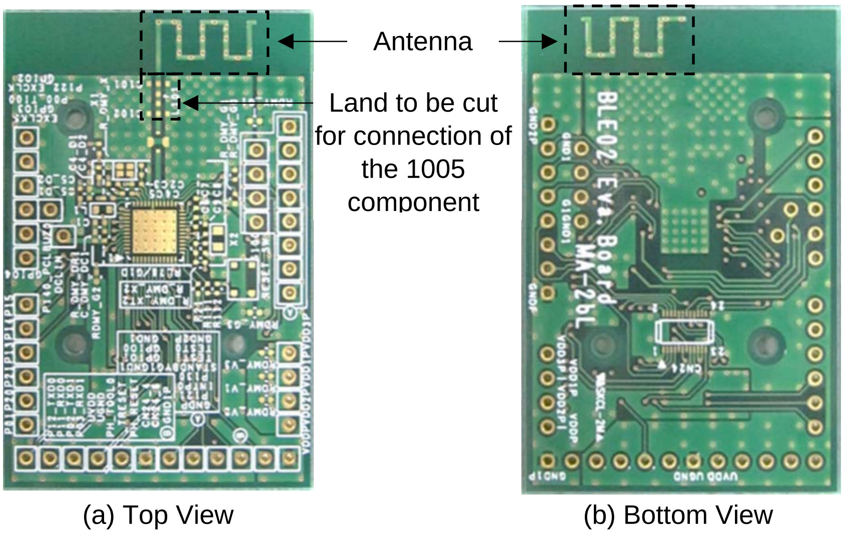
1.1 Related Documents

- RL78/G1D Guidelines for RF Board Design (R01AN2465E)
- RL78/G1D User's Manual: Hardware (R01UH0515E)

2. Configuration of a Reference Antenna

The antenna is a pattern antenna formed on the RL78/G1D evaluation board. Figure 1 consists of photographs of the evaluation board on which the antenna is formed. The antenna is formed as a meandering land pattern on the board, and is connected to a feeder with an impedance of 50 Ω. The land pattern connects the feeder of the antenna with the adjacent GND on the evaluation board. Mounting a 1005 (1-mm long) component in series between the feeder and the GND on the land allows adjustment of the resonance frequency and impedance of the antenna and gives the antenna a wide adjustable range.

Caution To mount the adjusting component, cut the part of the feeder between the land for the ground and for the antenna beforehand.



* The photograph is of the board with no components mounted.

Figure 1 Appearance of the Evaluation Board on which the Reference Antenna is Formed

2.1 Antenna Layout

Figure 2 shows layouts of the patterns formed for the antenna in each layer of the evaluation board.
Size of the evaluation board: 33 mm × 51 mm
The evaluation board has four layers: L1, L2, L3, and L4. The 33 mm × 7 mm area in which the pattern antenna is formed in each layer includes no other pattern. The body of the antenna is formed in layers L1 and L4. The pattern in L1 is connected to the pin for antenna connection (50 Ω). Multiple via holes connect the pattern in L4 to that in L1.

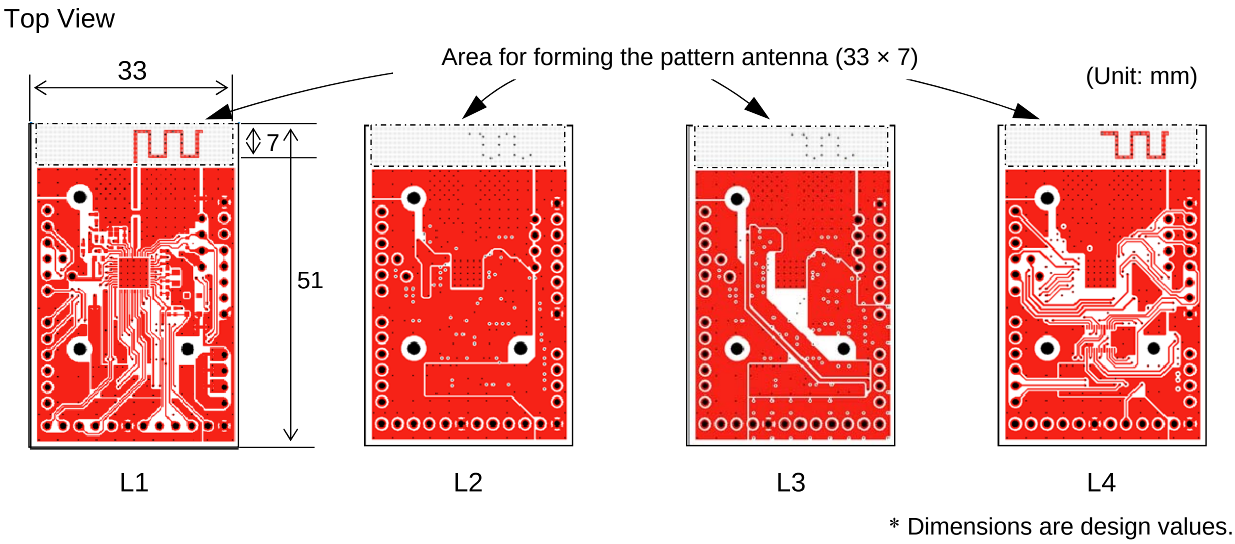
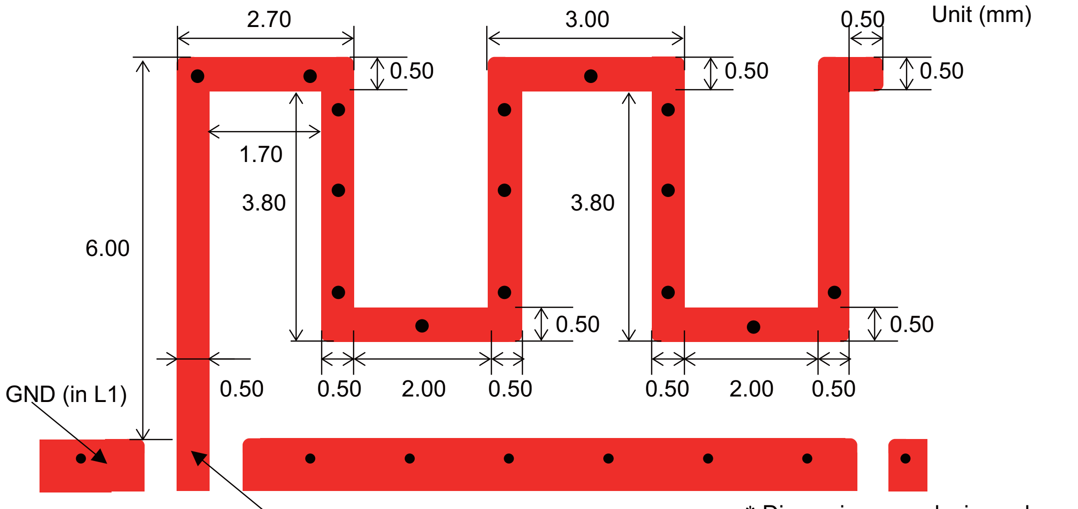


Figure 2 Pattern Layouts in Each Layer of the Evaluation Board

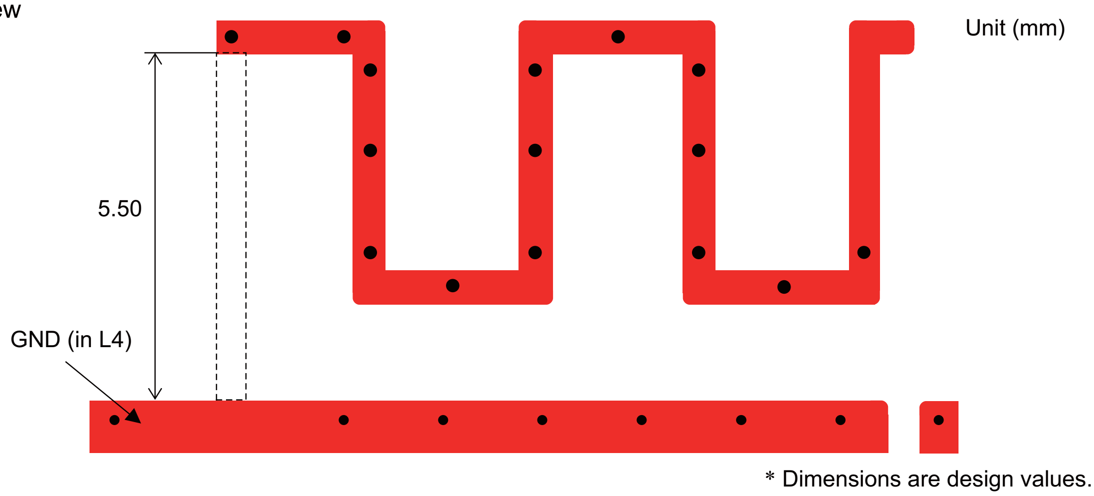
Figure 3 shows dimensions of the antenna.

Top View



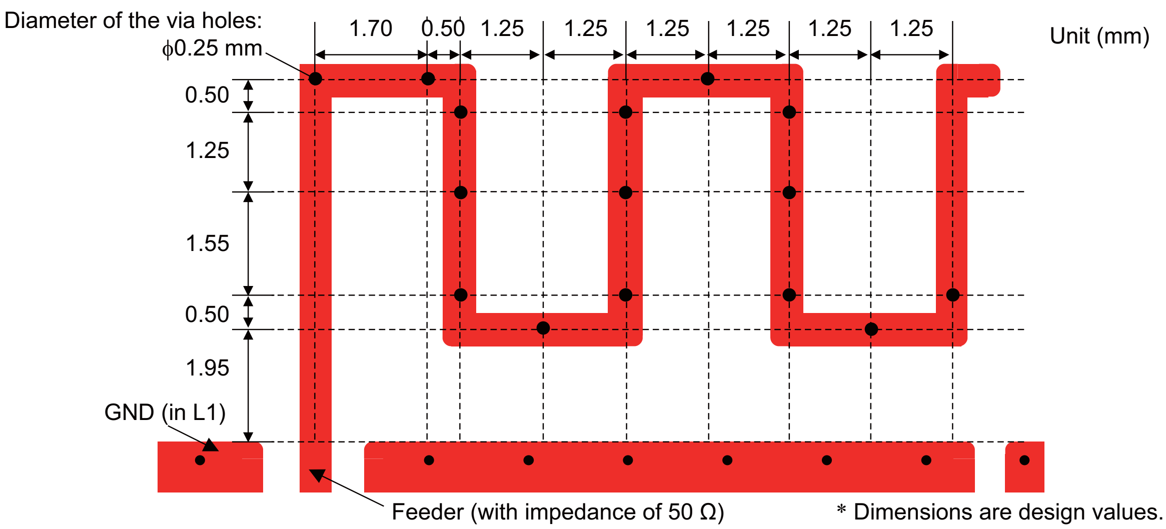
(a) Dimensions of the Pattern Antenna (in L1)

Top View



(b) Dimensions of the Pattern Antenna (in L4)

Top View



(c) Locations of Via Holes

Figure 3 Dimensions of the Reference Antenna

The resonance frequency and impedance of the antenna differ with elements of its surrounding environment, including the size and shape of the board to which the antenna is connected, the wiring patterns on the board, and the housing of the board. Changes to any of these factors require adjustment of the antenna. To start with, adjusting the length of the antenna is more effective than using an adjusting component such as a capacitor or inductor.

To attain the target frequency for the product you are developing, we recommend the following procedure.

<1> Lower the resonance frequency of the antenna by lengthening it relative to the dimensions shown in figure 3.

Caution In lengthening the antenna, repeat the meandering section of the pattern in L1 and L4 so that the wiring in each has the same length.

<2> Shorten the antenna while confirming that the resonance frequency is still approaching the target value.

Caution Shorten the patterns for the antenna in L1 and L4 from the end of the meandering pattern so that the wiring in each layer has the same length.

2.2 Layer Configuration of the Printed Circuit Board

The layer configuration of the printed circuit board including the antenna and chip-evaluation sections is given below.

- Board configuration
  Four wiring layers

Configuration	Thickness (mm)
Resist	0.030
Cu (L1)	0.043
PP	0.280
Cu (L2)	0.035
Core material	0.830
Cu (L3)	0.035
PP	0.280
Cu (L4)	0.043
Resist	0.030

* Dimensions are design values.

Figure 4 Layer Configuration of the Board

- Board material
  MCL-E-67 (FR4) manufactured by Hitachi Chemical Co., Ltd.
- Thickness
  Board: 1.6 mm
  Wiring:
  - L1, L4 : Cu 43 µm
  - L2, L3 : Cu 35 µm

Figure 4 shows the layer configuration and thicknesses of each layer.

3. Antenna Characteristics

This section describes the voltage standing wave ratio (VSWR) and emission characteristics of the antenna.

In the measurements, a 1.8-pF capacitor (1005-sized package) is mounted as the adjusting component (A in the figure below) on the evaluation board, and is semi-rigidly attached to the feeder.

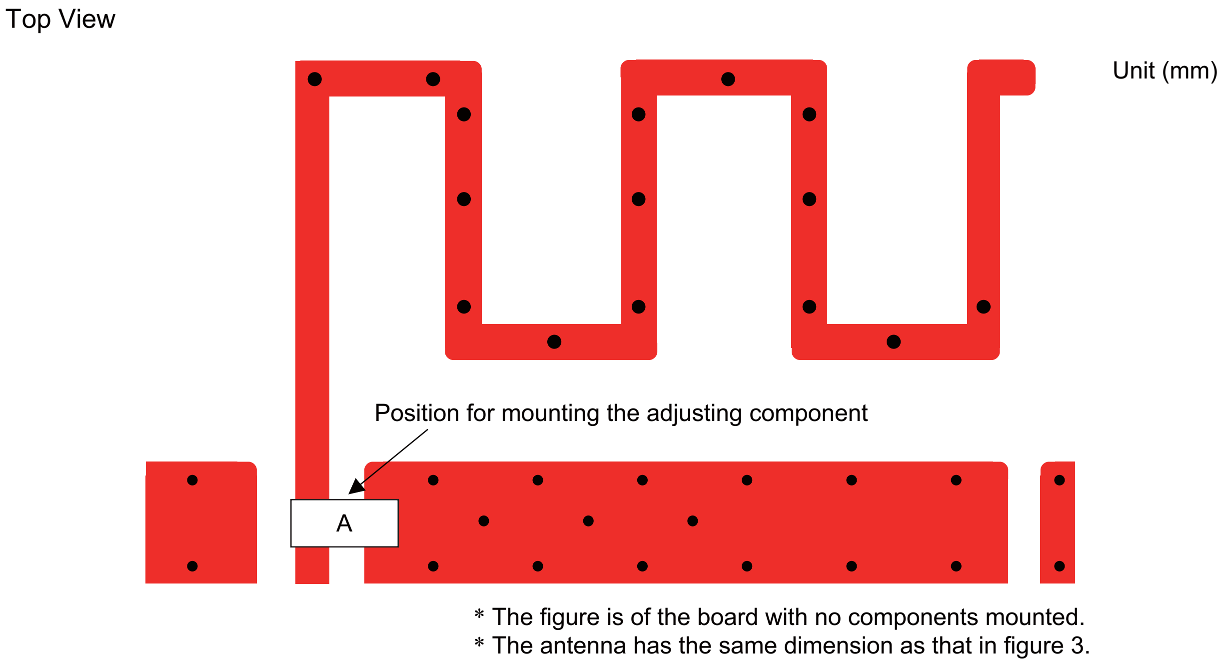


Figure 5 Position for Mounting the Adjusting Component

3.1 VSWR

The results for measurement of the VSWR are given in figure 6. The measurements were made by using a network analyzer in a shield room.

The antenna satisfies VSWR ≤ 2 over a bandwidth of 115 MHz, including the band from 2400 MHz to 2484 MHz stipulated in the Bluetooth v. 4.1 specification (the section on low-energy single mode).

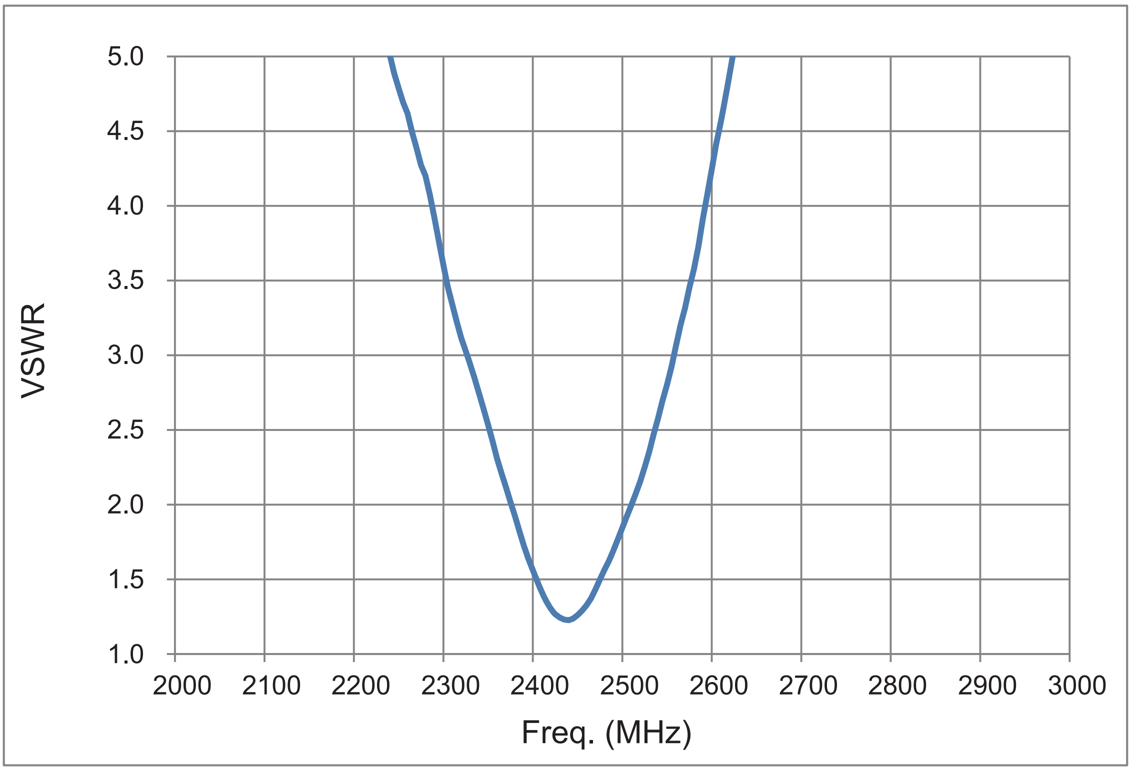
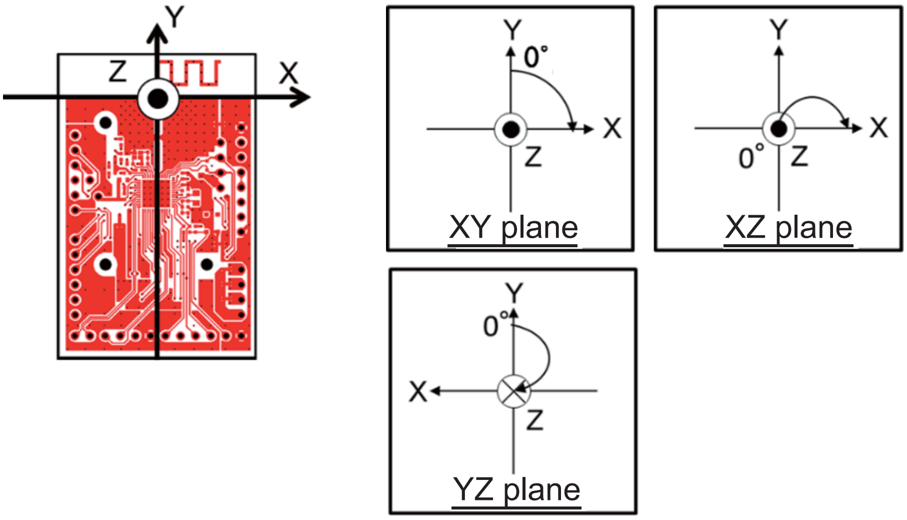


Figure 6 VSWR of the Reference Antenna

3.2 Emission Characteristics

Figure 7 shows the coordinate axes, the positions where rotation starts (0°), and the directions of rotation. The coordinate axes are defined on the basis of the top view of the evaluation board as shown in figure 7(a). The positions where rotation starts (0°) and its directions in obtaining the emission patterns in each plane are defined as shown in figure 7(b).

Top View



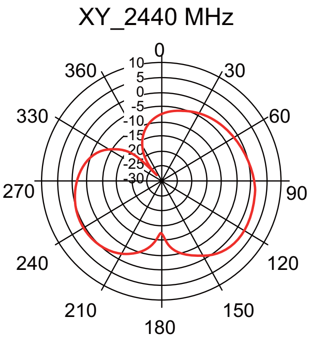
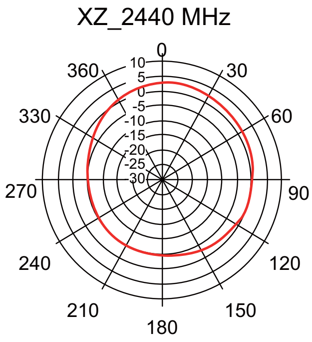
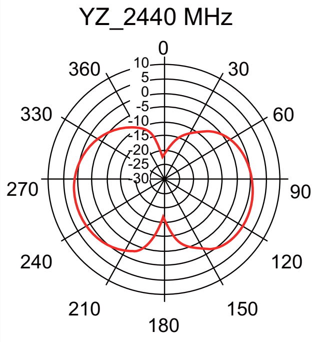
(a) Coordinate Axes

(b) Positions where Rotation Starts (0°) and its Directions

Figure 7 Coordinate Axes and Directions of Rotation for Obtaining the Emission Patterns

Table 1 shows the emission patterns and average gains measured with the antennas separated by 3 m from each other in a six-surface radio-wave-dark room. The measurements were made in three planes: XY, XZ, and YZ.

Table 1 Emission Patterns of the Reference Antenna and Average Gains

Item	XY Plane (Horizontally Polarized Wave)	XZ Plane (Vertically Polarized Wave)	YZ Plane (Horizontally Polarized Wave)
Emission patterns of the reference antenna			
Average gain	-2.30 dBi	-1.79 dBi	-2.30 dBi

Caution The values of the adjusting component and for the antenna characteristics in this application note are for reference. They are not guaranteed values.
Since the characteristics will differ with the conditions of mounting and the surrounding environment, make the required adjustments for the needs of your actual application.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision Record	RL78/G1D Application Note

Rev.	Date	Description	
		Page	Summary
0.90	Mar 19, 2015	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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