WMC529R Series QuecOpen Hardware Design

Automotive Module Series

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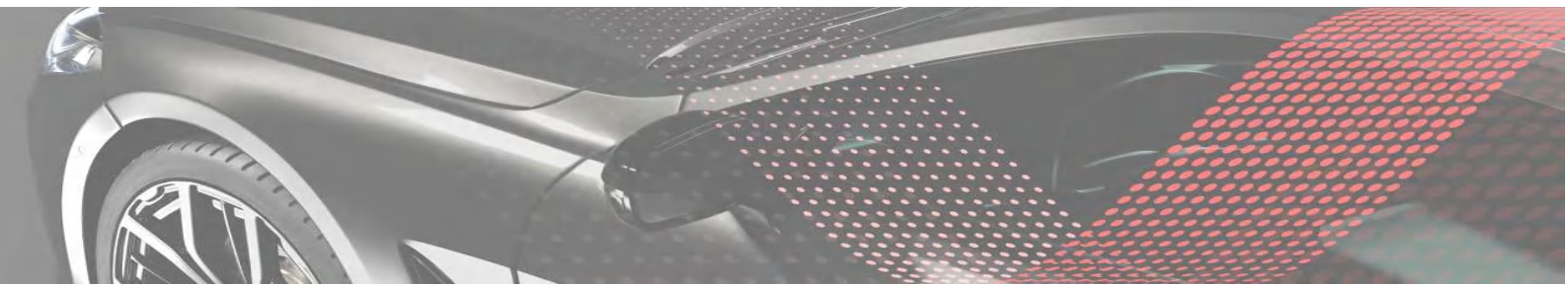

About the Document

Document History

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-	2024-02-02	Colton YANG/Arlen LIU	Creation of the document
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1 Background

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1.5. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Wireless Mobility assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

The document defines WMC529R series in QuecOpen® solution and describes its air interface and hardware interfaces which are connected with your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up automotive mobile applications with the module.

Table 1: Applicable Modules

Module Series	Model
WMC529R	WMC529R-EUAQB
	WMC529R-NAAQ
	WMC529R-ROWAQ
	WMC529R-INAQ
	WMC529R-ROWAQ&INAQ

2.1. Special Marks

Table 2: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

3 Product Overview

3.1. Frequency Bands and Functions

WMC529R series are automotive-grade LTE/WCDMA/GSM wireless communication modules with diversity reception, and provide data connectivity on LTE-FDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides single-band GNSS and voice functionalities to meet specific application demands.

Engineered to meet the demanding requirements in automotive applications and other harsh operating conditions, the module offers a premium solution for high performance automotive and intelligent transportation system (ITS) applications.

With a compact profile of 38.0 mm × 42.0 mm × 2.65 mm, the module can be embedded into applications through the 400 LGA pins.

Table 3: Brief Information

Basic Information	
Pin Number and Package	400 LGA Pins
Dimensions	(38.0 ±0.2) mm × (42.0 ±0.2) mm × (2.65 ±0.2) mm
Weight	Approx.9.9 g
Wireless technologies	● LTE-FDD, WCDMA, GSM ● GNSS (optional)

Table 4: Frequency Bands, Supported Category and GNSS Function of the Module

Network Type/ Feature	WMC529R-EUAQB	WMC529R-NAAQ	WMC529R-ROWAQ	WMC529R-INAQ	WMC529R-ROWAQ&INAQ
Ordering Code	WMC529REUAQB-M28-BYJ	WMC529RNAAQ-M28-BYJ	WMC529RROWAQ-M28-BYJ2	WMC529RINAQ-M28-BYJ	WMC529RROWAQ-M28-BYJ
LTE-FDD (with Diversity antenna)	**2 × 2 MIMO** B1/B3/B7/B8/B20/B28A	**2 × 2 MIMO** B2/B4/B5/B7/B12/ B13/B14/B17/B66	**2 × 2 MIMO** B1/B3/B5/B7/B8/ B18/B19/B28A/B28B	**2 × 2 MIMO** B1/B3/B5/B8	**2 × 2 MIMO** B1/B3/B5/B7/B8/ B18/B19/B28A/B28B
LTE-TDD (with Diversity antenna)	-	-	B41	B40/B41	B40 (optional)/B41
WCDMA (with Diversity antenna)	B1/B8	-	B1/B8	-	B1/B8
GSM	EGSM900/DCS1800	-	-	EGSM900/DCS1800	EGSM900/DCS1800
C-V2X	-	-	-	-	-
Default Category	Cat 6	Cat 6	Cat 6	Cat 6	Cat 6
GNSS (Optional)	• Single-band GNSS: L1 • Constellation: GPS, GLONASS, BDS, Galileo and QZSS • GNSS augmentation system: SBAS				

3.2. Key Features

The following table describes detailed features of the module.

Table 5: Key Features

Feature	Details
Power Supply	**VBAT_BB:** ● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V **VBAT_RF:** ● Supply voltage: 3.7–4.3 V (WMC529R-EUAQB/WMC529R-INAQ/ WMC529R-ROWAQ&INAQ) ● Supply voltage: 3.3–4.3 V (WMC529R-NAAQ/WMC529R-ROWAQ) ● Typical supply voltage: 3.8 V
Transmitting Power	● LTE-FDD bands: Class 3 (23 dBm ±2 dB) ● LTE-TDD bands: Class 3 (23 dBm ±2 dB) ● WCDMA bands: Class 3 (23 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB)
LTE Features	Default configuration: ● Up to Cat 6 LTE FDD and TDD ● 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports QPSK,16QAM and 64QAM Modulation (DL) ● Supports QPSK,16QAM and 64QAM Modulation (UL) ● Multi-user 2 × 2 MIMO in DL direction ● FDD: Max. 300 Mbps (DL)/75 Mbps (UL) ● TDD: Max. 130 Mbps (DL)/30 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA ● Supports QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. 107 kbps (DL)/85.6 kbps (UL)

	EDGE: ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 296 kbps (DL)/236.8 kbps (UL)
Internet Protocol Features	Supports TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS/MMS/FTPS/ SSL/SMTP/TLS protocols
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	● Support dual (U)SIM cards ● (U)SIM1 and (U)SIM2: 1.8V/3.0V
Audio Features	● One digital audio interface: I2S interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
I2S Interface	● Used for codec configuration by default ● Supports master and slave modes
I2C Interface	● Compliant with *I2C Specification Version 3.0* ● Multi-master is not supported ● Used for codec configuration by default
PCM Interface	● Used for Bluetooth audio transmission by default ● Supports 16-bit linear data format ● Supports long frame and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization
USB Interface	● Compliant with USB 3.0 and 2.0 specifications (slave mode by default; supports USB host mode), with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Both USB 3.0 and USB 2.0 can be used for AT command communication, data transmission, software debugging, GNSS NMEA sentence output, and voice over USB*. ● USB 3.0 is used for data communication with AP by default. ● Only USB 2.0 can be used for firmware upgrading. ● When USB 3.0 and USB 2.0 are connected to the same host, USB 3.0 takes effect by default. ● Supports USB serial drivers for: Windows 8/8.1/10/11; Linux 2.6–6.5

UART	**UART1:** ● Supports baud rate up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Bluetooth UART:** ● Supports baud rate up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● Supports 115200 bps baud rate
SDIO Interface	Supports eMMC 4.5.1
SPI Interfaces	● 2 SPI interfaces, and SPI2 is optional ● Support master mode only ● Support max. clock frequency rate up to 50 MHz
RGMII Interface	Supports 10/100/1000 Mbps
WLAN and Bluetooth Application Interfaces	● Supports a PCIe Gen 2 interface for WLAN function ● Supports UART and PCM interfaces for Bluetooth function
Diversity antenna	Supports LTE/WCDMA Diversity antenna
GNSS Features (Optional)	● Supports single-band (L1) ● Constellation: GPS, GLONASS, BDS, Galileo, QZSS ● Augmentation system: SBAS ● Protocol: NMEA 0183 ● The data update rate is 10Hz by default and can support a max. value of 10Hz
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Diversity antenna interface (ANT_DIV) ● GNSS antenna interface (ANT_GNSS)
Temperature Range	● Operating temperature range [1]: -35 °C to + 75 °C ● Extended temperature range [2]: -40 °C to + 85 °C ● eCall temperature range [3]:-40 °C to + 95 °C ● Storage temperature range: -40 °C to + 95 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within this range, the module's indicators comply with 3GPP specification requirements.
[2] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and eCall, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.
[3] Within this range, the eCall function must remain operational. The module triggers thermal management mechanisms at high temperatures, such as power reduction or throughput decrease, to ensure normal eCall operation even at temperatures up to 95 °C.

3.3. EVB Kit

Wireless Mobility supplies an evaluation board (V2X&5G EVB) with accessories to develop and test the module. For more details, please contact Wireless Mobility Technical Support.

4 Application Interfaces

4.1. General Description

WMC529R series is equipped with 400 LGA pins that can be connected to cellular application platforms. The subsequent chapters will provide detailed descriptions of the following interfaces:

- Power supply
- (U)SIM interfaces
- USB interface
- UART
- I2S and I2C interfaces
- PCM interface
- SDIO interface
- SPI interfaces
- RGMII interface
- WLAN and Bluetooth application interfaces
- ADC interfaces
- USB_BOOT interface
- RTC
- GPIO interfaces
- Audio interface (optional)

4.2. Pin Assignment

The following figure shows the pin assignment of the module.

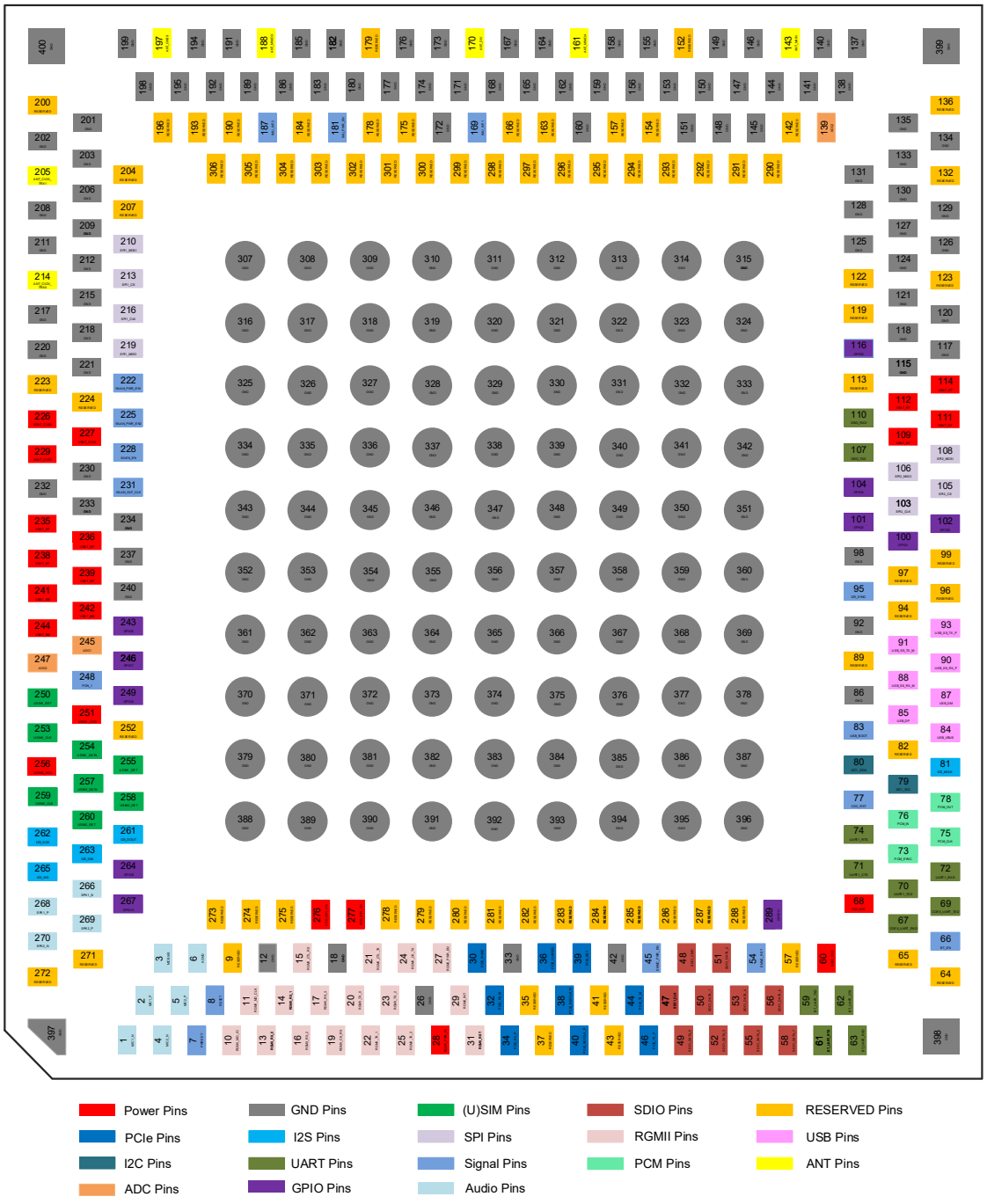


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.
3. GPIO9, GPIO10, GPIO11 are not supported by default.
4. ADC2 is not supported by WMC529R series.
5. ANT_MIMO3 and ANT_MIMO4 are not supported by WMC529R series.
6. GNSS is optional.
7. WMC529R series does not support C-V2X by default.

4.3. Pin Description

The following tables show the pin definition of the module.

Table 6: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 7: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	241, 242, 244	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF [4]	109, 111, 112, 114 235, 236 238, 239	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3/3.7 V Vnom = 3.8 V	It must be provided with sufficient current up to 2.0 A in a burst transmission.
VBAT_CV2X [5]	226, 227, 229	PI	Power supply for the module's C-V2X part	Vmax = 5.25 V Vmin = 4.75 V Vnom = 5.0 V	It must be provided with sufficient current up to 1.5 A.
VDD_EXT	68	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	This pin can be used to connect with VDD_IO of AF50T or AF51Y, and it also can be used as power supply for external pull-up circuits.
VDD_WIFI_VM	276	PO	Medium-voltage power supply for Wi-Fi	Vnom = 1.21 V Vmax=1.35V $I_O$max = 400 mA	After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module.
VDD_WIFI_VH	277	PO	High-voltage power supply for Wi-Fi	Vnom = 1.81 V Vmax=1.95V $I_O$max = 400 mA	
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131, 133–135, 137, 138, 140, 141, 144–151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–400				
Turn On/Off					

[4] The minimum input voltage of WMC529R-EUAQB and WMC529R-ROWAQ is 3.7 V, while the minimum input voltage of WMC529R-NAAQ is 3.3 V.
[5] WMC529R series does not support C-V2X by default.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	7	DI	Turn on/off the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	Internally pulled up to 1.8 V. Active low.
PON_1	248	DI	Power on the module upon rising edge		Valid voltage range: 0.78–1.89 V.
RESET	8	DI	Reset the module	V_{IH}max = 1.89 V V_{IH}min = 1.17 V V_{IL}max = 0.63 V	Internally pulled up to 1.8 V. Active low.
(U)SIM Interfaces [6]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	251	PO	(U)SIM1 card power supply	**For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM1_DATA	254	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.36 V V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM1_CLK	253	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.

[6] (U)SIM2 interface is optional.

USIM1_RST	250	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM1_DET	255	DI	(U)SIM1 card insertion detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
USIM2_VDD	256	PO	(U)SIM2 card power supply	**For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V $I_O$max = 50 mA	Either 1.8 V or 3.0 V is supported by the module automatically. If unused, keep it open.
USIM2_DATA	257	DIO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.36 V V_{IH}min = 1.26 V V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{IL}max = 0.57 V V_{IH}min = 2.0 V V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM2_CLK	259	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.
USIM2_RST	260	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 1.44 V **For 3.0 V (U)SIM:** V_{OL}max = 0.4 V V_{OH}min = 2.28 V	If unused, keep it open.

USIM2_DET	258	DI	(U)SIM2 card insertion detect	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep it open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	84	DI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Maximum current: 0.1 mA. Typical 5.0 V.
USB_DP	85	AIO	USB 2.0 differential data (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	87	AIO	USB 2.0 differential data (-)		
USB_SS_TX_P	93	AO	USB 3.0 SuperSpeed transmit (+)		Compliant with USB 3.0 standard specification. Require differential impedance of 90 Ω.
USB_SS_TX_M	91	AO	USB 3.0 SuperSpeed transmit (-)		
USB_SS_RX_P	90	AI	USB 3.0 SuperSpeed receive (+)		
USB_SS_RX_M	88	AI	USB 3.0 SuperSpeed receive (-)		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	100	DI	WAKEUP_IN	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	This pin is used as WAKEUP_IN by default to control the module entering/ exiting the low power mode. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO		General-purpose input/output

GPIO2	101	DIO	GPIO		General-purpose input/output
GPIO3	102	DIO	SLEEP_SYS_IND		Used as SLEEP_SYS_IND by default to indicate the low power mode of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO		General-purpose input/output
GPIO4	104	DIO	GPIO		General-purpose input/output
GPIO5	116	DIO	GPIO		
GPIO6	243	DIO	GPIO		
GPIO7	246	DIO	GPIO		
GPIO8	249	DO	GPIO	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	General-purpose output
GPIO9 [7]	264	DIO	GPIO	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V	General-purpose input/output
GPIO10 [7]	267	DIO	GPIO		
GPIO11 [7]	289	DIO	GPIO		

UART1 Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
UART1_CTS	71	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep these pins open. Connect to the MCU's CTS.
UART1_RTS	74	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep

[7] Make sure no GPIO9, GPIO10, GPIO11 are not supported by WMC529R series.

					these pins open. Connect to the MCU's RTS.
UART1_TXD	70	DO	UART1 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep these pins open.
UART1_RXD	72	DI	UART1 receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
Bluetooth UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_UART_TXD	59	DO	Bluetooth UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep these pins open.
BT_UART_RXD	63	DI	Bluetooth UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
BT_UART_RTS	61	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep these pins open. Connect to AF50T/ AF51Y's RTS.
BT_UART_CTS	62	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep these pins open. Connect to AF50T/ AF51Y's CTS.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	110	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Test points must be reserved for debug UART.
DBG_TXD	107	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

I2C Interface (for Codec Configuration by Default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	79	OD	I2C serial clock		External pull-up resistor is required. 1.8 V only. Can be configured to GPIOs. If unused, keep them open.
I2C1_SDA	80	OD	I2C serial data		
I2S Interface (for Codec Configuration by Default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CDC_RST	77	DO	External codec reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep them open.
I2S_MCLK	81	DO	Clock output for codec	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2S_WS	265	DIO	I2S word select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
I2S_SCK	262	DIO	I2S clock		
I2S_DIN	263	DI	I2S data in	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
I2S_DOUT	261	DO	I2S data out	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	73	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep them open.
PCM_CLK	75	DIO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V	

				V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
PCM_IN	76	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
PCM_OUT	78	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)		Require differential impedance of 95 Ω.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)		
PCIE_TX_M	44	AO	PCIe transmit (-)		
PCIE_TX_P	46	AO	PCIe transmit (+)		
PCIE_RX_M	32	AI	PCIe receive (-)		
PCIE_RX_P	34	AI	PCIe receive (+)		
PCIE_CLKREQ	36	DIO	PCIe clock request	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain If unused, keep them open.
PCIE_RST	39	DIO	PCIe reset		
PCIE_WAKE	30	DIO	PCIe wake up		
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_MD_IO	10	DIO	RGMII management data		If unused, keep them open. Power domain is determined by RGMII_PWR_IN.
RGMII_MD_CLK	11	DO	RGMII management data clock		
RGMII_RX_0	13	DI	RGMII receive data bit 0		
RGMII_RX_1	14	DI	RGMII receive data bit 1		

RGMII_CTL_RX	15	DI	RGMII receive control		
RGMII_RX_2	16	DI	RGMII receive data bit 2		
RGMII_RX_3	17	DI	RGMII receive data bit 3		
RGMII_CK_RX	19	DI	RGMII receive clock		
RGMII_TX_0	20	DO	RGMII transmit data bit 0		
RGMII_CTL_TX	21	DO	RGMII transmit control		
RGMII_TX_1	22	DO	RGMII transmit data bit 1		
RGMII_TX_2	23	DO	RGMII transmit data bit 2		
RGMII_CK_TX	24	DO	RGMII transmit clock		
RGMII_TX_3	25	DO	RGMII transmit data bit 3		
RGMII_PWR_EN	27	DO	Enable an external power supply to power RGMII_PWR_IN	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
RGMII_PWR_IN	28	PI	RGMII interface power supply input		1.8/2.5 V power supply input. If RGMII is not used, connect it to VDD_EXT.
RGMII_INT	29	DI	RGMII interrupt input	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. If unused, keep them open.
RGMII_RST	31	DO	Reset output for RGMII PHY	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SDIO Interface (for eMMC by Default)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_VDD	60	PI	SDIO power supply	Vmax = 1.85 V Vmin = 1.7 V Vnom = 1.8 V	Connect to an external 1.8 V power supply with a max. current of 10 mA. If

					SDIO interface is not used, connect this pin to VDD_EXT.
SDC1_DATA_0	49	DIO	SDIO data bit 0	V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V	If unused, keep them open.
SDC1_DATA_1	50	DIO	SDIO data bit 1		
SDC1_DATA_2	51	DIO	SDIO data bit 2		
SDC1_DATA_3	52	DIO	SDIO data bit 3		
SDC1_CMD	48	DIO	SDIO command		
SDC1_DATA_4	53	DIO	SDIO data bit 4	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. For eMMC configuration by default. Can be configured to GPIOs. If unused, keep them open.
SDC1_DATA_5	55	DIO	SDIO data bit 5		
SDC1_DATA_6	56	DIO	SDIO data bit 6		
SDC1_DATA_7	58	DIO	SDIO data bit 7		
SDC1_CLK	47	DIO	SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.4 V	If unused, keep it open.
EMMC_RST*	54	DO	eMMC reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI Interfaces [8]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	216	DO	SPI1 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep them open.
SPI1_CS	213	DO	SPI1 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI1_MISO	219	DI	SPI1 master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_CLK	103	DO	SPI2 clock	V_{OL}max = 0.45 V	

[8] SPI2 interface is optional.

				V_{OH}min = 1.35 V	
SPI2_CS	105	DO	SPI2 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
SPI2_MISO	106	DI	SPI2 master-in slave-out	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
SPI2_MOSI	108	DO	SPI2 master-out slave-in	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	247	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	If unused, keep them open.
ADC1	245	AI	General-purpose ADC interface		
ADC2 [9]	139	AI	General-purpose ADC interface		
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	83	DI	Force the module into download mode		1.8 V power domain. Active high. It is recommended to reserve a test point.
BT_EN	66	DO	Bluetooth enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DR_SYNC	95	DO	Dead reckoning sync	V_{OL}max = 0.45 V V_{OH}min =1.35 V	
IMU_INT1	169	DI	IMU interrupt 1	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	1.8 V power domain. Can be configured to GPIOs. If unused, keep them open.
IMU_INT2	187	DI	IMU interrupt 2	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
IMU_PWR_EN	181	DO	IMU power enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

[9] WMC529R series does not support ADC2.

WLAN and Bluetooth Application Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
WLAN_PWR_EN2	225	DO	WLAN power supply enable control 2	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_EN	228	DO	WLAN function enable control	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
COEX_UART_RXD	67	DI	LTE & WLAN & Bluetooth coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V V_{IH}max = 2.1 V	
COEX_UART_TXD	69	DO	LTE & WLAN & Bluetooth coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_SLP_CLK	231	DO	WLAN sleep clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	143	AIO	Main antenna interface		50 Ω impedance.
ANT_DIV	170	AI	Diversity antenna interface		
ANT_MIMO3 [10]	188	AI	4 × 4 MIMO antenna interface		
ANT_MIMO4 [10]	161	AI	4 × 4 MIMO		
ANT_GNSS [11]	197	AI	GNSS antenna interface		
ANT_CV2X_TRX1 [12]	205	AIO	C-V2X TRX1 antenna interface		
ANT_CV2X_TRX0 [12]	214	AIO	C-V2X TRX0 antenna interface		

[10] ANT_MIMO3 and ANT_MIMO4 are not supported by WMC529R series.
[11] GNSS is optional.
[12] WMC529R series does not support C-V2X by default.

Analog Audio Interface (Optional)					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC1_P	2	AI	Microphone input channel 1 (+)		Analog audio interface is optional, and is not supported by default. SPK signals are used for headset application. If unused, keep these pins open.
MIC1_N	1	AI	Microphone input channel 1 (-)		
MIC2_P	5	AI	Microphone input channel 2 (+)		
MIC2_N	4	AI	Microphone input channel 2 (-)		
MICBIAS	3	PO	Bias voltage output for microphone	Vmax = 1.55 V Vmin = 1.5 V Vnom = 1.525 V	
SPK1_P	268	AO	Analog audio differential output 1 (+)		
SPK1_N	266	AO	Analog audio differential output 1 (-)		
SPK2_P	269	AO	Analog audio differential output 2 (+)		
SPK2_N	270	AO	Analog audio differential output 2 (-)		
AGND	6	-	Analog ground		Connect it to GND or keep it open if unused.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	9, 35, 37, 41, 43, 57, 64, 65, 82, 89, 94, 96, 97, 99, 113, 119, 122, 123, 132, 136, 142, 152, 154, 157, 163, 166, 175, 178, 179, 184, 190, 193, 196, 200, 204, 207, 223, 224, 252, 271–275, 278–288, 290–306				Keep these pins open.

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.

4.4. Pin Multiplexing and BLSP Assignment

For details about the pin multiplexing and BLSP assignment of the module, please contact Wireless Mobility Technical Support.

4.5. Operating Modes

The table below briefly summarizes the various operating modes of the module referred in the following chapters.

Table 8: Overview of Operating Modes

Mode	Details	
Full functionality mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Voice/Data	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** or device management related API function can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or device management related API function can set the module into airplane mode where the RF function is invalid.	
Sleep Mode	The module retains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the power consumption is reduced to a very low level.	
Power OFF Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

For details of device management API functions and **AT+CFUN**, please contact Wireless Mobility Technical Support.

4.6. Power Saving

4.6.1. Low Power Mode (LPM)

The module is able to reduce its power consumption to an ultra-low level during the low power mode. This chapter mainly introduces the way to make the module enter or exit from LPM. The diagram below illustrates the power consumption of the module during LPM. For more details about low power mode of the module, please contact Wireless Mobility Technical Support.

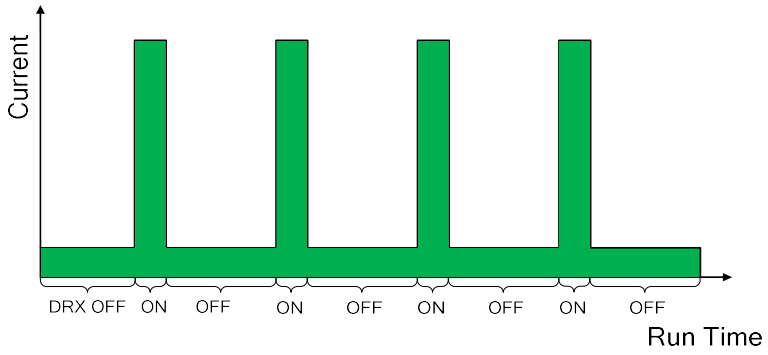


Figure 2: Low Power Mode Current Consumption Diagram

NOTE

The DRX cycle values are broadcasted by the wireless network.

4.6.1.1. LPM and Wakeup Solutions

The module provides some specific GPIOs to implement the LPM/wakeup solution between the module and the MCU.

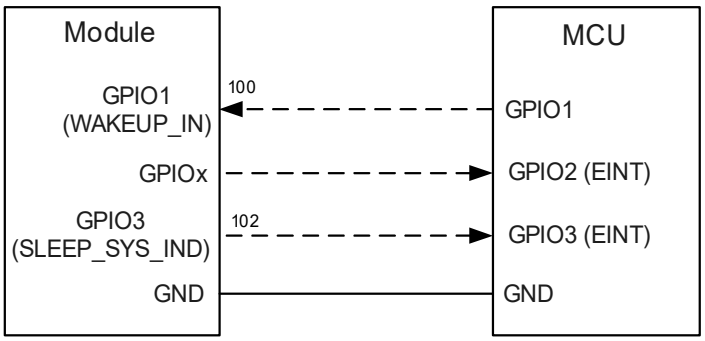


Figure 3: LPM/Wakeup Implementation Solution

Table 9: GPIO Configuration Related to LPM/Wakeup Solution

Pin Name	Pin No.	Default Function	Status Indication
GPIO1	100	WAKEUP_IN	● Falling edge: MCU controls the module to enter LPM ● Rising edge: MCU wakes up from LPM
GPIO3	102	SLEEP_SYS_IND	● Low level: the module enters LPM by default ● High level: the module exits LPM by default
GPIOx	User Specified	WAKEUP_OUT	Recommended design: ● Low level: the user application enters LPM ● High level: the user application exits LPM

For details, please contact Wireless Mobility Technical Support.

NOTE

1. Pay attention to the level mismatch of the connection signal between the module and the external MCU if the MCU interface is not in the 1.8 V voltage domain.
2. GPIO1 of the module is used as WAKEUP_IN (input signal) by default, through which the MCU controls the module to enter/exit LPM.
3. GPIOx can be any GPIO of the module, i.e., you can define any GPIO into WAKEUP_OUT (output signal).
4. Keep USB_VBUS low when the module is in LPM.

4.6.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands and API functions correlative with RF function will be inaccessible.

AT command:

The mode can be set via **AT+CFUN=<fun>**. The parameter **<fun>** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

API functions:

The mode can be set via device management related API functions. For more details about device management API functions, please contact Wireless Mobility Technical Support.

NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

4.7. Power Supply

4.7.1. Power Supply Pins

The module provides 11 VBAT pins for connection with an external power supply.

- Three VBAT_BB pins for module's baseband part.
- Eight VBAT_RF pins for module's RF part.

The following table shows the details of VBAT pins and ground pins.

Table 10: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	241, 242, 244	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF [13]	109, 111, 112, 114 235, 236, 238, 239	PI	Power supply for the module's RF part	3.3/3.7	3.8	4.3	V
GND	12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124–131,133–135, 137, 138, 140, 141, 144–151,153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171–174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307–400						

4.7.2. Voltage Stability Requirements

The power supply range of VBAT_BB is 3.3–4.3 V, VBAT_RF is 3.7–4.3 V. Ensure that the input voltage of VBAT_BB will never drop below 3.3 V, VBAT_RF will never drop below 3.7 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

[13] The minimum input voltage of WMC529R-EUAQB ,WMC529R-INAQ WMC529R-ROWAQ&INAQ is 3.7 V, while the minimum input voltage of WMC529R-NAAQ and WMC529R-ROWAQ is 3.3 V.

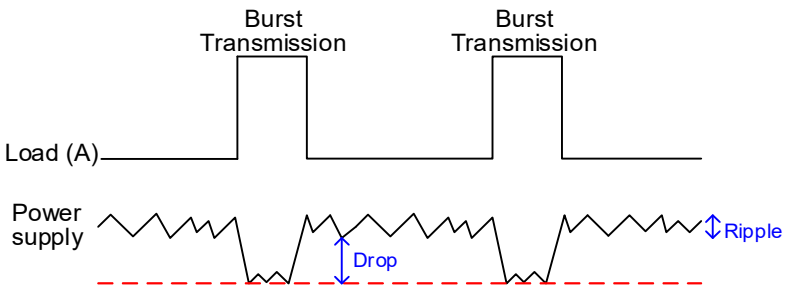


Figure 4: Power Supply Limits During Burst Transmission

To decrease voltage drop, the bypass capacitors of about 100 μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved for VBAT_BB and VBAT_RF respectively, due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The external 3.8 V main power supply connected to VBAT_BB and VBAT_RF has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 1 mm. The width of VBAT_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use TVS diodes to prevent EOS, and place them as close to the VBAT pins as possible. The recommended power supply structure is presented in the figure below.

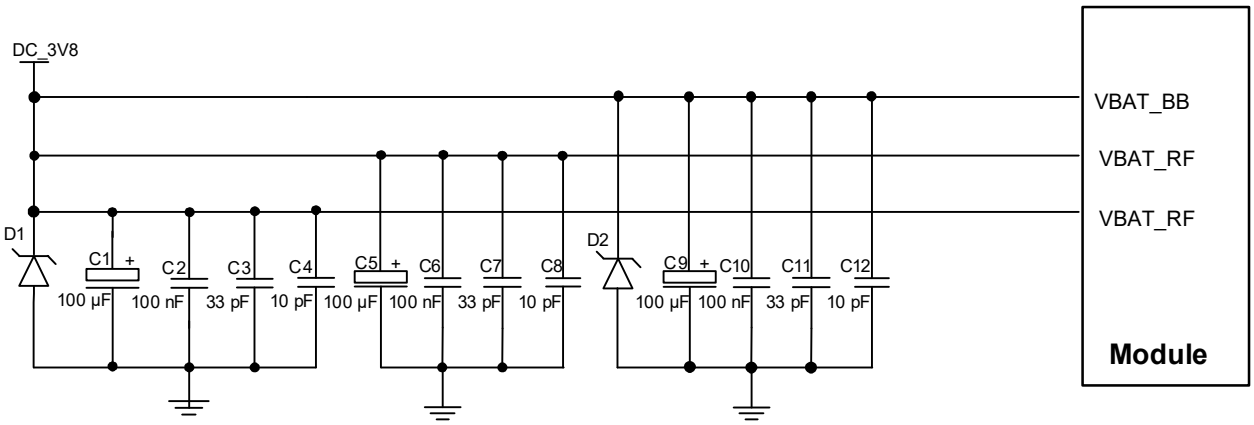


Figure 5: Power Supply Design

4.7.3. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is

preferred to be used as the power supply.

The following figure shows a reference design for +12/+24 V input power source. The designed output for the power supply is about 5.0 V and the maximum rated current is 5.0 A.

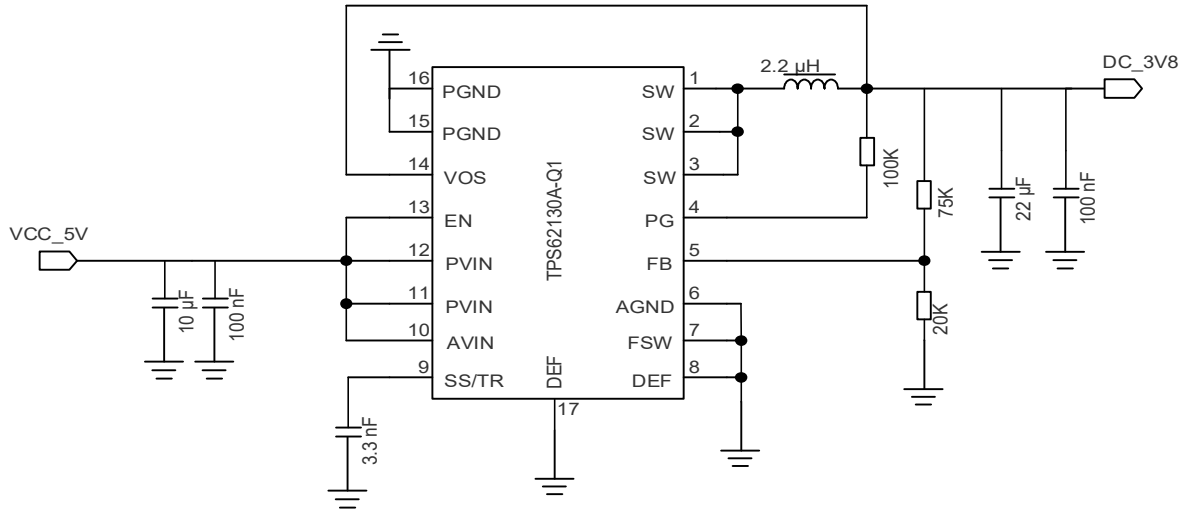


Figure 6: 12/24 V Power Supply System Reference Design

NOTE

1.To avoid damaging the data of internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or Linux commands, the power supply can be cut off.
2. When you turn off module with Linux commands, keep PWRKEY at high level after the execution of Linux command. Otherwise, the module will be turned on again after successful turn-off.

4.7.4. Power Supply Monitoring

API can be used to monitor the VBAT_BB voltage value. For more details of the command, please contact Wireless Mobility Technical Support.

4.8. Turn On

4.8.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 11: PWRKEY Pin Description

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is turned off, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

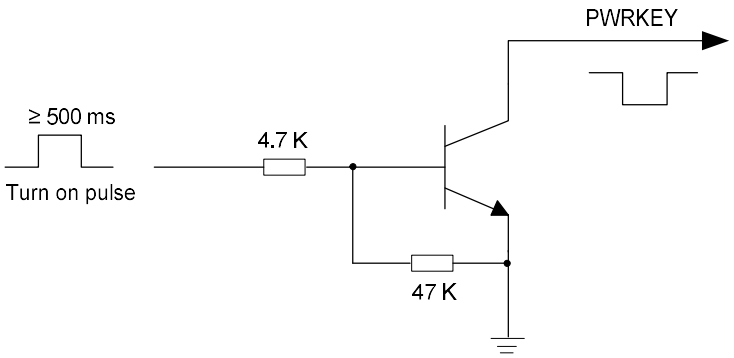


Figure 7: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

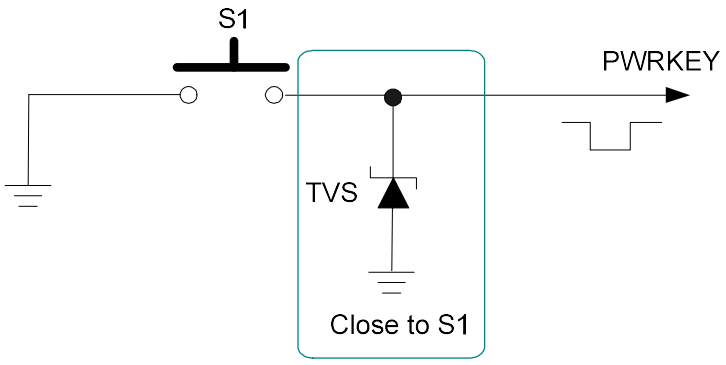


Figure 8: Turn On the Module Using a Button

The power-up timing is illustrated in the following figure.

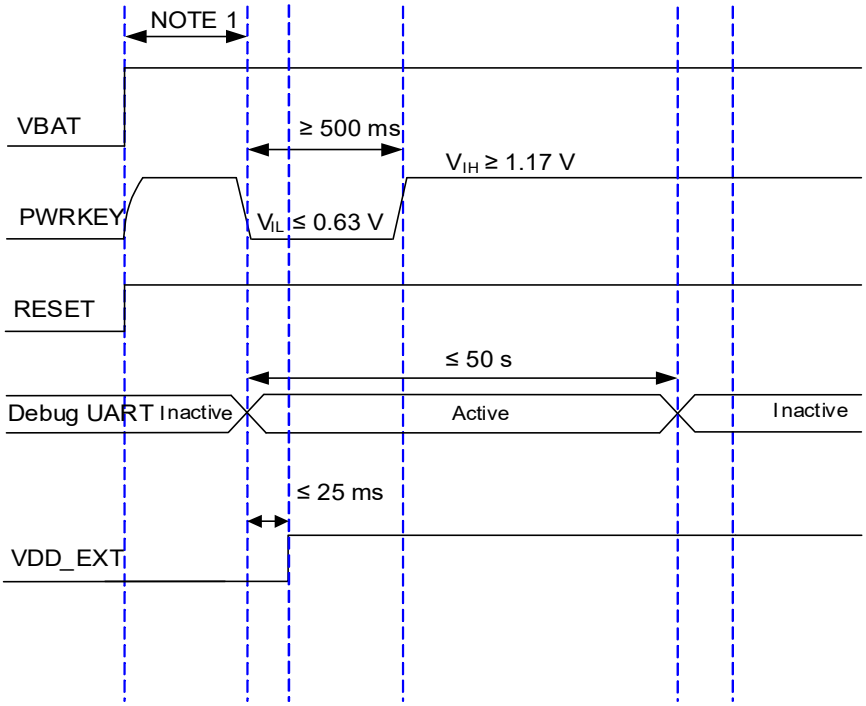


Figure 9: Power-up Timing

NOTE

1. Ensure that VBAT is stable for at least 30 ms before pulling down PWRKEY.
2. It is recommended to use an external OD/OC circuit to control the PWRKEY pin.
3. Make sure that there is no large capacitance load on PWRKEY pin.

4.8.2. Turn On with PON_1

The following table shows the pin definition of PON_1.

Table 12: PON_1 Pin Description

Pin Name	Pin No.	I/O	Description	Comment
PON_1	248	DI	Power on the module upon rising edge	Valid voltage range: 0.78–1.89 V.

When the module is powered off, driving PON_1 high (rising edge) will make the module turn on automatically. A simple reference circuit is illustrated in the following figure.

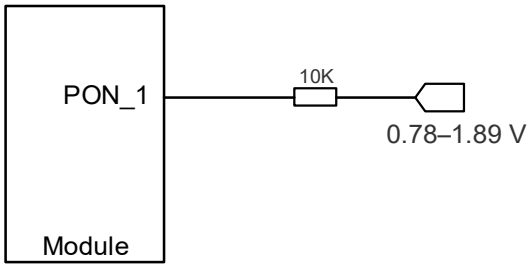


Figure 10: Turn On the Module Using PON_1

NOTE

If PON_1 is not used, it is recommended to connect it to the ground.

4.9. Turn Off

Either of the following methods can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using API interface.
- Turn off the module using Linux commands.

4.9.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 2 s, the module will execute power-down procedure after PWRKEY is released. The power-down timing is illustrated in the following figure.

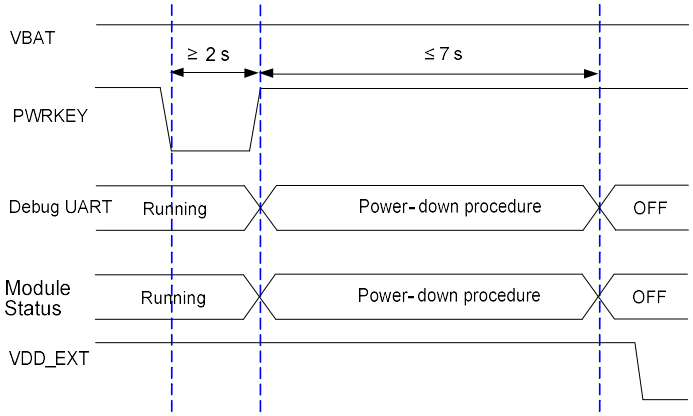


Figure 11: Power-down Timing

4.9.2. Turn Off with API Interface

It is a safe way to use API interface to turn off the module, which is similar to turning off the module via PWRKEY Pin. For details about API function, please contact Wireless Mobility Technical Support.

4.9.3. Turn Off with Linux Commands

It is also a safe way to use Linux commands, such as **shutdown** and **poweroff**, to turn off the module, which is similar to turning off the module via PWRKEY pin.

NOTE

1. To avoid damaging the data of internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or API interface or Linux commands, the power supply can be cut off.
2. When you turn off module with API interface or Linux commands, keep PWRKEY at high level after the execution of power-off command. Otherwise, the module will be turned on again after successful turn-off.

4.10. Reset

The module can be reset by driving RESET low for 250–550 ms. As the RESET pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

Table 13: RESET Pin Description

Pin Name	Pin No.	I/O	Description	Comment
RESET	8	DI	Reset the module	Internally pulled up to 1.8 V. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET.

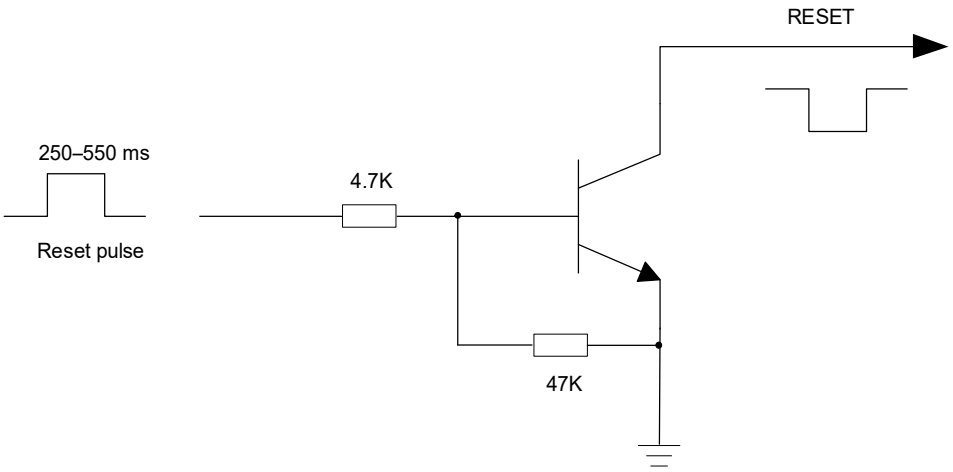


Figure 12: Reference Circuit of RESET by Using Driving Circuit

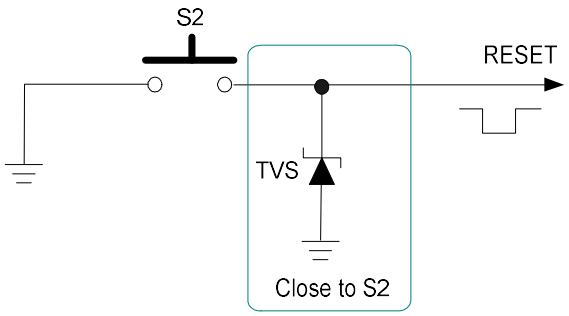


Figure 13: Reference Circuit of RESET by Using a Button

The reset scenario is illustrated in the following figure.

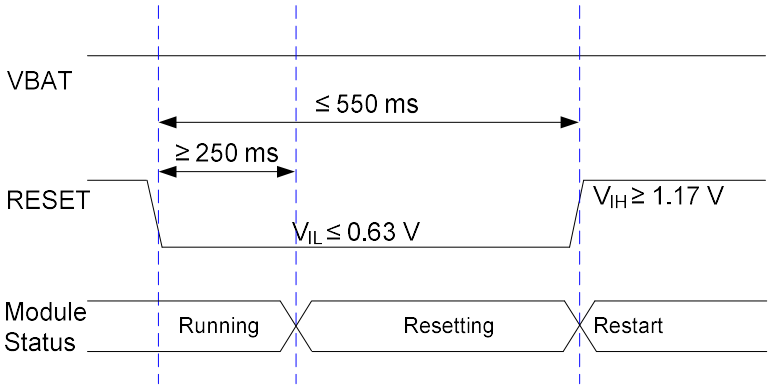


Figure 14: Reset Timing

NOTE

1. Ensure that there is no large capacitance load on RESET pin.
2. RESET should only be used when turning off the module by API interface, Linux commands and PWRKEY pin all failed.

4.11. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 14: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	251	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	254	DIO	(U)SIM1 card data	
USIM1_CLK	253	DO	(U)SIM1 card clock	
USIM1_RST	250	DO	(U)SIM1 card reset	
USIM2_VDD	256	PO	(U)SIM2 card power supply	
USIM2_DATA	257	DIO	(U)SIM2 card data	
USIM2_CLK	259	DO	(U)SIM2 card clock	
USIM2_RST	260	DO	(U)SIM2 card reset	
USIM1_DET	255	DI	(U)SIM1 card insertion detect	1.8 V power domain. If unused, keep them open.
USIM2_DET	258	DI	(U)SIM2 card insertion detect	

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

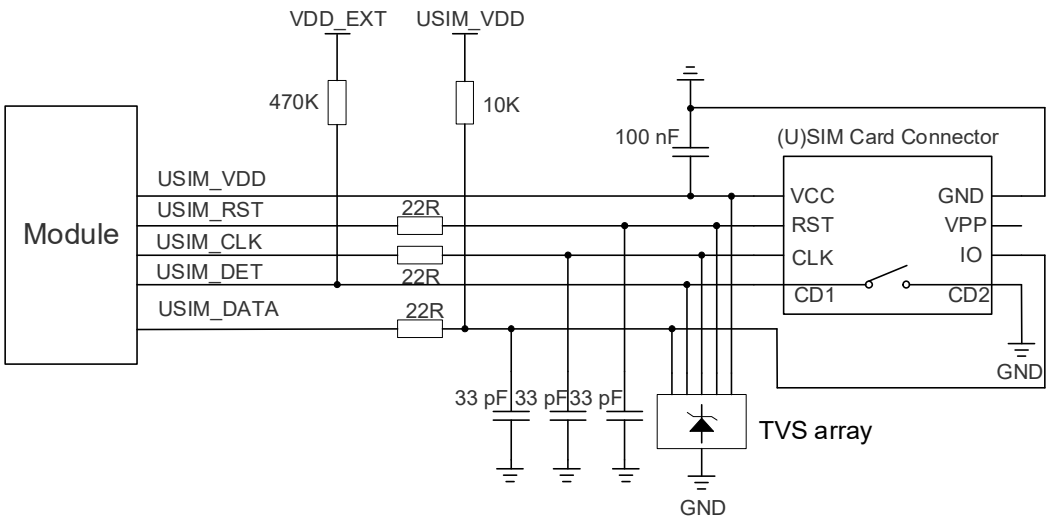


Figure 15: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

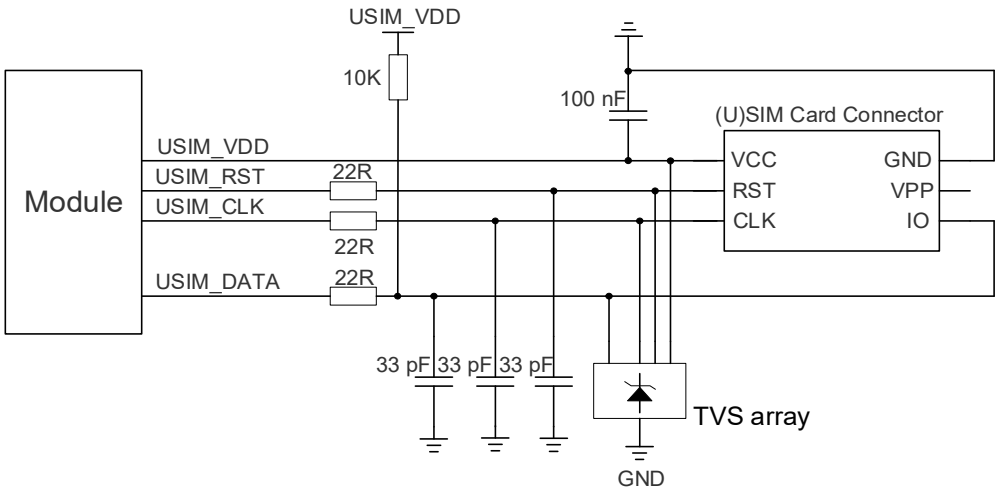


Figure 16: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in your applications, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and power supply traces.
- Assure the trace between the ground of the module and that of the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and

shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used for filtering out RF interferences. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 10 kΩ pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

NOTE

1. The load capacitance of (U)SIM interface will affect the rising and falling time of the data exchange.
2. (U)SIM2 interface is optional.

4.12. USB Interface

The module provides one integrated USB interface which complies with the USB 3.0/2.0 specifications, and supports SuperSpeed (5 Gbps on USB 3.0) and high-speed (480 Mbps on USB 2.0) modes.

Both USB 2.0 and USB 3.0 support AT command communication, data transmission, GNSS NMEA sentence output, software debugging and voice over USB*.

USB 3.0 is used for data communication with AP by default. Only USB 2.0 can be used for firmware upgrading. When USB 2.0 and USB 3.0 are connected to the same host, USB 3.0 takes effect by default.

Table 15: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	84	DI	USB connection detect	Maximum current: 0.1 mA. Typical 5.0 V
USB_DP	85	AIO	USB 2.0 differential data (+)	Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	87	AIO	USB 2.0 differential data (-)	
USB_SS_TX_P	93	AO	USB 3.0 SuperSpeed transmit (+)	Compliant with USB 3.0 standard specification. Require differential impedance of 90 Ω.
USB_SS_TX_M	91	AO	USB 3.0 SuperSpeed transmit (-)	
USB_SS_RX_P	90	AI	USB 3.0 SuperSpeed receive (+)	

USB_SS_RX_M	88	AI	USB 3.0 SuperSpeed receive (-)

For more details about the USB 3.0 and 2.0 specifications, visit http://www.usb.org/home.

It is recommended to reserve USB 2.0 for firmware upgrade in application designs, and test points must be reserved for debugging purpose. The following figure is the reference circuits of USB 2.0 interface.

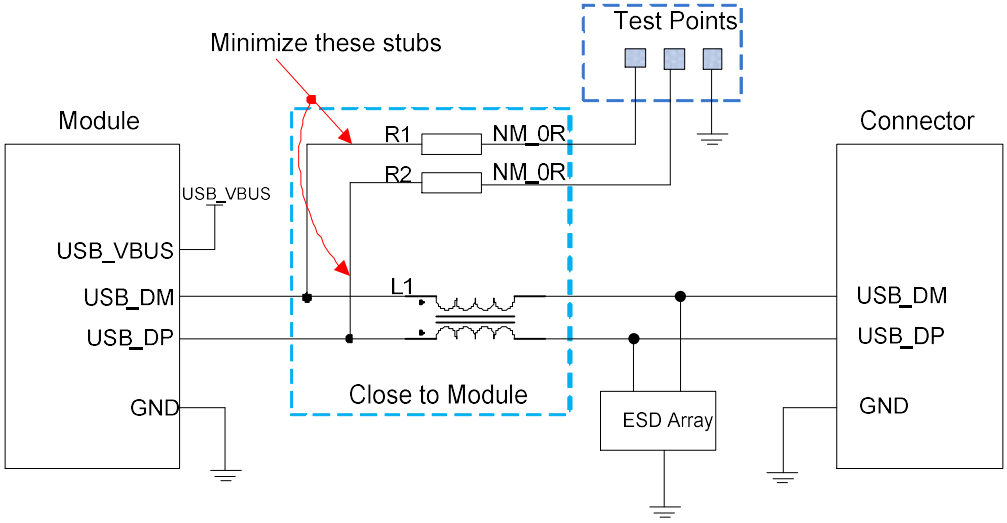


Figure 17: Reference Circuit of USB 2.0 Application

In USB 2.0 applications, a common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure signal integrity of USB data traces, place R1, R2 and L1 close to the module, and also place these resistors close to each other. The extra stubs of trace must be as short as possible.

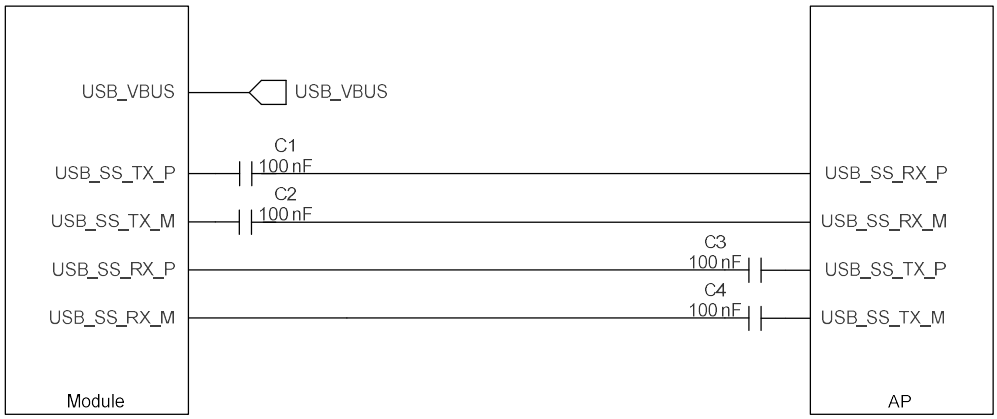


Figure 18: Reference Circuit of USB 3.0 Application

In USB 3.0 application, place C1 and C2 near the module, and place C3 and C4 near the AP. The extra stubs of trace must be as short as possible.

To meet USB 2.0 and USB 3.0 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB 2.0 and 3.0 signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- The length of each trace in USB 2.0 differential pair should be less than 120 mm, and the length matching of the differential pair should be less than 0.7 mm (5 ps).
- The length of each trace in USB 3.0 differential pairs should be less than 100 mm, and the length matching of each differential pair should be less than 0.7 mm (5 ps).
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. Route the RF signals operating at 2.4 GHz frequency with the highest isolation possible from USB_SS_TX/RX traces.
- Keep the ESD protection components as close to the USB connector as possible.
- Junction capacitance of the ESD protection component might cause influences on USB data traces, so you should pay attention to the selection of the device. Typically, the capacitance value should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- USB_SS_TX AC coupling capacitors can be anywhere along the line, but better to be placed close to the source or the ESD/connector side to keep good signal integrity of main route on PCB.

NOTE

1. The module supports USB master mode, but works in slave mode by default.
2. The high-speed PHY and SuperSpeed PHY share the same controller inside baseband chipset, so USB 2.0 and USB 3.0 cannot be used simultaneously.

4.13. UART Interfaces

The module provides three UART interfaces: UART1, Bluetooth UART and debug UART. The following are the features of these UART interfaces.

Table 16: Basic Information of UART Interface

UART Type	Supported Baud Rate (bps)	Default Baud Rate (bps)	Description
UART1	4800,9600,19200, 38400,57600,115200, 230400,460800, 921600	115200	• Support RTS and CTS hardware flow control • Data transmission

Bluetooth UART		115200	• Support RTS and CTS hardware flow control • Data transmission
Debug UART	115200	115200	Linux console and log output

The following tables show the pin definition of the UART interfaces.

Table 17: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_CTS	71	DO	Clear to send signal from the module	1.8 V power domain. Can be configured to GPIOs. Connect to the MCU's CTS.
UART1_RTS	74	DI	Request to send signal to the module	1.8 V power domain. Can be configured to GPIOs. Connect to the MCU's RTS.
UART1_TXD	70	DO	UART1 transmit	1.8 V power domain. Can be configured to GPIOs.
UART1_RXD	72	DI	UART1 receive	

Table 18: Pin Definition of Bluetooth UART Interface

Pin Name	Pin No.	I/O	Description	Comment
BT_UART_TXD	59	DO	Bluetooth UART transmit	1.8 V power domain. Can be configured to GPIOs.
BT_UART_RXD	63	DI	Bluetooth UART receive	
BT_UART_RTS	61	DI	Request to send signal to the module	1.8 V power domain. Can be configured to GPIOs. Connect to AF50T/ AF51Y's RTS.
BT_UART_CTS	62	DO	Clear to send signal from the module	1.8 V power domain. Can be configured to GPIOs. Connect to AF50T/

	AF51Y's CTS.

Table 19: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	107	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved for debug UART.
DBG_RXD	110	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

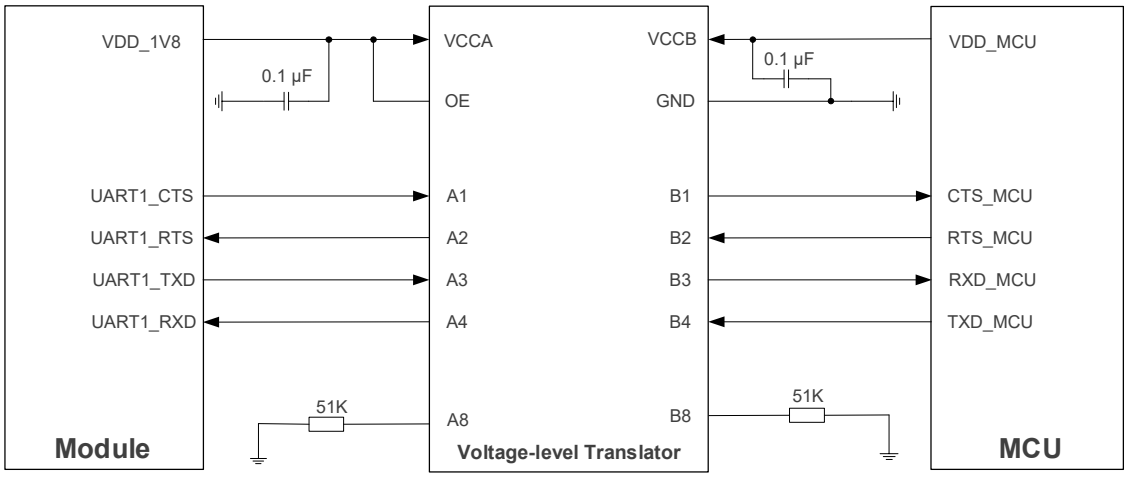


Figure 19: Reference Circuit with Translator Chip(UART1)

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but pay attention to the direction of connection.

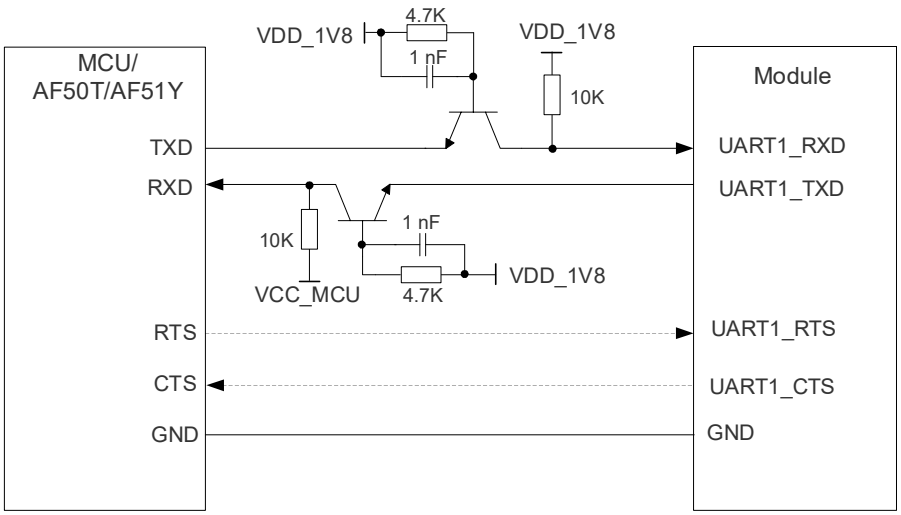


Figure 20: Reference Design of UART Interface with Transistor Circuit (UART1)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. For the purpose of reducing power consumption, it is recommended to switch off the power supply for VDD_1V8 in sleep mode.
3. If hardware flow control is intended to be used, then CTS and RTS should also be designed with the level-shifting circuit. Note that the module's CTS is connected to the MCU's CTS (or that of AF51Y/AF50T), and the module's RTS is connected to the MCU's RTS (or that of AF51Y/AF50T).
4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.14. I2S and I2C Interfaces

The module provides I2S and I2C interfaces for audio design. The following table shows the pin definition of I2S and I2C interfaces which can be applied on audio codec design.

Table 20: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
CDC_RST	77	DO	External codec reset	1.8 V power domain.

I2S_MCLK	81	DO	Clock output for codec	Can be configured to GPIOs.
I2S_WS	265	DIO	I2S word select	
I2S_SCK	262	DIO	I2S clock	
I2S_DIN	263	DI	I2S data in	
I2S_DOUT	261	DO	I2S data out	

Table 21: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	79	OD	I2C serial clock	Require external pull-up to 1.8 V. Can be configured to GPIOs.
I2C1_SDA	80	OD	I2C serial data	

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.

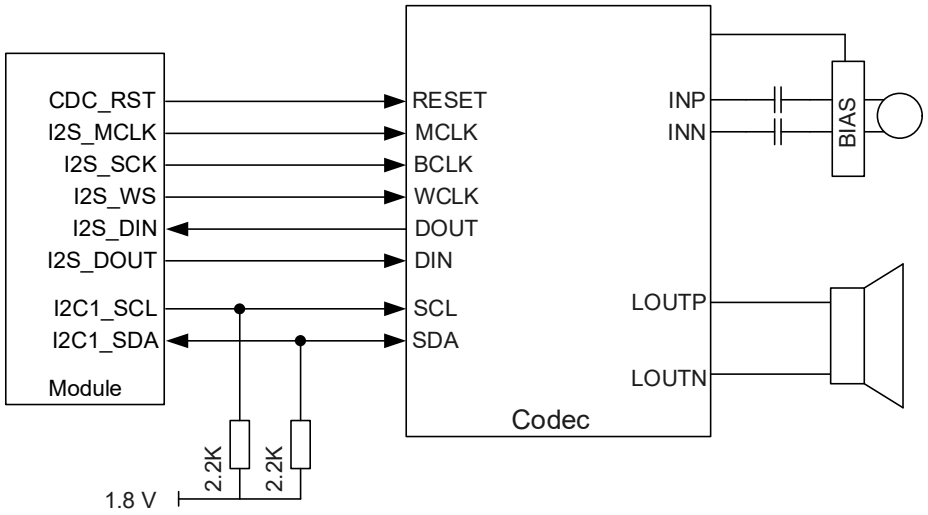


Figure 21: Reference Circuit of I2S and I2C Application with Audio Codec

NOTE

The module works as a master device in applications pertaining to I2C interface.

4.15. PCM Interface

The module provides one PCM interface for Bluetooth audio transmission function by default. See ***Chapter 4.19*** for more details.

The PCM interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

Table 22: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	73	DIO	PCM data frame sync	In master mode, it is an output signal. In slave mode, it is an input signal. 1.8 V power domain. Can be configured to GPIO.
PCM_CLK	75	DIO	PCM clock	
PCM_IN	76	DI	PCM data input	1.8 V power domain. Can be configured to GPIO.
PCM_OUT	78	DO	PCM data output	

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50% duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

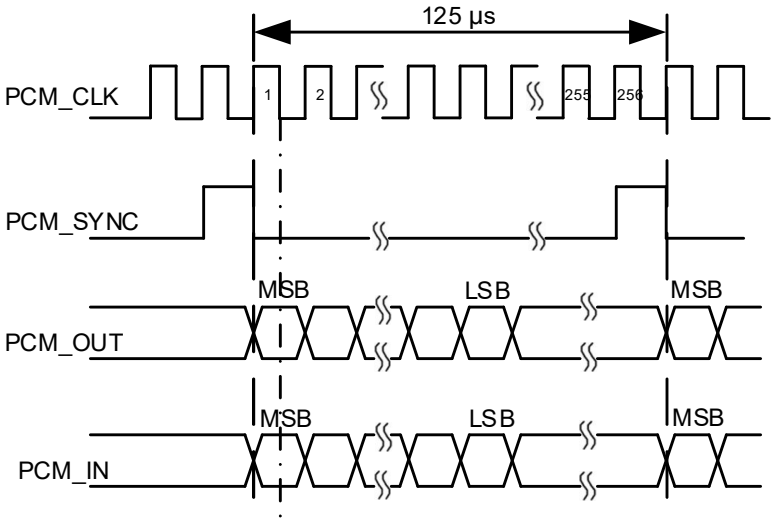


Figure 22: Primary Mode Timing

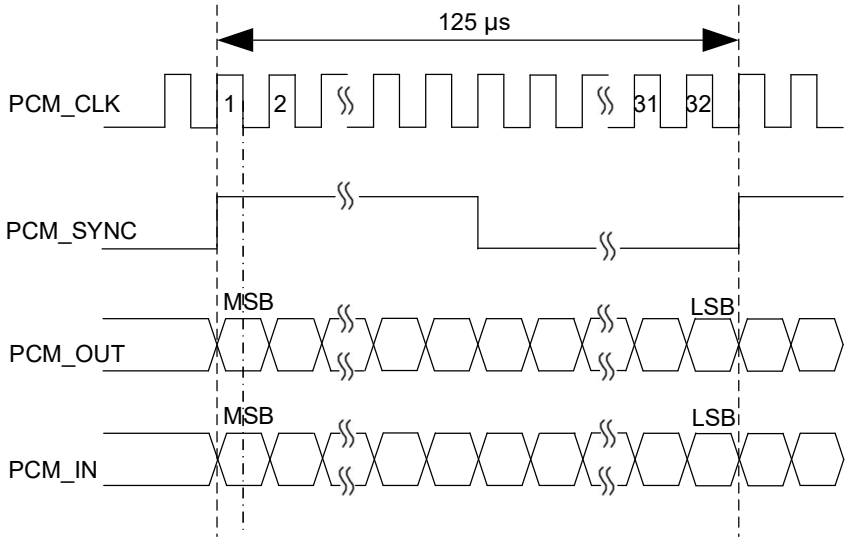


Figure 23: Auxiliary Mode Timing

Clock and mode can be configured by software, and the default configuration is master mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC.

NOTE

When using Bluetooth function, PCM_SYNC and PCM_CLK can only be used as output signal.

4.16. SDIO Interface

The module provides an SDIO interface, which can be used for eMMC (4-bit by default, max. 8-bit).

The following tables show the pin definition of SDIO interface.

Table 23: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SDIO_VDD	60	PI	SDIO power supply	Connect to an external 1.8 V power supply with a max. current of 10 mA. If SDIO interface is not used, connect this pin to VDD_EXT.
SDC1_DATA_0	49	DIO	SDIO data bit 0	1.8 V power domain.
SDC1_DATA_1	50	DIO	SDIO data bit 1	
SDC1_DATA_2	51	DIO	SDIO data bit 2	
SDC1_DATA_3	52	DIO	SDIO data bit 3	
SDC1_CMD	48	DIO	SDIO command	
SDC1_DATA_4	53	DIO	SDIO data bit 4	1.8 V power domain. For eMMC configuration by default. Can be configured to GPIOs. If unused, keep them open.
SDC1_DATA_5	55	DIO	SDIO data bit 5	
SDC1_DATA_6	56	DIO	SDIO data bit 6	
SDC1_DATA_7	58	DIO	SDIO data bit 7	
SDC1_CLK	47	DIO	SDIO clock	1.8 V power domain.
EMMC_RST*	54	DO	eMMC reset	1.8 V power domain.
EMMC_PWR_EN	45	DO	eMMC power supply enable control	

4.16.1. Reference Design for eMMC Application

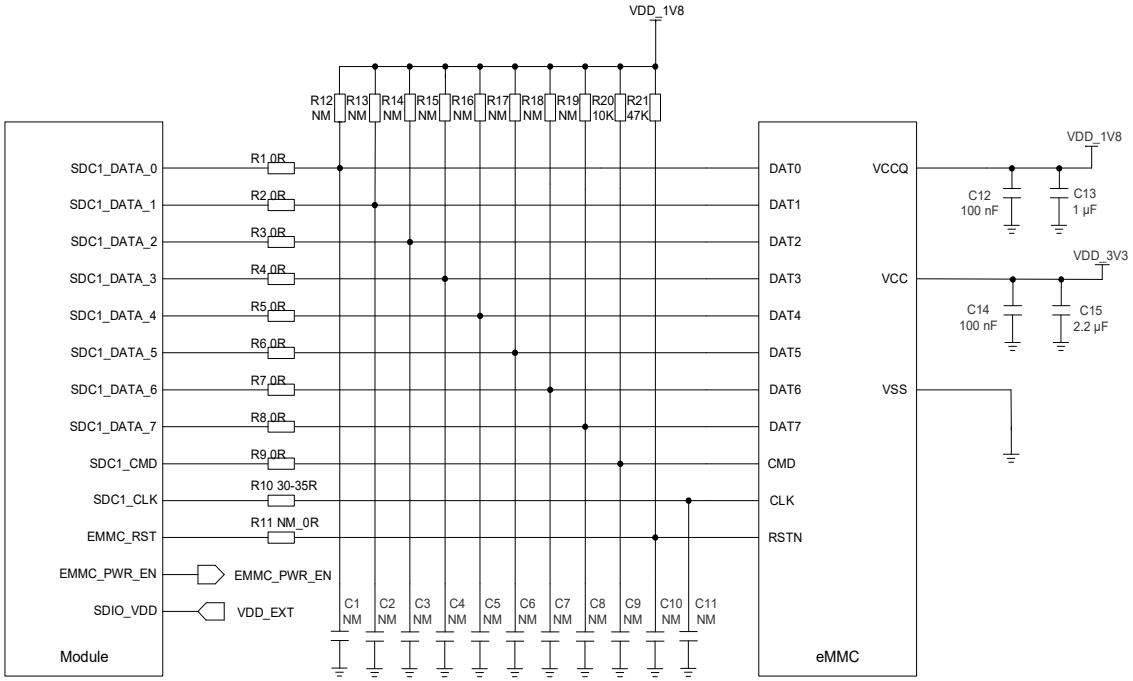


Figure 24: Reference Design for eMMC Application

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve resistors R12–R19 (10–100 kΩ) to pull up SDIOs to VDD_1V8. Resistors R12–R19 are not mounted by default.
- To improve signal quality, it is recommended to add 0 Ω resistors R1–R9 and R11 in series between the module and eMMC. Resistor R10 should be 30–35 Ω. The bypass capacitors C1–C11 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- SDIO signal traces should comply with the following principles:
  1) It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω ±10 %.
  2) Keep the spacing between adjacent SDC1_DATA traces and that between SDC1_DATA and SDC1_CLK traces at least twice the trace width.
  3) Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
  4) It is recommended to keep the trace length difference between SDC1_CLK and SDC1_DATA[0:7]/SDC1_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 17 mm, so the exterior total trace length should be less than 33 mm.
  5) Keep the spacing between SDIO and other signal traces at least twice the trace width and the load capacitance of SDIO bus less than 40 pF.

4.17. SPIs

The module provides two SPIs supporting only master mode. The maximum clock frequency of SPI is up to 50 MHz.

The following tables show the pin definition of SPIs.

Table 24: Pin Definition of SPIs

Pin Name	Pin No.	I/O	Description	Comment
SPI1_CLK	216	DO	SPI1 clock	1.8 V power domain. Can be configured to GPIOs.
SPI1_CS	213	DO	SPI1 chip select	
SPI1_MISO	219	DI	SPI1 master-in slave-out	
SPI1_MOSI	210	DO	SPI1 master-out slave-in	
SPI2_CLK [14]	103	DO	SPI2 clock	
SPI2_CS [14]	105	DO	SPI2 chip select	
SPI2_MISO [14]	106	DI	SPI2 master-in slave-out	
SPI2_MOSI [14]	108	DO	SPI2 master-out slave-in	

The following figure shows the timing relationship of SPI interfaces. The related parameters of SPI timing are shown in the table below.

[14] SPI2 interface is optional.

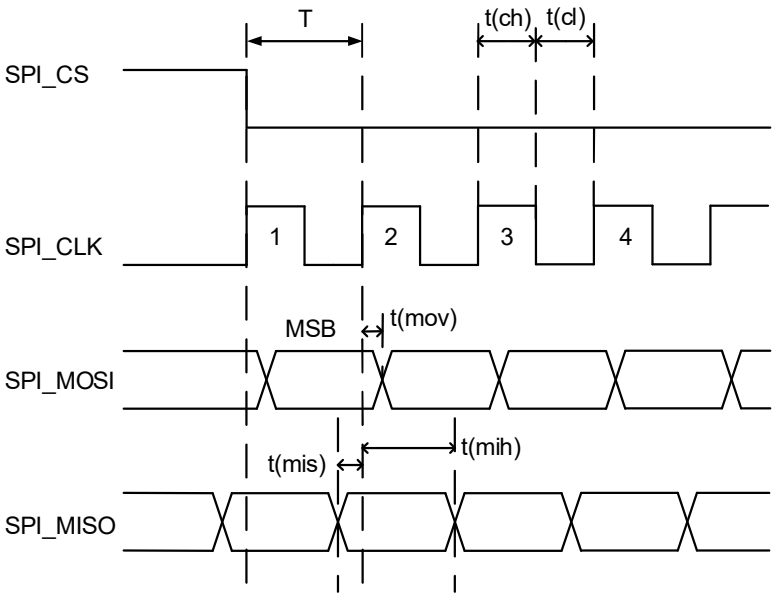


Figure 25: SPI Timing

Table 25: Parameters of SPI Interfaces Timing

Parameter	Description	Min.	Typ.	Max.	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high-level time	9.0	-	-	ns
t(cl)	SPI clock low-level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides two 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the MCU if your application is equipped with a 3.3 V processor or device interface.

4.18. RGMII Interface

The module includes an integrated Ethernet MAC with a RGMII interface. Key features of the RGMII interface are shown below:

- Supports IEEE 1588-2008, IEEE 802.1AS-2011 and IEEE 802.1Qav-2009
- Supports half/full duplex for 10/100/1000 Mbps [15]
- Supports VLAN tagging
- Supports connection to an external Ethernet PHY such as Marvell 88Q2112, or an external switch

The following table shows the pin definition of RGMII interface.

Table 26: Pin Definition of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_MD_IO	10	DIO	RGMII management data input/output	
RGMII_MD_CLK	11	DO	RGMII management data clock	
RGMII_RX_0	13	DI	RGMII receive data bit 0	
RGMII_RX_1	14	DI	RGMII receive data bit 1	
RGMII_CTL_RX	15	DI	RGMII receive control	
RGMII_RX_2	16	DI	RGMII receive data bit 2	
RGMII_RX_3	17	DI	RGMII receive data bit 3	Power domain determined by RGMII_PWR_IN.
RGMII_CK_RX	19	DI	RGMII receive clock	
RGMII_TX_0	20	DO	RGMII transmit data bit 0	
RGMII_CTL_TX	21	DO	RGMII transmit control	
RGMII_TX_1	22	DO	RGMII transmit data bit 1	
RGMII_TX_2	23	DO	RGMII transmit data bit 2	
RGMII_CK_TX	24	DO	RGMII transmit clock	
RGMII_TX_3	25	DO	RGMII transmit data bit 3	
RGMII_PWR_EN	27	DO	Enable external power supply to power RGMII_PWR_IN	1.8 V power domain. If unused, keep it open.

[15] The module's RGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

RGMII_PWR_IN	28	PI	RGMII interface power supply input	Typical voltage: 1.8/2.5 V. If RGMII interface is not used, connect this pin to VDD_EXT.
RGMII_INT	29	DI	RGMII interrupt output	1.8 V power domain.
RGMII_RST	31	DO	RGMII reset external PHY	

The following figure shows the simplified block diagram for Ethernet application.

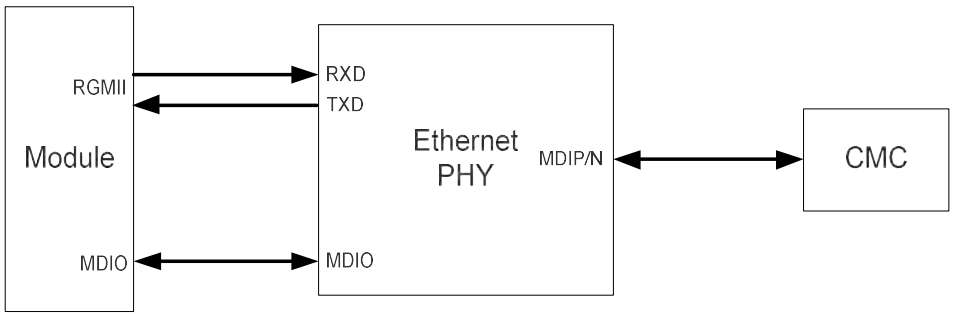


Figure 26: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of RGMII interface with PHY application. For more details, please contact Wireless Mobility Technical Support.

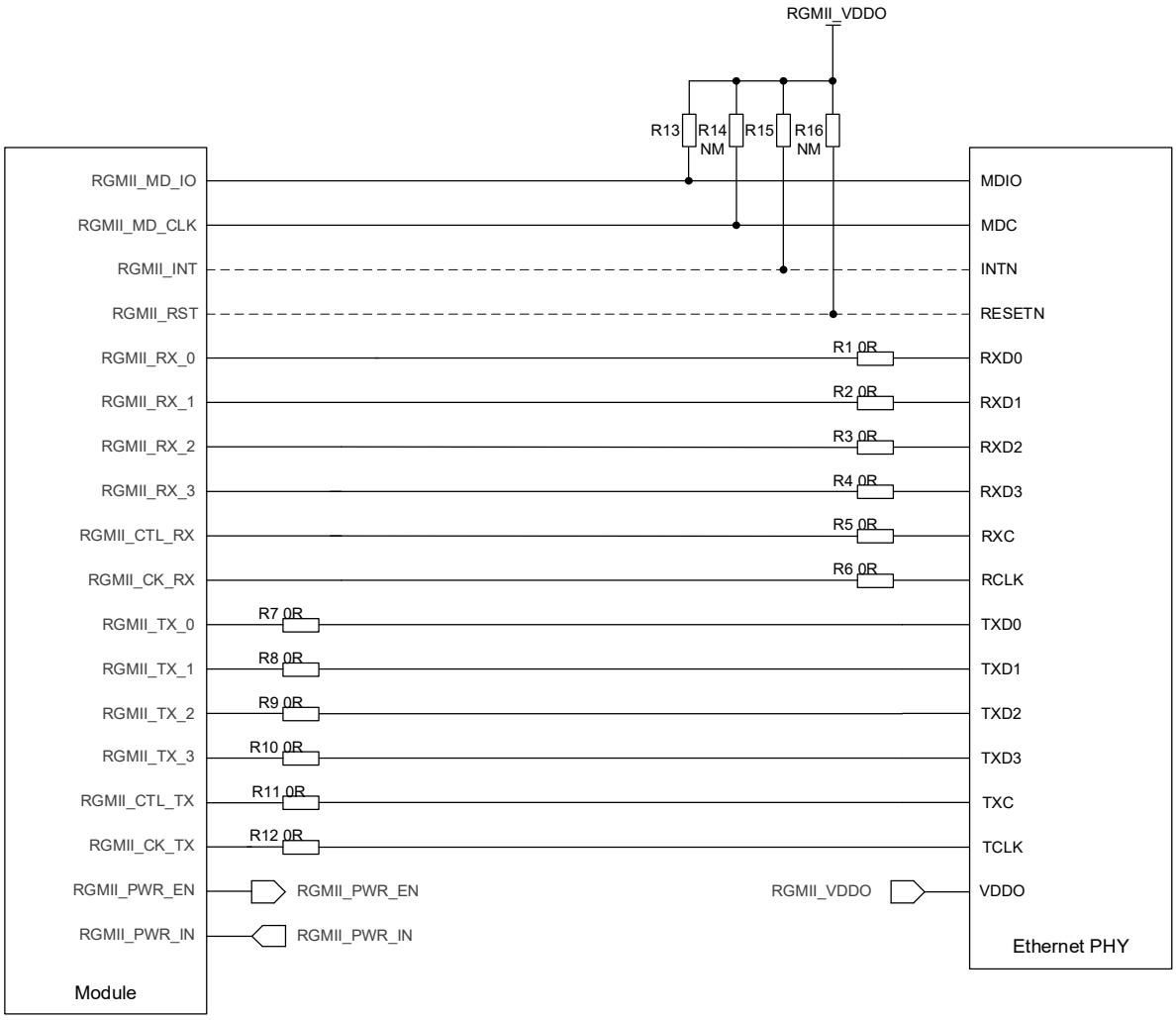


Figure 27: Reference Circuit of RGMII Interface with PHY Application

To enhance the reliability and availability of your application, follow the criteria below in the Ethernet PHY circuit design:

- The I/O voltage of RGMII matches with that of PHY.
- The typical power consumption of RGMII_PWR_IN is 150 mA @ 1.8 V.
- Keep RGMII data and control signals away from sensitive signals, such as RF, clock, VBAT and analog signals.
- Ensure the impedance of RGMII signals trace is 50 Ω ±20 %.
- The length matching between Tx signals (RGMII_CK_TX, RGMII_CTL_TX and RGMII_TX_[0:3]) or Rx signals (RGMII_CK_RX, RGMII_CTL_RX and RGMII_RX_[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII_CK_TX, RGMII_CTL_TX, RGMII_TX_[0:3]) or that between Rx bus traces (RGMII_CK_RX, RGMII_CTL_RX, RGMII_RX_[0:3]) at least twice the trace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width.
- Keep the spacing between of RGMII and other signal traces at least 3 times trace width.
- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the

Ethernet PHY. The value of R1–R16 varies with the selection of PHY.

4.19. WLAN and Bluetooth Application Interfaces

The module provides a PCIe interface for WLAN function, and UART and PCM interfaces for Bluetooth function. If Bluetooth function is needed, the module should be connected with WLAN & Bluetooth module.

The following table shows the pin definition of wireless connectivity interfaces.

Table 27: Pin Definition of WLAN and Bluetooth Application Interfaces

PCIe Interface				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	Serves as an output signal in RC mode. Serves as an input signal in EP mode. The differential impedance should be the same as that for PCIe TX/RX.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	
PCIE_TX_M	44	AO	PCIe transmit (-)	Require differential impedance of 95 Ω.
PCIE_TX_P	46	AO	PCIe transmit (+)	
PCIE_RX_M	32	AI	PCIe receive (-)	
PCIE_RX_P	34	AI	PCIe receive (+)	
PCIE_CLKREQ	36	DIO	PCIe clock request	1.8 V power domain. Serves as an input signal in RC mode. Serves as an output signal in EP mode.
PCIE_WAKE	30	DIO	PCIe wakeup	
PCIE_RST	39	DIO	PCIe reset	1.8 V power domain. Serves as an output signal in RC mode. Serves as an input signal in EP mode.

Coexistence Interface				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
COEX_UART_RXD	67	DI	LTE & WLAN & Bluetooth coexistence receive	1.8 V power domain.
COEX_UART_TXD	69	DO	LTE & WLAN & Bluetooth coexistence transmit	
Bluetooth Application Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
BT_UART_TXD	59	DO	Bluetooth UART transmit	1.8 V power domain. Can be configured to GPIOs.
BT_UART_RXD	63	DI	Bluetooth UART receive	
BT_UART_RTS	61	DI	Request to send signal to the module	1.8 V power domain. Can be configured to GPIOs. Connect to AF50T/AF51Y's RTS.
BT_UART_CTS	62	DO	Clear to send signal from the module	1.8 V power domain. Can be configured to GPIOs. Connect to AF50T/AF51Y's CTS.
PCM_SYNC	73	DIO	PCM data frame sync	1.8 V power domain. Can be configured to GPIOs.
PCM_CLK	75	DIO	PCM data bit clock	
PCM_IN	76	DI	PCM data input	
PCM_OUT	78	DO	PCM data output	
Other Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
WLAN_PWR_EN1	222	DO	WLAN power supply enable control 1	1.8 V power domain.
WLAN_PWR_EN2	225	DO	WLAN power supply enable control 2	
WLAN_EN	228	DO	WLAN function enable control	
BT_EN	66	DO	Bluetooth enable control	
WLAN_SLP_CLK	231	DO	WLAN sleep clock	

VDD_WIFI_VM	276	PO	Medium-voltage power supply for Wi-Fi	After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module.
VDD_WIFI_VH	277	PO	High-voltage power supply for Wi-Fi	After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module.

NOTE

1. When WLAN or Bluetooth function is used, the coexistence interface must be used simultaneously. And the coexistence interface cannot be used as a general UART interface.
2. When Bluetooth function is enabled on the module, PCM_SYNC and PCM_CLK serve as output signals only.
3. It is recommended to pull up PCIE_CLKREQ and PCIE_WAKE to VDD_EXT.

The following figure shows a reference design for WLAN and Bluetooth interface application. For more details, please contact Wireless Mobility Technical Support.

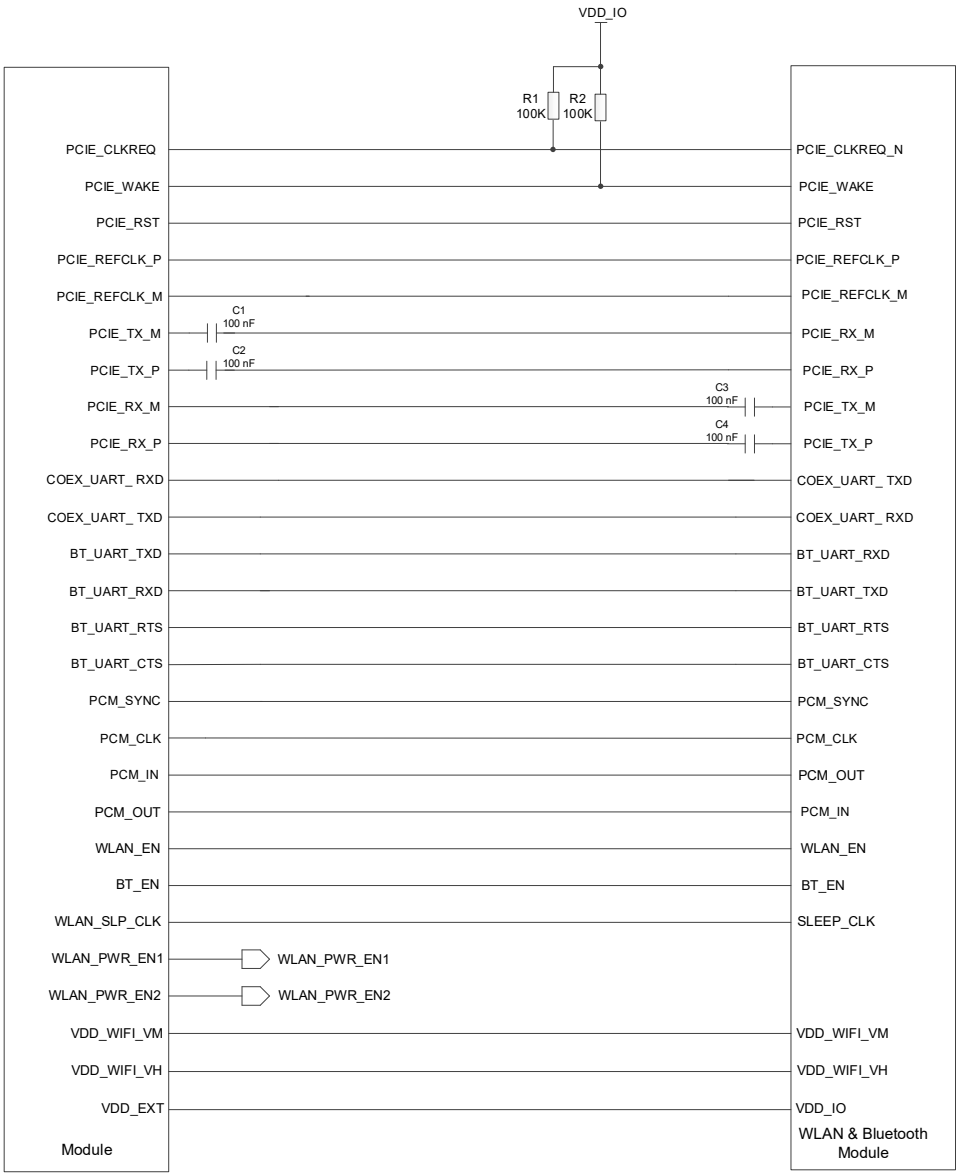


Figure 28: Reference Circuit for Connection with WLAN & Bluetooth Module

To ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the module, and C3 and C4 should be placed close to the WLAN & Bluetooth module. The extra stubs of trace must be as short as possible.

To meet PCIe Gen 2 specifications, the following principles of PCIe interface design should be complied with.

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. And the differential impedance is 95 Ω ±10 %.
- The length of each trace in PCIE_TX, PCIE_RX and PCIE_REFCLK differential pairs should be less than 270 mm, and the length matching of each differential pair should be less than 0.7 mm (5 ps).
- Keep the spacing between Tx and Rx pairs at least 3 times trace width, and the spacing between

Tx/Rx pairs and other signal traces at least 4 times trace width.

- Do not route PCIe signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the PCIe differential traces in inner-layer with ground planes above and below.

4.20. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 28: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	247	General purpose ADC interface
ADC1	245	General purpose ADC interface
ADC2 错误!未定义书签。	139	General purpose ADC interface

The voltage value on ADC pins can be read via **AT+QADC=<port>**, through setting **<port>** into 0, 1 or 2. For more details about the AT command, please contact Wireless Mobility Technical Support.

ADC related API can also read the voltage value of ADC. For more details, please contact Wireless Mobility Technical Support.

The following table describes the characteristic of ADC interfaces.

Table 29: Characteristic of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V
ADC1 Voltage Range	0	-	1.875	V
ADC Resolution	-	14	-	bits
ADC Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

4.21. USB_BOOT Interface

The module provides a USB_BOOT for forced download. Pulling up the USB_BOOT to VDD_EXT before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 30: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	83	DI	Force the module into download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

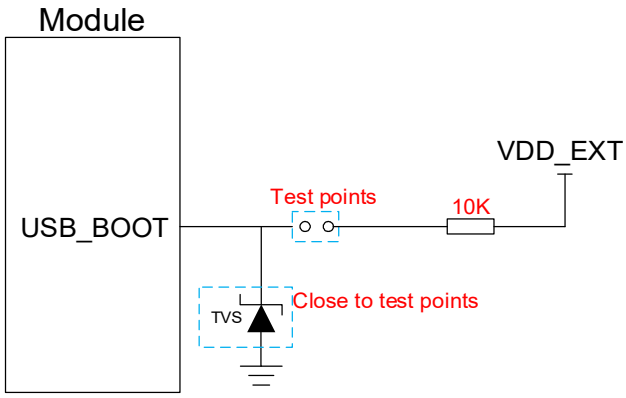


Figure 29: Reference Circuit of USB_BOOT Interface

4.22. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC

is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not be maintained.

Table 31: RTC Performance Specification

Parameter	Test Condition	Max.	Unit
Accuracy	Power on	24	ppm
	Power down, but with power supply connected	200	ppm

4.23. GPIO Interfaces

The module provides 8 GPIOs.

Table 32: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Configurable Function	Comment
GPIO1	100	DI	WAKEUP_IN	This pin is used as WAKEUP_IN by default to control the module entering/exiting the low power mode. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO	General-purpose input/output
GPIO2	101	DIO	GPIO	General-purpose input/output
GPIO3	102	DO	SLEEP_SYS_IND	Used as SLEEP_SYS_IND by default to indicate the low power mode of the module. If the default function is not used, it can be configured to GPIO.
		DIO	GPIO	General-purpose input/output
GPIO4	104	DIO	GPIO	General-purpose input/output
GPIO5	116	DIO	GPIO	
GPIO6	243	DIO	GPIO	
GPIO7	246	DIO	GPIO	
GPIO8	249	DO	GPIO	General-purpose input/output

GPIO9 [16]	264	DIO	GPIO	General-purpose input/output
GPIO10 [16]	267	DIO	GPIO	
GPIO11 [16]	289	DIO	GPIO	

4.24. Audio Interface (Optional)

The module is designed with an optional built-in audio codec to enable analog audio function. The following table shows the pin definition of analog audio interface.

Table 33: Pin Definition of Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	2	AI	Microphone input channel 1 (+)	Analog audio interface is optional, and is not supported by default. SPK signals are used for headset application. If unused, keep these pins open.
MIC1_N	1	AI	Microphone input channel 1 (-)	
MIC2_P	5	AI	Microphone input channel 2 (+)	
MIC2_N	4	AI	Microphone input channel 2 (-)	
MICBIAS	3	PO	Bias voltage output for microphone	
SPK1_P	268	AO	Earphone analog output 1 (-)	
SPK1_N	266	AO	Earphone analog output 1 (-)	
SPK2_P	269	AO	Earphone analog output 2 (+)	
SPK2_N	270	AO	Earphone analog output 2 (-)	
AGND	6	-	Analog ground	Connect it to GND or keep it open if unused.

NOTE

1. The built-in codec uses the same signals as the module's I2C interface (pins 79, 80) and I2S interface (pins 261, 262, 263, 265) for external digital audio design. Therefore, when the built-in codec is utilized, the module's I2S interface cannot be used for other purposes (that is, keep pins 261, 262, 263 and 265 unconnected).

[16] GPIO9, GPIO10, GPIO11 are not supported by default.

2. Connect AGND of the analog audio interface to the main ground through a 0 Ω resistor.
3. The built-in audio codec (analog audio function) is optional.

5 GNSS Receiver (Optional)

5.1. General Description

The module includes a fully integrated dual-band, multi-constellation GNSS solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1–10 Hz (1 Hz by default) data update rate via USB interface.

By default, GNSS engine of the module is switched off. It has to be switched on via API. For more details about GNSS engine technology and configurations, please contact Wireless Mobility Technical Support.

5.2. GNSS Performance

The module's internal GNSS path does not include an external LNA (eLNA), so an active GNSS antenna with an LNA must be used.

The GNSS performance of the module is shown in the table below. The sensitivity test environment: an eLNA with approximately 18 dB gain is used outside the test instrument.

Table 34: WMC529R Series GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF	Cold start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s

	Warm start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
	Hot start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (the module lost lock 3 times in 5 minutes for 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

6 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides three antenna interfaces, include main antenna, diversity antenna [17] and GNSS antenna, and the impedance of antenna ports is 50 Ω.

6.1. Cellular Antenna Interface

6.1.1. Pin Definition

The pin definition of main, diversity antenna interfaces is shown below.

Table 35: Pin Definition of Main/ Diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	143	AIO	Main antenna interface	50 Ω impedance
ANT_DIV	170	AI	Diversity antenna interface	

6.1.2. Operating Frequency

Table 36: WMC529R-EUAQB Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz

[17] The diversity antenna is used to resist the fall of signals caused by high-speed movement and multipath effect.

WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B28A	703–733	758–788	MHz

Table 37: WMC529R-NAAQ Operating Frequencies

3GPP Band	Transmit	Receive	Unit
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B14	788–798	758–768	MHz
LTE-FDD B17	704–716	734–746	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz

Table 38: WMC529R-ROWAQ Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz

LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B28A	703–733	758–788	MHz
LTE-FDD B28B	718–748	773–803	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 39: WMC529R-INAQ Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

Table 40: WMC529R-ROWAQ&INAQ Operating Frequencies

3GPP Band	Transmit	Receive	Unit

EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B8	880–915	925–960	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B28A	703–733	758–788	MHz
LTE-FDD B28B	718–748	773–803	MHz
LTE-TDD B40 (optional)	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

6.1.3. Reference Design

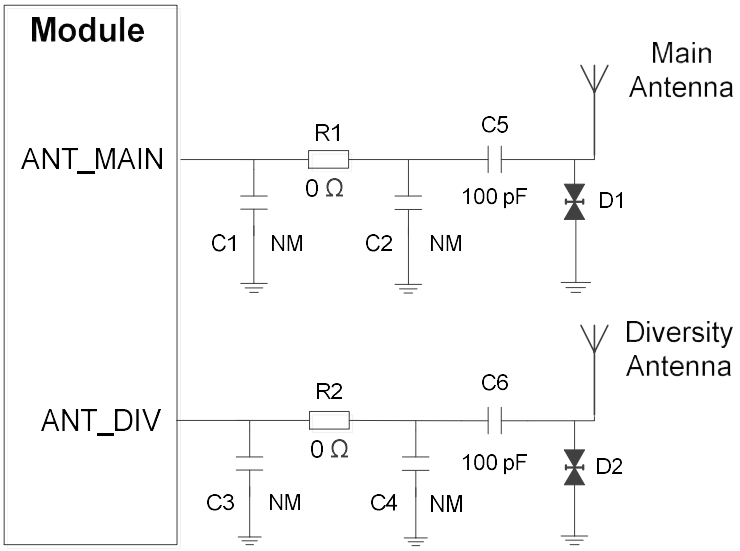


Figure 30: Reference Design of Main Antenna and Diversity Antenna

NOTE

1. Keep a proper distance between the main antenna, diversity antennas to improve receiving sensitivity.
2. Junction capacitance of ESD protection components on the antenna interface is recommended to be 0.05 pF.
3. Use a dual L-type matching circuit for each antenna interface to improve RF performance and facilitate debugging.
4. C1–C4 capacitors are not mounted by default.
5. Place the dual L-type matching components (R1/C1/C2C5 and R2/C3/C4/C6) as close to antennas as possible.
6. C5 and C6 are used for DC-blocking and the capacitance value is recommended to be 100 pF.

6.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 39: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	GNSS-L1 (MHz)	Description	Comment
ANT_GNSS	197	AI	1575.42	GNSS antenna interface	50 Ω impedance

Table 40: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023 (L1)	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046 (E1)	MHz
BDS	1561.098 ±2.046(B1I) 1575.42 ±16.368 (B1C)	MHz
QZSS	1575.42 (L1)	MHz

A reference design of GNSS antenna is shown as below.

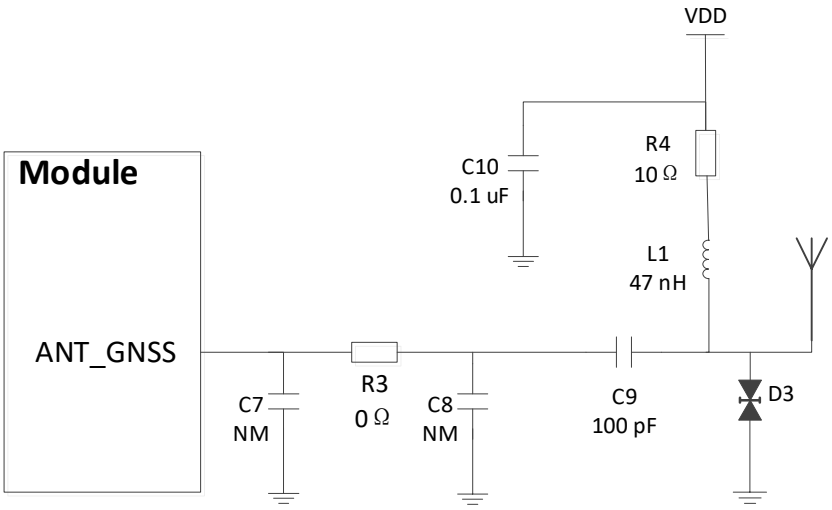


Figure 31: Reference Design of GNSS Antenna

NOTE

1. GNSS is an optional function. If GNSS function is not used, keep ANT_GNSS unconnected.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. C9 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements.
4. Junction capacitance of ESD protection components on the antenna interface is recommended to be 0.05 pF.
5. It is recommended to add a 25 dB notch filter at the LNA input end of the active antenna when LTE B13 or B14 is supported.

6.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

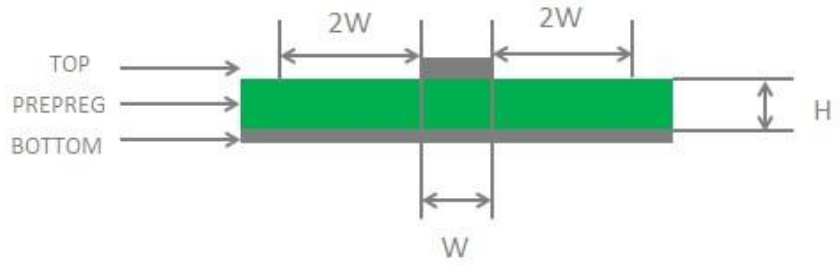


Figure 32: Microstrip Design on a 2-layer PCB

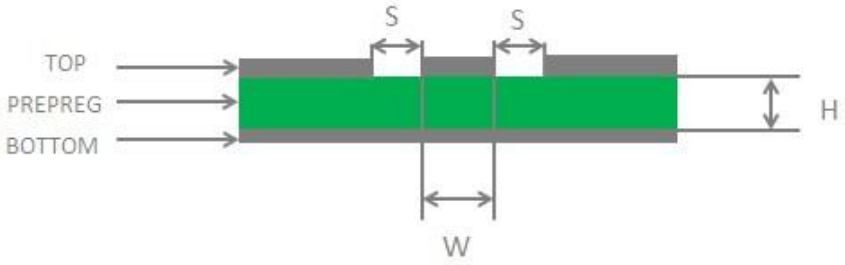


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

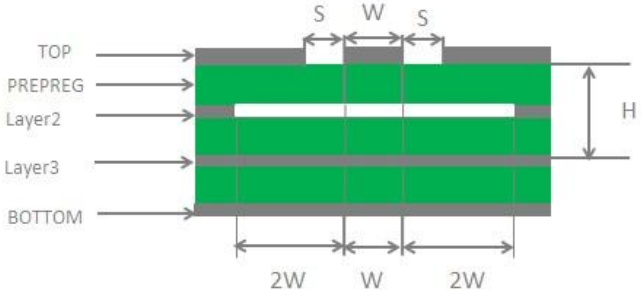


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

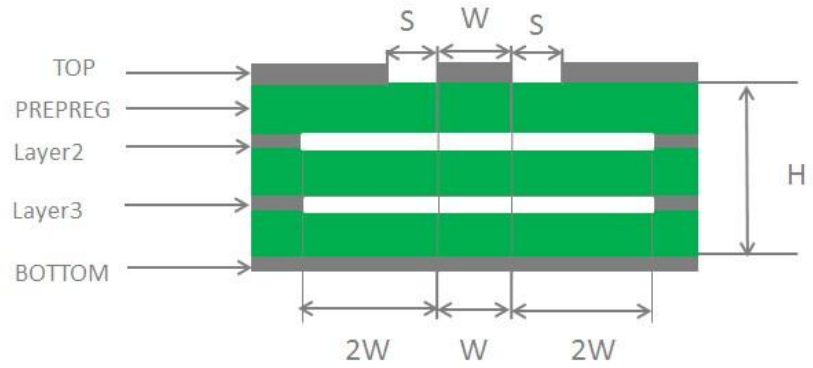


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice as wide as RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please contact Wireless Mobility Technical Support.

6.4. Antenna Design Requirements

The following table shows the requirements on main antenna, diversity antenna and GNSS antenna.

Table 41: Antenna Design Requirements

Type	Requirements
GNSS	Frequency range: 1559–1606 MHz Polarization: RHCP VSWR: ≤ 2 (Typ.) Antenna gain: > 0 dBi Active antenna embedded LNA noise coefficient: < 1.5 dB Active antenna embedded LNA gain: see **NOTE 3** & **NOTE 4** below for design considerations
GSM/UMTS/LTE	VSWR: ≤ 2 Efficiency: > 30 % Input impedance: 50 Ω Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

1. Antenna isolation:
   > 20 dB @ above 1000 MHz;
   > 15 dB @ 600–1000 MHz;
   > 10 dB @ 400–600 MHz.
2. The isolation between each antenna traces on PCB is recommended to be over 75 dB.
3. GNSS receiver is designed to work with an external LNA (eLNA) in range of 18–20 dB. That is, ensure that the total gain from eLNA to the module (including external active antenna, cable loss, connectors, PCB traces, and attenuator) meets 18–20 dB.
4. Attenuator (π-type attenuation circuit) can be used when the total gain exceeds 20 dB.
5. Maximize the distance among GNSS antenna, main antenna, diversity antenna.

6.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

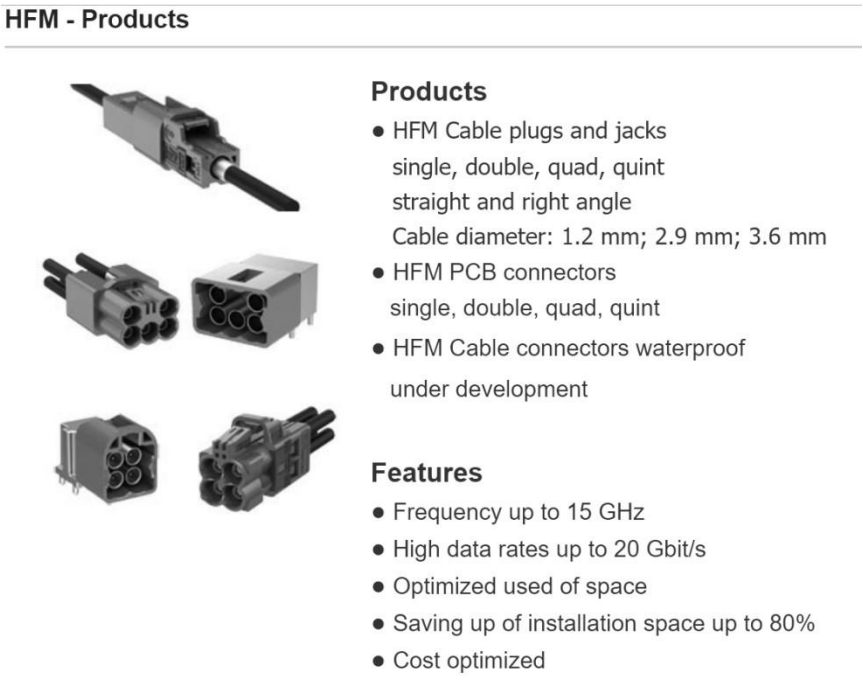


Figure 36: Description of the HFM Connector

For more details, visit https://www.rosenbergerap.com.

7 Reliability, Radio and Electrical Characteristics

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 42: **Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.0	A
Voltage at Digital Pins	-0.3	2.04	V
Voltage at ADC0	0	1.91	V
Voltage at ADC1	0	1.91	V

7.2. Power Supply Ratings

Table 43: **Power Supply Ratings**

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	VBAT_RF		3.3/3.7 [18]	3.8	4.3	V
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

7.3. Operating and Storage Temperatures

Table 44: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [19]	-35	+25	+75	ºC
Extended Temperature Range [20]	-40	-	+85	ºC
eCall Temperature Range [21]	-40	-	+95	ºC
Storage Temperature Range	-40	-	+95	ºC

[18] The minimum input voltage of WMC529R-EUAQB and WMC529R-ROWAQ is 3.7 V, while the minimum input voltage of WMC529R-NAAQ is 3.3 V.
[19] Within this range, the module's indicators comply with 3GPP specification requirements.
[20] Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and eCall, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.
[21] Within this range, the eCall function must remain operational. The module triggers thermal management mechanisms at high temperatures, such as power reduction or throughput decrease, to ensure normal eCall operation even at temperatures up to 95 °C.

7.4. Power Consumption

Table 45: WMC529R-EUAQB Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	0.035	mA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
	EGSM900 @ DRX = 2 (USB disconnected)	3.189	mA
	EGSM900 @ DRX = 5 (USB disconnected)	2.237	mA
	EGSM900 @ DRX = 5 (USB suspend)	3.757	mA
	EGSM900 @ DRX = 9 (USB disconnected)	2.689	mA
	DCS1800 @ DRX = 2 (USB disconnected)	3.191	mA
	DCS1800 @ DRX = 5 (USB disconnected)	2.288	mA
	DCS1800 @ DRX = 5 (USB suspend)	3.750	mA
	DCS1800 @ DRX = 9 (USB disconnected)	3.377	mA
	WCDMA @ PF = 64 (USB disconnected)	2.713	mA
	WCDMA @ PF = 64 (USB suspend)	4.085	mA
	WCDMA @ PF = 128 (USB disconnected)	2.228	mA
	WCDMA @ PF = 256 (USB disconnected)	2.050	mA
	WCDMA @ PF = 512 (USB disconnected)	1.398	mA
	LTE-FDD @ PF = 32 (USB disconnected)	4.248	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.848	mA
	LTE-FDD @ PF = 64 (USB suspend)	4.273	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.276	mA
	LTE-FDD @ PF = 256 (USB disconnected)	2.183	mA
Idle state	EGSM900 @ DRX = 5 (USB connected)	15.91	mA

	EGSM900 @ DRX = 5 (USB disconnected)	33.12	mA
	WCDMA @ PF = 64 (USB connected)	15.97	mA
	WCDMA @ PF = 64 (USB disconnected)	42.96	mA
	LTE-FDD @ PF = 64 (USB connected)	16.29	mA
	LTE-FDD @ PF = 64 (USB disconnected)	43.90	mA
GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 33 dBm	338.90	mA
	EGSM900 3DL/2UL @ 32 dBm	562.80	mA
	EGSM900 2DL/3UL @ 30 dBm	689.70	mA
	EGSM900 1DL/4UL @ 29 dBm	761.20	mA
	DCS1800 4DL/1UL @ 29.5 dBm	216.30	mA
	DCS1800 3DL/2UL @ 29.0 dBm	321.60	mA
	DCS1800 2DL/3UL @ 26.5 dBm	370.90	mA
	DCS1800 1DL/4UL @ 25.5 dBm	537.90	mA
EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 27.0 dBm	233.30	mA
	EGSM900 3DL/2UL @ 26.0 dBm	365.20	mA
	EGSM900 2DL/3UL @ 24.0 dBm	422.20	mA
	EGSM900 1DL/4UL @ 23.0 dBm	493.70	mA
	DCS1800 4DL/1UL @ 26.0 dBm	163.70	mA
	DCS1800 3DL/2UL @ 25.0 dBm	225.90	mA
	DCS1800 2DL/3UL @ 23.0 dBm	265.90	mA
	DCS1800 1DL/4UL @ 22.0 dBm	368.80	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @ 22.0 dBm	642.00	mA
	WCDMA B8 HSDPA @ 22.5 dBm	628.00	mA
	WCDMA B1 HSUPA @ 22.5 dBm	651.00	mA
	WCDMA B8 HSUPA @ 22.5 dBm	637.00	mA

LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 23.0 dBm	658.00	mA
	LTE-FDD B3 @ 23.0 dBm	593.00	mA
	LTE-FDD B7 @ 23.0 dBm	670.00	mA
	LTE-FDD B8 @ 23.0 dBm	636.00	mA
	LTE-FDD B20 @ 23.0 dBm	648.00	mA
	LTE-FDD B28A @ 23.0 dBm	636.00	mA
GSM voice call	EGSM900, PCL = 5 @ 33 dBm	368.00	mA
	EGSM900, PCL = 12 @ 19.0 dBm	154.90	mA
	EGSM900, PCL = 19 @ 5.0 dBm	110.80	mA
	DCS1800, PCL = 0 @ 29.5 dBm	227.20	mA
	DCS1800, PCL = 7 @ 16.0 dBm	128.70	mA
WCDMA voice call	WCDMA B1 @ 23 dBm	676.00	mA
	WCDMA B8 @ 23 dBm	654.00	mA

Table 46: WMC529R-NAAQ Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	mA
Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
Idle state	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA

LTE data transfer (GNSS OFF)	LTE-FDD B2 @ 23.0 dBm	TBD	mA
	LTE-FDD B4 @ 23.0 dBm	TBD	mA
	LTE-FDD B5 @ 23.0 dBm	TBD	mA
	LTE-FDD B7 @ 23.0 dBm	TBD	mA
	LTE-FDD B12 @ 23.0 dBm	TBD	mA
	LTE-FDD B13 @ 23.0 dBm	TBD	mA
	LTE-FDD B14 @ 23.0 dBm	TBD	mA
	LTE-FDD B17 @ 23.0 dBm	TBD	mA
	LTE-FDD B66 @ 23.0 dBm	TBD	mA

Table 47: WMC529R-ROWAQ Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	mA
Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
	WCDMA @ PF = 64 (USB disconnected)	TBD	mA
	WCDMA @ PF = 64 (USB suspend)	TBD	mA
	WCDMA @ PF = 128 (USB disconnected)	TBD	mA
	WCDMA @ PF = 256 (USB disconnected)	TBD	mA
	WCDMA @ PF = 512 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 32 (USB disconnected)	TBD	mA

	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-TDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 256 (USB disconnected)	TBD	mA
Idle state	WCDMA @ PF = 64 (USB connected)	TBD	mA
	WCDMA @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB connected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @ 22.0 dBm	TBD	mA
	WCDMA B8 HSDPA @ 22.5 dBm	TBD	mA
	WCDMA B1 HSUPA @ 22.5 dBm	TBD	mA
	WCDMA B8 HSUPA @ 22.5 dBm	TBD	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 23.0 dBm	TBD	mA
	LTE-FDD B3 @ 23.0 dBm	TBD	mA
	LTE-FDD B5 @ 23.0 dBm	TBD	mA
	LTE-FDD B7 @ 23.0 dBm	TBD	mA
	LTE-FDD B8 @ 23.0 dBm	TBD	mA
	LTE-FDD B18@ 23.0 dBm	TBD	mA
	LTE-FDD B19@ 23.0 dBm	TBD	mA
	LTE-FDD B28A @ 23.0 dBm	TBD	mA
	LTE-FDD B28B @ 23.0 dBm	TBD	mA
	LTE-TDD B41 @ 23.0 dBm	TBD	mA
WCDMA voice call	WCDMA B1 @ 23 dBm	TBD	mA

	WCDMA B8 @ 23 dBm	TBD	mA

Table 48: WMC529R-INAQ Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	mA
	AT+CFUN=0 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 2 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB suspend)	TBD	mA
	EGSM900 @ DRX = 9 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 2 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB suspend)	TBD	mA
	DCS1800 @ DRX = 9 (USB disconnected)	TBD	mA
Sleep state	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-TDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 256 (USB disconnected)	TBD	mA
Idle state	EGSM900 @ DRX = 5 (USB connected)	TBD	mA

	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB connected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 33 dBm	TBD	mA
	EGSM900 3DL/2UL @ 32 dBm	TBD	mA
	EGSM900 2DL/3UL @ 30 dBm	TBD	mA
	EGSM900 1DL/4UL @ 29 dBm	TBD	mA
	DCS1800 4DL/1UL @ 29.5 dBm	TBD	mA
	DCS1800 3DL/2UL @ 29.0 dBm	TBD	mA
	DCS1800 2DL/3UL @ 26.5 dBm	TBD	mA
	DCS1800 1DL/4UL @ 25.5 dBm	TBD	mA
EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 27.0 dBm	TBD	mA
	EGSM900 3DL/2UL @ 26.0 dBm	TBD	mA
	EGSM900 2DL/3UL @ 24.0 dBm	TBD	mA
	EGSM900 1DL/4UL @ 23.0 dBm	TBD	mA
	DCS1800 4DL/1UL @ 26.0 dBm	TBD	mA
	DCS1800 3DL/2UL @ 25.0 dBm	TBD	mA
	DCS1800 2DL/3UL @ 23.0 dBm	TBD	mA
	DCS1800 1DL/4UL @ 22.0 dBm	TBD	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 23.0 dBm	TBD	mA
	LTE-FDD B3 @ 23.0 dBm	TBD	mA
	LTE-FDD B5 @ 23.0 dBm	TBD	mA
	LTE-FDD B8 @ 23.0 dBm	TBD	mA

	LTE-TDD B40 @ 23.0 dBm	TBD	mA
	LTE-TDD B41 @ 23.0 dBm	TBD	mA
GSM voice call	EGSM900, PCL = 5 @ 33 dBm	TBD	mA
	EGSM900, PCL = 12 @ 19.0 dBm	TBD	mA
	EGSM900, PCL = 19 @ 5.0 dBm	TBD	mA
	DCS1800, PCL = 0 @ 29.5 dBm	TBD	mA
	DCS1800, PCL = 7 @ 16.0 dBm	TBD	mA
	DCS1800, PCL = 15 @ 0 dBm	TBD	mA

Table 49: WMC529R-ROWAQ&INAQ Power Consumption (25 °C, 3.8 V Power Supply)

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	mA
Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 2 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB suspend)	TBD	mA
	EGSM900 @ DRX = 9 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 2 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB suspend)	TBD	mA
	DCS1800 @ DRX = 9 (USB disconnected)	TBD	mA
	WCDMA @ PF = 64 (USB disconnected)	TBD	mA
	WCDMA @ PF = 64 (USB suspend)	TBD	mA
	WCDMA @ PF = 128 (USB disconnected)	TBD	mA
	WCDMA @ PF = 256 (USB disconnected)	TBD	mA

	WCDMA @ PF = 512 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-TDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 256 (USB disconnected)	TBD	mA
Idle state	EGSM900 @ DRX = 5 (USB connected)	TBD	mA
	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	WCDMA @ PF = 64 (USB connected)	TBD	mA
	WCDMA @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-TDD @ PF = 64 (USB connected)	TBD	mA
	LTE-TDD @ PF = 64 (USB disconnected)	TBD	mA
GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 33 dBm	TBD	mA
	EGSM900 3DL/2UL @ 32 dBm	TBD	mA
	EGSM900 2DL/3UL @ 30 dBm	TBD	mA
	EGSM900 1DL/4UL @ 29 dBm	TBD	mA
	DCS1800 4DL/1UL @ 29.5 dBm	TBD	mA
	DCS1800 3DL/2UL @ 29.0 dBm	TBD	mA

	DCS1800 2DL/3UL @ 26.5 dBm	TBD	mA
	DCS1800 1DL/4UL @ 25.5 dBm	TBD	mA
EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @ 27.0 dBm	TBD	mA
	EGSM900 3DL/2UL @ 26.0 dBm	TBD	mA
	EGSM900 2DL/3UL @ 24.0 dBm	TBD	mA
	EGSM900 1DL/4UL @ 23.0 dBm	TBD	mA
	DCS1800 4DL/1UL @ 26.0 dBm	TBD	mA
	DCS1800 3DL/2UL @ 25.0 dBm	TBD	mA
	DCS1800 2DL/3UL @ 23.0 dBm	TBD	mA
	DCS1800 1DL/4UL @ 22.0 dBm	TBD	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @ 22.0 dBm	TBD	mA
	WCDMA B8 HSDPA @ 22.5 dBm	TBD	mA
	WCDMA B1 HSUPA @ 22.5 dBm	TBD	mA
	WCDMA B8 HSUPA @ 22.5 dBm	TBD	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @ 23.0 dBm	TBD	mA
	LTE-FDD B3 @ 23.0 dBm	TBD	mA
	LTE-FDD B5 @ 23.0 dBm	TBD	mA
	LTE-FDD B7 @ 23.0 dBm	TBD	mA
	LTE-FDD B8 @ 23.0 dBm	TBD	mA
	LTE-FDD B18@ 23.0 dBm	TBD	mA
	LTE-FDD B19@ 23.0 dBm	TBD	mA
	LTE-FDD B28A @ 23.0 dBm	TBD	mA
	LTE-FDD B28B @ 23.0 dBm	TBD	mA
	LTE-TDD B40 (optional) @ 23.0 dBm	TBD	mA
	LTE-TDD B41 @ 23.0 dBm	TBD	mA

GSM voice call	EGSM900, PCL = 5 @ 33 dBm	TBD	mA
	EGSM900, PCL = 12 @ 19.0 dBm	TBD	mA
	EGSM900, PCL = 19 @ 5.0 dBm	TBD	mA
	DCS1800, PCL = 0 @ 29.5 dBm	TBD	mA
	DCS1800, PCL = 7 @ 16.0 dBm	TBD	mA
	DCS1800, PCL = 15 @ 0 dBm	TBD	mA
WCDMA voice call	WCDMA B1 @ 23 dBm	TBD	mA
	WCDMA B8 @ 23 dBm	TBD	mA

NOTE

1. Power consumption test is carried out under 3.8 V, 25 °C.
2. The above power consumption data are all tested with the GNSS OFF by default.
3. The data of maximum throughput are tested at the condition of maximum power.
4. The above power consumption data are for reference only, which may vary among different modules. For more details about the power consumption of other module models, please consult Wireless Mobility Technical Support for power consumption test report.

7.5. Tx Power

The following table shows the RF output power of the module.

Table 48: WMC529R-EUAQB Tx Power (25 °C, 3.8 V Power Supply)

Frequency Bands	Max. Tx Power	Min. Tx Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA B1	23 dBm ±2 dB	< -49 dBm
WCDMA B8	23 dBm ±2 dB	< -49 dBm

LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-FDD B20	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28A	23 dBm ±2 dB	< -39 dBm

Table 49: WMC529R-NAAQ Tx Power (25 °C, 3.8 V Power Supply)

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE-FDD B2	23 dBm ±2 dB	< -39 dBm
LTE-FDD B4	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B12	23 dBm ±2 dB	< -39 dBm
LTE-FDD B13	23 dBm ±2 dB	< -39 dBm
LTE-FDD B14	23 dBm ±2 dB	< -39 dBm
LTE-FDD B17	23 dBm ±2 dB	< -39 dBm
LTE-FDD B66	23 dBm ±2 dB	< -39 dBm

Table 50: WMC529R-ROWAQ Tx Power (25 °C, 3.8 V Power Supply)

Frequency Bands	Max. Tx Power	Min. Tx Power
WCDMA B1	23 dBm ±2 dB	< -49 dBm
WCDMA B8	23 dBm ±2 dB	< -49 dBm
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm

LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-FDD B18	23 dBm ±2 dB	< -39 dBm
LTE-FDD B19	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28A	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28B	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

Table 51: WMC529R-INAQ Tx Power (25 °C, 3.8 V Power Supply)

Frequency Bands	Max. Tx Power	Min. Tx Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

Table 52: WMC529R-ROWAQ&INAQ Tx Power (25 °C, 3.8 V Power Supply)

Frequency Bands	Max. Tx Power	Min. Tx Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA B1	23 dBm ±2 dB	< -49 dBm

WCDMA B8	23 dBm ±2 dB	< -49 dBm
LTE-FDD B1	23 dBm ±2 dB	< -39 dBm
LTE-FDD B3	23 dBm ±2 dB	< -39 dBm
LTE-FDD B5	23 dBm ±2 dB	< -39 dBm
LTE-FDD B7	23 dBm ±2 dB	< -39 dBm
LTE-FDD B8	23 dBm ±2 dB	< -39 dBm
LTE-FDD B18	23 dBm ±2 dB	< -39 dBm
LTE-FDD B19	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28A	23 dBm ±2 dB	< -39 dBm
LTE-FDD B28B	23 dBm ±2 dB	< -39 dBm
LTE-TDD B40 (optional)	23 dBm ±2 dB	< -39 dBm
LTE-TDD B41	23 dBm ±2 dB	< -39 dBm

NOTE

1. For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***.
2. WCDMA maximum output power conforms to *3GPP TS 34.121-1* requirements.
3. LTE maximum output power conforms to *3GPP TS 36.521-1* requirements and the module is tested @ BW = 10 MHz, 1RB.

7.6. Rx Sensitivity

Table 53: WMC529R-EUAQB RF Receiving Sensitivity (dBm) (25 °C, 3.8 V Power Supply)

Frequency Bands	SIMO			3GPP (SIMO)
	Max. (Worst Case)	Typ.	Min. (Best Case)	
EGSM900 (1RX)	-104	-107	-108.5	-102
DCS1800 (1RX)	-104	-107	-108.5	-102
WCDMA B1 (1RX)	-108.7	-109	-111.3	-106.7
WCDMA B8 (1RX)	-105.7	-109	-114.3	-103.7
LTE-FDD B1 (10 MHz)	-98.3	-100.3	-101.3	-96.3
LTE-FDD B3 (10 MHz)	-95.3	-97.3	-99.9	-93.3
LTE-FDD B7 (10 MHz)	-96.3	-98.3	-100.2	-94.3
LTE-FDD B8 (10 MHz)	-95.3	-97.3	-102.4	-93.3
LTE-FDD B20 (10 MHz)	-95.3	-96.3	-102.3	-93.3
LTE-FDD B28A (10 MHz)	-96.8	-97.8	-103.1	-94.8

Table 54: WMC529R-NAAQ RF Receiving Sensitivity (dBm) (25 °C, 3.8 V Power Supply)

Frequency Bands	SIMO			3GPP (SIMO)
	Max. (Worst Case)	Typ.	Min. (Best Case)	
LTE-FDD B2	TBD	TBD	TBD	TBD
LTE-FDD B4	TBD	TBD	TBD	TBD
LTE-FDD B5	TBD	TBD	TBD	TBD
LTE-FDD B7	TBD	TBD	TBD	TBD
LTE-FDD B12	TBD	TBD	TBD	TBD
LTE-FDD B13	TBD	TBD	TBD	TBD
LTE-FDD B14	TBD	TBD	TBD	TBD
LTE-FDD B17	TBD	TBD	TBD	TBD

LTE-FDD B66	TBD	TBD	TBD	TBD

Table 55: WMC529R-ROWAQ RF Receiving Sensitivity (dBm) (25 °C, 3.8 V Power Supply)

Frequency Bands	SIMO			3GPP (SIMO)
	Max. (Worst Case)	Typ.	Min. (Best Case)	
WCDMA B1 (1RX)	TBD	TBD	TBD	TBD
WCDMA B8 (1RX)	TBD	TBD	TBD	TBD
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B28A (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B28B (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	TBD

Table 56: WMC529R-INAQ RF Receiving Sensitivity (dBm) (25 °C, 3.8 V Power Supply)

Frequency Bands	SIMO			3GPP (SIMO)
	Max. (Worst Case)	Typ.	Min. (Best Case)	
EGSM900 (1RX)	TBD	TBD	TBD	TBD
DCS1800 (1RX)	TBD	TBD	TBD	TBD
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	TBD

LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B40 (10 MHz) (optional)	TBD	TBD	TBD	TBD
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	TBD

Table 57: WMC529R-ROWAQ&INAQ RF Receiving Sensitivity (dBm) (25 °C, 3.8 V Power Supply)

Frequency Bands	SIMO			3GPP (SIMO)
	Max. (Worst Case)	Typ.	Min. (Best Case)	
EGSM900 (1RX)	TBD	TBD	TBD	TBD
DCS1800 (1RX)	TBD	TBD	TBD	TBD
WCDMA B1 (1RX)	TBD	TBD	TBD	TBD
WCDMA B8 (1RX)	TBD	TBD	TBD	TBD
LTE-FDD B1 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B3 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B5 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B7 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B8 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B18 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B19 (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B28A (10 MHz)	TBD	TBD	TBD	TBD
LTE-FDD B28B (10 MHz)	TBD	TBD	TBD	TBD
LTE-TDD B40 (10 MHz) (optional)	TBD	TBD	TBD	TBD
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	TBD

1. GSM sensitivity values meet *3GPP TS 51.010-1* requirements.
2. WCDMA Rx-sensitivity values meet *3GPP TS 34.121-1* requirements.
3. LTE Rx-sensitivity values meet *3GPP TS 36.521-1* requirements and it is tested under BW = 10 MHz according to 3GPP 1 RB configuration.

7.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatic discharge characteristics.

Table 58: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±10	kV
Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

7.8. Thermal Dissipation

The module exhibits the best performance when all internal chips are working within their designated operating temperature ranges. However, if any chip reaches or exceeds its maximum temperature, the module may still work but its performance and functionalities (such as RF output power and data rate) will be compromised. Therefore, the thermal design should be maximally optimized to ensure that all internal chips consistently remain within their recommended operating temperature ranges.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on the PCB motherboard, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper on the backside of the PCB where the module is mounted.

- Follow the principles below when designing the heatsink:
  - It is recommended to integrate the heatsink with the outer shell of telematic control unit (TCU) according to the module's application scenario. This allows for rapid transfer of the heat generated by the module to the outer shell, thus enhancing heat dissipation efficiency and eliminating the need for fixing the heatsink.
  - The entire shell of the TCU or the shell of the area where the module is located must be made of materials with excellent heat dissipation properties. It is recommended to use die-cast aluminum with higher thermal conductivity.
  - Based on the heat dissipation direction of the module, you can choose either of the following optional heatsink installation positions:
    a) The top surface of the module shielding cover;
    b) The bottom surface of the PCBA under the module;
    c) Both the top surface of the module shielding cover and the bottom surface of the PCBA under the module.

    If the heatsink is located only on one side, option a) is recommended; if the situation allows, option c) is recommended.

  - The heatsink must meet the following requirements:
    a) The base plate area of the heatsink should be larger than the module area for full coverage;
    b) Choose a heatsink with adequate fins to ensure effective heat dissipation. The fins should be located within the area where the module is mounted.
  - Since the heatsink is in contact with either the top surface of the shielding cover or the bottom surface of the PCBA through the thermal interface material (TIM), it is necessary to choose a TIM with high thermal conductivity, good flexibility, and good wettability.
  - Fasten the shell (heatsink) with screws around the TCU to prevent the heatsink from falling off during the drop tests, shock and vibration tests, or transportation.
- Implement other auxiliary cooling methods, such as air cooling or liquid cooling.

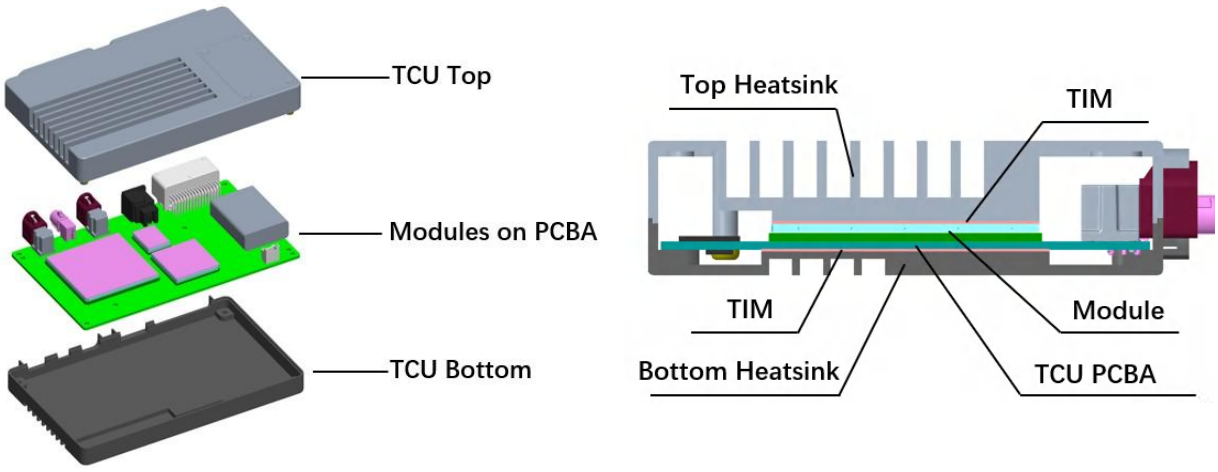


Figure 37: Heatsink Design Example

NOTE

1. The module works normal when the internal BB chip is below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module detaches from the network and enters Limited Service State in which only eCall is available, and it will recover to network connected state after the maximum temperature falls below 90 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. Specified commands can be used to query the current temperature. For details about the command and the detailed information on software thermal management, please contact Wireless Mobility Technical Support.
2. For more detailed introduction on thermal design, please contact Wireless Mobility Technical Support.

8 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

8.1. Mechanical Dimensions

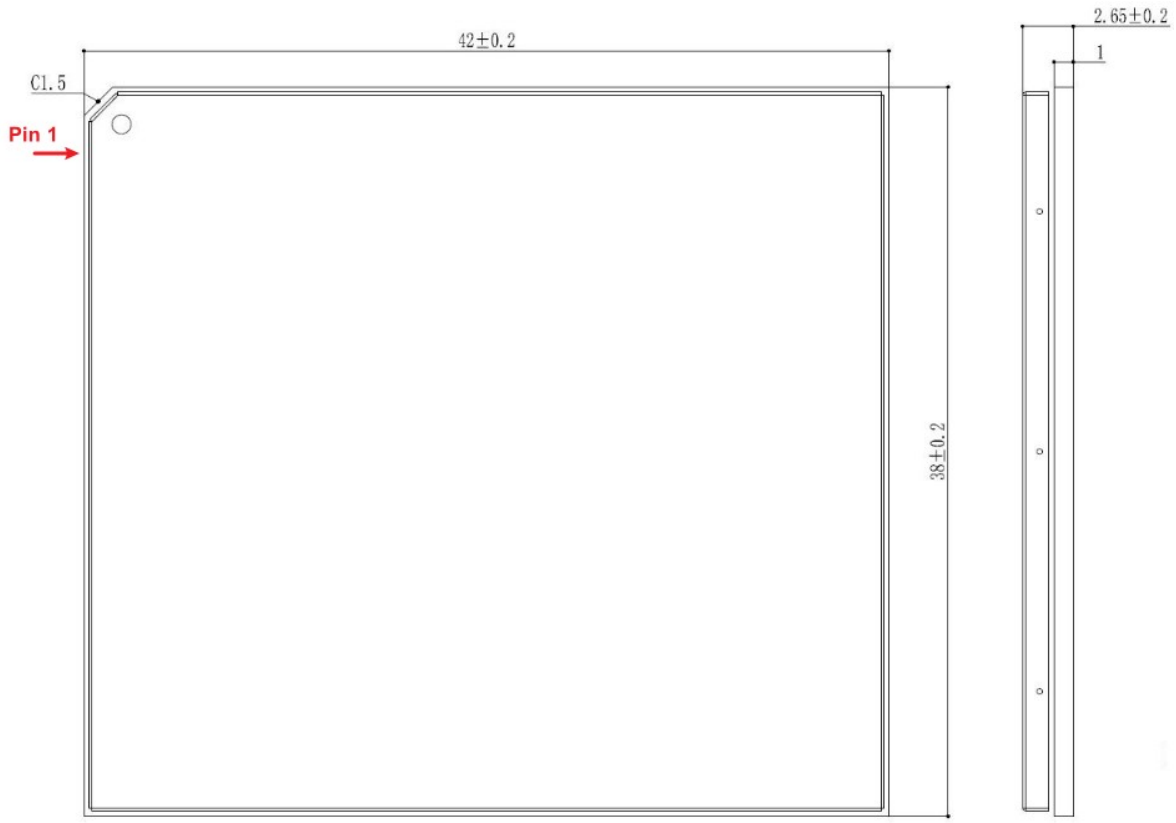


Figure 38: Module Top and Side Dimensions (Unit: mm)

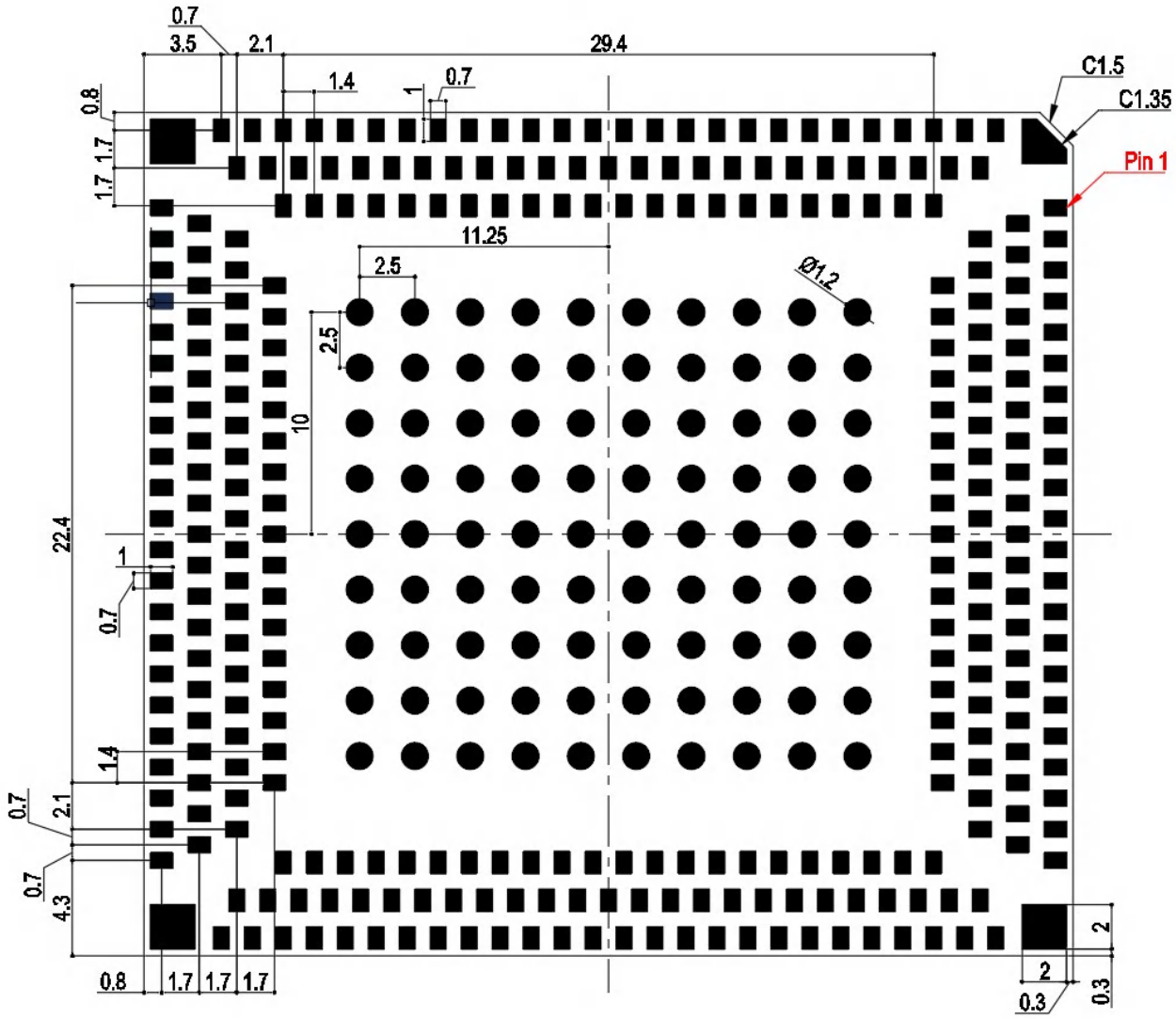


Figure 39: Module Bottom Dimensions (Bottom View) (Unit: mm)

NOTE

The package warpage level of the module refers to *JEITA ED-7306 standard*.

8.2. Recommended Footprint

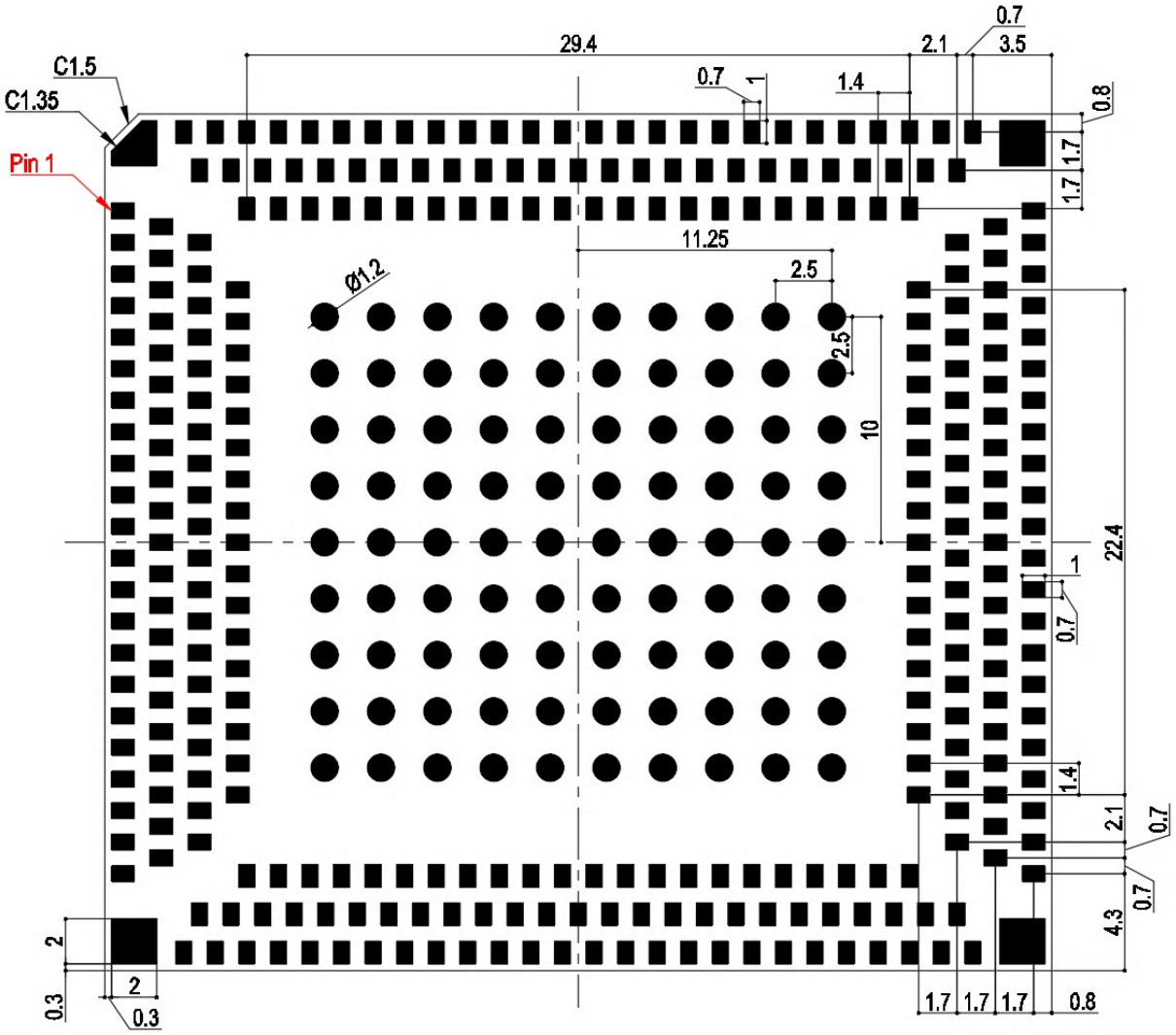


Figure 40: Recommended Footprint (Perspective View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

8.3. Top and Bottom Views

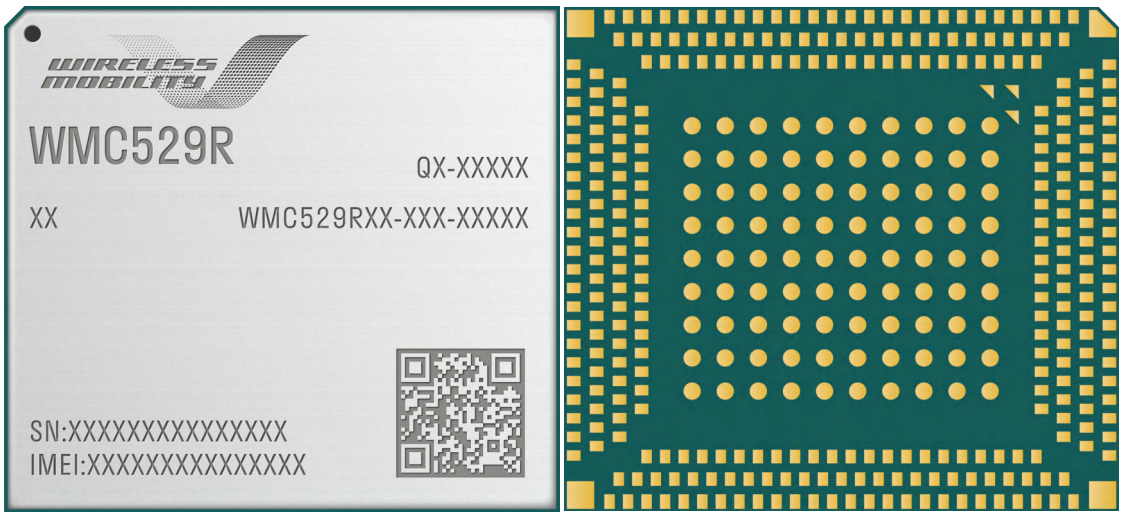


Figure 41: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Wireless Mobility.

9 Storage, Manufacturing and Packaging

9.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [22] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[22] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, please contact Wireless Mobility Technical Support.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

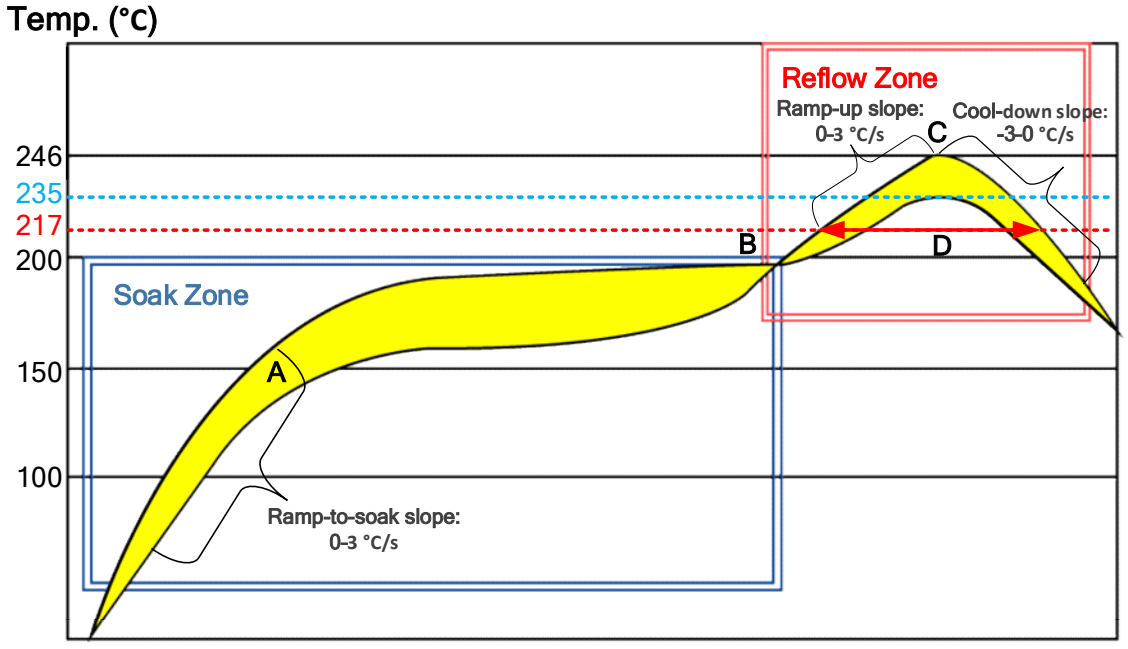


Figure 42: Recommended Reflow Soldering Thermal Profile

Table 59: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s (refer to NOTE 1 below)
Reflow Cycle	
Max reflow cycle	1

NOTE

1. For large-form-factor modules (that is, minimum side length ≥ 30 mm) with two-piece shielding covers, use a cool-down slope of -1~0 °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size form factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact Wireless Mobility Technical Support in

advance for any situation or any process (e.g. selective soldering, ultrasonic soldering) that you are not sure about.

9.3. Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

9.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

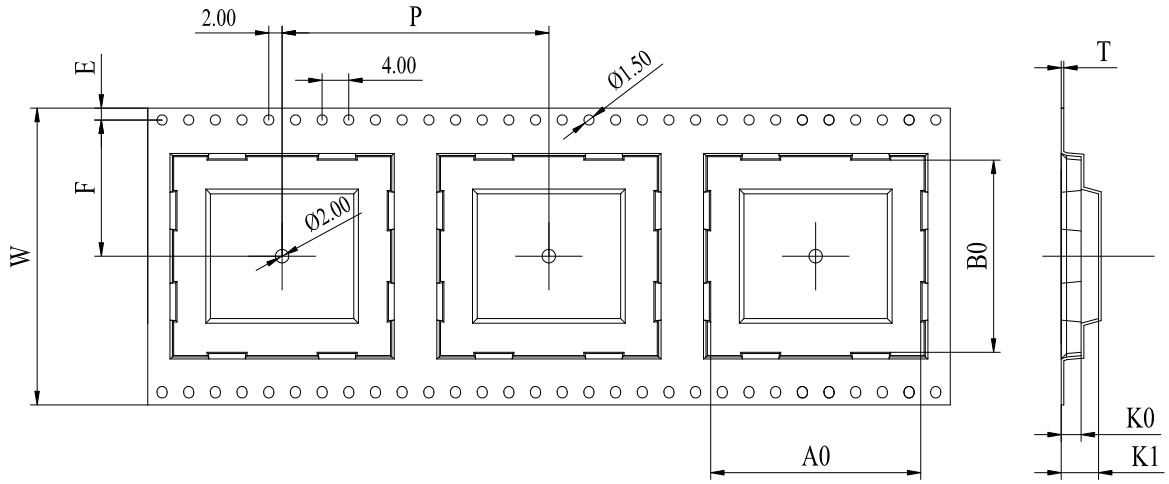


Figure 43: Carrier Tape Dimension Drawing (Unit: mm)

Table 60: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.5	42.5	38.5	4.05	4.65	34.2	1.75

9.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

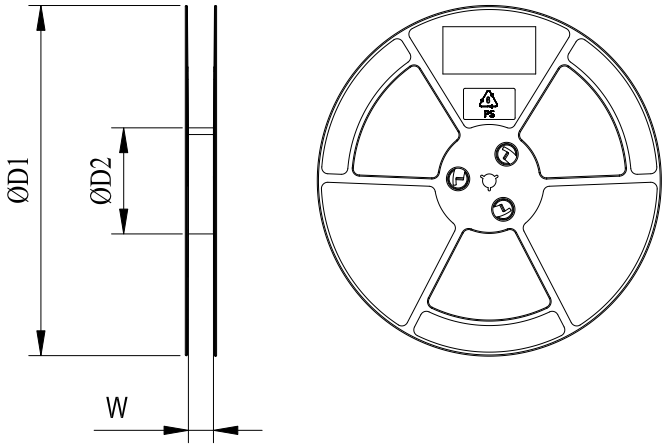


Figure 44: Plastic Reel Dimension Drawing

Table 61: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

9.3.3. Mounting Direction

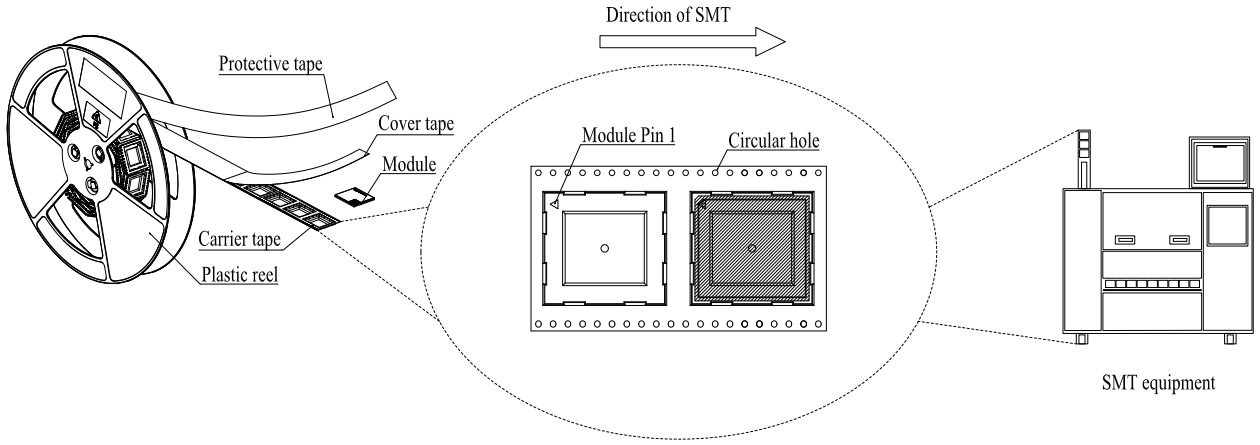
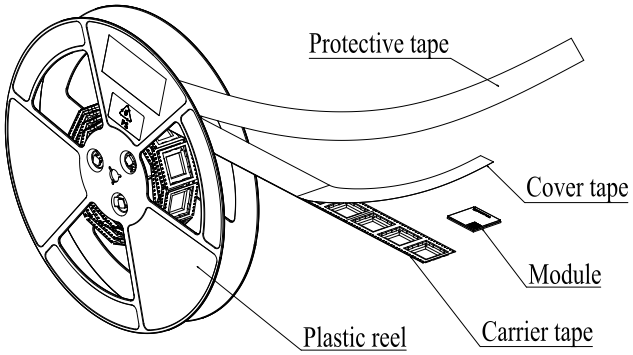


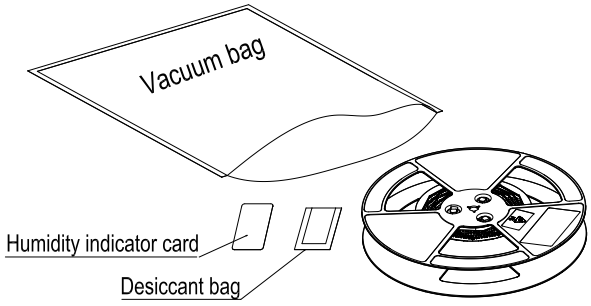
Figure 45: Mounting Direction

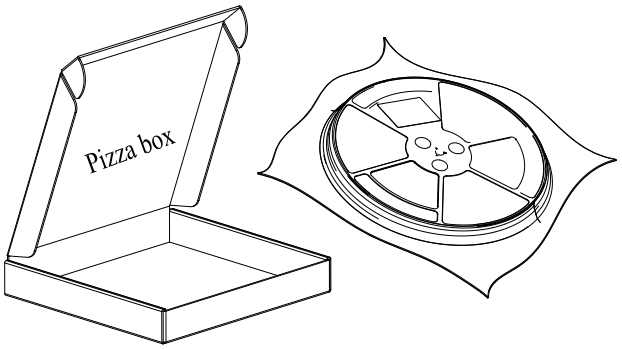
9.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.

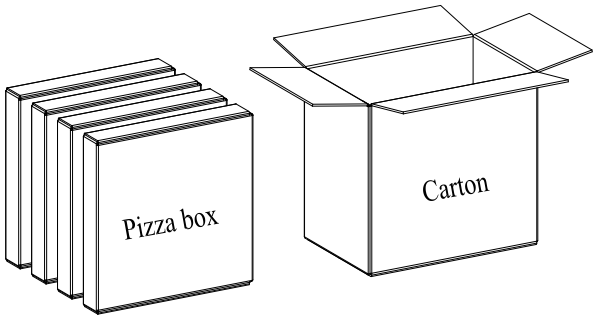


Figure 46: Packaging Process

10 Appendix Reference

Table 62: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
API	Application Program Interface
bps	Bits Per Second
BW	Bandwidth
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying

GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HB	High-Band
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
LB	Low-Band
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LPM	Low Power Mode
LTE	Long Term Evolution
MB	Mid-Band
MDIO	Management Data Input/Output
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMIC	Power Management IC
PPP	Point-to-Point Protocol

QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RB	Resource Block
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage

V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: 2BH2C24WMC529RNAAQ.
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: 2BH2C24WMC529RNAAQ" or "Contains FCC ID: 2BH2C24WMC529RNAAQ" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the

module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN
"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF
L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.
The host product shall be properly labeled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:
"Contains IC: 32403-WMC529RNAAQ" or "where: 32403-WMC529RNAAQ is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 32403-WMC529RNAAQ" ou "où: 32403-WMC529RNAAQ est le numéro de certification du module".