Bluetooth low energy Module

129150

nRF51822 BT4.2 Module

Shenzhen RF-star Technology Co., Ltd.

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● Device Overview

129150 module is a Bluetooth low energy module independently developed by RF-star based on Nordic Semiconductor nRF51822-QFAC as the core processor.

The 129150 module integrates a 2.4GHz transceiver, 32-bit ARM Cortex-M0 CPU, 256 kB flash, and 32 kB RAM. The module integrates an industrial-grade 32 MHz crystal with a 32.768kHz low-power clock crystal and includes a variety of peripherals such as I2C, UART, SPI, ADC and GPIO.

This makes it ideal for a wide range of commercial and industrial wireless applications, including professional lighting, asset tracking, smart home products, advanced wearable devices and gaming solutions.

➢Functional Block Diagram

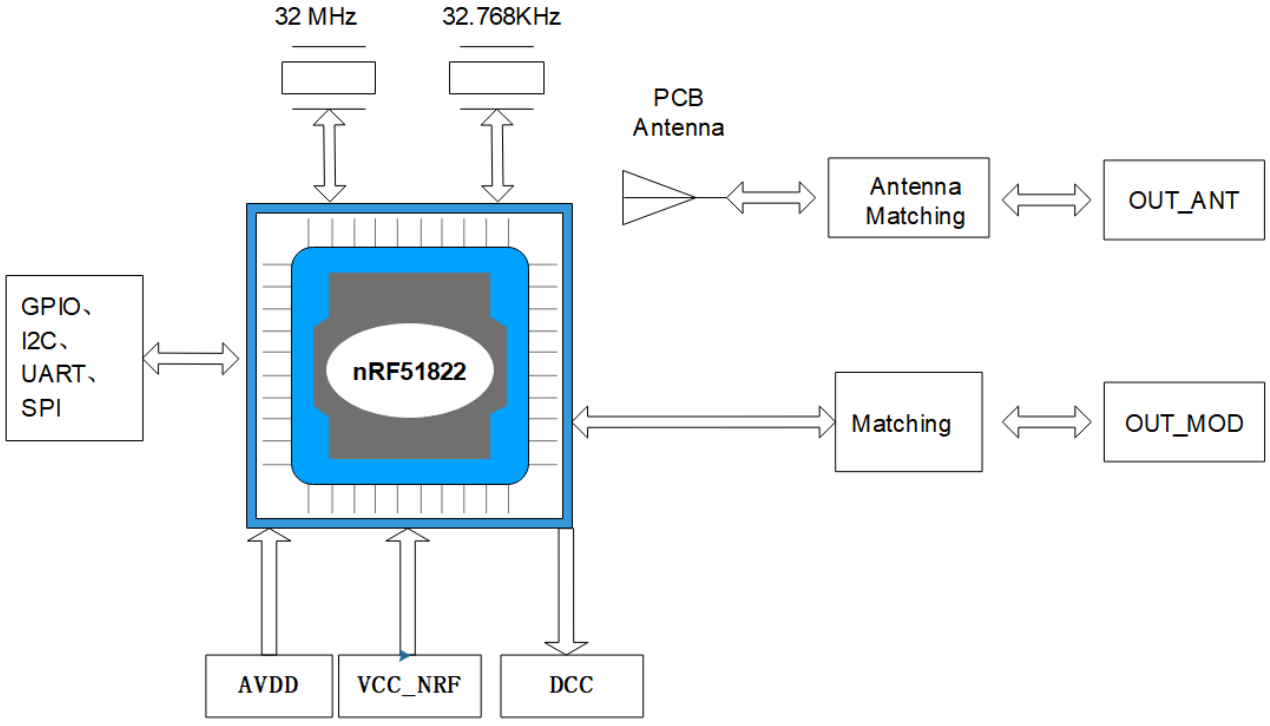


Figure 1. Functional Block Diagram

➢Module Configuration and Functions

➢Operating conditions

Symbol	Parameter	Min.	Typ.	Max	Units
VCC_NRF	Supply voltage, internal LDO setup	1.8	3.3	3.6	V
	Supply voltage, DC/DC converter setup	2.1	3.3	3.6	V
tR_ VCC_NRF	Supply rise time (0 V to VCC_NRF) [1]			100	ms
TA	Operating temperature	-25	25	75	℃

1. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

➢Absolute maximum ratings

Symbol	Parameter	Min.	Max	Units
Supply voltages				
VCC_NRF		-0.3	+3.6	V
GND			0	V
I/O pin voltage				
VIO		-0.3	VCC_NRF+0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model		2	kV
ESD CDM	Charged Device Model		500	V
Flash memory				
Endurance		20 000		write/erase cycles
Retention		10 years		
Number of times an address can be written between erase cycles			2	times

➢GPIO specifications

Symbol	Parameter	Min.	Typ.	Max	Units
V_{IH}	Input high voltage.	0.7 VCC_NRF		VCC_NRF	V
V_{IL}	Input low voltage.	GND		0.3 VCC_NRF	V
V_{OH}	Output high voltage (std. drive, 0.5 mA).	VCC_NRF - 0.3		VCC_NRF	V
V_{OH}	Output high voltage (high-drive, 5 mA).	VCC_NRF - 0.3		VCC_NRF	V
V_{OL}	Output high voltage (std. drive, 0.5 mA).	GND		0.3	V
V_{OL}	Output high voltage (high-drive, 5 mA).	GND		0.3	V
R_{PU}	Pull-up resistance.	11	13	16	kΩ
R_{PD}	Pull-down resistance.	11	13	16	kΩ

➢Current specifications

Symbol	Parameter	Min.	Typ.	Max	Units
$I_{TX,+4dBm}$	TX only run current at POUT = +4 dBm.		16		mA
$I_{TX,0dBm}$	TX only run current at POUT = 0 dBm.		10.5		mA
I_{RX}	RX only run current		13		mA
I_{OFF}	Current in SYSTEM OFF, no RAM retention.		0.6		μA

➢UART specifications

Symbol	Parameter	Min.	Typ.	Max	Units
I_{UART1M}	Run current at max baud rate.		230		μA
$I_{UART115k}$	Run current at 115200 bps.		220		μA
$I_{UART1k2}$	Run current at 1200 bps.		210		μA
f_{UART}	Baud rate for UART.	1.2		1000	kbps

➢SPI Slave specifications

Symbol	Parameter	Min.	Typ.	Max	Units
$I_{SPIS125K}$	Run current for SPI slave at 125 kbps. [1]		180		μA
I_{SPIS2M}	Run current for SPI slave at 2 Mbps. [1]		183		μA
f_{SPIS}	Bit rates for SPIS.	0.125		2	Mbps

1.CSN asserted.

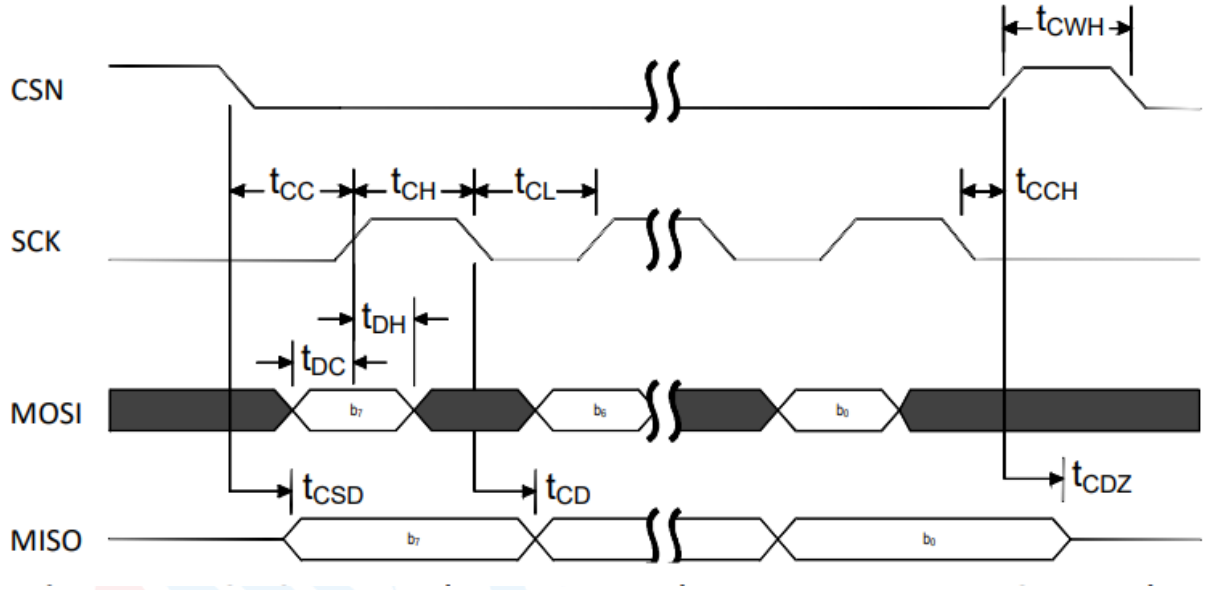


Figure 2. SPIS timing diagram, one byte transmission, SPI Mode 0

Symbol	Parameter	Note	Min.	Typ.	Max	Units
t_{DC}	Data to SCK setup.		10			ns
t_{DH}	SCK to data hold.		10			ns
t_{CSD}	CSN to data valid.	Low power mode. [1] Constant latency mode. [1]			7100 2100	ns
t_{CD}	SCK to data valid.	CLOAD = 10 pF			97 [2]	ns
t_{CL}	SCK low time.		40			ns
t_{CH}	SCK high time.		40			ns
t_{CC}	CSN to SCK setup.	Low power mode. [1] Constant latency mode. [1]	7000 2000			ns
t_{CCH}	Last SCK edge to CSN hold.		2000			ns
t_{CWH}	CSN inactive time.		300			ns
t_{CDZ}	CSN to output high Z.				40	ns
f_{SCK}	SCK frequency.		0.125		2	MHz
t_R, t_F	SCK rise and fall time.				100	ns

1. For more information on how to control the sub power modes, see the nRF51 Series Reference Manual.
2. Increases/decreases with 1.2 ns/pF load.

➢SPI Master specifications

Symbol	Parameter	Min.	Typ.	Max	Units
$I_{SPI125K}$	Run current for SPI slave at 125 kbps.		180		μA
I_{SPI4M}	Run current for SPI slave at 4 Mbps.		200		μA
f_{SPI}	Bit rates for SPI.	0.125		4	Mbps

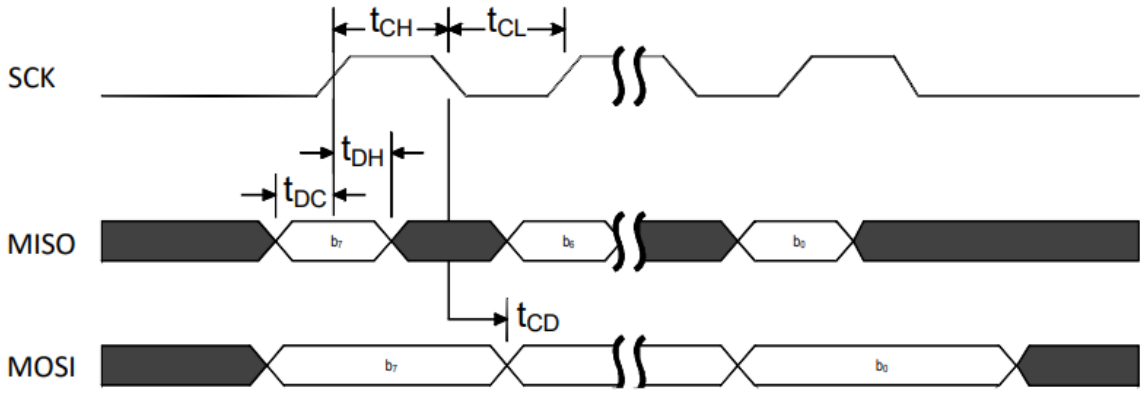


Figure 3. SPI timing diagram, one byte transmission, SPI mode 0

Symbol	Parameter	Note	Min.	Typ.	Max	Units
t_{DC}	Data to SCK setup.		10			ns
t_{DH}	SCK to data hold.		10			ns
t_{CD}	SCK to data valid.	CLOAD = 10 pF			97 [1]	ns
t_{CL}	SCK low time.		40			ns
t_{CH}	SCK high time.		40			ns
f_{SCK}	SCK frequency.		0.125		4	MHz
t_R, t_F	SCK rise and fall time.				100	ns

1. Increases/decreases with 1.2 ns/pF load.

➢I2C compatible Two Wire Interface (TWI) specifications

Symbol	Parameter	Note	Min.	Typ.	Max	Units
I_{2W100K}	Run current for TWI at 100 kbps.			380		μA
I_{2W400K}	Run current for TWI at 400 kbps.			400		μA
f_{2W}	Bit rates for TWI.		100		400	kbps
$t_{TWI,START}$	Time from STARTRX/STARTTX task is given until start condition.	Low power mode. [1] Constant latency mode. [1]		3 1	4.4	μs

1. For more information on how to control the sub power modes, see the nRF51 Series Reference Manual.

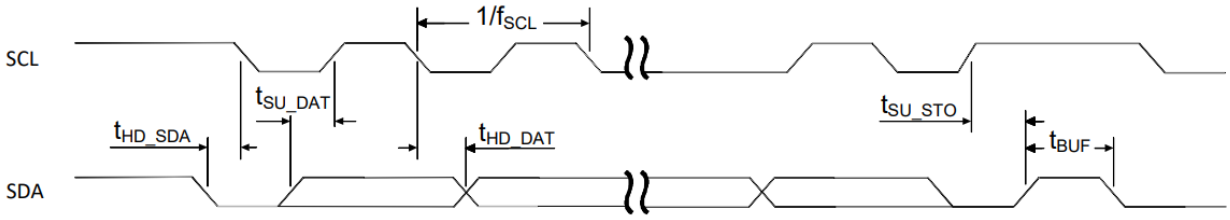


Figure 4. SCL/SDA timing

Symbol	Description	Standard		Fast		Units
		Min.	Max	Min.	Max	
f_{SCL}	SCL clock frequency.		100		400	kHz
t_{HD_STA}	Hold time for START and repeated START condition.	5200		1300		ns
t_{SU_DAT}	Data setup time before positive edge on SCL.	300		300		ns
t_{HD_DAT}	Data hold time after negative edge on SCL.	300		300		ns
t_{SU_STO}	Setup time from SCL goes high to STOP condition.	5200		1300		ns
t_{BUF}	Bus free time between STOP and START conditions.	4700		1300		ns

➢GPIOTE（GPIO Tasks and Events）specifications

Symbol	Description	Min.	Typ.	Max	Units
$I_{GPIOTE,IN}$	Run current with 1 or more GPIOTE active channels in Input mode.		22		μA
$I_{GPIOTE,OUT}$	Run current with 1 or more GPIOTE active channels in Output mode.		0.1		μA
$I_{GPIOTE,IDLE}$	Run current when all channels are in Idle mode. PORT event can be generated with a delay of up to t_{1V2}.		0.1		μA

Note: Setting up one or more GPIO DETECT signals to generate PORT EVENT, which can be used either as a wakeup source or to give an interrupt, will not lead to an increase of the current consumption.

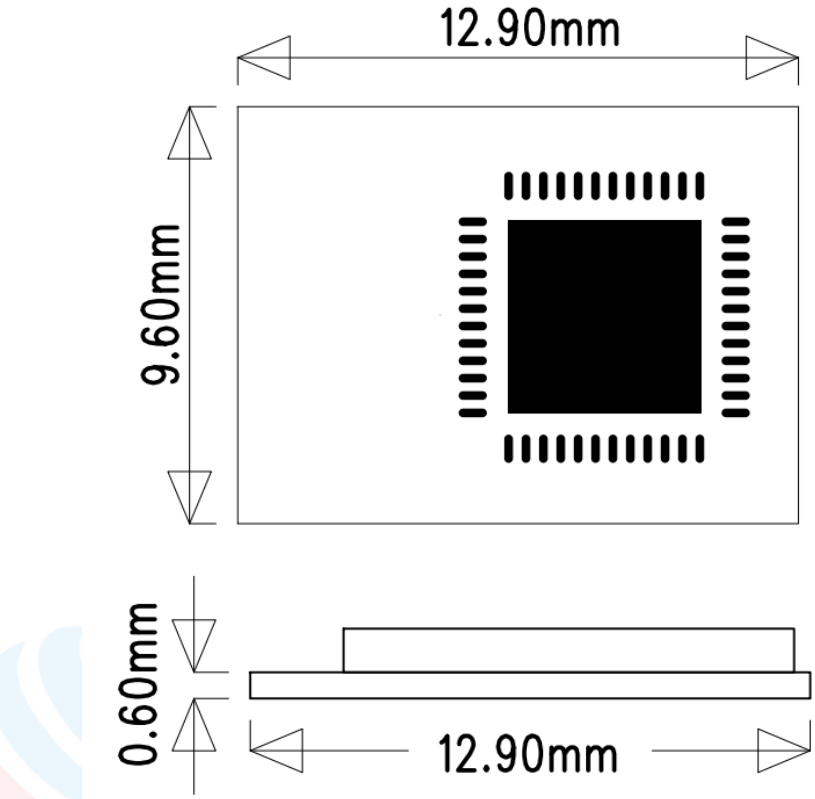
➢RF specifications

Symbol	Description	Min.	Typ.	Max	Units
F_{op}	Operating frequencies	2402		2480	MHz
PLL_{res}	PLL programming resolution		1		MHz
Δf_{BLE}	Frequency deviation at BLE.	±225	±250	±275	kHz
P_{RF}	Maximum output power.		4		dBm
P_{RFC}	RF power control range.	20	24		dB
P_{RFCR}	RF power accuracy.			±4	dB
P_{WHISP}	RF power whisper mode.		-30		dBm
P_{BW2}	20 dB bandwidth for modulated carrier (2 Mbps).		1800	2000	kHz
P_{BW1}	20 dB bandwidth for modulated carrier (1 Mbps).		950	1100	kHz
$P_{RF1.2}$	1st Adjacent Channel Transmit Power. ±2 MHz (2 Mbps).			-20	dBc
$P_{RF2.2}$	2nd Adjacent Channel Transmit Power. ±4 MHz (2 Mbps).			-45	dBc
$P_{RF1.1}$	1st Adjacent Channel Transmit Power. ±1 MHz (1 Mbps).			-20	dBc
$P_{RF2.1}$	2nd Adjacent Channel Transmit Power. ±2 MHz (1 Mbps).			-40	dBc
P_{RXMAX}	Maximum received signal strength at < 0.1% PER.		0		dBm
$P_{RXSENS,2M}$	Sensitivity at 2 Mbps.		-82		dBm
$P_{RXSENS,1M}$	Sensitivity at 1 Mbps.		-87		dBm

➢Module Pin Diagram

➢dimension figure

TOP VIEW



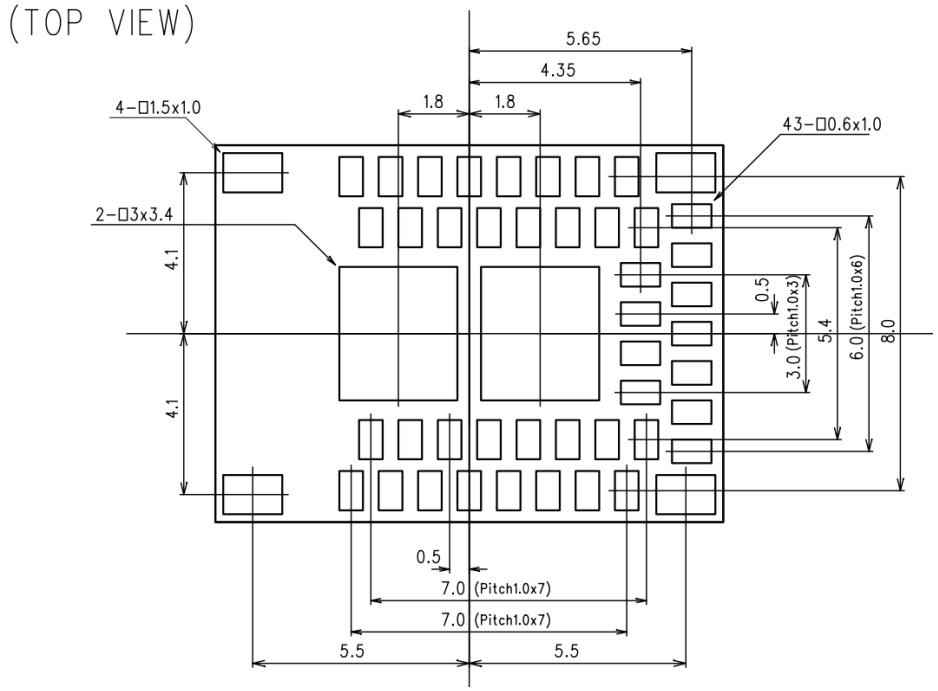


figure 5. dimension figure

➢Pin

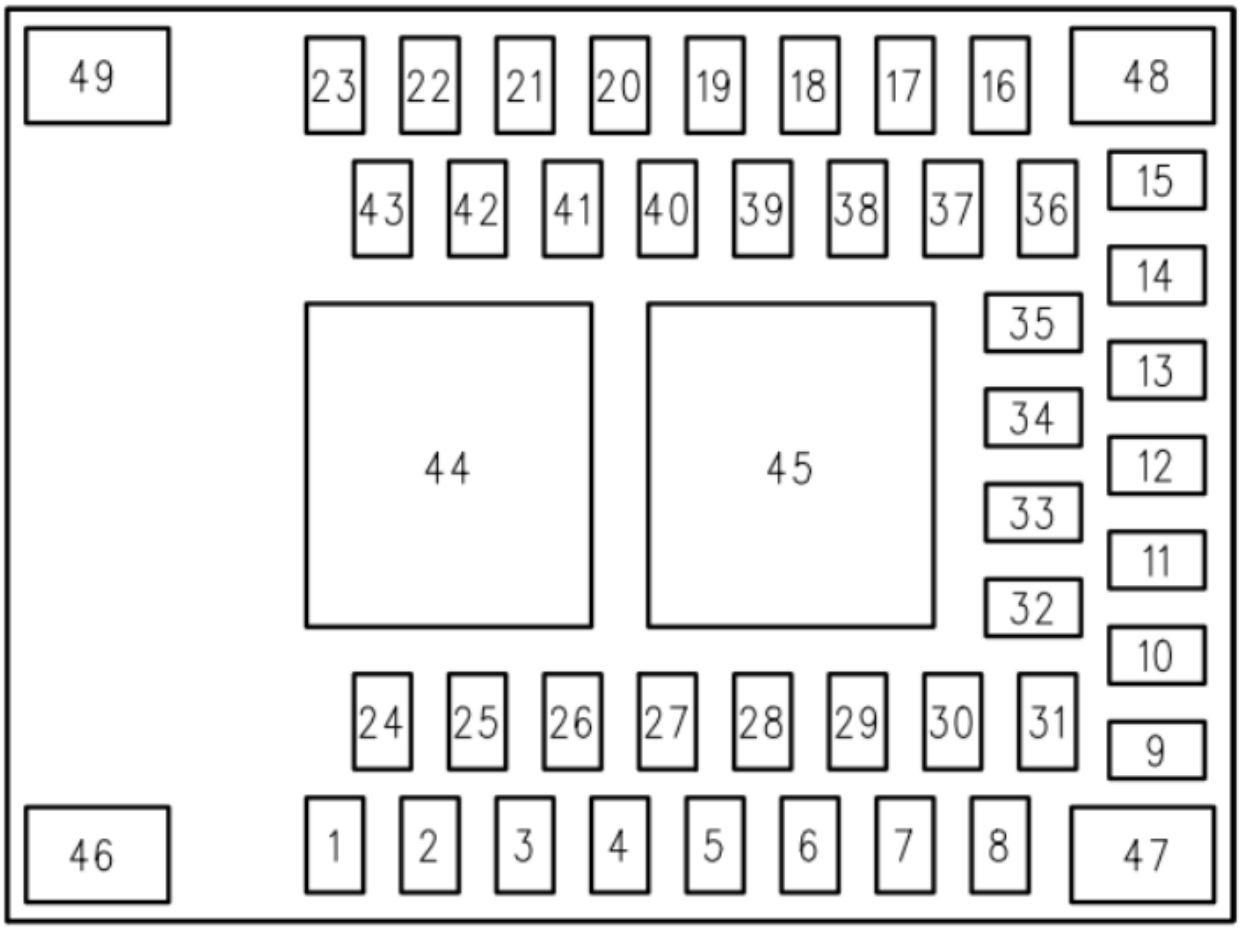


figure 6. Pin

➢Pin Functions

Pin	Name	Function	Description
Pin1	DCC	Power	DC/DC Output
Pin2	AVDD	Power	Analog power supply (Radio).
Pin3	GND	Ground	Ground
Pin4	VCC_NRF	Power	Power supply
Pin5	GND	Ground	Ground (0 V)
Pin6	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin ADC Reference voltage
Pin7	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin ADC input 2
Pin8	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin ADC input 3
Pin9	P0.06	Digital I/O	Generalpurpose I/O pin ADC input 7

	AIN7 AREF1	Analog input Analog input	ADC Reference voltage
Pin10	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin ADC input 6
Pin11	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin ADC input 5
Pin12	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin ADC input 4
Pin13	GND	Ground	Ground (0 V)
Pin14	SWDIO	Digital I/O	System reset (active low). Hardware debug and flash programming I/O.
Pin15	SWDCLK	Digital input	Hardware debug and flash programming I/O.
Pin16	P0.17	Digital I/O	General purpose I/O pin
Pin17	P0.19	Digital I/O	General purpose I/O pin
Pin18	P0.21	Digital I/O	General purpose I/O pin
Pin19	P0.23	Digital I/O	General purpose I/O pin
Pin20	P0.25	Digital I/O	General purpose I/O pin
Pin21	GND	Ground	Ground (0 V)
Pin22	OUT_MOD	RF In/Out	RF I/O pin. Connect to Pin 23 OUT_ANT for normal use
Pin 23	OUT_ANT	Antenna In/Out	Module internal antenna, please connect to the Pin 22 OUT ANT when normal use
Pin 24	P0.28	Digital I/O	General purpose I/O pin
Pin 25	P0.29	Digital I/O	General purpose I/O pin
Pin 26	P0.30	Digital I/O	General purpose I/O pin
Pin 27	P0.07	Digital I/O	General purpose I/O pin
Pin 28	P0.11	Digital I/O	General purpose I/O pin
Pin 29	P0.10	Digital I/O	General purpose I/O pin
Pin 30	P0.09	Digital I/O	General purpose I/O pin
Pin 31	P0.08	Digital I/O	General purpose I/O pin
Pin 32	P0.12	Digital I/O	General purpose I/O pin
Pin 33	P0.13	Digital I/O	General purpose I/O pin
Pin 34	P0.14	Digital I/O	General purpose I/O pin
Pin35	P0.15	Digital I/O	General purpose I/O pin
Pin 36	P0.16	Digital I/O	General purpose I/O pin
Pin 37	P0.18	Digital I/O	General purpose I/O pin
Pin 38	P0.20	Digital I/O	General purpose I/O pin

Pin 39	P0.22	Digital I/O	General purpose I/O pin
Pin 40	P0.24	Digital I/O	General purpose I/O pin
Pin 41 to 45	GND	Ground	Ground (0 V)
Pin 46	NC	Not Connected	Not Connected
Pin 47 to 48	GND	Ground	Ground (0 V)
Pin 49	NC	Not Connected	Not Connected

Reference design

➢LDO and DC/DC Select

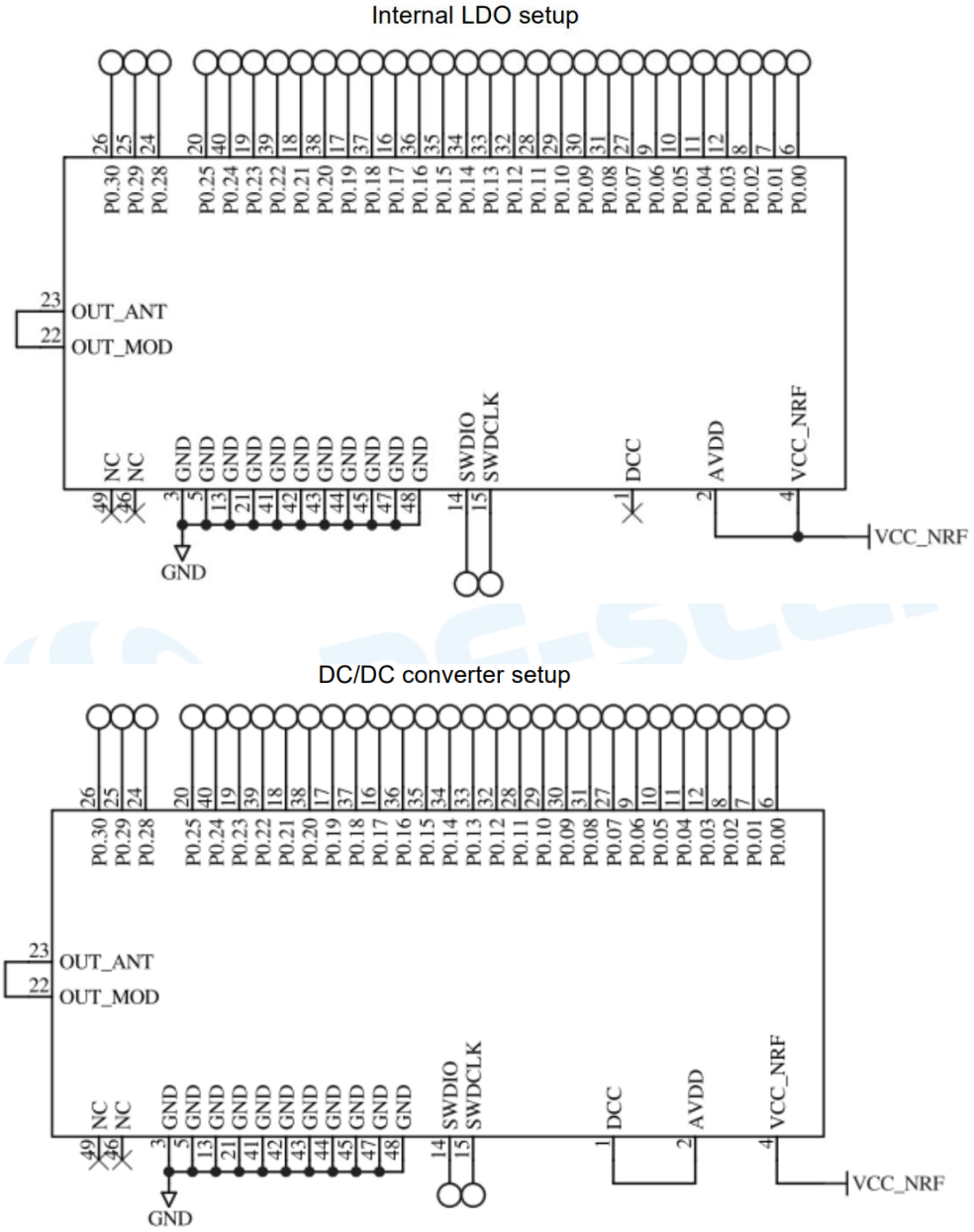


figure 7. LDO and DC/DC Select

➢Reference design circuit（LDO）

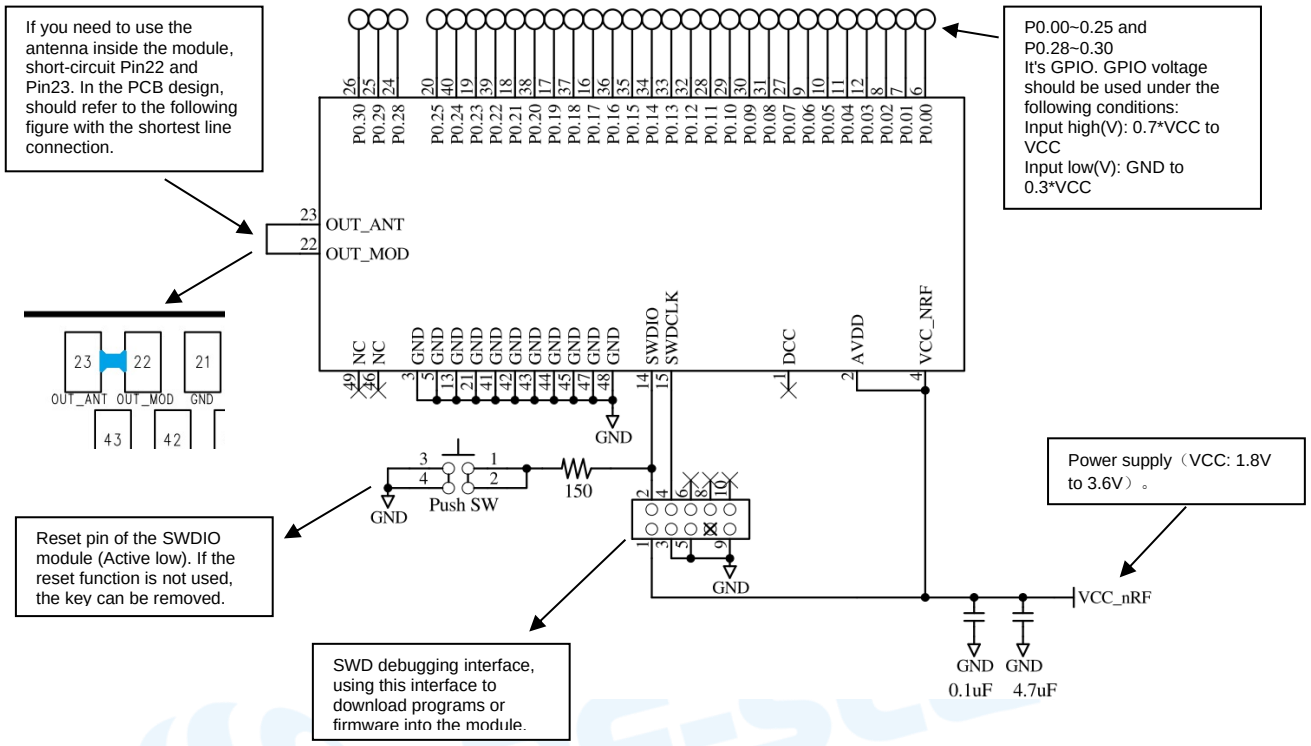


figure 8. Reference design circuit（LDO）

Basic Operation of Hardware Design

- It is recommended to offer the module a DC stabilized power supply, a tiny power supply ripple coefficient, and reliable ground. Please pay attention to the correct connection between the positive and negative poles of the power supply. Otherwise, the reverse connection may cause permanent damage to the module;
- Please ensure the supply voltage is between the recommended values. The module will be permanently damaged if the voltage exceeds the maximum value. Please ensure a stable power supply and no frequently fluctuating voltage.
- When designing the power supply circuit for the module, it is recommended to reserve more than 30% of the margin, which is beneficial to the long-term stable operation of the whole machine. The module should be far away from the power electromagnetic, transformer, high-frequency wiring, and other parts with large electromagnetic interference.
- The bottom of the module should avoid high-frequency digital routing, high-frequency analog routing, and power routing. If it has to route the wire on the bottom of the module, for example, it is assumed that the module is soldered to the Top Layer, the copper must be spread on the connection part of the top layer and the module, and be close to the digital part of the module and routed in the Bottom Layer (all copper is well-grounded).
- Assuming that the module is soldered or placed in the Top Layer, it is also wrong to randomly route the Bottom Layer or other layers, which will affect the spurs and receiving sensitivity of the module to some degree;
- Assuming that there are devices with large electromagnetic interference around the module, which will greatly affect the module performance. It is recommended to stay away from the module according to the strength of the interference. If circumstances permit, appropriate isolation and shielding can be done.
- Assuming that there are routings of large electromagnetic interference around the module (high-frequency digital, high-frequency analog, power routings), which will also greatly affect the module performance. It is recommended to stay away from the module according to the strength of the interference. If circumstances permit, appropriate isolation and shielding can be done.
- It is recommended to stay away from the devices whose TTL protocol is the same 2.4 GHz physical layer, for example, USB 3.0.
- For the layout of the module antenna, see the following figure. The placement of the antenna directly affects the radiation efficiency of the antenna, it is recommended that the customer conduct an antenna debugging on the actual product, the yellow area is keep out, and the distance is recommended to be greater than 10 mm:

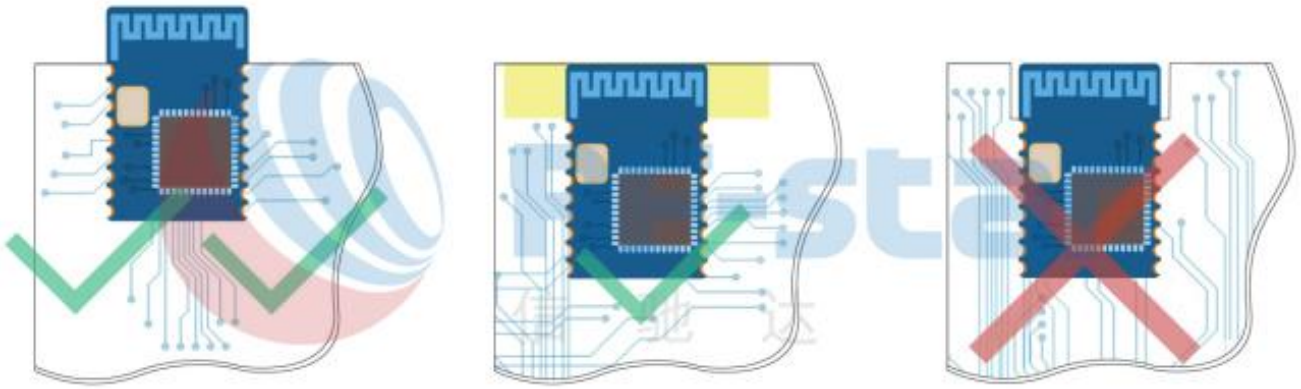


Figure 9. Recommendation of Antenna Layout

● Trouble Shooting

➢Unsatisfactory Transmission Distance

➢When there is a linear communication obstacle, the communication distance will be correspondingly weakened. Temperature, humidity, and co-channel interference will lead to an increase in the communication packet loss rate. The performances of ground absorption and reflection of radio waves will be poor when the module is tested close to the ground.

➢Seawater has a strong ability to absorb radio waves, so the test results by the seaside are poor.

➢The signal attenuation will be very obvious if there is metal near the antenna or if the module is placed inside the metal shell.

➢The incorrect power register set or the high data rate in the open air may shorten the communication distance. The higher the data rate, the closer the distance.

➢The low voltage of the power supply is lower than the recommended value at ambient temperature, and the lower the voltage, the smaller the power is.

➢The unmatchable antennas and modules or the poor quality of antenna will affect the communication distance.

➢Vulnerable Module

➢Please ensure the supply voltage is between the recommended values. The module will be permanently damaged if the voltage exceeds the maximum value. Please ensure a stable power supply and no frequently fluctuating voltage.

➢Please ensure the anti-static installation and the electrostatic sensitivity of high-frequency devices.

➢Due to some humidity-sensitive components, please ensure the suitable humidity during installation and application. If there is no special demand, it is not recommended to use at too high or too low temperature.

➢High Bit Error Rate

➢There are co-channel signal interferences nearby. It is recommended to be away from the interference sources or modify the frequency and channel to avoid interferences.

➢The unsatisfactory power supply may also cause garbled. It is necessary to ensure the power supply's reliability.

➢If the extension wire or feeder wire is of poor quality or too long, the bit error rate will be high.

Soldering and Reflow Condition

- Heating method: Conventional Convection or IR/convection.
- Solder paste composition: Sn96.5/Ag3.0/Cu0.5
- Allowable reflow soldering times: 2 times based on the following reflow soldering profile.
- Temperature profile: Reflow soldering shall be done according to the following temperature profile.
- Peak temperature: 245 ℃.

Table 1. Temperature Table of Soldering and Reflow

Profile Feature	Sn-Pb Assembly	Pb-Free Assembly
Solder Paste	Sn63 / Pb37	Sn96.5 / Ag3.0 / Cu0.5
Min. Preheating Temperature (T_{min})	100 ℃	150 ℃
Max. Preheating Temperature (T_{max})	150 ℃	200 ℃
Preheating Time (T_{min} to T_{max}) (t_1)	60 s ~ 120 s	60 s ~ 120 s
Average Ascend Rate (T_{max} to T_p)	Max. 3 ℃/s	Max. 3 ℃/s
Liquid Temperature (T_L)	183 ℃	217 ℃
Time above Liquidus (t_L)	60 s ~ 90 s	30 s ~ 90 s
Peak Temperature (T_p)	220 ℃ ~ 235 ℃	230 ℃ ~ 250 ℃
Average Descend Rate (T_p to T_{max})	Max. 6 ℃/s	Max. 6 ℃/s
Time from 25 ℃ to Peak Temperature (t_2)	Max. 6 minutes	Max. 8 minutes
Time of Soldering Zone (t_P)	20±10 s	20±10 s

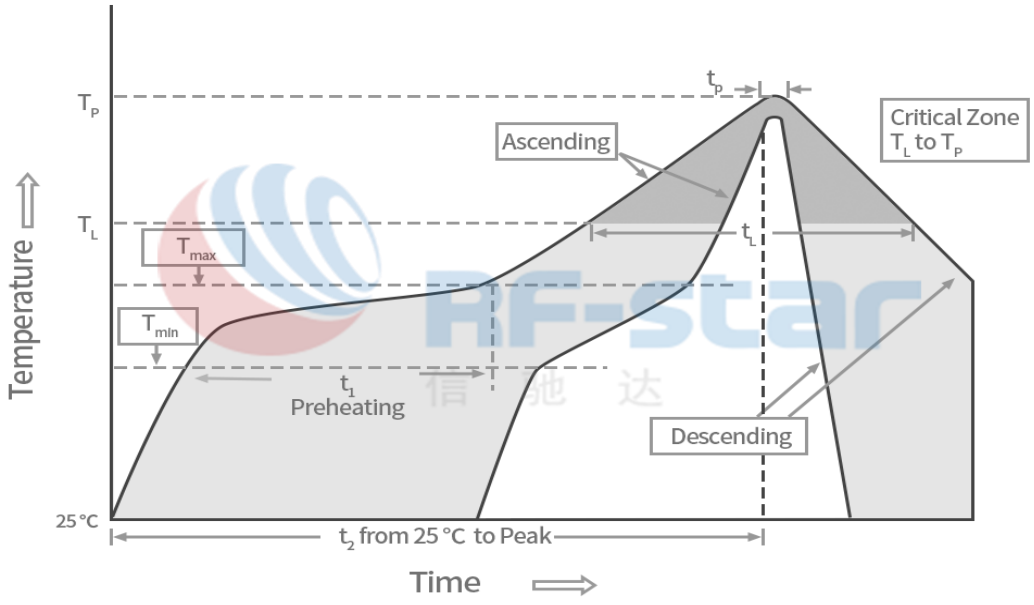


Figure 10. Recommended Reflow for Lead-Free Solder

● Electrostatic discharge warning

Modules can be damaged by static release, and RF-star recommends that all modules be handled under the following 3 precautions:

1. Observe ESD measures. Do not hold the module with bare hands.

2, the module must be placed in a place that can prevent static electricity.

3, in the product design should consider the high voltage input or high frequency input at the anti-static circuit.

Static electricity can result in subtle performance degradation to the failure of the entire device. Since very small parameter changes can cause a device to fail to meet the value limits of its certification requirements, modules are more vulnerable.

● CE market

● FCC Warning

FCC regulatory compliance statement

§15.19 Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§15.21 Information to user

Warning: changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

- List of applicable FCC rules:

47 CFR Part 15, Subpart C 15.247

47 CFR Part 2.1091

- Summarize the specific operational use conditions

This module can be used in IOT devices, the input voltage to the module is nominally 3.3V.

- Limited module procedures

This module is a single module.

- Trace antenna designs

The antenna is not a trace antenna.

- RF exposure considerations

This Module complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

- Antennas

If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

- Label and compliance information

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside

of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains FCC ID: 2BGLE-129150” any similar wording that expresses the same meaning may be used.

§ 15.19 Labelling requirements shall be complied on end user device.

Labelling rules for special device, please refer to §2.925, § 15.19 (a)(5) and relevant KDB publications. For E-label, please refer to §2.935.

- Information on test modes and additional testing requirements

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.

The module is limited to installation in mobile application, a separate approval is required for all other operating configurations, including portable configurations with respect to §2.1093 and difference antenna configurations.

Test software access to different test modes: Bluetooth test 3 (V2.6)

Testing item, Frequencies, Transmit Power, Modulation Type can be selected on the test script instructions.

- FCC other Parts, Part 15B Compliance Requirements for Host product manufacturer

This modular transmitter is only FCC authorized for the specific rule parts listed on our grant, host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.

Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in *§15.105 Information to the user* or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:

For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

For Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

● Revision History

Date	Version No.	Description
2023/09/14	V1.0	The initial version is released.

● Contact Us

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