SUS600-LD&SUS609-LD

Hardware Design

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1 Introduction

This document defines the SUS600-LD and SUS609-LD and describes their air interfaces and hardware interfaces which are connected with your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

NOTE

For conciseness purposes, SUS600-LD and SUS609-LD will hereinafter be referred to collectively as "the module/modules" in parts hereof applicable to both module series, and individually as "SUS600-LD" and "SUS609-LD" in parts hereof referring to the differences between them.

1.1. Text Conventions

Table 1: Text Conventions

dev	Unless stated otherwise, the presence of the mark "dev" following a function, feature, interface, pin name, command, argument, etc., signifies that it is still in the development phase and not yet supported. Additionally, when "dev" appears after a model, it indicates that the model sample is currently unavailable.
NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

SUS600-LD and SUS609-LD are smart LTE modules providing industrial-grade performance. SUS600-LD is based on Android operating system while SUS609-LD is based on Linux operating system. The module supports multiple audio and video codecs, built-in high performance Adreno™ 610 GPU and multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

Related information and details of the module are listed in the table below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LCC: 152; LGA: 171
Dimensions	(43.0 ±0.15) mm × (44.0 ±0.15) mm × (2.85 ±0.20) mm
Weight	Approx. 12.0 g

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	SUS600-LD & SUS609-LD
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41 (200 MHz)
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz (*Restrict to indoor operation only in the band 5150-5250 MHz)
BLE 5.0	2402–2480 MHz
GNSS (Optional)	**GPS/QZSS:** 1575.42 ±1.023 MHz **GLONASS:** 1597.5–1605.8 MHz **BDS:** 1561.098 ±2.046 MHz **Galileo:** 1575.42 ±2.046 MHz **SBAS:** 1575.42 ±1.023 MHz

2.2. Key Features

Table 4: Key Features

Feature	Details
Application Processor	ARM Kryo™ 260 CPU (octa-core 64-bit): ● Kryo Gold: One high performance quad-core @ 2.0 GHz with 1 MB L2 cache ● Kryo Silver: One low power consumption quad-core @ 1.8 GHz with 512 KB L2 cache

Modem System	LTE Cat 4 (FDD & TDD)
GPU	Adreno™ 610 GPU with 64-bit addressing @ 950 MHz
DSP	Hexagon™ DSP, supports Dual HVX 512
Memory	**SUS600-LD:** ● eMCP: 32 GB eMMC + 3 GB LPDDR4X (optional) ● eMCP: 64 GB eMMC + 4 GB LPDDR4X (default) ● uMCP: 128 GB UFS + 8 GB LPDDR4X (optional) **SUS609-LD:** ● eMCP: 16 GB eMMC + 2 GB LPDDR4X
Operating System	**SUS600-LD:** Android 10/11/13 dev **SUS609-LD:** Linux 4.14
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: does not support by default
LCM Interface	● Support one group of 4-lane MIPI_DSI, up to 1.5 Gbps/lane ● Support up to 1920 × 1200 @ 60 fps or 1080 × 2520 @ 60 fps
Camera Interfaces	● Support three groups of 4-lane MIPI_CSI, up to 2.1 Gbps/lane ● Support three cameras (4-lane + 4-lane + 4-lane), each camera (4-lane) can be divided into 2-lane + 1-lane. Support up to six cameras (up to two cameras at the same time) ● Support up to 16 MP + 16 MP or 24 MP with dual ISP
Video Codec	● Encoding: 4K @ 30 fps, HEVC/H.264/VP8 ● Decoding: 4K @ 30 fps, HEVC/H.264/VP8/VP9 1080P @ 30 fps, MPEG-2
Audio Interfaces	**Audio inputs:** ● Three analog microphone inputs. MIC1/MIC2 has internal bias, MIC3 has no internal bias **Audio outputs:** ● Class AB stereo headphone output ● Class AB earpiece differential output ● Class K loudspeaker differential output
Audio Codec	● EVRC, EVRC-B, EVRC-WB ● G.711, G.729A/AB, GSM-FR, GSM-EFR, GSM-HR ● AMR-NB, AMR-WB, AMR-eAMR, AMR-BeAMR
USB Interfaces	● Comply with USB 3.1 Gen 1 or 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 Gen 1 and 480 Mbps on USB 2.0 ● Support USB OTG ● Support USB 3.1 Type-C interface, compatible with USB 2.0 ● Used for data communication with external AP, AT command transmission, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB
DisplayPort Interface	● Support DisplayPort 1.4 interface function through USB_SS1 and USB_SS2 ● Support DP standard interface only ● Support up to 1920 ×1200 @ 60 fps ● DisplayPort cannot be used with USB 3.1 simultaneously for now
(U)SIM Interfaces	● Two (U)SIM interfaces ● Support (U)SIM card: 1.8 V, 2.95 V ● Support dual SIM dual Standby (supported by default), Dual Active is not supported
SD Card Interfaces	● Support SD 3.0 specification ● Support 1.8/2.95 V SD card ● Support SD card hot-plug

UART Interfaces [1]	Support up to five groups of UART interfaces, three of them are default configurations, two of them are multiplexed from other interfaces: ● Three default UART interfaces: DBG_UART, UART03 and UART00 - Debug UART: 2-wire UART interface, dedicated for debugging by default - UART03: 2-wire UART interface - UART00: 4-wire UART interface, RTS and CTS hardware flow control are supported, up to 4 Mbps ● Two multiplexed UART interfaces: see ***Table 23*** for details.
SPI [1]	Support up to four groups of SPI, two of them are default configurations, and two of them are multiplexed from other interfaces: ● Support master mode only ● For details about two SPIs that multiplexed from other interfaces, see ***Table 23***
I2C Interfaces [1]	Support up to eight groups of I2C interfaces: ● Three dedicated I2C interfaces: used for cameras and sensors. ● Two generic I2C interfaces: used for TPs and other peripherals ● Three multiplexed I2C interfaces: see ***Table 23*** for details
I2S Interfaces [1]	Support up to three groups of I2S interfaces: ● One default I2S interface ● Two multiplexed I2S interfaces: see ***Table 23*** for details.
ADC Interfaces	● Two general-purpose ADC interfaces ● Support up to 15-bit resolution
Real Time Clock	Supported
Bluetooth Features	● Support *Bluetooth Core Specification Version 5.0* ● Support Bluetooth Classic & BLE
GNSS Features (Optional)	GPS/GLONASS/BDS/Galileo/QZSS/SBAS
Antenna Interfaces	Main antenna, Rx-diversity antenna, GNSS antenna and Wi-Fi/Bluetooth antenna
Transmitting Power	LTE: Class 3 (23 dBm ±2 dB)
LTE Features	● Support 3GPP Rel-12 Cat 4 FDD and TDD ● Support 1.4/3/5/10/15/20 MHz RF bandwidths ● Support DL 2 × 2 MIMO ● Support uplink QPSK and 16QAM modulations ● Support downlink QPSK, 16QAM and 64QAM modulations ● LTE-FDD: Max. 150 Mbps (DL)/50 Mbps (UL) ● LTE-TDD: Max. 130 Mbps (DL)/30 Mbps (UL)
WLAN Features	● Support AP and STA modes ● 2.4 GHz, 5 GHz, 802.11a/b/g/n/ac, maximally up to 433 Mbps
Temperature Ranges	● Operating temperature [2]: -35 °C to +75 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Use USB interface or OTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] For details about the multiplexing and conflict relationships of UART, I2C, SPI and I2S interfaces, see ***Table 23***.
[2] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

2.3. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36–38	PI	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	Provide sufficient current up to 3 A. It is suggested to add a TVS for surge protection.
LDO9A_1V8	9	PO	1.8 V output (Power supply for external I/O pull up circuits and level-shifting circuit)	Vnom = 1.8 V $I_O$max = 20 mA	Cannot be used for peripheral equipment. External capacitor is not required.
LDO12A_1V8	10	PO	1.8 V output (Power supply for I/O of cameras, LCM and sensors)	Vnom = 1.8 V $I_O$max = 300 mA	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 9 µF. If unused, keep it open.
LDO14A_1V8	158	PO	1.8 V output (Power supply for external Codec)	Vnom = 1.8 V $I_O$max = 600 mA	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 18.8 µF. If unused, keep it open.

ELDO1_2V8	11	PO	2.8 V output (Power supply for external sensor and touch panel)	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 9 µF. If unused, keep them open.
ELDO2_2V85	12	PO	2.85 V output (Power supply for LCM and camera's AFVDD)	Vnom = 2.85 V $I_O$max = 300 mA	
LDO1C_1V2	15	PO	1.2 V output (Power supply for DVDD of front cameras)	Vnom = 1.2 V $I_O$max = 800 mA	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 15.3 µF. If unused, keep them open. Power supply only for cameras.
LDO2C_1V1	13	PO	1.1 V output (Power supply for DVDD of rear cameras)	Vnom = 1.1 V $I_O$max = 800 mA	
LDO3C_2V8	14	PO	2.8 V output (Power supply for AVDD of cameras)	Vnom = 2.8 V $I_O$max = 300 mA	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 47.8 µF. If unused, keep it open. Power supply only for cameras.
VRTC	16	PIO	Power supply for RTC	$V_O$max = 3.2 V When there is no VBAT connection: Vmin = 2.1 V Vmax = 3.25 V Vnom = 3.0 V	
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128, 130, 133, 135, 148, 150, 159, 163, 170, 173, 176, 182, 193, 195, 219, 225, 243, 257–323				

Keypad Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	39	DI	Turn on/off the module	1.8 V	
VOL_UP	146	DI	Volume up		
VOL_DOWN	147	DI	Volume down		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	41, 42	AI	USB insertion interruption detect	Vmax = 6.0 V Vmin = 4.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	32	AIO	USB 2.0 differential data (+)		USB 2.0 standard compliant. 90 Ω differential impedance. Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)		
USB_SS1_RX_P	171	AI	USB 3.1 channel 1 super-speed receive (+)		USB 3.1 Gen 1 compliant.

USB_SS1_RX_M	172	AI	USB 3.1 channel 1 super-speed receive (-)		90 Ω differential impedance. USB Type-C (USB 3.1) interface uses USB_SS1 by default. Insert front and back sides of USB through external switch. Use USB_SS1 and USB_SS2 to achieve functions of DisplayPort 1.4 interface.
USB_SS1_TX_P	174	AO	USB 3.1 channel 1 super-speed transmit (+)		
USB_SS1_TX_M	175	AO	USB 3.1 channel 1 super-speed transmit (-)		
USB_SS2_RX_P	162	AI	USB 3.1 channel 2 super-speed receive (+)		USB 3.1 Gen 1 compliant. 90 Ω differential impedance. Use USB_SS1 and USB_SS2 to achieve functions of DisplayPort 1.4 interface.
USB_SS2_RX_M	161	AI	USB 3.1 channel 2 super-speed receive (-)		
USB_SS2_TX_P	165	AO	USB 3.1 channel 2 super-speed transmit (+)		
USB_SS2_TX_M	164	AO	USB 3.1 channel 2 super-speed transmit (-)		
USB_CC1	224	AIO	USB Type-C detect 1		
USB_CC2	223	AIO	USB Type-C detect 2		
USB_SS_SEL	226	DO	USB Type-C switch control	1.8 V	
USB_ID	30	DO	USB 3.1 ID indication signal		USB Type-C interface USB ID status indicates output. High level by default.
GPIO_130	247	DI	USB ID interruption detect		Internal pull up by default.

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	141	PO	(U)SIM1 card power supply	$I_O$max = 150 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **2.95 V (U)SIM:** Vmax = 3.03 V Vmin = 2.7 V	Can recognize 1.8 V or 2.95 V (U) SIM card automatically. External capacitance shall not exceed 4 µF.
USIM1_DATA	142	DIO	(U)SIM1 card data	1.8/2.95 V	Pull it up to USIM1_VDD with an external 10 kΩ resistor. Cannot be multiplexed into a generic GPIO.
USIM1_CLK	143	DO	(U)SIM1 card clock		Cannot be multiplexed into a generic GPIO.
USIM1_RST	144	DO	(U)SIM1 card reset		
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect		Require external pull-up to LDO9A_1V8. Active low. If unused, keep it open. This function is disabled by default. Cannot be multiplexed into a generic GPIO.

USIM2_VDD	210	PO	(U)SIM2 card power supply	$I_O$max = 150 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **2.95 V (U)SIM:** Vmax = 3.03 V Vmin = 2.7 V	Either 1.8 V or 2.95 V (U)SIM card is supported. External capacitance shall not exceed 4 µF.
USIM2_DATA	209	DIO	(U)SIM2 card data	1.8/2.95 V	Pull it up to USIM2_VDD with an external 10 kΩ resistor. Cannot be multiplexed into a generic GPIO.
USIM2_CLK	208	DO	(U)SIM2 card clock		Cannot be multiplexed into a generic GPIO.
USIM2_RST	207	DO	(U)SIM2 card reset		
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect		Require external pull-up to LDO9A_1V8. Active low. If unused, keep it open. This function is disabled by default. Cannot be multiplexed into a generic GPIO.

SD Card Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SD_CLK	70	DO	SD card clock	1.8/2.95 V	Control characteristic impedance as 50 Ω.
SD_CMD	69	DIO	SD card command		
SD_DATA0	68	DIO	SDIO data bit 0		
SD_DATA1	67	DIO	SDIO data bit 1		
SD_DATA2	66	DIO	SDIO data bit 2		
SD_DATA3	65	DIO	SDIO data bit 3		
SD_DET	64	DI	SD card hot-plug detect		Active low. Require external pull-up to LDO9A_1V8.
SD_VDD	63	PO	SD card power supply	Vnom = 1.8/2.95 V $I_O$max = 600 mA	External capacitance shall not exceed 13.5 µF.
SD_PU_VDD	179	PO	SD card pull-up power supply: 1.8 V/2.95 V output	Vnom = 1.8/2.95 V $I_O$max = 50 mA	Only for SD card pull-up circuits. External capacitance shall not exceed 4 µF.

UART Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	5	DO	Debug UART transmit	1.8 V	If unused, keep them open. Test points must be reserved.
DBG_RXD	6	DI	Debug UART receive		
UART03_TXD	7	DO	UART03 transmit		If unused, keep them open.
UART03_RXD	8	DI	UART03 receive		

UART00_TXD	199	DO	UART00 transmit		If unused, keep them open. When UART00_RTS and UART00_CTS are multiplexed into I2C, UART00_TXD and UART00_RXD can only be used as generic GPIOs.
UART00_RXD	198	DI	UART00 receive		
UART00_RTS	245	DO	Request to send signal from the module		
UART00_CTS	246	DI	Clear to send signal to the module		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C11_SCL	205	OD	I2C serial clock	1.8 V	External pull-up resistor is required.
I2C11_SDA	204	OD	I2C serial data		
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI10_CS	58	DO	SPI10 chip select	1.8 V	Support master mode only.
SPI10_CLK	59	DO	SPI10 clock		
SPI10_MOSI	60	DO	SPI10 master-out slave-in		
SPI10_MISO	61	DI	SPI10 master-in slave-out		
SPI13_CS	203	DO	SPI13 chip select		
SPI13_CLK	250	DO	SPI13 clock		
SPI13_MOSI	249	DO	SPI13 master-out slave-in		
SPI13_MISO	251	DI	SPI13 master-in slave-out		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MI2S_DATA1	155	DIO	I2S data channel 1	1.8 V	
MI2S_DATA0	154	DIO	I2S data channel 0		
MI2S_WS	156	DO	I2S word select		
MI2S_SCLK	212	DO	I2S serial clock		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DSI_CLK_P	115	AO	LCD MIPI clock (+)		Require differential impedance of 100 Ω.
DSI_CLK_N	116	AO	LCD MIPI clock (-)		
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)		

DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)		
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	121	AO	LCD MIPI lane 2 data (+)		
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)		
LCD_TE	126	DI	LCD tearing effect	1.8 V	
LCD_RST	127	DO	LCD reset		External pull-up is not required.
PWM	152	DO	PWM output	Voltage shall be the same as VBAT.	Cannot be multiplexed into a generic GPIO.

Touch Panel Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
TP_RST	138	DO	TP reset	1.8 V	Cannot be pulled up during the module's turning-on process.
TP_INT	139	DI	TP interrupt		
TP_I2C_SCL	140	OD	TP I2C clock		Used for touch panel. External pull-up is required.
TP_I2C_SDA	206	OD	TP I2C data		

Camera Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)		Require differential impedance of 100 Ω. Used for front camera by default.
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)		
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)		
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)		Require differential impedance of 100 Ω.

CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)		Used for rear camera by default.
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)		
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)		
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)		Require differential impedance of 100 Ω. Used for depth camera by default.
CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)		
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)		
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)		
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)		
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)		
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)		Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI data (+).
CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)		Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI data (-).
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)		Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI clock (+).
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)		Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI clock (-).
MCAM_MCLK	99	DO	Master clock of rear camera	1.8 V	
SCAM_MCLK	100	DO	Master clock of front camera		

DCAM_MCLK	194	DO	Master clock of depth camera		
CAM4_MCLK	236	DO	Master clock of the 4th camera		
MCAM_RST	74	DO	Reset of rear camera		
SCAM_RST	72	DO	Reset of front camera		
DCAM_RST	180	DO	Reset of depth camera		
MCAM_PWDN	73	DO	Power down of rear camera		
SCAM_PWDN	71	DO	Power down of front camera		
DCAM_PWDN	181	DO	Power down of depth camera		
CAM_I2C_SCL	75	OD	I2C clock of front and rear camera		External pull-up is required. Dedicated for camera. Cannot be multiplexed into a generic GPIO.
CAM_I2C_SDA	76	OD	I2C data of front and rear camera		
DCAM_I2C_SCL	196	OD	I2C clock of depth camera		
DCAM_I2C_SDA	197	OD	I2C data of depth camera		

Audio Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC1_P	44	AI	Microphone input for channel 1 (+)		Integrated with internal bias voltage.
MIC1_M	45	AI	Microphone input for channel 1 (-)		
MIC2_P	46	AI	Microphone input for headset (+)		
MIC3_P	169	AI	Microphone input for headset (+)		Integrated without internal bias voltage
MIC_GND	168		Microphone reference ground		If unused, connect it to ground.
MIC_BIAS1	167	AO	Bias voltage 1 output for microphone	V_{O}min = 1.0 V V_{O}max = 2.85 V	
MIC_BIAS3	28	AO	Bias voltage 3 output for microphone		
HS_DET	48	AI	Headset hot-plug detect		Cannot be externally pulled up.
HPH_L	49	AO	Headphone left channel output		
HPH_GND	50		Headphone reference ground		If unused, connect it to ground.
HPH_R	51	AO	Headphone right channel output		
EAR_M	52	AO	Earpiece output (-)		
EAR_P	53	AO	Earpiece output (+)		
SPK_M	54	AO	Loudspeaker output (-)		
SPK_P	55	AO	Loudspeaker output (+)		

Sensor Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ALPS_INT	253	DI	Light/Proximity sensor interrupt	1.8 V	1.8 V power domain. Can be multiplexed into a generic GPIO.
ACCL_INT	252	DI	Acceleration sensor interrupt		
GYRO_INT	255	DI	Gyroscope sensor interrupt		
MAG_INT	254	DI	Geomagnetic sensor interrupt		
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor		Dedicated for external sensor. Cannot be used for touch panel, NFC, I2C keyboard, etc. Cannot be multiplexed into a generic GPIO.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor		

GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_8	227	DIO	General-purpose input/output	1.8 V	
GPIO_9	228	DIO			Support wakeup interrupt.
GPIO_26	136	DIO			
GPIO_27	137	DIO			
GPIO_43	238	DIO			
GPIO_83	200	DIO			
GPIO_84	201	DIO			
GPIO_85	237	DIO			Support wakeup interrupt.
GPIO_95	113	DIO			
GPIO_97	114	DIO			
GPIO_117	213	DIO			
GPIO_119	234	DIO			
GPIO_123	230	DIO			Support wakeup interrupt.
GPIO_124	229	DIO			
GPIO_125	232	DIO			
GPIO_126	231	DIO			Support wakeup interrupt.
GPIO_127	178	DIO			
GPIO_128	177	DIO			Support wakeup interrupt.

GPIO_130	247	DIO			
GPIO_131	248	DIO			
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	19	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_DRX	149	AI	Rx-diversity antenna interface		
ANT_GNSS	134	AI	GNSS antenna interface		
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface		
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_36	242	DIO	Generic RF controller	1.8 V	Only used for RF debugging, cannot be multiplexed into a generic GPIO. Cannot be pulled up during module's turning-on process.
GRFC_33	241	DIO			Only used for RF debugging, cannot be multiplexed into a generic GPIO.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	151	AI	General-purpose ADC interface		1.8 V power domain.
ADC1	153	AI			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CBL_PWR_N	240	DI	Initiate turning-on when grounded	1.8 V	The module cannot be turned off when this pin is pulled down.
USB_BOOT	57	DI	Force the module into download mode		Force the module to enter download mode by pulling this pin up to LDO9A_1V8 during turning-on. A test point is recommended to be reserved.
GNSS_LNA_EN	202	DO	GNSS LNA enable control		Only for internal test, cannot be multiplexed into a generic GPIO. If unused, keep it open.
S2A	211	-			

S2B	233	-	S2A and S2B are directly connected inside the module		
DP_AUX_P	216	AIO	DP auxiliary channel (+)		
DP_AUX_N	215	AIO	DP auxiliary channel (-)		
DP_HPD	217	DI	DP hot-plug detection	1.8 V	Cannot be externally pulled up.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	1, 2, 17, 21–27, 29, 102–111, 157, 160, 166, 214, 218, 220–222, 235, 239, 244				Keep them open.

NOTE

For more details about module's multiplexing functions, see ***document 1***.

2.4. EVB Kit

NetPrisma supplies an evaluation board (Smart EVB G5) with accessories to develop and test the module. For more details, see ***document 2***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides three VBAT pins, which are dedicated for connection with external power supply. Power supply range of the module is from 3.55 V to 4.4 V and the recommended value is 3.8 V.

Table 7: Pin Definition of Power Supply

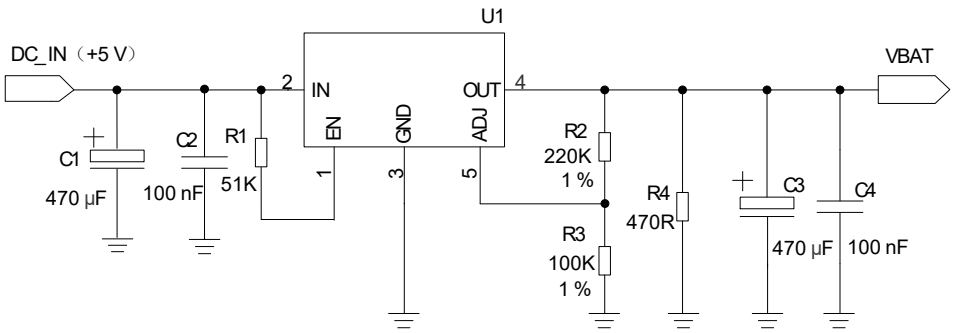
Pin Name	Pin No.	I/O	Description	Comment
VBAT	36–38	PI	Power supply for the module	Provide sufficient current up to 3 A. It is suggested to add a TVS for surge protection.

3.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3 A at least. If the voltage drops between input and output is not too high, it is suggested to use an LDO in the power system design. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure illustrates a reference design for +5 V input power source.

Figure 1: Reference Design of Power Supply



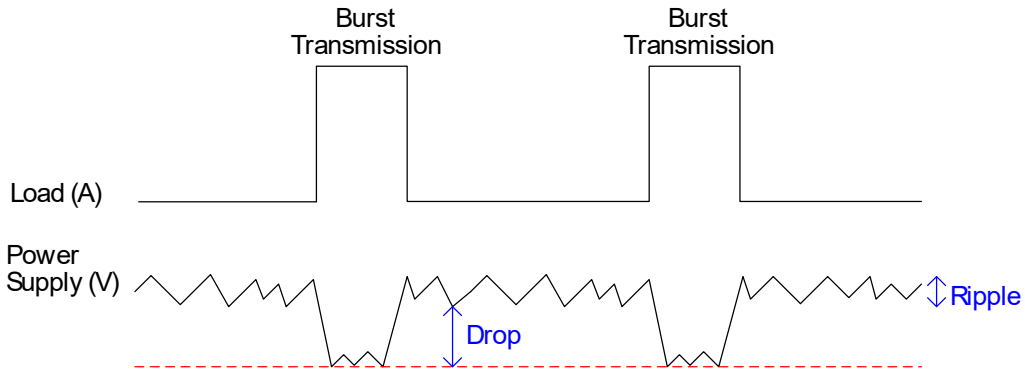
NOTE

It is recommended to switch off the power supply when the module is in abnormal state to turn off the module, and then switch on the power supply to restart the module.

3.2.1. Voltage Stability Requirements

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.3 V, the module will be turned off automatically. Therefore, make sure the input voltage never drops below 3.3 V.

Figure 2: Voltage Drop Sample

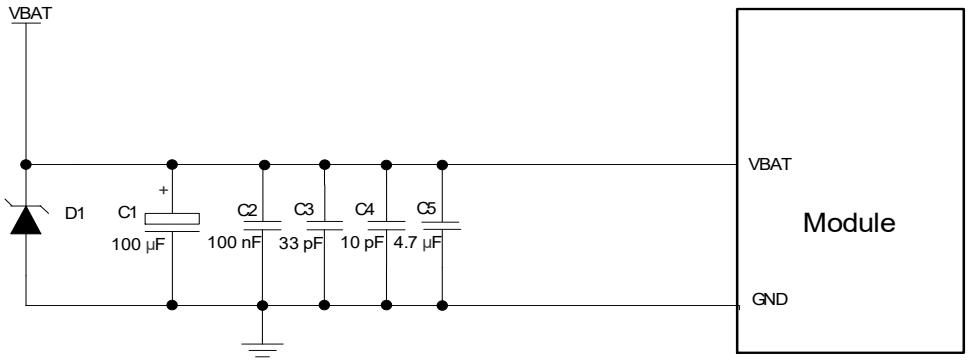


To prevent the voltage from dropping below 3.3 V, it is recommended to connect a 100 µF bypass capacitor with low ESR (ESR ≤ 0.7 Ω) as well as 100 nF, 33 pF and 10 pF filter capacitors. Additionally, add a 4.7 µF capacitor in parallel close to VBAT pins. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power.

The width of VBAT trace should be not less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power supply source, it is suggested to use a TVS and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows the structure of the power supply.

Figure 3: Structure of Power Supply



3.3. Turn On

3.3.1. Turn On with PWRKEY

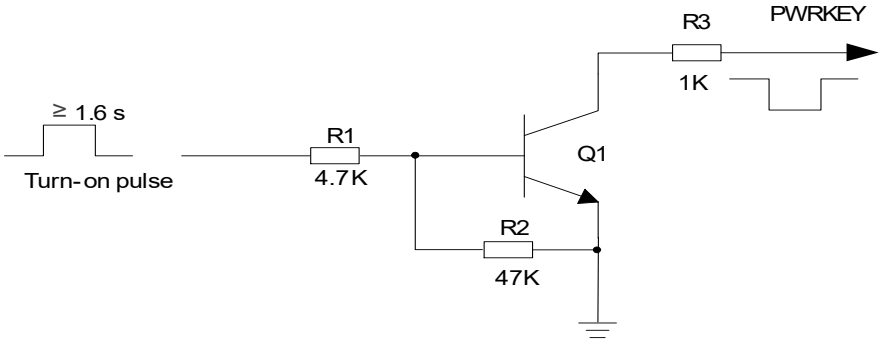
Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	1.8 V power domain.

The module can be turned on by driving the PWRKEY pin low for at least 1.6 s. PWRKEY is pulled up to 1.8 V internally.

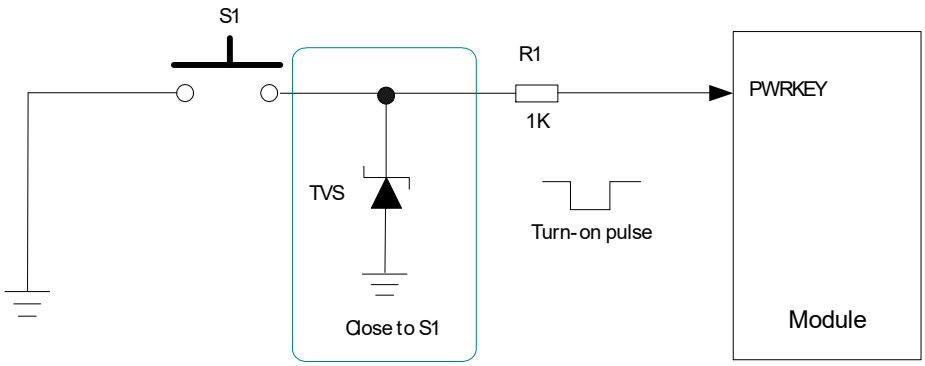
It is recommended to use an open collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

Figure 4: Turn On the Module Using Driving Circuit



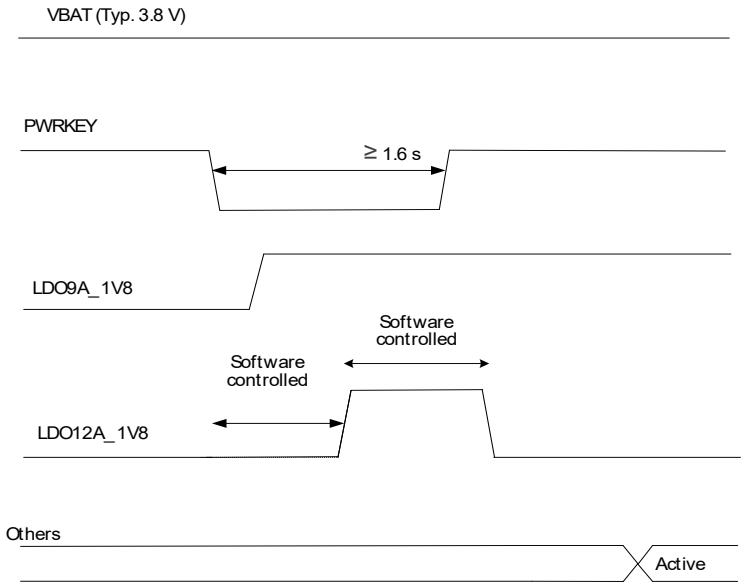
Another way to control PWRKEY is by using a button directly. You must place a TVS nearby the button and add a 1 kΩ resistor in series for ESD protection. A reference circuit is shown in the following figure.

Figure 5: Turn On the Module Using Button



The turn-on timing is illustrated in the following figure.

Figure 6: Turn-on Timing



NOTE

1. When the module is turned on for the first time, the timing may be different from that shown above.
2. Ensure the voltage of VBAT is stable before driving the PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 3.8 V and remains stable for 30 ms. PWRKEY cannot be driven low all the time.
3. Note that USB_VBUS cannot trigger the module to start.

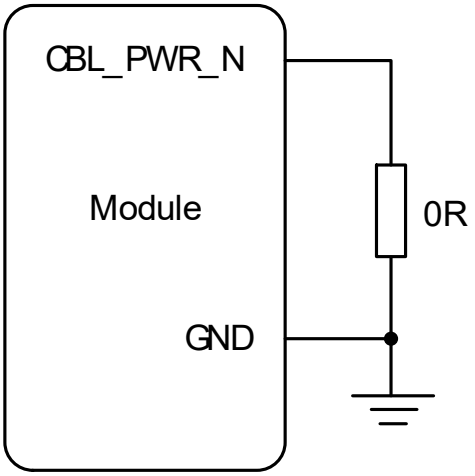
3.3.2. Turn On the Module Automatically

Table 9: Pin Definition of CBL_PWR_N

Pin Name	Pin No.	I/O	Description	Comment
CBL_PWR_N	240	DI	Initiate turning-on when grounded	1.8 V power domain. The module cannot be turned off when this pin is pulled down.

The module can be turned on automatically through CBL_PWR_N:

Figure 7: Turn On the Module Automatically



NOTE

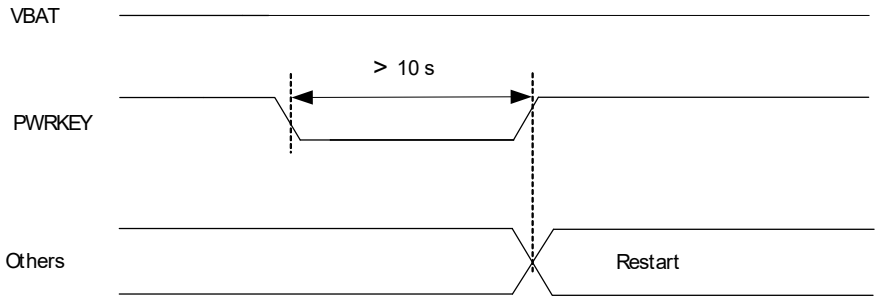
If the module turns on automatically through CBL_PWR_N pin, it cannot be turned off manually. In such case, it can be turned off only by cutting off the power supply of system.

3.4. Turn Off/Restart

The module can be turned off by driving the PWRKEY pin low for at least 1 s. Choose whether to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY low for at least 10 s. The module will execute the forced shut-down. The forced power-down timing is illustrated in the following figure.

Figure 8: Power-down Timing



3.5. VRTC

Table 10: Pin Definition of VRTC

Pin Name	Pin No.	I/O	Description
VRTC	16	PIO	Power supply for RTC

The RTC of the module can be powered by an external power supply pin VRTC. When VBAT is disconnected and you need to reserve RTC function, then VRTC cannot be kept unconnected. The RTC can be powered by an external power source when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

Figure 9: RTC Powered by a Rechargeable Cell Battery

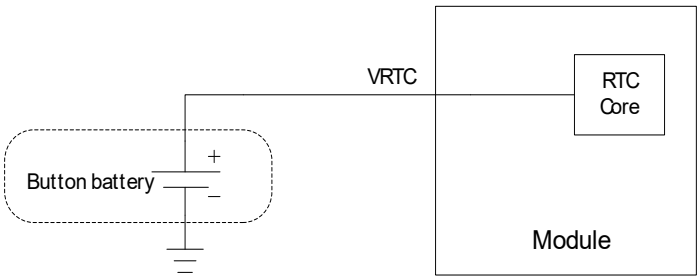
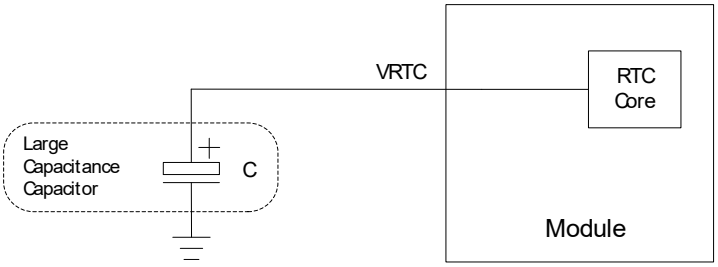


Figure 10: RTC Powered by Capacitor



- If RTC fails, the module can synchronize time over the network after being powered up.
- The recommended input voltage range for VRTC is 2.1–3.25 V and the recommended typical value is 3.0 V.
- When powered by VBAT, the RTC error is 50 ppm. When powered by VRTC, the RTC error is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.
- If you do not need RTC function, a 4.7 µF capacitor need to be connected to VRTC.

3.6. Power Output

The module supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 33 pF capacitor and a 10 pF capacitor in parallel in the circuit to suppress high-frequency noise.

Table 11: Power Description

Pin Name	Default Voltage (V)	Driving Current (mA)	@ Idle State
LDO9A_1V8	1.8	20	Keeps ON
LDO12A_1V8	1.8	300	-
LDO14A_1V8	1.8	600	-
ELDO1_2V8	2.8	300	-

ELDO2_2V85	2.85	300	-
LDO2C_1V1	1.1	800	-
LDO3C_2V8	2.8	300	-
LDO1C_1V2	1.2	800	-
USIM1_VDD	1.8/2.95	150	-
USIM2_VDD	1.8/2.95	150	-
SD_VDD	1.8/2.95	600	-
SD_PU_VDD	1.8/2.95	50	-

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with USB 3.1 Gen 1 and USB 2.0 specifications and supports USB OTG. It supports USB Type-C interface, DisplayPort mode and Micro USB interface. It also supports SuperSpeed mode (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps) and full-speed (12 Mbps) modes for USB 2.0. The USB interface is used for data communication with external AP, AT command transmission, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

4.1.1. USB Type-C Mode

The following table shows the pin definition of USB Type-C interface.

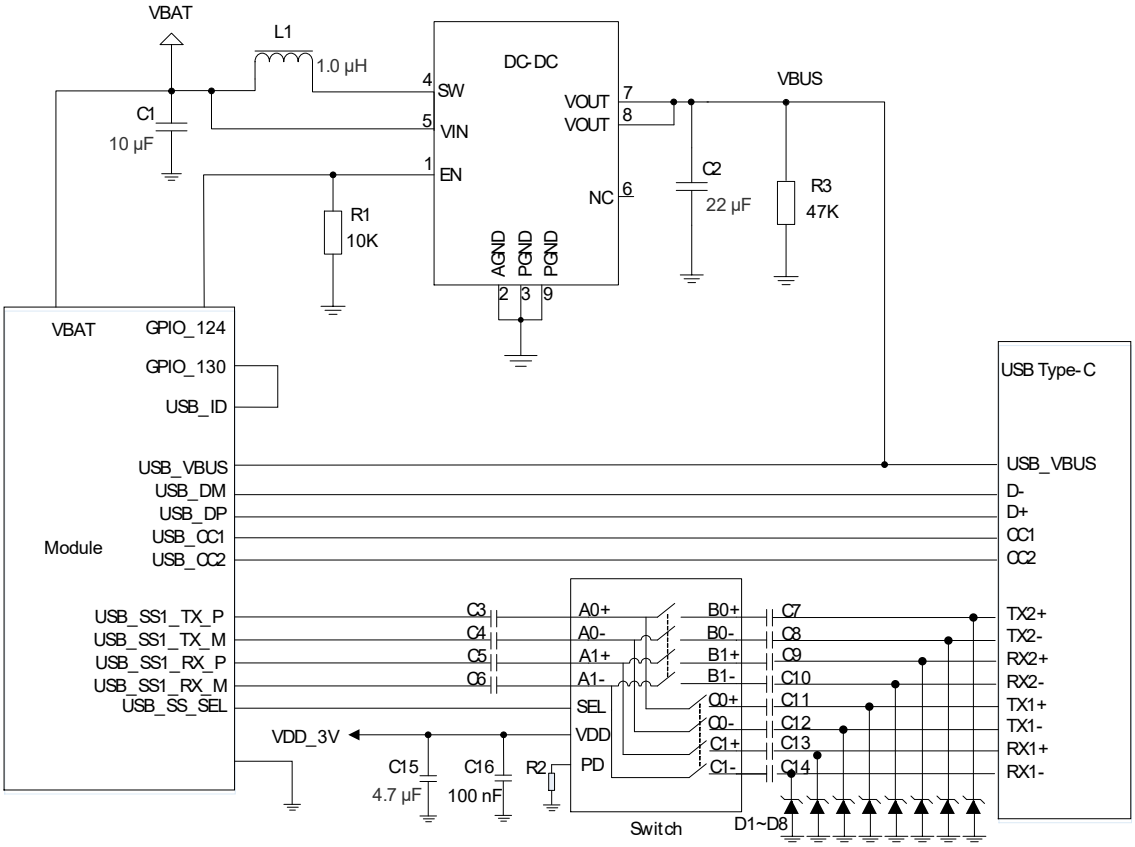
Table 12: Pin Definition of USB Type-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	AI	USB insertion interruption detect	A test point must be reserved.
USB_DP	32	AIO	USB 2.0 differential data (+)	USB 2.0 standard compliant. 90 Ω differential impedance. Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)	
USB_SS1_RX_P	171	AI	USB 3.1 channel 1 super-speed receive (+)	USB 3.1 Gen 1 compliant. 90 Ω differential impedance. USB Type-C (USB 3.1) interface use USB_SS1 by default. Insert front and back sides of USB through external switch. Use USB_SS1 and USB_SS2 to achieve functions of DisplayPort 1.4 interface.
USB_SS1_RX_M	172	AI	USB 3.1 channel 1 super-speed receive (-)	
USB_SS1_TX_P	174	AO	USB 3.1 channel 1 super-speed transmit (+)	
USB_SS1_TX_M	175	AO	USB 3.1 channel 1 super-speed transmit (-)	
USB_SS2_RX_P	162	AI	USB 3.1 channel 2 super-speed receive (+)	USB 3.1 Gen 1 compliant. 90 Ω differential impedance. Use USB_SS1 and USB_SS2 to achieve functions of DisplayPort 1.4 interface.
USB_SS2_RX_M	161	AI	USB 3.1 channel 2 super-speed receive (-)	
USB_SS2_TX_P	165	AO	USB 3.1 channel 2 super-speed transmit (+)	
USB_SS2_TX_M	164	AO	USB 3.1 channel 2 super-speed transmit (-)	
USB_CC1	224	AIO	USB Type-C detect 1	
USB_CC2	223	AIO	USB Type-C detect 2	
USB_SS_SEL	226	DO	USB Type-C switch control	
USB_ID	30	DO	USB 3.1 ID indication signal	USB Type-C interface USB ID status indicates output. High level by default.
GPIO_130	247	DI	USB ID interruption detect	Internal pull up by default.

NOTE

1. DisplayPort 1.4 interface is realized by using USB_SS1 and USB_SS2. For details, please see ***document 3***.
2. Master/Slave detection of USB Type-C (USB 3.1 Gen 1) interface is achieved by USB_CC1 or USB_CC2. USB_CC1 or USB_CC2 will control USB_ID and then notice GPIO_130 by USB_ID. When the inserted USB Type-C device is in slave mode, USB_ID will output low voltage level to pull GPIO_130 down and then notice the module to enter master mode. If OTG function is not needed, then USB_ID can be kept open.
3. USB Type-C (USB 3.1 Gen 1) interface uses USB_SS1 by default. Reverse insertion of USB can be achieved through external switch. Meanwhile, USB_SS1 and USB_SS2 can also help to achieve reverse insertion of USB. For details, please contact NetPrisma Technical Support.

Figure 11: USB Type-C Interface Reference Design



The USB interface of the module supports OTG function. If this function is required, please follow the design above to add an external 5 V power supply.

VDD_3V in the circuit is not the internal power supply of the platform, you can use an external LDO as the power supply.

4.1.2. Micro USB Interface

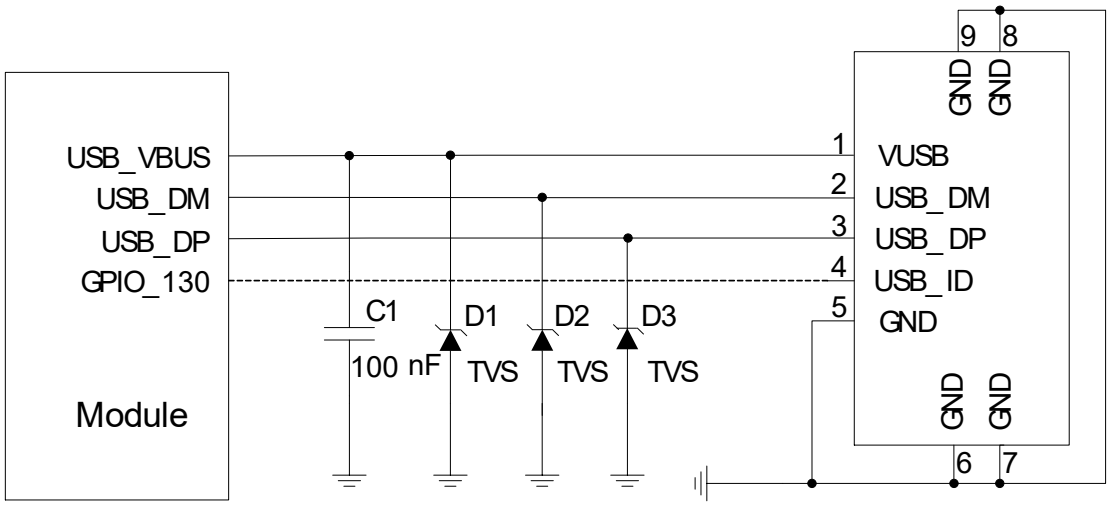
The following table shows the pin definition of Micro USB interface:

Table 13: Pin Definition of Micro USB

Pin Name	Pin No.	I/O	Description	Comment

USB_VBUS	41, 42	AI	USB insertion interruption detect	A test point must be reserved.
USB_DP	32	AIO	USB 2.0 differential data (+)	USB 2.0 standard compliant. 90 Ω differential impedance. Test points must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)	
GPIO_130	247	DI	USB ID interruption detect	Internal pull up by default.

Figure 12: Micro-USB Interface Reference Design



In the design of USB 2.0 interface, it is suggested to connect GPIO_130 directly to USB_ID of the external Micro USB interface to detect USB ID. When inserted device of the external Micro USB interface is in slave mode, USB_ID will output low voltage level to pull GPIO_130 down and then notice the module to enter master mode.

4.1.3. Design Principles for USB Interfaces

To ensure USB performance, comply with the following principles when designing the USB interface.

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- The reference ground plane under the USB signal traces must be continuous without any cuts or vias to ensure impedance continuity.
- Keep the ESD protection components as close as possible to the USB connector. Typically, stray capacitance should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1 Gen 1.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route USB 3.1 Gen 1 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden. Isolation between USB 3.1 Gen 1 signals and RF signals should be over 90 dB. Otherwise, the RF signals will be seriously affected.
- Ensure the intra-pair (P/M) trace length difference does not exceed 0.7 mm and that the inter-pair (RX/TX) trace length difference does not exceed 10 mm.
- Make sure the trace length difference between USB 2.0 DP and USB 2.0 DM differential pair does not exceed 2 mm.
- For USB 3.1 Gen 1, the spacing between Rx and Tx signal traces should be four times the signal trace width. The spacing between USB 3.1 signal trace and other signal traces should be four times the signal trace width. For USB 2.0, the spacing between DP and DM signal traces should be three times the signal trace width and the spacing between USB 2.0 signal traces and other signal traces should be four times the signal trace width.

Table 14: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Mismatch (DP-DM)
32	USB_DP	38.0	0.1
33	USB_DM	37.9	
171	USB_SS1_RX_P	42.7	-0.1
172	USB_SS1_RX_M	42.8	
174	USB_SS1_TX_P	27.0	0.2
175	USB_SS1_TX_M	26.8	
162	USB_SS2_RX_P	27.1	0.1
161	USB_SS2_RX_M	27.0	
165	USB_SS2_TX_P	34.0	0.1
164	USB_SS2_TX_M	33.9	

4.2. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported and either 1.8 V or 2.95 V (U)SIM card is supported. The pin definition of (U)SIM interface is shown below.

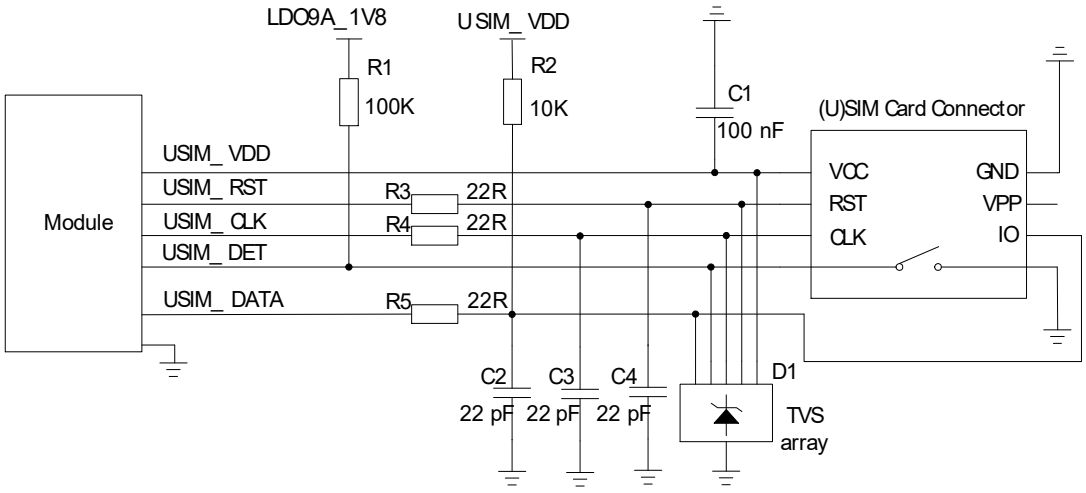
Table 15: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	141	PO	(U)SIM1 card power supply	Can recognize 1.8 V or 2.95 V (U) SIM card automatically. External capacitance shall not exceed 4 µF.
USIM1_DATA	142	DIO	(U)SIM1 card data	Pull it up to USIM1_VDD with an external 10 kΩ resistor. Cannot be multiplexed into a generic GPIO.
USIM1_CLK	143	DO	(U)SIM1 card clock	Cannot be multiplexed into a generic GPIO.
USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	Require external pull-up to LDO9A_1V8. Active low. If unused, keep it open. This function is disabled by default. Cannot be multiplexed into a generic GPIO.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.

				External capacitance shall not exceed 4 µF.
USIM2_DATA	209	DIO	(U)SIM2 card data	Pull it up to USIM2_VDD with an external 10 kΩ resistor. Cannot be multiplexed into a generic GPIO.
USIM2_CLK	208	DO	(U)SIM2 card clock	Cannot be multiplexed into a generic GPIO.
USIM2_RST	207	DO	(U)SIM2 card reset	
USIM2_DET	256	DI	(U)SIM2 card hot-plug detect	Require external pull-up to LDO9A_1V8. Active low. If unused, keep tit open. This function is disabled by default. Cannot be multiplexed into a generic GPIO.

The module supports (U)SIM card hot-plug via the USIM_DET. This function is disabled by default via software. To enable it, please contact NetPrisma Technical Support. A reference circuit for (U)SIM card interface with an 8-pin (U)SIM card connector is illustrated in the following figure.

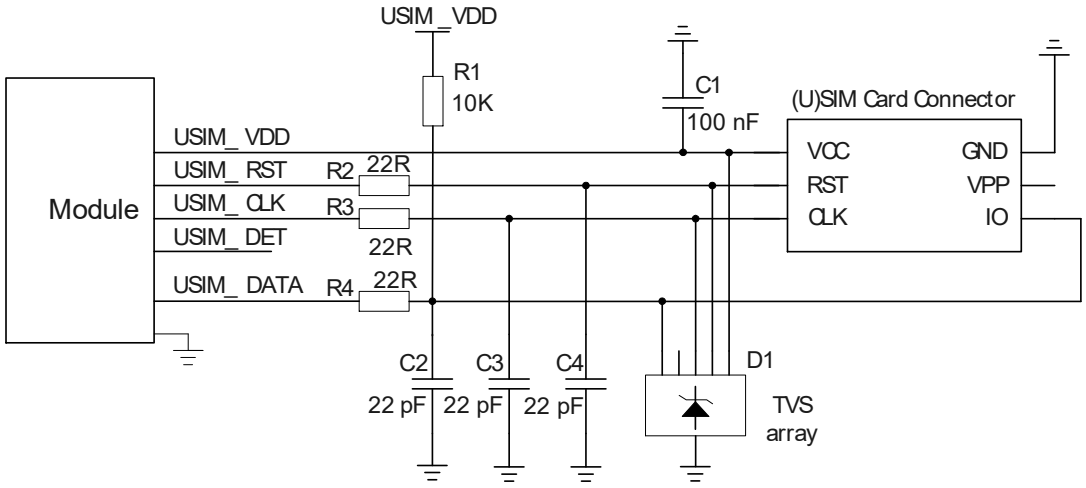
Figure 13: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector



If you do not need hot-plug detection, keep USIM1_DET and USIM2_DET pins open.

The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector.

Figure 14: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector



To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST also needs ground protection.
- To ensure good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 30 pF. Add 22 Ω resistors in series between the module and (U)SIM card to suppress EMI and enhance ESD protection. Add 22 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST signal traces to filter RF interference, and place them as close to the (U)SIM card connector as possible. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor close to the (U)SIM card connector.

4.3. SD Card Interface

The module supports SD 3.0 specifications and SD card hot-plug. The pin definition of the SD card interface is shown below.

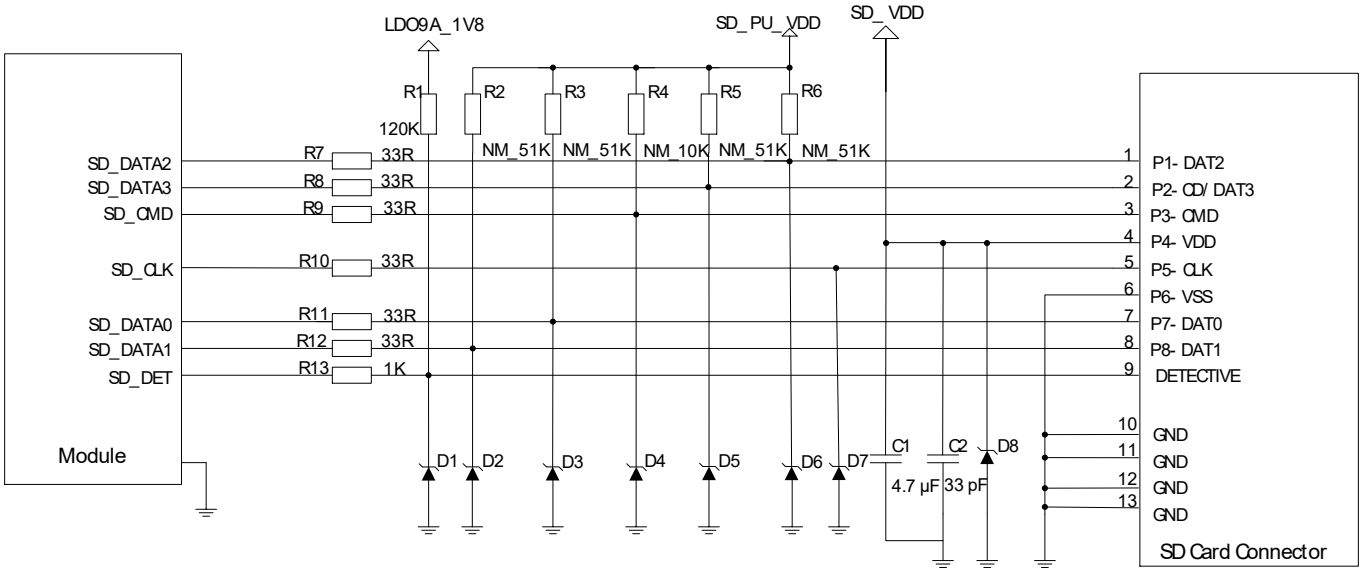
Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	70	DO	SD card clock	
SD_CMD	69	DIO	SD card command	
SD_DATA0	68	DIO	SDIO data bit 0	Control characteristic impedance as 50 Ω.
SD_DATA1	67	DIO	SDIO data bit 1	
SD_DATA2	66	DIO	SDIO data bit 2	

SD_DATA3	65	DIO	SDIO data bit 3	
SD_DET	64	DI	SD card hot-plug detect	Active low. Require external pull-up to LDO9A_1V8.
SD_VDD	63	PO	SD card power supply	External capacitance shall not exceed 13.5 µF.
SD_PU_VDD	179	PO	SD card pull-up power; supply 1.8/2.95 V output	Only for SD card pull-up, maximum power supply is 50 mA. External capacitance shall not exceed 4 µF.

A reference circuit for the SD card interface is shown below.

Figure 15: Reference Design for SD Card Interface



SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended that the trace width is 0.5 mm or above. To ensure the stability of drive power, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 50 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB. Additionally, SD_CLK needs ground shielding separately.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- Trace length difference between SD_CLK and SD_CMD/SD_DATA should be less than 2 mm.
- Trace length requirements: less than 150 mm for traces of 50 Mbps; less than 50 mm for traces of 104 Mbps.
- The spacing between signal traces should be 1.5 times the trace width.
- The capacitive reactance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 8 pF.
- The capacitive reactance of D1–D7 should be less than 5 pF.

Table 17: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
70	SD_CLK	63.9

69	SD_CMD	63.9
68	SD_DATA0	64.2
67	SD_DATA1	63.9
66	SD_DATA2	64.4
65	SD_DATA3	64.0

4.4. GPIO Interfaces

The module has abundant GPIO interfaces with a power domain of 1.8 V. The pin definition is listed below.

Table 18: Pin Definition of GPIOs

Pin Name	Pin No.	I/O	Description	Comment
GPIO_8	227	DIO	General-purpose input/output	
GPIO_9	228	DIO		Support wakeup interrupt.
GPIO_26	136	DIO		
GPIO_27	137	DIO		
GPIO_43	238	DIO		
GPIO_83	200	DIO		
GPIO_84	201	DIO		
GPIO_85	237	DIO		Support wakeup interrupt.
GPIO_95	113	DIO		
GPIO_97	114	DIO		
GPIO_117	213	DIO		
GPIO_119	234	DIO		
GPIO_123	230	DIO		Support wakeup interrupt.
GPIO_124	229	DIO		
GPIO_125	232	DIO		
GPIO_126	231	DIO		Support wakeup interrupt.
GPIO_127	178	DIO		
GPIO_128	177	DIO		Support wakeup interrupt.

GPIO_130	247	DIO
GPIO_131	248	DIO

NOTE

For more details about GPIO configuration, see ***document 1***.

4.5. UART Interfaces

The module supports up to five groups of UART interfaces. Three of them are default configurations, see ***Table 19***. Two of them are multiplexed from other interfaces, see ***Table 23***.

Three UART interfaces:

- UART00: 4-wire UART interface, supporting RTS and CTS hardware flow control, up to 4 Mbps;
- Debug UART: 2-wire UART interface, dedicated for debugging by default;
- UART03: 2-wire UART interface.

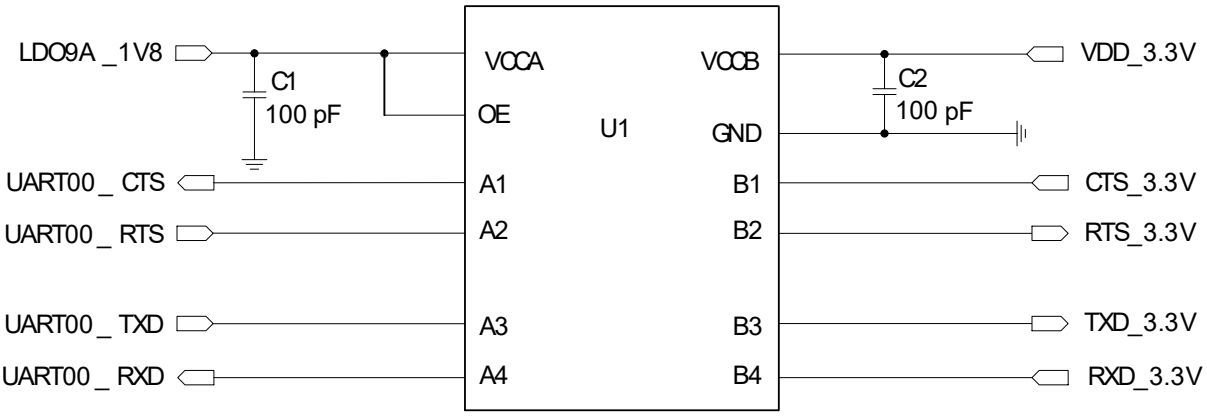
Pin definition of the UART interface is here as follows:

Table 19: Pin Definition of UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	5	DO	Debug UART transmit.	1.8 V power domain. If unused, keep them open. Test points must be reserved.
DBG_RXD	6	DI	Debug UART receive.	
UART03_TXD	7	DO	UART03 transmit	1.8 V power domain. If unused, keep them open.
UART03_RXD	8	DI	UART03 receive	
UART00_TXD	199	DO	UART00 transmit	1.8 V power domain. If unused, keep them open. When UART00_RTS and UART00_CTS are multiplexed into I2C, UART00_TXD and UART00_RXD can only be used as generic GPIO.
UART00_RXD	198	DI	UART00 receive	
UART00_RTS	245	DO	Request to send signal from the module	
UART00_CTS	246	DI	Clear to send signal to the module	

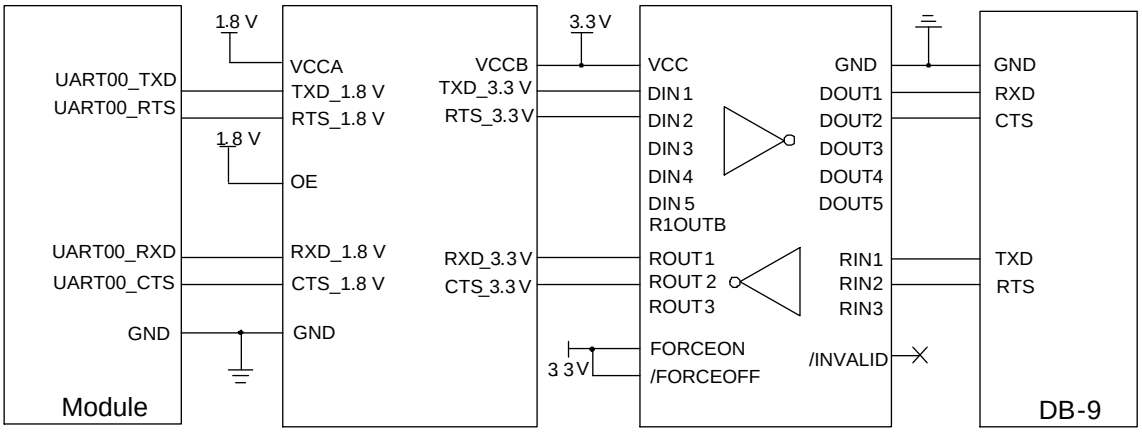
UART00 is a 4-wire UART interface with 1.8 V power domain. A level-shifting chip should be used if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

Figure 16: Reference Design of UART with Level-shifting Chip (for UART00)



A voltage-level translator and an RS-232 level-shifting chip are recommended to be added between the module and PC. The following figure shows a reference design.

Figure 17: Reference Design of UART with RS-232 Level-shifting Chip (for UART00)



NOTE

The debug UART and UART03 are similar to UART00. For the reference designs, please refer to UART00.

4.6. SPI

The module provides four groups of SPI which only support master mode. It can be used for fingerprint recognition. Two of them are default configurations, see ***Table 20***; The other two of them are multiplexed from other interfaces, see ***Table 23***.

Table 20: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI10_CS	58	DO	SPI10 chip select	1.8 V power domain; Support master mode only.
SPI10_CLK	59	DO	SPI10 clock	
SPI10_MOSI	60	DO	SPI10 master-out slave-in	

SPI10_MISO	61	DI	SPI10 master-in slave-out
SPI13_CS	203	DO	SPI13 chip select
SPI13_CLK	250	DO	SPI13 clock
SPI13_MOSI	249	DO	SPI13 master-out slave-in
SPI13_MISO	251	DI	SPI13 master-in slave-out

4.7. I2C Interfaces

The module provides eight groups of I2C interfaces. Three of them are dedicated I2C interfaces used for cameras and sensors. Two of them are generic I2C interfaces used for TPs and other peripherals, see ***Table 21***; three of them are multiplexed from other interfaces, see ***Table 23***.

All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The sensor I2C interface only supports sensors of aDSP architecture. CAM_I2C and DCAM_I2C signals are controlled by Linux Kernel code and support connection to video-output-related devices.

Table 21: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CAM_I2C_SCL	75	OD	I2C clock of front and rear camera,	1.8 V power domain. Dedicated for camera only. External pull-up is required. Cannot be multiplexed into a generic GPIO
CAM_I2C_SDA	76	OD	I2C data of front and rear camera	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	
DCAM_I2C_SDA	197	OD	I2C data of depth camera	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	1.8 V power domain. Dedicated for external sensor. Cannot be multiplexed into a generic GPIO External pull-up is required.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	
I2C11_SCL	205	OD	I2C serial clock	1.8 V power domain. External pull-up is required.
I2C11_SDA	204	OD	I2C serial data	
TP_I2C_SCL	140	OD	TP I2C clock	
TP_I2C_SDA	206	OD	TP I2C data	

4.8. I2S Interfaces

The module supports up to three groups of I2S interfaces. One of them is default configuration, and the power domain is 1.8 V, see ***Table 22***. Two of them are multiplexed from other interfaces, see ***Table 23***.

Table 22: Pin Definition of I2S Interface

Pin Name	Pin No.	I/O	Description	Comment
MI2S_DATA1	155	DIO	I2S data channel 0	1.8 V power domain.
MI2S_DATA0	154	DIO	I2S data channel 1	
MI2S_WS	156	DO	I2S word select	
MI2S_SCLK	212	DO	I2S serial clock	
GPIO_119	234	DIO	General-purpose input/output	1.8 V power domain. Can be used as I2S master clock

4.9. Multiplexing Relationship of UART/SPI/I2C/I2S

The module supports six groups of configurable functional interfaces, which can be configured into UART, SPI, I2C or I2S interfaces. For details, see the table below (dedicated I2C interfaces, debug UART and interfaces those are already used inside the module are not included):

Table 23: Multiplexing Relationship of UART/SPI/I2C/I2S

Channel	Pin No.	Pin Name	GPIO No.	Multiplexing Function			
				UART	SPI	I2C	I2S
QUP0-SE0	246	UART00_CTS	GPIO_0	UART00_CTS	SPI00_MISO	I2C00_SDA	-
	245	UART00_RTS	GPIO_1	UART00_RTS	SPI00_MOSI	I2C00_SCL	-
	199	UART00_TXD	GPIO_2	UART00_TXD	SPI00_CLK	-	-
	198	UART00_RXD	GPIO_3	UART00_RXD	SPI00_CS	-	-
QUP0-SE2	206	TP_I2C_SDA	GPIO_6	UART02_CTS	SPI02_MISO	I2C02_SDA	-
	140	TP_I2C_SCL	GPIO_7	UART02_RTS	SPI02_MOSI	I2C02_SCL	-
	227	GPIO_8	GPIO_8	UART02_TXD	SPI02_CLK	-	-
	228	GPIO_9	GPIO_9	UART02_RXD	SPI02_CS	-	-
QUP0-SE3	7	UART03_TXD	GPIO_14	UART03_TXD	-	I2C03_SDA	-
	8	UART03_RXD	GPIO_15	UART03_RXD	-	I2C03_SCL	-
QUP1-SE0	61	SPI10_MISO	GPIO_22	UART10_CTS	SPI10_MISO	I2C10_SDA	-
	60	SPI10_MOSI	GPIO_23	UART10_RTS	SPI10_MOSI	I2C10_SCL	-
	59	SPI10_CLK	GPIO_24	UART10_TXD	SPI10_CLK	-	-
	58	SPI10_CS	GPIO_25	UART10_RXD	SPI10_CS	-	-
QUP1-SE1	204	I2C11_SDA	GPIO_30	-	-	I2C11_SDA	-
	205	I2C11_SCL	GPIO_31	-	-	I2C11_SCL	-

QUP1-SE3	251	SPI13_MISO	GPIO_18	-	SPI13_MISO	-	I2S2_SCLK
	249	SPI13_MOSI	GPIO_19	-	SPI13_MOSI	-	I2S2_WS
	250	SPI13_CLK	GPIO_20	-	SPI13_CLK	-	I2S2_DATA0
	203	SPI13_CS	GPIO_21	-	SPI13_CS	-	I2S2_DATA1
-	232	GPIO_125	GPIO_125	-	-	-	I2S1_SCLK
-	231	GPIO_126	GPIO_126	-	-	-	I2S1_WS
-	178	GPIO_127	GPIO_127	-	-	-	I2S1_DATA0
-	177	GPIO_128	GPIO_128	-	-	-	I2S1_DATA1
-	212	MI2S_SCLK	GPIO_113	-	-	-	-
-	156	MI2S_WS	GPIO_114	-	-	-	-
-	154	MI2S_DATA0	GPIO_115	-	-	-	-
-	155	MI2S_DATA1	GPIO_116	-	-	-	-

NOTE

1. The module supports QUP-SE channel and I2S interface, and QUP-SE channel can be used flexibly, and it supports UART, SPI, and I2C interfaces.
2. Note that QUP SE interfaces in the same group cannot support two protocols. For instance: QUP in the same group cannot support UART and I2C at the same time. If one protocol only occupies parts of pins in one group of QUP, then other pins in this group can only be used as GPIO.
3. MI2S in the table is the default interface. I2S1 interface is configured from default GPIO. To allocate interfaces more conveniently, they are all listed in the table.

4.10. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces and the pin definition is shown below. The ADC interfaces support resolution of up to 15 bits.

Table 24: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	151	AI	General-purpose ADC interface	1.8 V power domain.
ADC1	153	AI		

4.11. LCM Interface

The module provides one LCM interface, which is MIPI_DSI standard compliant. The interface supports one group of 4-lane high-speed differential data transmission with maximum speed rate of 1.5 Gbps/lane

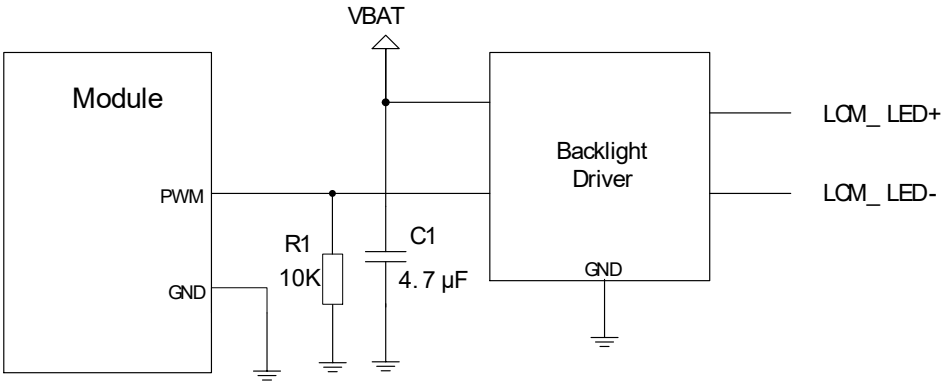
and supports HD+ display (1920 x 1200 @ 60 fps or 1080 x 2520 @ 60 fps). The pin definition of the LCM interface is shown below.

Table 25: Pin Definition of LCM

Pin Name	Pin No.	I/O	Description	Comment
LDO12A_1V8	10	PO	1.8 V output (Power supply for I/O of cameras, LCM and sensors)	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 9 µF. If unused, keep them open.
ELDO2_2V85	12	PO	2.85 V output (Power supply for LCM and camera's AFVDD)	
DSI_CLK_P	115	AO	LCD MIPI clock (+)	Require differential impedance of 100 Ω.
DSI_CLK_N	116	AO	LCD MIPI clock (-)	
DSI_LN0_P	117	AO	LCD MIPI lane 0 data (+)	
DSI_LN0_N	118	AO	LCD MIPI lane 0 data (-)	
DSI_LN1_P	119	AO	LCD MIPI lane 1 data (+)	
DSI_LN1_N	120	AO	LCD MIPI lane 1 data (-)	
DSI_LN2_P	121	AO	LCD MIPI lane 2 data (+)	
DSI_LN2_N	122	AO	LCD MIPI lane 2 data (-)	
DSI_LN3_P	123	AO	LCD MIPI lane 3 data (+)	
DSI_LN3_N	124	AO	LCD MIPI lane 3 data (-)	
LCD_TE	126	DI	LCD tearing effect	1.8 V power domain.
LCD_RST	127	DO	LCD reset	1.8 V power domain. External pull-up is not required.
PWM	152	DO	PWM output	Voltage shall be the same as VBAT. Cannot be multiplexed into a generic GPIO.

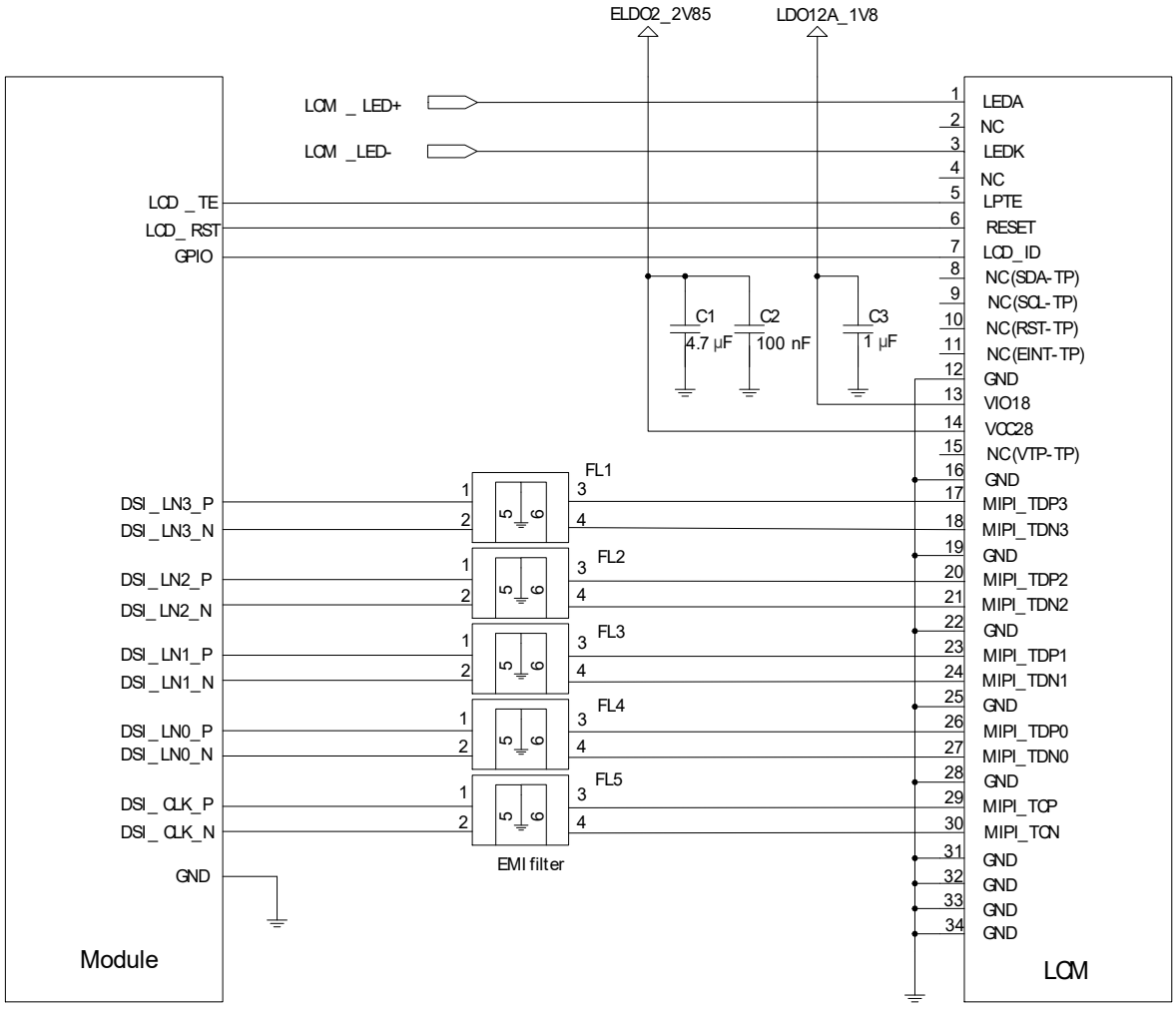
You can design external backlight drive circuit for LCM according to actual requirement. The reference designs are shown in the figures below, in which PWM (pin 152) is used for backlight brightness adjustment.

Figure 18: LCM External Backlight Driver Reference Design



A reference circuit for the LCM interface is shown below.

Figure 19: Reference Design for LCM Interface



MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that the LCM factory should burn an OTP register to distinguish different screens.

4.12. Touch Panel Interface

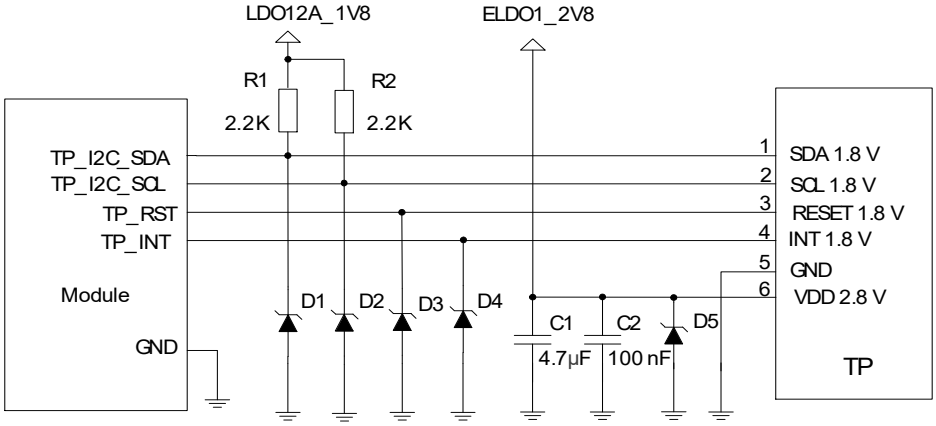
The module provides one group of I2C interfaces for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins. The definitions of TP interface pins are illustrated below.

Table 26: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
LDO12A_1V8	10	PO	1.8 V output (Power supply for I/O of cameras, LCM and sensors)	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 9 µF. If unused, keep them open.
ELDO1_2V8	11	PO	2.8 V output (Power supply for external cameras and LCM)	
TP_RST	138	DO	TP reset	1.8 V power domain; For TP_RST: it cannot be pulled up during module's turning on process; For TP_I2C: external pull-up is required.
TP_INT	139	DI	TP interrupt	
TP_I2C_SCL	140	OD	TP I2C clock	
TP_I2C_SDA	206	OD	TP I2C data	

A reference design for TP interface is shown below.

Figure 20: Reference Design for TP0 Interface



4.13. Camera Interfaces

Based on MIPI_CSI, the module supports three cameras (4-lane + 4-lane + 4-lane) with the speed rate of up to 2.1 Gbps/lane. Each camera (4-lane) can be divided into 2-lane + 1-lane. The module supports up to six cameras (up to two cameras at the same time) and up to 16 MP + 16 MP or 24 MP with dual ISP. The video and photo quality are determined by various factors such as the camera sensor, camera lens quality. Pin definition of camera interface is shown in the table below:

Table 27: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment

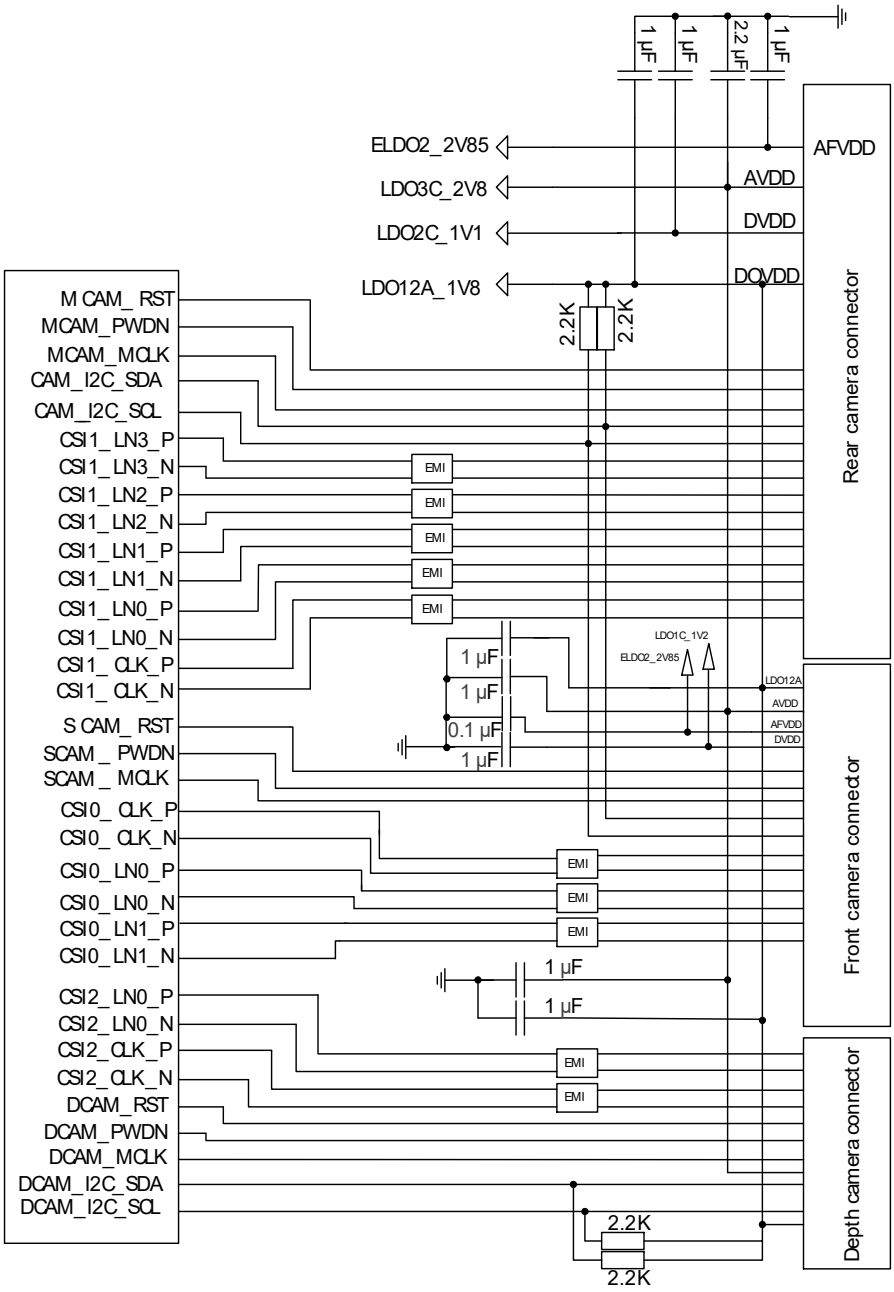
CSI0_CLK_P	77	AI	MIPI CSI0 clock (+)	Require differential impedance of 100 Ω. Used for front camera by default.
CSI0_CLK_N	78	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	79	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	80	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	81	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	82	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	83	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN2_N	84	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN3_P	85	AI	MIPI CSI0 lane 3 data (+)	
CSI0_LN3_N	86	AI	MIPI CSI0 lane 3 data (-)	
CSI1_CLK_P	88	AI	MIPI CSI1 clock (+)	Require differential impedance of 100 Ω. Used for rear camera by default.
CSI1_CLK_N	89	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	90	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN0_N	91	AI	MIPI CSI1 lane 0 data (-)	
CSI1_LN1_P	92	AI	MIPI CSI1 lane 1 data (+)	
CSI1_LN1_N	93	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN2_P	94	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN2_N	95	AI	MIPI CSI1 lane 2 data (-)	
CSI1_LN3_P	96	AI	MIPI CSI1 lane 3 data (+)	
CSI1_LN3_N	97	AI	MIPI CSI1 lane 3 data (-)	
CSI2_CLK_P	183	AI	MIPI CSI2 clock (+)	Require differential impedance of 100 Ω. Used for depth camera by default.
CSI2_CLK_N	184	AI	MIPI CSI2 clock (-)	
CSI2_LN0_P	185	AI	MIPI CSI2 lane 0 data (+)	
CSI2_LN0_N	186	AI	MIPI CSI2 lane 0 data (-)	
CSI2_LN1_P	187	AI	MIPI CSI2 lane 1 data (+)	
CSI2_LN1_N	188	AI	MIPI CSI2 lane 1 data (-)	
CSI2_LN2_P	189	AI	MIPI CSI2 lane 2 data (+)	Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI data (+).

CSI2_LN2_N	190	AI	MIPI CSI2 lane 2 data (-)	Require differential impedance of 100 Ω. Used for depth camera by default. Can be multiplexed into the 4th camera's MIPI data (-).
CSI2_LN3_P	191	AI	MIPI CSI2 lane 3 data (+)	Require differential impedance of 100 Ω. Used for depth camera by default Can be multiplexed into the 4th camera's MIPI clock (+).
CSI2_LN3_N	192	AI	MIPI CSI2 lane 3 data (-)	Require differential impedance of 100 Ω. Used for depth camera by default Can be multiplexed into the 4th camera's MIPI clock (-).
MCAM_MCLK	99	DO	Master clock of rear camera	1.8 V power domain.
SCAM_MCLK	100	DO	Master clock of front camera	
DCAM_MCLK	194	DO	Master clock of depth camera	
CAM4_MCLK	236	DO	Master clock of the 4th camera	
MCAM_RST	74	DO	Reset of rear camera	
SCAM_RST	72	DO	Reset of front camera	
DCAM_RST	180	DO	Reset of depth camera	
MCAM_PWDN	73	DO	Power down of rear camera	
SCAM_PWDN	71	DO	Power down of front camera	
DCAM_PWDN	181	DO	Power down of depth camera	
LDO2C_1V1	13	PO	1.1 V output (Power supply for DVDD of rear cameras)	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 15.3 µF. If unused, keep it open. Power supply only for cameras.
LDO3C_2V8	14	PO	2.8 V output (Power supply for AVDD of cameras)	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 47.8 µF. If unused, keep it open. Power supply only for cameras.
LDO1C_1V2	15	PO	1.2 V output (Power supply for DVDD of front cameras)	Add a 1.0–4.7 µF bypass capacitor if used. Total capacitance cannot exceed 15.3 µF. If unused, keep it open. Power supply only for cameras.
ELDO2_2V85	12	PO	2.85 V output	Add a 1.0–4.7 µF bypass capacitor if used.

			(Power supply for LCM and camera's AFVDD)	Total capacitance cannot exceed 9 µF. If unused, keep them open.
LDO12A_1V8	10	PO	1.8 V output (Power supply for I/O of cameras, LCM and sensors)	
CAM_I2C_SCL	75	OD	I2C clock of front and rear camera	1.8 V power domain. External pull-up is required. Dedicated for camera only. Cannot be multiplexed into a generic GPIO.
CAM_I2C_SDA	76	OD	I2C data of front and rear camera	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	
DCAM_I2C_SDA	197	OD	I2C data of depth camera	

The following is a reference design for three-camera applications.

Figure 21: Reference Design for Three-Camera Applications



NOTE

1. The module supports three groups of CSI. CSI0 is used for front camera by default, CSI1 is used for rear camera and CSI2 is used for depth camera by default.
2. CSI2_LN2_P, CSI2_LN2_N, CSI2_LN3_P and CSI2_LN3_N can be multiplexed into the MIPI signal traces of the 4th camera. In this circumstance, the related RST and PWDN signals use generic GPIO configurations.
3. The module supports up to 2-lane simultaneously transmission (up to 16 MP for each lane).

MIPI design considerations:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate of up to 2.1 Gbps for CSI and up to 1.5 Gbps for DSI. The differential impedance should be controlled to 100 Ω. Additionally, it is

recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces of the same length.

- Make sure the reference ground plane for CSI/DSI is complete and integral, without any cut or void.
- Route the camera CLK signals in the inner layer of the PCB and surround them with ground.
- Route CSI and DSI traces according to the following rules:
  a) The intra-pair (P/N) spacing should be 1 time the trace width.
  b) The inter-lane spacing should be 1.5 times the trace width.
  c) The spacing to other signal traces should be 2.5 times the trace width.
- Route MIPI traces according to the following rules:
  a) Control the differential impedance to 100 Ω ±10 %.
  b) Control intra-lane(P/N) length difference within 0.7 mm;
  c) Control inter-lane length difference within 1.4 mm (For CSI2, trace length between lanes needs to be controlled on your baseboard as a whole).

Table 28: Relationship Between CSI Rate and Trace Length (D-PHY)

Data rate	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 125
1.5 Gbps/lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/lane	76.2	-1.3	< 170
	152.4	-2.3	< 90

Table 29: Relationship Between DSI Rate and Trace Length (D-PHY)

Data rate	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.8	< 280
	152.4	-1.4	< 210
750 Mbps/lane	76.2	-1	< 210
	152.4	-1.5	< 150
1.0 Gbps/lane	76.2	-1.1	< 200
	152.4	-1.7	< 100
1.5 Gbps/lane	76.2	-1.2	< 135

152.4	-2.2	< 40

NOTE

1. The cable length listed above is an example with specified insertion loss.
2. The cable insertion loss can be obtained from the cable datasheet provided by the related manufacturer. The cable insertion loss on the design should not be worse than what is listed in this table.
3. The length in the above table includes the length of the trace inside the module.

Table 30: Trace Length of MIPI Differential Pairs Inside the Module

Pin No.	Signal	Length (mm)	Length Mismatch (P-N) (mm)
115	DSI_CLK_P	49.2	-0.5
116	DSI_CLK_N	49.7	
117	DSI_LN0_P	49.2	0.2
118	DSI_LN0_N	49.0	
119	DSI_LN1_P	49.3	0
120	DSI_LN1_N	49.3	
121	DSI_LN2_P	49.1	0.1
122	DSI_LN2_N	49.0	
123	DSI_LN3_P	48.8	0.3
124	DSI_LN3_N	48.5	
77	CSI0_CLK_P	25.2	0
78	CSI0_CLK_N	25.2	
79	CSI0_LN0_P	25.2	0
80	CSI0_LN0_N	25.2	
81	CSI0_LN1_P	25.2	0
82	CSI0_LN1_N	25.2	
83	CSI0_LN2_P	25.2	0
84	CSI0_LN2_N	25.2	
85	CSI0_LN3_P	25.3	0.1

86	CSI0_LN3_N	25.2		
88	CSI1_CLK_P	16.2	0	
89	CSI1_CLK_N	16.2		
90	CSI1_LN0_P	16.2	0	
91	CSI1_LN0_N	16.2		
92	CSI1_LN1_P	16.2	0	
93	CSI1_LN1_N	16.2		
94	CSI1_LN2_P	16.2	-0.2	
95	CSI1_LN2_N	16.4		
96	CSI1_LN3_P	16.1	0.1	
97	CSI1_LN3_N	16.0		
183	CSI2_CLK_P	16.6	-0.1	
184	CSI2_CLK_N	16.7		
185	CSI2_LN0_P	15.7	0.2	
186	CSI2_LN0_N	15.5		
187	CSI2_LN1_P	11.8	-0.3	
188	CSI2_LN1_N	12.1		
189	CSI2_LN2_P	5.6	-0.3	
190	CSI2_LN2_N	5.9		
191	CSI2_LN3_P	2.5	-0.3	
192	CSI2_LN3_N	2.8		

4.14. Sensor Interfaces

The module supports communication with sensors via I2C interfaces, and it supports ALS/PS, compass, accelerometer, gyroscope, etc. Pin definition of sensor interfaces are shown below:

Table 31: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ALPS_INT	253	DI	Light/proximity sensor interrupt	1.8 V power domain.

ACCL_INT	252	DI	Acceleration sensor interrupt	
GYRO_INT	255	DI	Gyroscope sensor interrupt	
MAG_INT	254	DI	Geomagnetic sensor interrupt	
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	1.8 V power domain. Dedicated for external sensors. Cannot be used for touch panel, NFC, I2C keyboard, etc. Cannot be multiplexed into a generic GPIO.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	

4.15. Audio Interfaces

The module provides three analog input channels and three analog output channels. The following table shows the pin definition.

Table 32: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC1_P	44	AI	Microphone input for channel 1 (+)	Integrated with internal bias voltage
MIC1_M	45	AI	Microphone input for channel 1 (-)	
MIC2_P	46	AI	Microphone input for headset (+)	
MIC3_P	169	AI	Microphone input for headset (+)	Integrated without internal bias voltage
MIC_GND	168		Microphone reference ground	If unused, connect it to ground.
MIC_BIAS1	167	AO	Bias voltage 1 output for microphone	
MIC_BIAS3	28	AO	Bias voltage 3 output for microphone	
HS_DET	48	AI	Headset hot-plug detect	Cannot be externally pulled up.
HPH_L	49	AO	Headphone left channel output	
HPH_GND	50		Headphone reference ground	If unused, connect it to ground.
HPH_R	51	AO	Headphone right channel output	
EAR_M	52	AO	Earpiece output (-)	
EAR_P	53	AO	Earpiece output (+)	
SPK_M	54	AO	Loudspeaker output (-)	
SPK_P	55	AO	Loudspeaker output (+)	

- The module offers three audio input channels, including one differential input channel and two single ended input channels. MIC1/MIC2 has internal bias voltage. MIC3 has no internal bias voltage.

- Two MIC_BIAS output. The output voltage range is programmable between 1.0 V to 2.85 V, and the maximum output current is 6 mA. Both MIC_BIAS can supply power to the MEMS microphone.
- The earpiece interface uses differential output.
- The loudspeaker interface uses the differential output as well. The output channel is available with a Class-K amplifier whose output power is 1.2 W when load is 8 Ω.
- The headphone interface features stereo left and right channel output, and supports headphone insertion detect.

4.15.1. Reference Design for Microphone Interfaces

Figure 22: Reference Design for ECM Microphone Interface

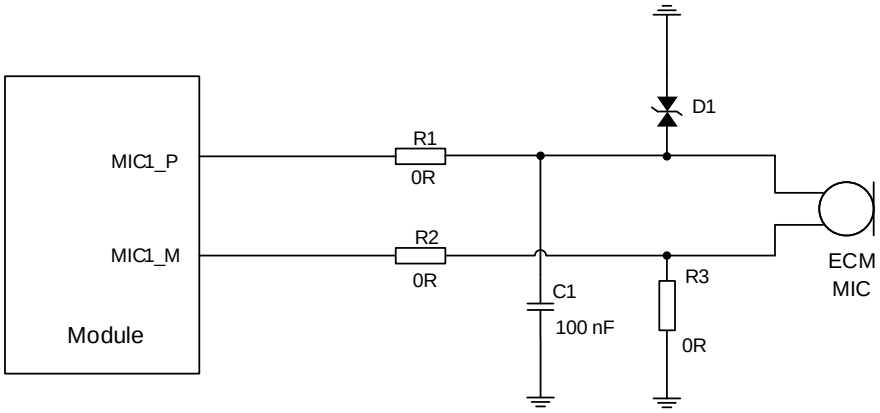
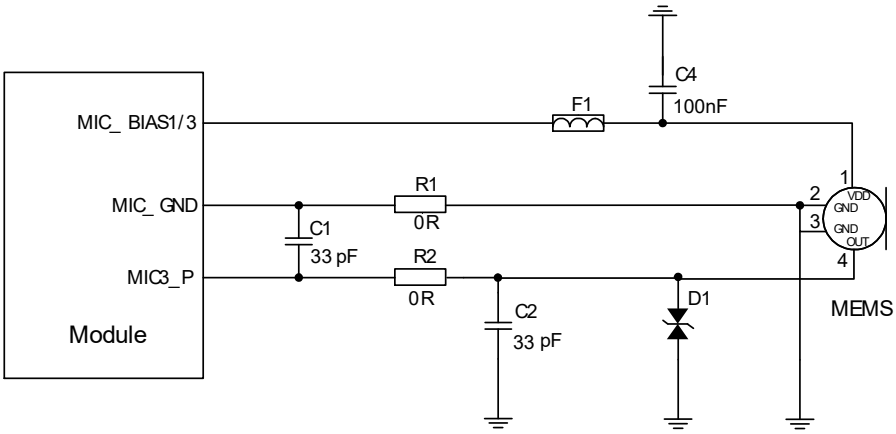
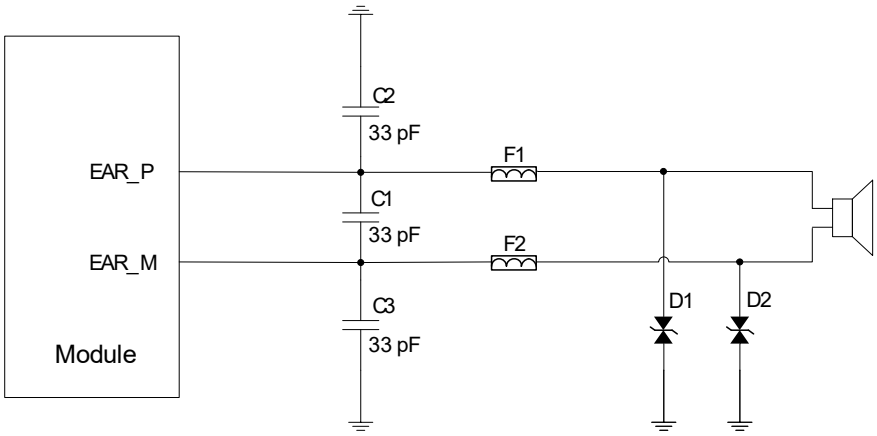


Figure 23: Reference Design for MEMS Microphone Interface



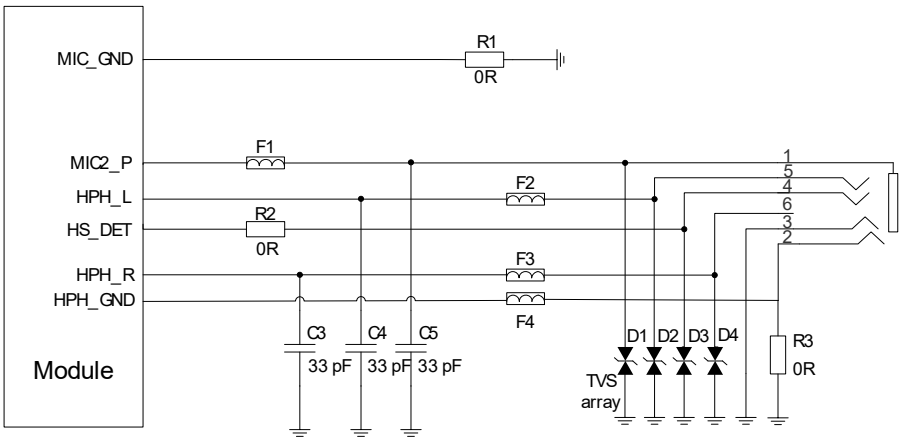
4.15.2. Reference Design for Headset Interface

Figure 24: Reference Design for Headset Interface



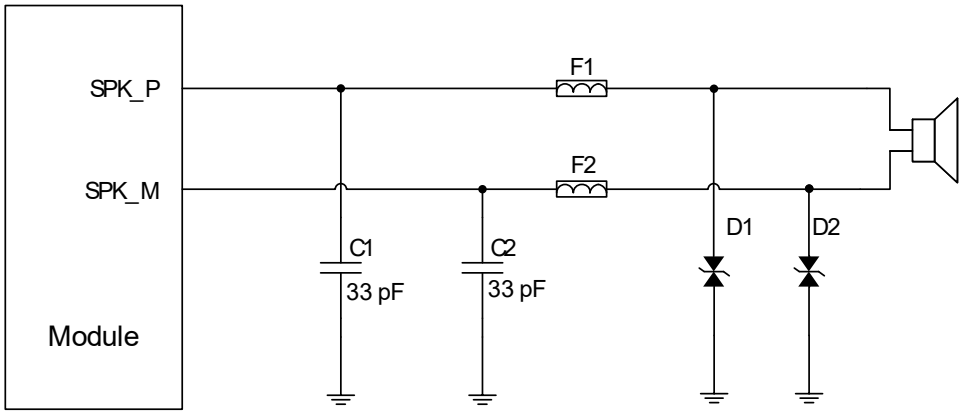
4.15.3. Reference Design for Headphone Interface

Figure 25: Reference Design for Headphone Interface



4.15.4. Reference Design for Loudspeaker Interface

Figure 26: Reference Design for Loudspeaker Interface



4.15.5. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without these capacitors, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

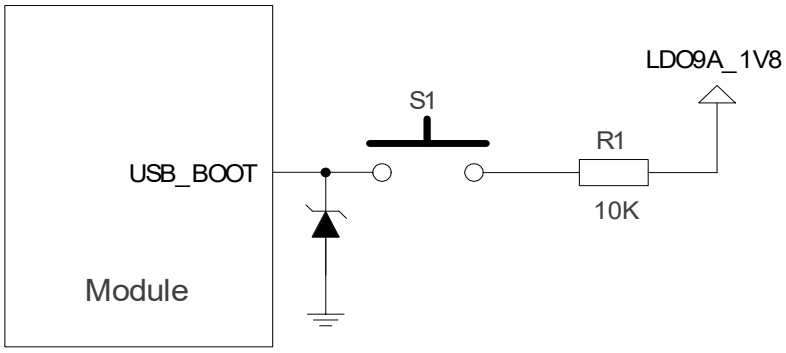
4.16. Forced Download Interface

Table 33: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	57	DI	Force the module into download mode	1.8 V power domain. Force the module to enter download mode by pulling this pin up to LDO9A_1V8 during turning-on. A test point is recommended to be reserved.

USB_BOOT is an forced download interface. Pull it up to LDO9A_1V8 during power-up will force the module into forced download mode. There is an emergency option when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Figure 27: Reference Design for Forced Download Interface



5 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition is shown below:

Table 34: Pin Definition of Cellular Network Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DRX	149	AI	Rx-diversity antenna interface	

NOTE

Only passive antennas are supported.

Table 35: Operating Frequency

Operating Frequency	Receive (MHz)	Transmit (MHz)
LTE-FDD B2	1930–1990	1850–1910
LTE-FDD B4	2110–2155	1710–1755
LTE-FDD B5	869–894	824–849
LTE-FDD B7	2620–2690	2500–2570
LTE-FDD B12	729–746	699–716
LTE-FDD B13	746–756	777–787
LTE-FDD B14	758–768	788–798
LTE-FDD B17	734–746	704–716
LTE-FDD B25	1930–1995	1850–1915
LTE-FDD B26	859–894	814–849

LTE-FDD B66	2110–2200	1710–1780
LTE-FDD B71	617–652	663–698
LTE-TDD B41 [3]	2496–2690	2496–2690

5.1.2. Tx Power

The following table shows the RF output power of the module.

Table 36: Tx Power

Frequency	Max. RF output power	Min. RF output power
LTE Bands	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 37: Conducted RF Rx Sensitivity

Frequency	Rx Sensitivity (Typ.) (dBm)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	-98.5	-99.5	-102.2	-94.3
LTE-FDD B4 (10 MHz)	-97.6	-98.7	-101.2	-96.3
LTE-FDD B5 (10 MHz)	-98.5	-99.6	-101.9	-94.3
LTE-FDD B7 (10 MHz)	-97.8	-99.1	-100.8	-94.3
LTE-FDD B12 (10 MHz)	-99.5	-99.9	-102.1	-93.3
LTE-FDD B13 (10 MHz)	-98.9	-100.4	-102.1	-93.3
LTE-FDD B14 (10 MHz)	-98.9	-100.1	-101.7	-93.3
LTE-FDD B17 (10 MHz)	-98.8	-100.3	-101.7	-93.3
LTE-FDD B25 (10 MHz)	-98.4	-99.5	-102.1	-92.8
LTE-FDD B26 (10 MHz)	-98.1	-99.6	-101.9	-93.8
LTE-FDD B66 (10 MHz)	-98.0	-99.2	-101.2	-95.8
LTE-FDD B71 (10 MHz)	-99.7	-98.1	-101.8	-93.5
LTE-TDD B41 (10 MHz)	-96.9	-98.2	-100.5	-94.3

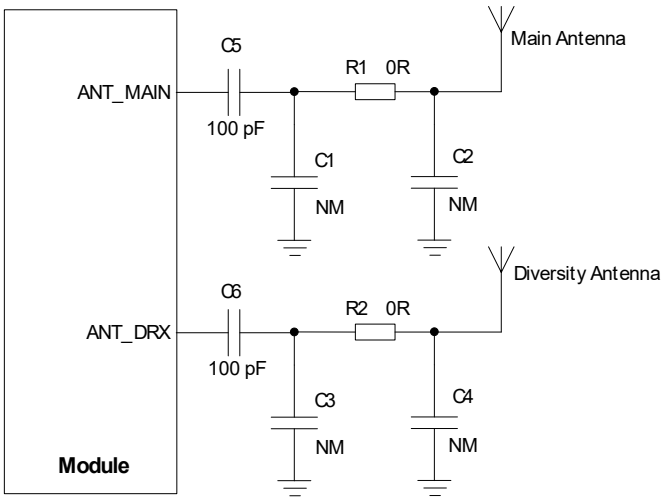
[3] Frequency band of module's LTE-TDD B41 is 200 MHz (2496–2690 MHz), range of channel is 39650–41589.

5.1.4. Reference Design of Cellular Antenna Interfaces

The module provides four RF antenna interfaces for antenna connection.

It is recommended to reserve a dual L-type circuit for better RF performance, and the dual L-type components (R1/C1/C2/C5, R2/C3/C4/C6) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

Figure 28: Reference Design for RF Antenna Interfaces



NOTE

Notes on C5 and C6:

1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
2) If there is no DC power in the peripheral design:
   a) Do not reserve C5 and C6.
   b) If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.

5.2. GNSS (Optional)

The module integrates the IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems including GPS, GLONASS, BDS, Galileo, SBAS and QZSS. With an embedded LNA, the positioning accuracy of the module can be greatly improved.

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 38: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment

ANT_GNSS	134	AI	GNSS antenna interface	50 Ω characteristic impedance.
GNSS_LNA_EN	202	DO	GNSS LNA enable control	Only for internal test, cannot be multiplexed into a generic GPIO. If it is unused, keep it open.

Table 39: Operating Frequency

Type	Frequency	Unit
GPS/QZSS	1575.42 ±1.023	MHz
GLONASS	1601.7 ±4.2	
Galileo	1575.42 ±2.046	
BDS	1561.098 ±2.046	
SBAS	1575.42 ±1.023	

5.2.2. GNSS Performance

Table 40: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Acquisition	-147	dBm
	Reacquisition	-158	
	Tracking	-159	
TTFF	Cold start	33	s
	Warm start	22	
	Hot start	1.2	
Accuracy	CEP-50	2.49	m

NOTE

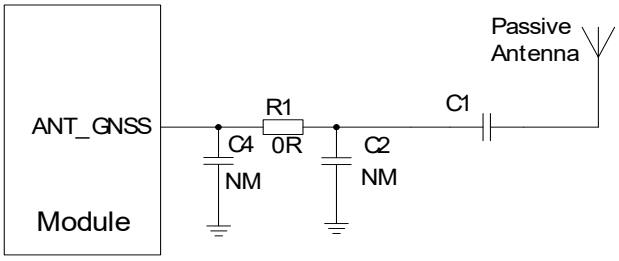
1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Reference Design for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference design is given below.

Figure 29: Reference Design for Passive Antenna



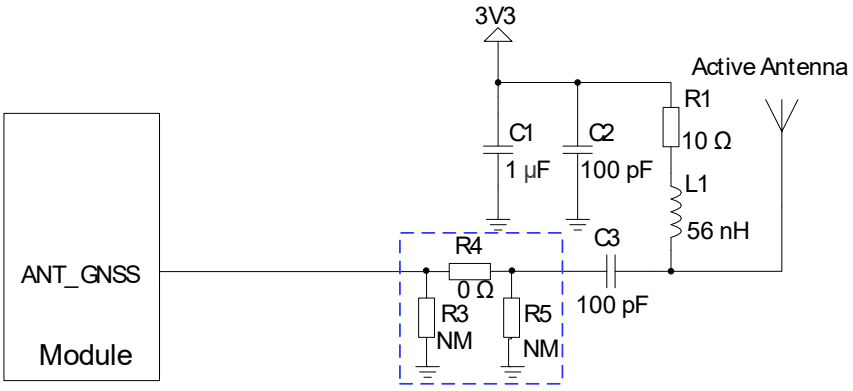
NOTE

1. It is not recommended to add an external LNA when using a passive GNSS antenna.
2. Notes on C1:
   1) If there is DC power at the antenna port, place capacitor on C1 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C1.
      b) If C1 has already been reserved, they should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.

5.2.3.2. Reference Design for Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. A reference design of the GNSS active antenna is shown below.

Figure 30: Reference Design for Active Antenna



NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.2.3.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. To avoid it, follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the other RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal traces and RF components should be placed far away from high-speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For harsh electromagnetic environment or a design that requires better ESD protection, diodes with ultra-low junction capacitance such as 0.5 pF can be selected and added in the antenna interface. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace to 50 Ω, and keep the trace length as short as possible.

5.3. Wi-Fi and Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

The following tables show the pin definition and frequency specification of the Wi-Fi/Bluetooth antenna interface.

Table 41: Pin Definition of Wi-Fi/Bluetooth Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω characteristic impedance.

Table 42: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi 802.11a/b/g/n/ac	2402–2482 5180–5825	MHz
BLE 5.0	2402–2480	MHz

5.3.1. Wi-Fi Overview

The module supports 2.4 GHz and 5 GHz dual-band Wi-Fi wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP and STA modes
- Support Wi-Fi Direct
- Support MCS 0–7 for HT20 and HT40
- Support MCS 0–8 for VHT20
- Support MCS 0–9 for VHT40 and VHT80

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 43: Wi-Fi Transmitting Performance

Frequency	Standard	Rate	Output
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB
	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	15 dBm ±2.5 dB
	802.11a	54 Mbps	13 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	15 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
	802.11ac VHT20	MCS0	14 dBm ±2.5 dB
	802.11ac VHT20	MCS8	13 dBm ±2.5 dB
	802.11ac VHT40	MCS0	13 dBm ±2.5 dB
	802.11ac VHT40	MCS9	12 dBm ±2.5 dB
	802.11ac VHT80	MCS0	13 dBm ±2.5 dB
	802.11ac VHT80	MCS9	12 dBm ±2.5 dB

Table 44: Wi-Fi Receiver Performance

Frequency	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-97 dBm
	802.11b	11 Mbps	-88 dBm
	802.11g	6 Mbps	-91 dBm
	802.11g	54 Mbps	-74 dBm

	802.11n HT20	MCS0	-90 dBm
	802.11n HT20	MCS7	-72 dBm
5 GHz	802.11a	6 Mbps	-91 dBm
	802.11a	54 Mbps	-74 dBm
	802.11n HT20	MCS0	-91 dBm
	802.11n HT20	MCS7	-71 dBm
	802.11n HT40	MCS0	-87 dBm
	802.11n HT40	MCS7	-68 dBm
	802.11ac VHT20	MCS0	-91 dBm
	802.11ac VHT20	MCS8	-69 dBm
	802.11ac VHT40	MCS0	-89 dBm
	802.11ac VHT40	MCS9	-65 dBm
	802.11ac VHT80	MCS0	-86 dBm
	802.11ac VHT80	MCS9	-61 dBm

NOTE

The product conforms to the IEEE specifications.

5.3.2. Bluetooth Overview

The module supports Bluetooth 5.0 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7 lanes of wireless connections.
- Maximally support up to 3.5 piconets at the same time.
- Support one SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 45: Bluetooth Data Rate and Version

Version	Rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0 + EDR	3 Mbit/s	> 80 kbit/s

3.0 + HS	24 Mbit/s	Reference 3.0 + HS
4.0	24 Mbit/s	Reference 4.0 LE
5.0	48 Mbit/s	Reference 5.0 LE

Reference specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

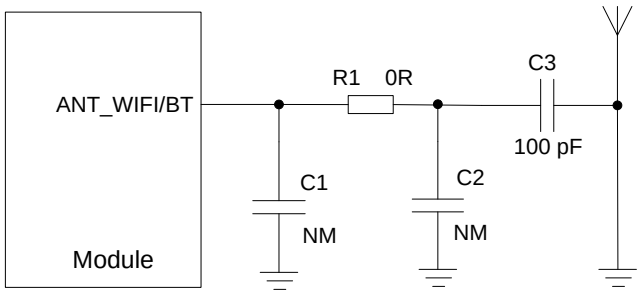
Table 46: Bluetooth Transmitting and Receiver Performance

Transmitting Performance			
Packet Type	DH5	2-DH5	3-DH5
Transmitting Power	8 ±2.5 dBm	6 ±2.5 dBm	6 ±2.5 dBm
Receiver Performance			
Packet Type	DH5	2-DH5	3-DH5
Receiver Sensitivity	-91 dBm	-91 dBm	-83 dBm

5.3.3. Reference Design

A reference design for Wi-Fi/Bluetooth antenna interface is shown as below. Capacitors are not mounted by default and the resistor is 0 Ω.

Figure 31: Reference Design for Wi-Fi/Bluetooth Antenna



NOTE

Notes on C3:
1) If there is DC power at the antenna port, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the

debugging results.

2) If there is no DC power in the peripheral design:
   a) Do not reserve C3.
   b) If C3 has already been reserved, they should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.

5.4. RF Routing Guidelines

When designing PCB, characteristic impedance of all RF traces should be controlled to 50 Ω. Generally, the impedance of RF traces is determined by materials' dielectric constant, trace width (W), spacing between RF traces and grounds (S) and height from the reference ground to the signal layer (H). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures when characteristic impedance of RF traces is controlled to 50 Ω.

Figure 32: Microstrip Design on a 2-layer PCB

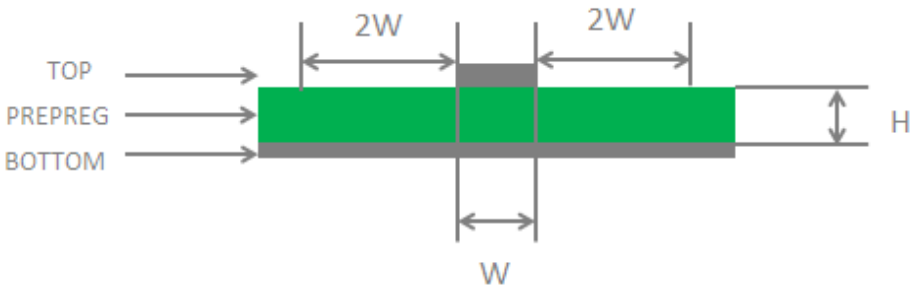


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

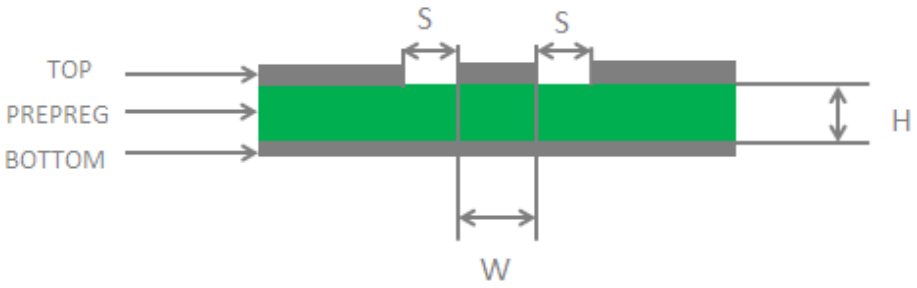


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

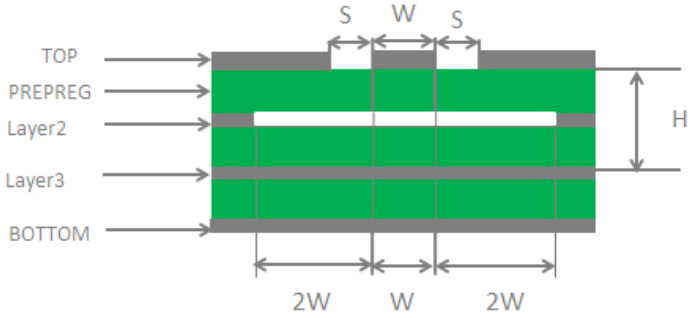
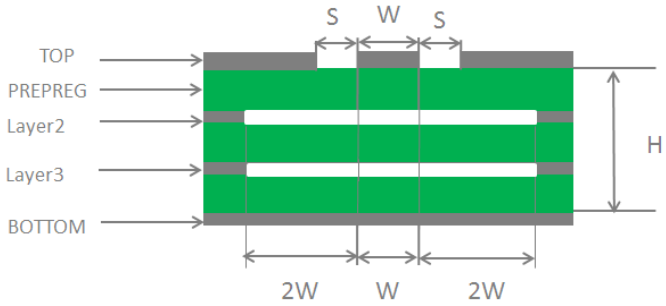


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- Clearance between RF pins and RF connector should be as short as possible, and all right-angle (90°) traces should be changed to the ones with the angle of 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground can improve RF performance. The clearance between ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document 4***.

5.5. Antenna Design Requirements

Requirements for antenna design are as follow:

Table 47: Requirements for Antenna Design

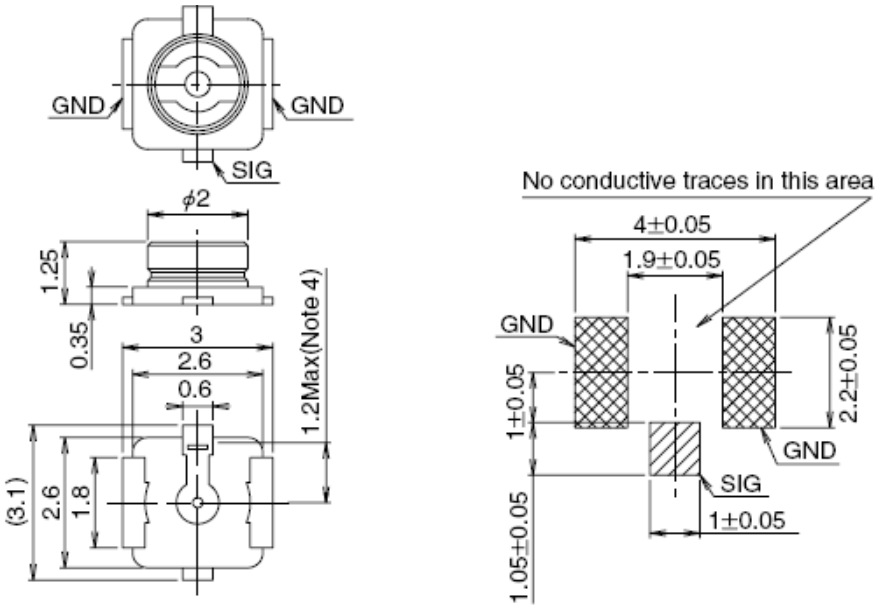
Antenna Type	Requirements
GNSS (Optional)	• Frequency range: 1559–1609 MHz • Polarization Type: RHCP or linear • VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise figure: < 1.5 dB (Typ.) Active antenna embedded LNA gain: < 17 dB (Typ.) Active Antenna Embedded LNA Gain: < 0 dBi (Typ.)

Cellular	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical ● Cable Insertion Loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
Wi-Fi/Bluetooth	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical ● Cable Insertion Loss: < 1 dB

5.6. RF Connector Recommendation

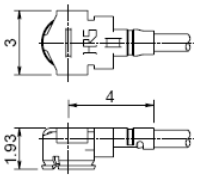
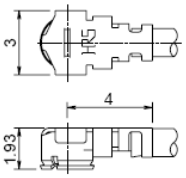
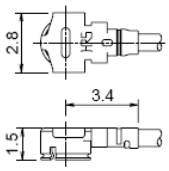
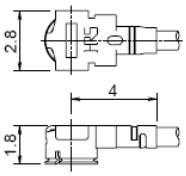
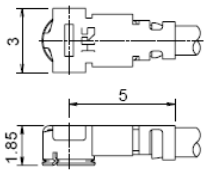
If you use an RF connector for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

Figure 36: Dimensions of the Receptacle (Unit: mm)



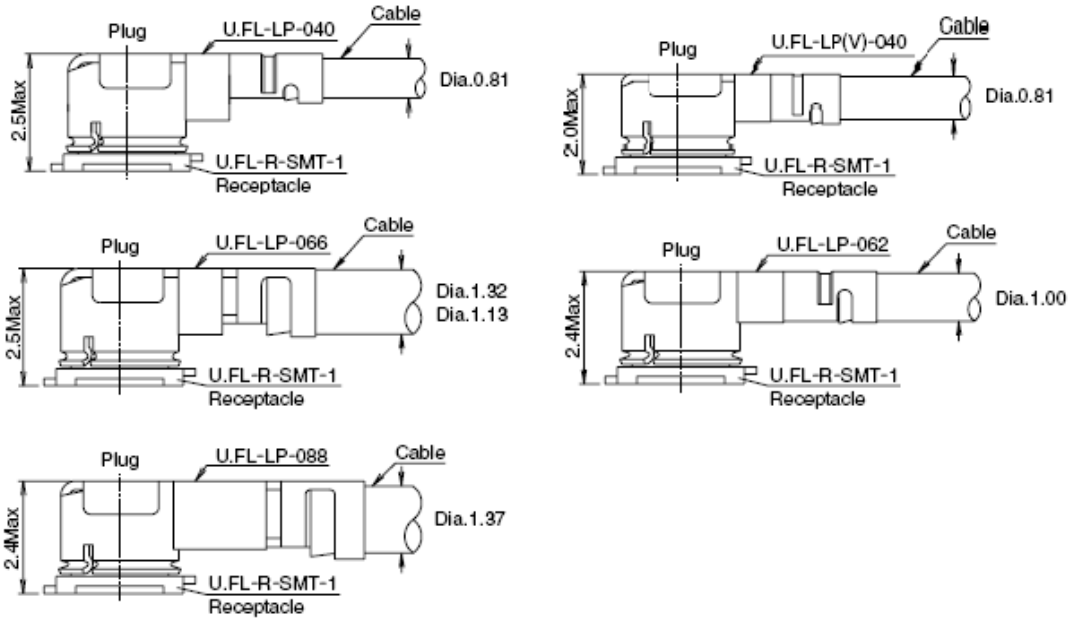
U.FL-LP series connectors listed in the following figure can be used to match the U.FL-R-SMT.

Figure 37: Specifications of Mated Plugs (Unit: mm)

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated connectors.

Figure 38: Space Factor of Mated Connectors (Unit: mm)



Please visit http://www.hirose.com for more information.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module is listed in the following table.

Table 48: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	4.75	V
USB_VBUS	-0.3	16	V
Peak Current of VBAT	-	3	A
Voltage on Digital Pins	-0.3	2.04	V

6.2. Power Supply Ratings

Table 49: The Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values	3.55	3.8	4.4	V
I_{VBAT}	Peak supply current	Maximum power control level	-	1.8	3.0	A
USB_VBUS	USB connection detect		4.0	5.0	6.0	V
VRTC	Power supply voltage of the backup battery		2.1	3.0	3.25	V

6.3. Power consumption

Table 50: Power Consumption

Description	**Condition**	**Typ.**	**Unit**
OFF state	Power down	100	μA
Sleep state	Screen out	5.5	mA

LTE-FDD supply current Sleep state (USB disconnected)	LTE-FDD PF = 32	5.77	mA
	LTE-FDD PF = 64	4.41	mA
	LTE-FDD PF = 128	3.82	mA
	LTE-FDD PF = 256	3.55	mA
LTE-TDD supply current Sleep state (USB disconnected)	LTE-TDD PF = 32	5.64	mA
	LTE-TDD PF = 64	4.62	mA
	LTE-TDD PF = 128	3.83	mA
	LTE-TDD PF = 256	3.45	mA
LTE data transmission	LTE-FDD B2 @ max power	635	mA
	LTE-FDD B4 @ max power	694	mA
	LTE-FDD B5 @ max power	585	mA
	LTE-FDD B7 @ max power	736	mA
	LTE-FDD B12 @ max power	678	mA
	LTE-FDD B13 @ max power	708	mA
	LTE-FDD B14 @ max power	604	mA
	LTE-FDD B17 @ max power	564	mA
	LTE-FDD B25 @ max power	618	mA
	LTE-FDD B26 @ max power	595	mA
	LTE-FDD B66 @ max power	650	mA
	LTE-FDD B71 @ max power	615	mA
	LTE-TDD B41 @ max power	395	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact NetPrisma Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 51: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.17	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.63	V
V_{OH}	High-level output voltage	1.35	1.8	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 52: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	High-level input voltage	1.26	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.36	V
V_{OH}	High-level output voltage	1.44	1.8	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 53: (U)SIM 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.03	V
V_{IH}	High-level input voltage	2.07	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.59	V
V_{OH}	High-level output voltage	2.36	2.95	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 54: SD Card 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_VDD	Power supply	1.7	1.9	V
V_{IH}	High-level input voltage	1.27	2	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	1.8	V

V_{OL}	Low-level output voltage	0	0.45	V

Table 55: SD Card 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_VDD	Power supply	2.7	3.1	V
V_{IH}	High-level input voltage	1.84	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.74	V
V_{OH}	High-level output voltage	2.21	2.95	V
V_{OL}	Low-level output voltage	0	0.37	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 56: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT & GND	±5	±10	kV
Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 57: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	°C
Storage temperature range	-40	-	+90	°C

[4] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heat sinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the tolerances for dimensions without tolerance values are ±0.2 mm.

7.1. Mechanical Dimensions

Figure 39: Module Top and Side Dimensions (Unit: mm)

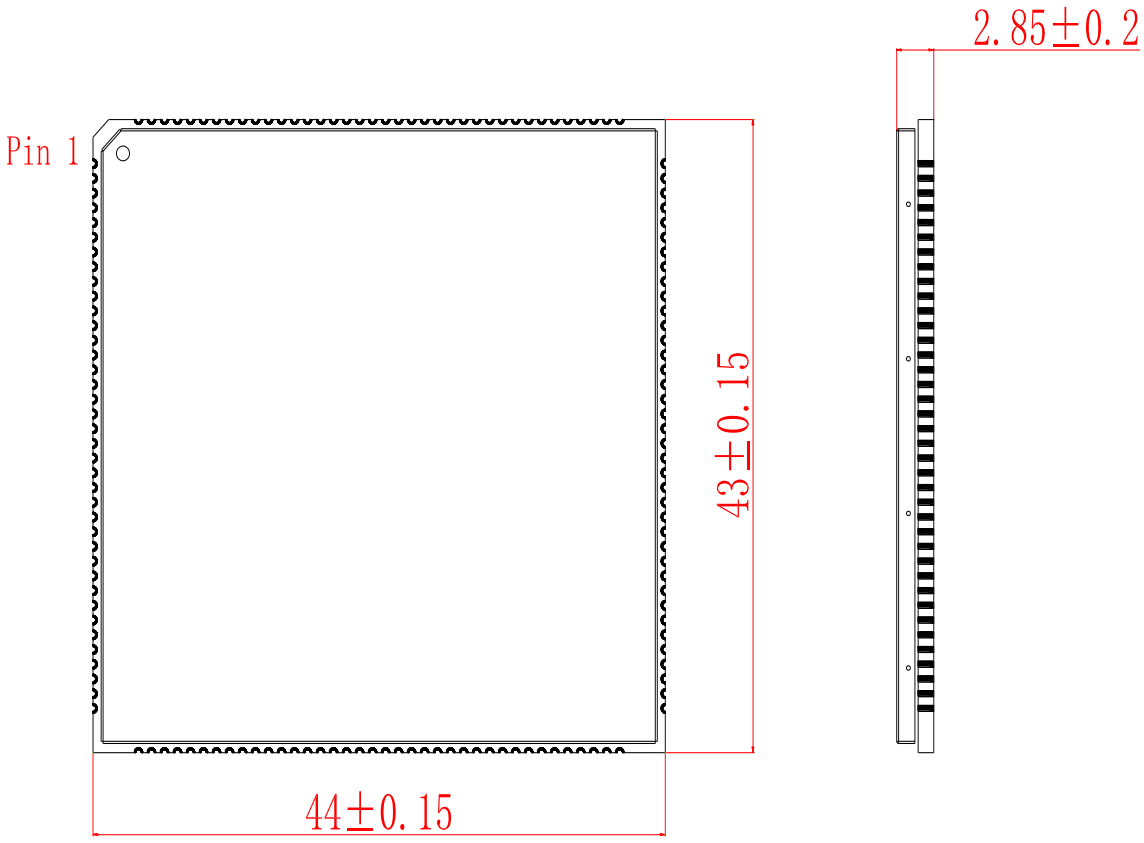
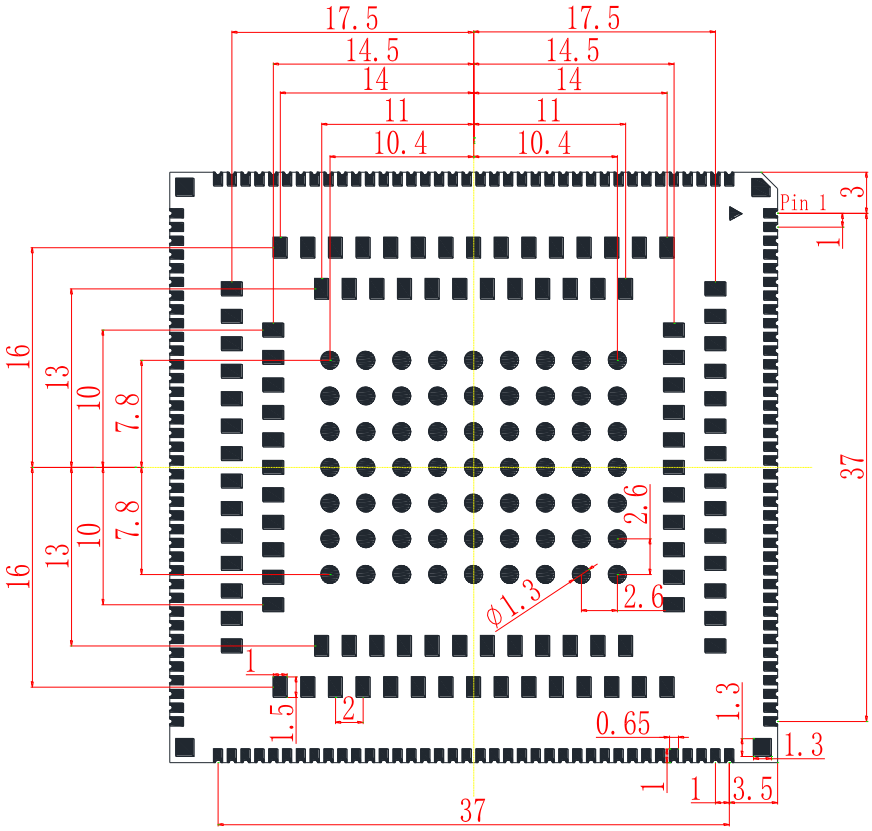


Figure 40: Module Bottom Dimensions (Unit: mm)

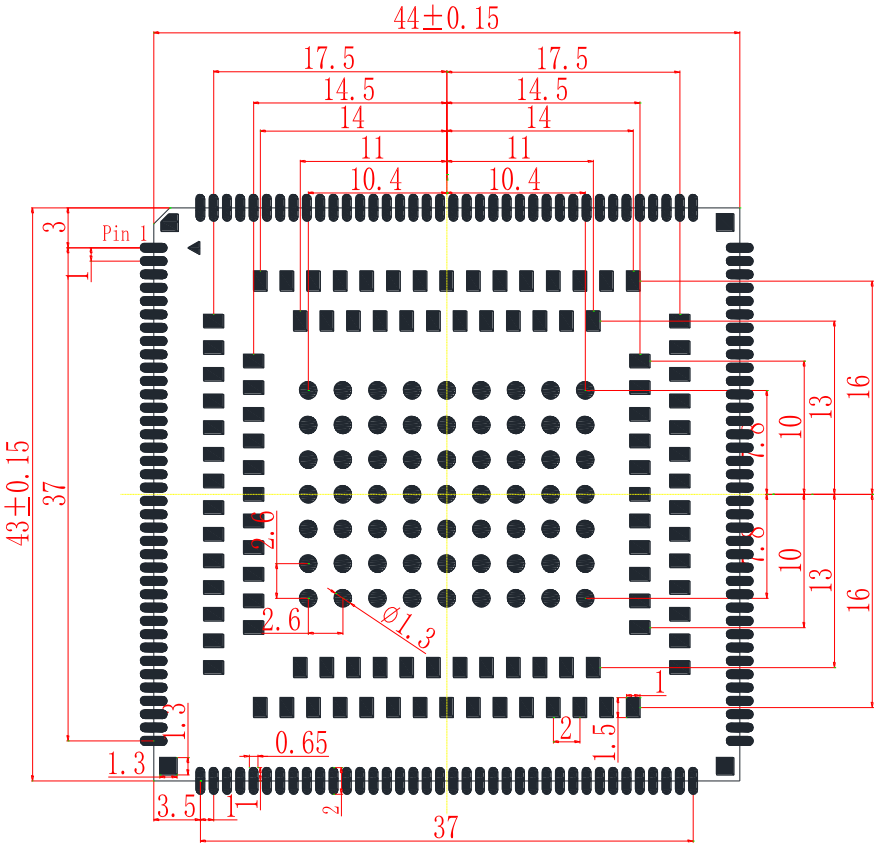


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

Figure 41: Recommended Footprint



NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. All RESERVED pins should be kept open and MUST NOT be connected to ground.

7.3. Top and Bottom Views

Figure 42: Top and Bottom Views of SUS600-LD

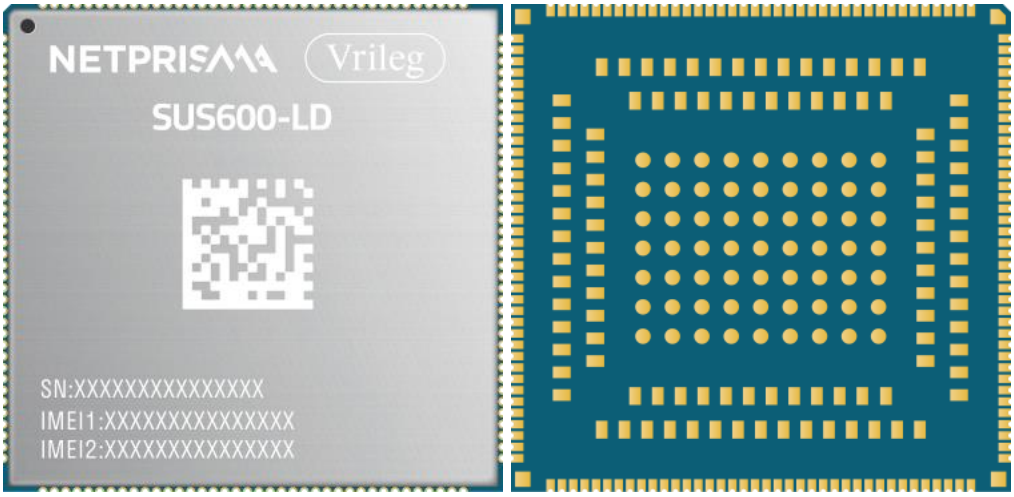
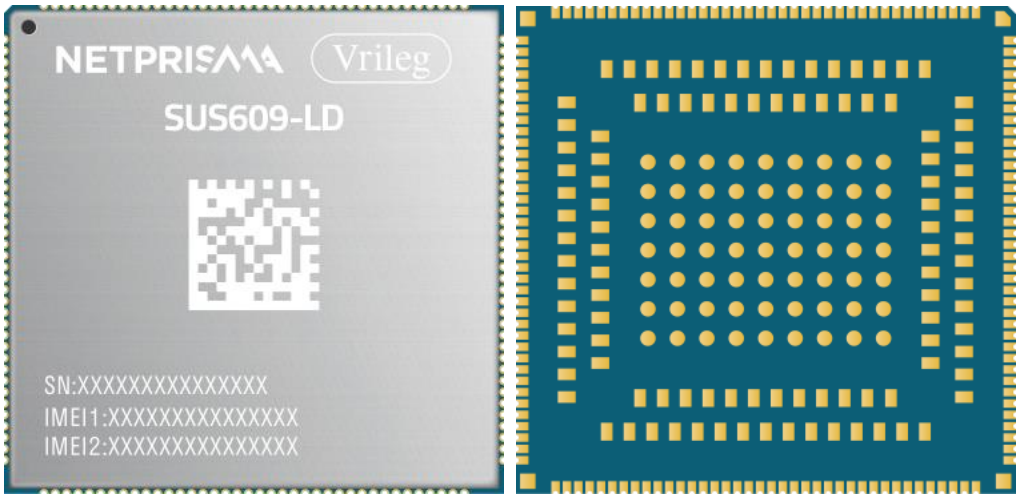


Figure 43: Top and Bottom Views of SUS609-LD



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document 5***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB

[5] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. And do not unpack the modules in large quantities until they are ready for soldering.

has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 44: Recommended Reflow Soldering Thermal Profile

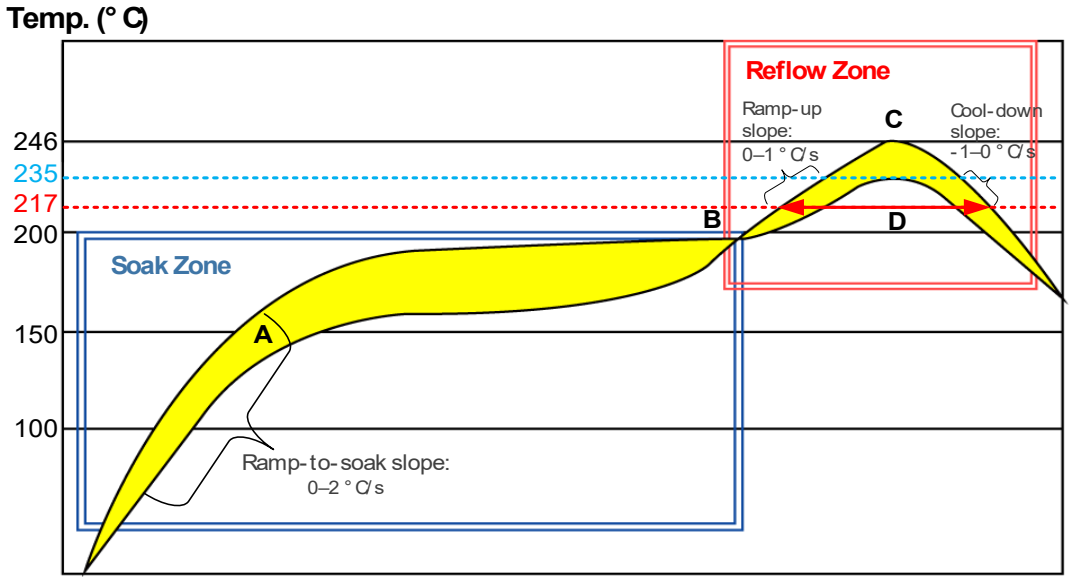


Table 58: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max. temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, an excessive temperature change may cause excessive thermal

deformation of the metal shielding frame and cover. Thus, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.

3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document 6***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 45: Carrier Tape Dimension Drawing (Unit: mm)

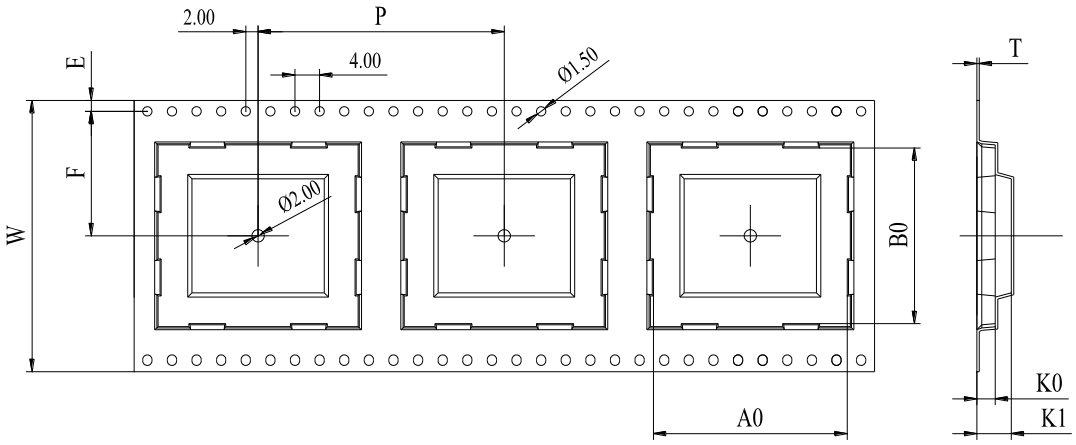


Table 59: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.35	44.5	43.5	4.1	5.4	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 46: Plastic Reel Dimension Drawing

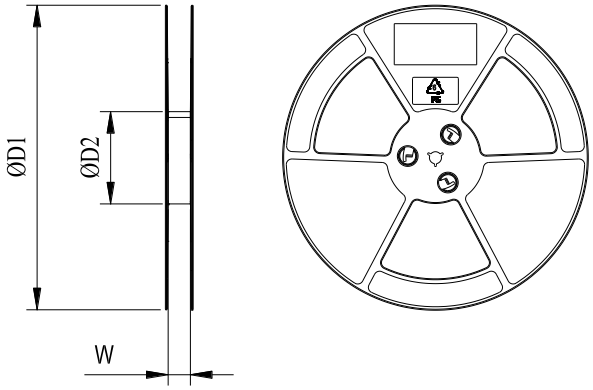
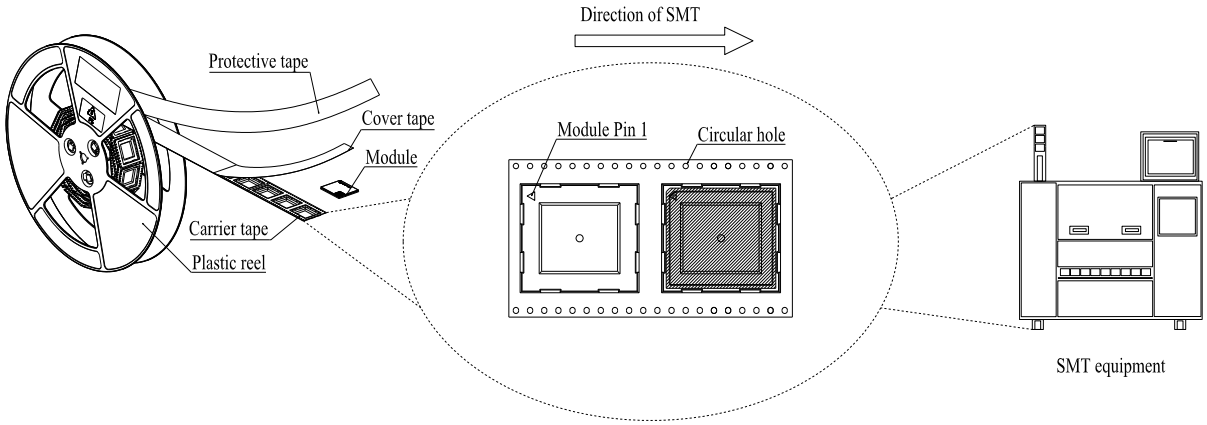


Table 60: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

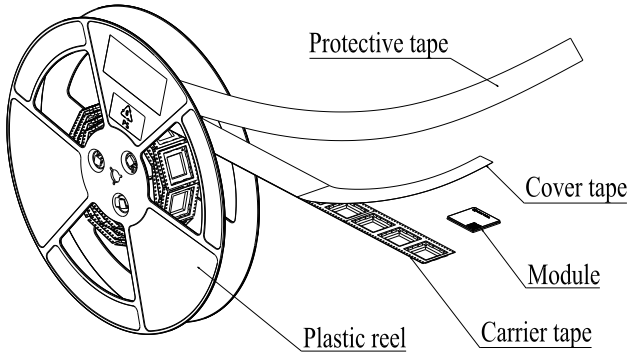
8.3.3. Mounting Direction

Figure 47: Mounting Direction



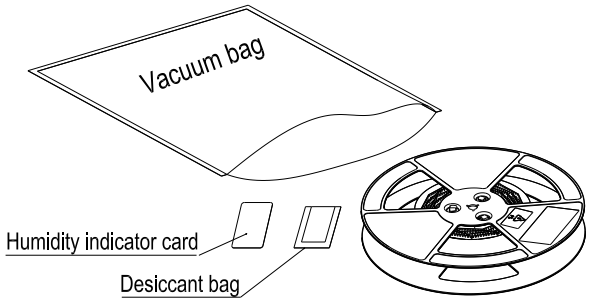
8.3.4. Packaging Process

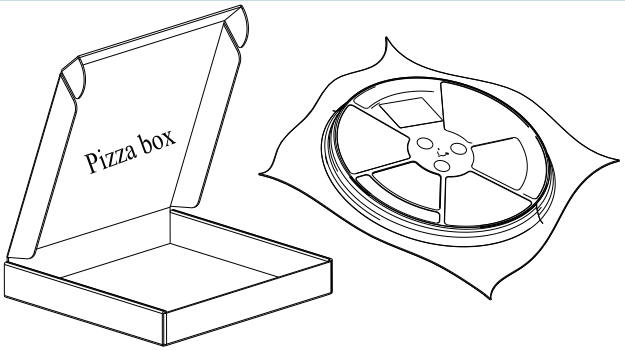
Figure 48: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

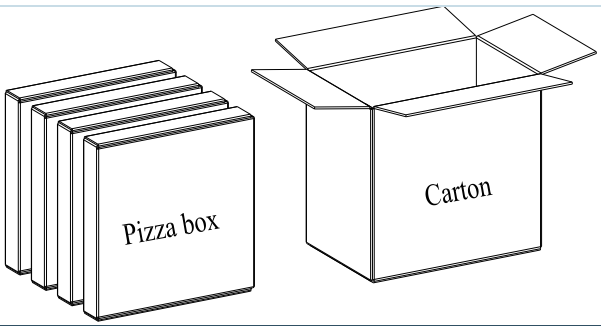
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.



9 Appendix References

Table 61: Related Documents

Document Name
1. NetPrisma-SUS600-LD&SUS609-LD-GPIO-Configuration
2. NetPrisma-Smart-EVB-G5-User-Guide
3. NetPrisma-SUS600-LD&SUS609-LD-DisplayPort-Application-Note
4. NetPrisma-RF-Layout-Application-Note
5. NetPrisma-Module-Stencil-Design-Requirements
6. NetPrisma-Module-SMT-Application-Note

Table 62: List of Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
aDSP	Audio Digital Signal Processor
AMR	Adaptive Multi-rate
ANT	Antenna
AP	Access Point/Application Processor
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear to Send
DL	Downlink
DRX	Discontinuous Reception

DSI	Display Serial Interface
DSP	Digital Signal Processing/Digital Signal Processor
EDGE	Enhanced Data Rate for GSM Evolution
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM900 band (including standard GSM900 band)
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
EVRC	Enhanced Variable Rate Codec
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input/Output
GPS	Global Positioning System
GPRS	General packet radio service
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
GNSS	Global Navigation Satellite System
GRFC	Generic RF Control
HR	Half Rate
HSDPA	High Speed Down Link Packet Access
HSPA	High Speed Packet Access

HEVC	High Efficiency Video Coding
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
Imax	Maximum Load Current
$I_O$max	Maximum Output Load Current
IMT-2000	International Mobile Telecom System-2000
LCC	Leadless Chip Carrier (package)
LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LGA	Land Grid Array
LNA	Low Noise Amplifier
LTE	Long-Term Evolution
M2M	Machine to Machine
MCU	Microcontroller Unit/Microprogrammed Control Unit
MIMO	Multi-input Multi-output
MIPI	Mobile Industry Processor Interface
MP	Million Pixel
MSL	Moisture Sensitivity Levels
OTA	Over-the-Air Technology
OTG	On-The-Go
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical
PMU	Power Management Unit

POS	Point of Sale
PSK	Phase Shift Keying
PWDN	Power Down
PWM	Pulse Width Modulation
PWRKEY	Power Key
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTC	Real Time Clock
RTS	Request to Send
RX	Receive
SCO	Synchronous Connection Oriented link
SD	Secure Digital
SMS	Short Message Service
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
STA	Station
TDD	Time Division Distortion
TE	Tearing Effect
TP	Touch Panel
TVS	Transient Voltage Suppressor
TX	Transmit
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
(U)SIM	(Universal) Subscriber Identity Module
USB	Universal Serial Bus
Vmax	Maximum Voltage

Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WAPI	Wireless LAN Authentication and Privacy Infrastructure
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

FCC ID: 2BEY3SUS600LDA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA INC. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

“Contains FCC ID: 2BEY3SUS600LDA”

“Contains IC: 32052-SUS600LDA”

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Band	Antenna Type	Max Gain Allowed (dBi)
LTE B2	External	8.00
LTE B4		5.00
LTE B5		13.41
LTE B7		8.00
LTE B12		11.92
LTE B13		11.92
LTE B14		11.92
LTE B17		11.92
LTE B25		8.00
LTE B26		13.36
LTE B41		8.00
LTE B66		5.00
LTE B71		11.92
Bluetooth		0.47
WiFi 2.4G		0.47
WiFi 5150-5250MHz		-0.67
WiFi 5250-5350MHz		-0.19
WiFi 5470-5725MHz		1.28
WiFi 5725-5850MHz		1.1

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 15 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC: 32052-SUS600LDA

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

	Antenna Type	Max Gain Allowed (dBi)
Bluetooth	External	0.47
WiFi 2.4G		0.47
WiFi 5150-5250MHz		-0.67
WiFi 5250-5350MHz		-0.19
WiFi 5470-5725MHz		1.28
WiFi 5725-5850MHz		1.1

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 32052-SUS600LDA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 32052-SUS600LDA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Document History

Revision	Date	Changes
A	2025-02-21	The first revision.

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