SUE200-LD&SUE209-LD

Hardware Design

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1 Introduction

This document defines SUE200-LD and SUE209-LD modules and describes their air interface and hardware interfaces which are connected to your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Text Conventions

Table 1: Text Conventions

NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1. Frequency Bands and Functions

SUE200-LD and SUE209-LD are Smart LTE modules based on Android and Linux operating systems respectively, and provide industrial grade performance. The modules' general features are listed below:

- Support worldwide LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EVDO/CDMA, EDGE, GSM and GPRS coverage.
- Support short-range wireless communication via Wi-Fi 802.11a/b/g/n/ac and Bluetooth 5.0 [1].
- Integrate GPS/GLONASS/BDS/Galileo/QZSS/SBAS satellite positioning systems.
- Support multiple audio and video codecs.
- Built-in high performance Adreno™ 702 graphics processing unit.
- Provide multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

Table 1: SUE200-LD & SUE209-LD Frequency Bands and Functions

Mode	Frequency Bands
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz 5180–5825 MHz (*Restrict to indoor operation only in the band 5150-5250 MHz)
Bluetooth 5.0	2402–2480 MHz
GNSS (optional)	GPS: 1575.42 ±1.023 MHz (L1) GLONASS: 1597.5–1605.8 MHz (L1) BDS: 1561.098 ±2.046 MHz (B1I) Galileo: 1575.42 ±2.046 MHz (E1) QZSS: 1575.42 ±1.023 MHz (L1) SBAS: 1575.42 ±1.023 MHz (L1)

SUE200-LD and SUE209-LD are SMD type modules, which can be embedded into applications through their 274 pins, including 146 LCC pins and 128 LGA pins. With a compact profile of 40.5 mm × 40.5 mm × 2.85 mm, the module can meet most of the requirements for M2M applications.

2.2. Key Features

The following table describes the detailed features of the modules.

[1] The module is compliant with all mandatory Bluetooth 5.0 features, but does not support Bluetooth 5.0 optional features like 2 Mbps BLE, Advanced Advertising Extension, etc.

Table 2: Key Features

Feature	Details
Application Processor	● 64-bit quad-core ARM Cortex-A53 microprocessor, up to 2.0 GHz ● 512 KB L2 cache
Modem DSP	● Hexagon DSP v66k core ● 512 KB L2 cache
GPU	Adreno™ 702 GPU with 64-bit addressing, up to 845 MHz
Memory (Optional)	SUE200-LD: ● 16 GB eMMC + 2 GB LPDDR4X ● 32 GB eMMC + 3 GB LPDDR4X ● 64 GB eMMC + 4 GB LPDDR4X SUE209-LD: ● 8 GB eMMC + 1 GB LPDDR4X
Operating System	SUE200-LD: Android 12, Android 13, Android 14 SUE209-LD: Yocto Linux (Kernel 5.4)
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 3 (23 dBm ±2 dB) for LTE-FDD bands ● Class 3 (23 dBm ±2 dB) for LTE-TDD bands
LTE Features	**SUE200-LD and SUE209-LD:** ● Supports 3GPP Rel-10 Cat 4 ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports Multiuser MIMO in DL direction ● Data rate (Max.): − Cat 4 FDD: 150 Mbps (DL)/50 Mbps (UL) − Cat 4 TDD: 130 Mbps (DL)/30 Mbps (UL)
WLAN Features	● 2.4 GHz, 802.11b/g/n, up to 150 Mbps ● 5 GHz, 802.11a/n/ac, up to 433 Mbps ● Supports AP mode and STA mode
Bluetooth Features [2]	*Bluetooth Core Specification Version* 5.0 Bluetooth Classic & Bluetooth Low Energy (BLE)
GNSS Features	GPS/GLONASS/BDS/Galileo/QZSS/SBAS, L1
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
LCM Interface	● Supports one group of 4-lane MIPI DSI ● Supports up to HD+ (1680 × 720) @ 60 fps
Camera Interfaces	● Support two groups of 4-lane MIPI CSI, up to 2.5 Gbps/lane ● Support two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane) ● Support up to 25 MP or 13 MP + 13 MP with dual ISPs
Video Codec	● Video encoding + decoding: 720p @ 30 fps + 1080p @ 30 fps ● Encoding: up to 1080p @ 30 fps; Decoding: up to 1080p @ 30 fps
Audio Interfaces	**Audio inputs:** ● Two differential microphone inputs ● One single-ended microphone input **Audio outputs:** ● Class AB stereo headphone output ● Class AB earpiece differential output ● Class AB line out differential output
Audio Codec	● EVS, EVRC, EVRC-B, EVRC-WB ● G.711, G.729A, and G.729AB ● GSM-FR, GSM-EFR, GSM-HR ● AMR-NB, AMR-WB
USB Interface	**Type-C interface type:** ● Complies with both USB 3.1 Gen 1 or USB 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 Gen 1 and 480 Mbps on USB 2.0 ● Supports USB OTG

[2] The module is compliant with all mandatory Bluetooth 5.0 features, but does not support Bluetooth 5.0 optional features like 2 Mbps BLE, Advanced Advertising Extension, etc.

	● Used for AT command communication, data transmission, software debugging, and firmware upgrade
UART Interfaces	Three UART interfaces: UART0, UART1, and UART4 (debug UART) ● UART0: four-wire UART interface supporting RTS and CTS hardware flow control ● UART1: two-wire UART interface ● UART4 (debug UART): two-wire UART interface dedicated for debugging
SD Card Interface	● Supports SD 3.0 ● Supports SD card hot-plug
(U)SIM Interfaces	● Two (U)SIM interfaces ● Support (U)SIM cards: 1.8/2.95 V ● Support Dual SIM Dual Standby (supported by default)
I2C Interfaces	● Four I2C interfaces ● Used for peripherals such as camera, sensor, touch panel
ADC Interface	One generic ADC interface, up to 15-bit resolution
Real Time Clock	Supported
Antenna Interfaces	**SUE200-LD and SUE209-LD:** Main antenna, Rx-diversity antenna, GNSS antenna and Wi-Fi/Bluetooth antenna interfaces
Physical Characteristics	● Size: (40.5 ±0.15) mm × (40.5 ±0.15) mm × (2.85 ±0.2) mm ● Package: LCC + LGA ● Weight: Approx. 10.3 g
Temperature Range	● Operating temperature range [3]: -35 °C to +75 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● USB interface ● OTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

3 Application Interfaces

3.1. General Description

SUE200-LD and SUE209-LD are SMD type modules with 146 LCC pins and 128 LGA pins. The following interfaces and functions are described in detail in these subsequent chapters:

- Power supply
- VRTC
- Power output
- Charging interface
- USB interface
- UART interfaces
- (U)SIM interfaces
- SD card interface
- GPIO interfaces
- I2C interfaces
- ADC interface
- Vibration motor driver interface
- LCM interface
- Flash & Torch interface
- Touch panel interface
- Camera interfaces
- Sensor interface
- Audio interfaces
- USB_BOOT control interface

[3] Within the operating temperature range, the module meets 3GPP specifications.

3.2. Pin Description

Table 3: I/O Parameter Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	1, 2, 145, 146	PIO	Power supply for the module	Vmin = 3.55 V Vnom = 3.8 V Vmax = 4.4 V	Provide sufficient current up to 3 A. It is suggested to use a TVS for surge protection.
VPH_PWR	184	PO	Power supply for peripherals	Vmin = 3.55 V Vnom = 3.8 V Vmax = 4.4 V	This pin is used to power peripheral devices. Maximum output current is 1 A.
LDO15A_1V8	111	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 200 mA	The power supply for LCM, sensor, cameras and I2C pull-up circuits.
LDO17A_3V0	156	PO	3.0 V output	Vnom = 3.0 V $I_O$max = 192 mA	The power supply for TP and sensor.
LDO_IOVDD	125	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	The power is reserved for LCM and camera's IOVDD. This voltage is not adjustable.
VRTC	126	PIO	Power supply for RTC	$V_O$max = 3.2 V $V_I$min = 2.5 V $V_I$max = 3.2 V	If unused, keep it open.
VDD_2V8	129	PO	2.8 V output	Vnom = 2.8 V $I_O$max = 500 mA	The power supply for camera’s AVDD. This voltage is not adjustable.

Audio Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC_BIAS1	147	PO	Bias voltage 1 output for microphone	Vmin = 1.6 V Vmax = 2.85 V	The rated output current is 3 mA. The default software setting output voltage is 1.8 V.
MIC1_P	4	AI	Microphone input for channel 1 (+)		
MIC1_M	5	AI	Microphone input for channel 1 (-)		
MIC2_P	6	AI	Microphone input for headset (+)		
MIC3_P	148	AI	Microphone input for channel 3 (+)		
MIC3_M	149	AI	Microphone input for channel 3 (-)		
MIC_BIAS3	155	PO	Bias voltage 3 output for microphone	Vnom = 1.8 V	The rated output current is 3 mA. The output voltage is fixed at 1.8 V and cannot be adjusted.
EAR_P	8	AO	Earpiece output (+)		
EAR_M	9	AO	Earpiece output (-)		
LINEOUT_P	10	AO	Audio line differential output (+)		The typical output voltage is 2 Vrms.
LINEOUT_M	11	AO	Audio line differential output (-)		
HPH_R	136	AO	Headphone right channel output		
HPH_GND	137	AO	Headphone reference ground		
HPH_L	138	AO	Headphone left channel output		
HS_DET	139	AI	Headset hot-plug detect		High level by default.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	141, 142	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	Vmax = 6.0 V Vmin = 4.0 V Vnom = 5.0 V	The maximum output current is 500 mA.
USB_DM	13	AIO	USB differential data (-)		90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	14	AIO	USB differential data (+)		
USB_SS1_RX_P	252	AI	USB 3.1 channel 1 super-speed receive (+)		90 Ω differential impedance. USB 3.1 standard compliant.
USB_SS1_RX_M	270	AI	USB 3.1 channel 1 super-speed receive (-)		
USB_SS1_TX_P	254	AO	USB 3.1 channel 1 super-speed transmit (+)		
USB_SS1_TX_M	253	AO	USB 3.1 channel 1 super-speed transmit (-)		

USB_SS2_RX_P	152	AI	USB 3.1 channel 2 super-speed receive (+)		
USB_SS2_RX_M	192	AI	USB 3.1 channel 2 super-speed receive (-)		
USB_SS2_TX_P	150	AO	USB 3.1 channel 2 super-speed transmit (+)		
USB_SS2_TX_M	151	AO	USB 3.1 channel 2 super-speed transmit (-)		
USB_CC1	249	AI	USB Type-C detect 1		
USB_CC2	246	AI	USB Type-C detect 2		

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	26	PO	(U)SIM1 card power supply	$I_O$max = 67 mA **1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	25	DIO	(U)SIM1 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1 VDD	Externally pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_CLK	24	DO	(U)SIM1 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_RST	23	DO	(U)SIM1 card reset		
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pulled up to 1.8 V. If unused, keep it open.
USIM2_VDD	21	PO	(U)SIM2 card power supply	$I_O$max = 67 mA **1.8 V (U)SIM:** Vmax = 1.85 V Vmin = 1.75 V **2.95 V (U)SIM:** Vmax = 3.1 V Vmin = 2.8 V	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	20	DIO	(U)SIM2 card data	V_{IL}max = 0.2 × USIM2_VDD V_{IH}min = 0.7 × USIM2_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	Externally pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_CLK	19	DO	(U)SIM2 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_RST	18	DO	(U)SIM2 card reset		
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low. Externally pulled up to 1.8 V. If unused, keep it open.

SD Card Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SD_CLK	39	DO	SD card clock	**1.8 V SD card:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{OL}max = 0.37 V V_{OH}min = 2.2 V	50 Ω characteristic impedance.
SD_CMD	40	DIO	SD card command	**1.8 V SD card:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.95 V SD card:** V_{IL}max = 0.73 V V_{IH}min = 1.84 V V_{OL}max = 0.37 V V_{OH}min = 2.2 V	
SD_DATA0	41	DIO	SDIO data bit 0		
SD_DATA1	42	DIO	SDIO data bit 1		
SD_DATA2	43	DIO	SDIO data bit 2		
SD_DATA3	44	DIO	SDIO data bit 3		
SD_DET	45	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	Active low.
SD_LDO21	38	PO	SD card power supply	2.95 V/ 841 mA	
SD_LDO4	32	PO	1.8/2.95 V output power for SD card pull-up circuits	1.8/2.95 V 22 mA	

Touch Panel Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
TP_RST	31	DO	TP reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active low.
TP_INT	30	DI	TP interrupt	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
TP_I2C_SCL	47	OD	TP I2C clock		Need to be pulled up to 1.8 V externally. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data		

LCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
LCD_RST	49	DO	LCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
LCD_TE	50	DI	LCD tearing effect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
DSI_CLK_N	52	AO	LCD MIPI clock (-)		
DSI_CLK_P	53	AO	LCD MIPI clock (+)		
DSI_LN0_N	54	AO	LCD MIPI lane 0 data (-)		
DSI_LN0_P	55	AO	LCD MIPI lane 0 data (+)		
DSI_LN1_N	56	AO	LCD MIPI lane 1 data (-)		
DSI_LN1_P	57	AO	LCD MIPI lane 1 data (+)		

DSI_LN2_N	58	AO	LCD MIPI lane 2 data (-)		
DSI_LN2_P	59	AO	LCD MIPI lane 2 data (+)		
DSI_LN3_N	60	AO	LCD MIPI lane 3 data (-)		
DSI_LN3_P	61	AO	LCD MIPI lane 3 data (+)		
PWM	29	DO	PWM output		1.8 V power domain.

Camera Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
CSI1_CLK_N	63	AI	MIPI CSI1 clock (-)		
CSI1_CLK_P	64	AI	MIPI CSI1 clock (+)		
CSI1_LN0_N	65	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN0_P	66	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN1_N	67	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN1_P	68	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN2_N	72	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN2_P	73	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN3_N	70	AI	MIPI CSI1 lane 3 data (-)		
CSI1_LN3_P	71	AI	MIPI CSI1 lane 3 data (+)		
CSI0_CLK_N	157	AI	MIPI CSI0 clock (-)		
CSI0_CLK_P	196	AI	MIPI CSI0 clock (+)		
CSI0_LN0_N	158	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN0_P	197	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN1_N	159	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN1_P	198	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN2_N	160	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN2_P	199	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN3_N	161	AI	MIPI CSI0 lane 3 data (-)		
CSI0_LN3_P	200	AI	MIPI CSI0 lane 3 data (+)		
CAM0_I2C_SCL	83	OD	I2C clock of camera 0		Need to be pulled up to 1.8 V externally. For I2C application, these pins can only be used for camera I2C and can not be
CAM0_I2C_SDA	84	OD	I2C data of camera 0		

					connected to other I2C devices.
CAM0_PWDN	80	DO	Power down of camera 0		
CAM1_PWDN	82	DO	Power down of camera 1		
CAM2_PWDN	163	DO	Power down of camera 2		
CAM0_MCLK	74	DO	Master clock of camera 0		
CAM1_MCLK	75	DO	Master clock of camera 1	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
CAM2_MCLK	165	DO	Master clock of camera 2		
CAM0_RST	79	DO	Reset of camera 0		
CAM1_RST	81	DO	Reset of camera 1		
CAM2_RST	164	DO	Reset of camera 2		
CAM1_I2C_SCL	166	OD	I2C clock of camera 1		Need to be pulled up to 1.8 V externally. For I2C application, these pins can only be used for camera I2C and can not be connected to other I2C devices.
CAM1_I2C_SDA	205	OD	I2C data of camera 1		
Flash & Torch Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED	180	AO	Flash/torch driver output	$I_O$max = 1 A	Supports flash and torch modes.
Indication Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CHG_LED	195	AI	Indicate the module's charging status	$I_I$max = 5 mA	
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	114	DI	Turn on/off the module		Pulled up to 1.1 V internally. Active low.
VOL_UP	95	DI	Volume up	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	If unused, keep it open. Cannot be externally pulled up. 1.8 V power domain.
VOL_DOWN	96	DI	Volume down		
RESET_N	225	DI	Reset the module		Disabled by default and it can be enabled via software configuration. A test point is recommended to be reserved if unused.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

DBG_TXD	94	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
DBG_RXD	93	DI	Debug UART receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART0_TXD	34	DO	UART0 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART0_RXD	35	DI	UART0 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART0_RTS	37	DO	Request to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART0_CTS	36	DI	Clear to send signal to the module	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
UART1_TXD	154	DO	UART1 transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
UART1_RXD	153	DI	UART1 receive	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	

Sensor I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor		Need to be pulled up to 1.8 V externally. Can only be used for sensors. SENSOR_I2C only supports sensors of ADSP architecture.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor		

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	87	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	121	AI	GNSS antenna interface		
ANT_DRX	131	AI	Diversity antenna interface		
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface		

Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC_13	173	DIO	Generic RF controller		Cannot be multiplexed into a generic GPIO. Cannot be pulled up during startup.
GRFC_14	260	DIO	Generic RF controller		
GRFC_15	262	DIO	Generic RF controller		Cannot be multiplexed into a generic GPIO.

ADC Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC	128	AI	General-purpose ADC interface		The maximum input voltage is 1.875 V.

Charging Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment

BAT_P	133	AI	Battery voltage detect (+)		Cannot be kept open.
BAT_M	183	AI	Battery voltage detect (-)		
BAT_ID	185	AI	Battery type detect	$V_I$min = 0 V $V_I$max = 1.875 V	Internally pulled down with a 100 kΩ resistor. If unused, keep it open.
BAT_THERM	134	AI	Battery temperature detect		Internally pulled up by default. Supports 47 kΩ NTC thermistor by default. If unused, connect it to GND with a 47 kΩ resistor.

Vibration Motor Driver Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VIB_DRV_P	28	PO	Vibration motor driver output control	Vmin = 1.5 V Vmax = 3.3 V $I_O$max = 100 mA	Connect it to the positive pole of the motor.

Other Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	46	DI	Force the module into download mode		Force the module to enter download mode by pulling this pin up to LDO15A_1V8 before turning on the module.
GNSS_LNA_EN	194	DO	GNSS LNA enable control		
NFC_CLK	181	DO	NFC clock		The default output frequency is 38.4 MHz.
CBL_PWR_N	186	DI	Cable power-on; Initiate power-on when grounded		The module cannot be turned off when this pin is pulled down. If unused, keep it open.

GPIO Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO_28	33	DIO	General-purpose input/output		1.8 V power domain
GPIO_31	97	DIO	General-purpose input/output		
GPIO_32	99	DIO	General-purpose input/output		
GPIO_33	108	DIO	General-purpose input/output		
GPIO_34	109	DIO	General-purpose input/output		
GPIO_35	107	DIO	General-purpose input/output		
GPIO_36	110	DIO	General-purpose input/output		
GPIO_55	100	DIO	General-purpose input/output		
GPIO_56	106	DIO	General-purpose input/output		

GPIO_57	112	DIO	General-purpose input/output	1.8 V power domain Cannot be pulled up during startup.
GPIO_58	113	DIO	General-purpose input/output	
GPIO_60	123	DIO	General-purpose input/output	
GPIO_86	182	DIO	General-purpose input/output	
GPIO_112	177	DIO	General-purpose input/output	
GPIO_111	267	DIO	General-purpose input/output	
GPIO_98	265	DIO	General-purpose input/output	
GPIO_99	105	DIO	General-purpose input/output	
GPIO_100	264	DIO	General-purpose input/output	
GPIO_101	239	DIO	General-purpose input/output	
GPIO_102	104	DIO	General-purpose input/output	
GPIO_103	103	DIO	General-purpose input/output	
GPIO_104	101	DIO	General-purpose input/output	1.8 V power domain
GPIO_105	102	DIO	General-purpose input/output	
GPIO_106	90	DIO	General-purpose input/output	
GPIO_107	98	DIO	General-purpose input/output	
GPIO_14	118	DIO	General-purpose input/output	
GPIO_15	119	DIO	General-purpose input/output	
GPIO_16	116	DIO	General-purpose input/output	
GPIO_17	117	DIO	General-purpose input/output	
PMU_GPIO03	124	DIO	General-purpose input/output	
PMU_GPIO04	115	DIO	General-purpose input/output	
PMU_GPIO08	127	DIO	General-purpose input/output	
PMU_GPIO07	201	DIO	General-purpose input/output	

GND

Pin Name	**Pin No.**
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 162, 171, 172, 176, 187–191, 202–204, 206–224, 226–231, 233–238, 240, 241, 243–245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271–274

RESERVED

Pin Name	**Pin No.**

RESERVED	16, 167, 168, 169, 170, 174, 175, 178, 179, 193, 232, 242, 257, 263

NOTE

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to the ground unless otherwise specified.

3.3. Power Supply

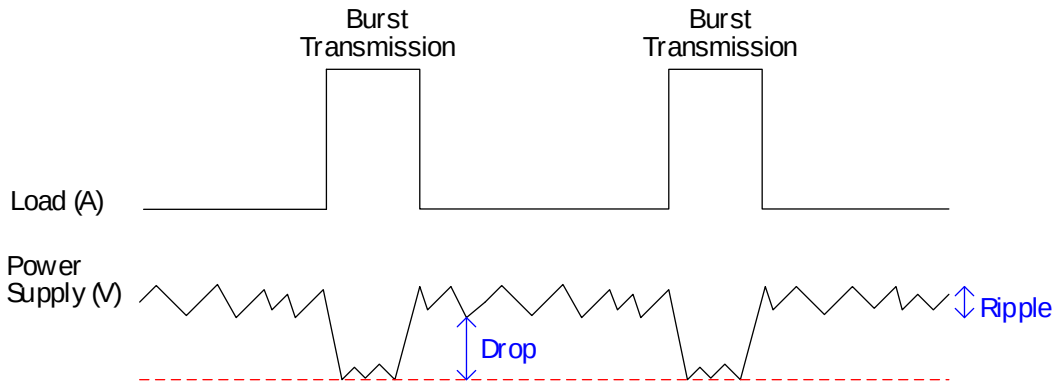
3.3.1. Power Supply Pins

The module provides four VBAT pins for connection with external power supply.

3.3.2. Voltage Stability Requirements

The power supply range of the module is 3.55–4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity and voltage ripple, will directly influence the module's performance and stability. Under ultimate conditions, the transient peak current of the module may surge up to 3 A. If the power supply capacity is not sufficient, there will be a risk that the module may turn off automatically if the voltage drops below 3.1 V. Therefore, make sure the input voltage never drops below 3.1 V.

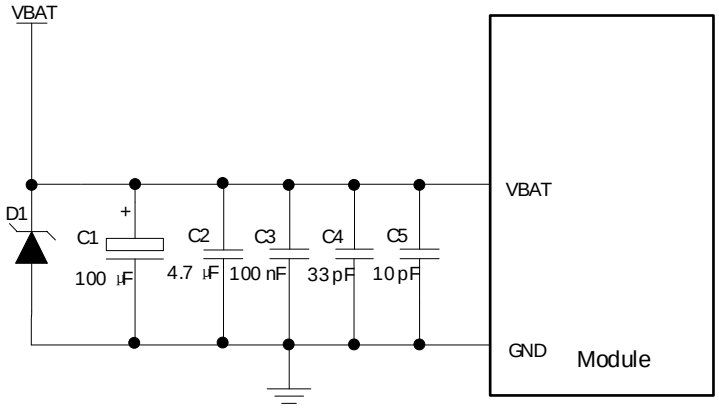
Figure 1: Power Supply Limits During Burst Transmission



To decrease voltage drop, use a bypass capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array and place these capacitors close to VBAT pins. Additionally, add a 4.7 µF capacitor in parallel. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration. The width of VBAT trace should be not less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to guarantee the stability of the power source, please use a TVS and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows the star configuration of the power supply.

Figure 2: Reference Circuit for Power Supply

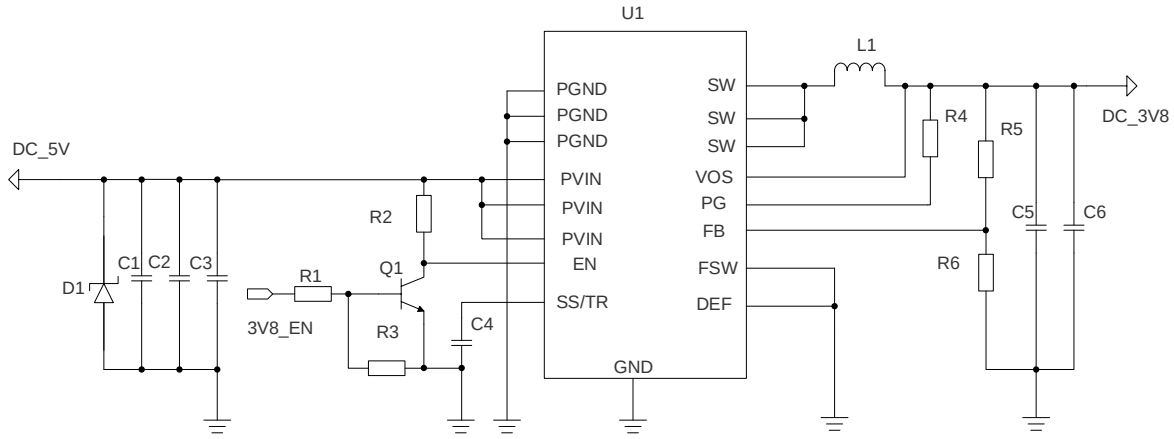


3.3.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3 A at least. If the voltage difference between the input and output is not too big, use an LDO when supplying power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5 V input power source. The typical output voltage is 3.8 V and the maximum load current is 5.0 A.

Figure 3: Reference Circuit of Power Supply



NOTE

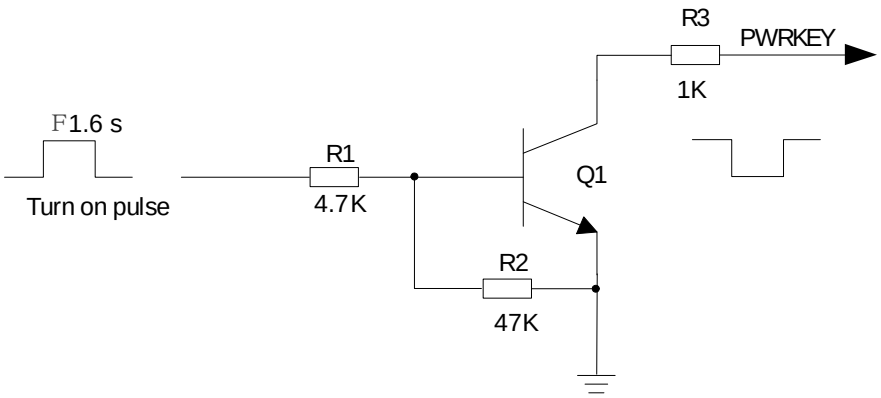
1. In an abnormal state, it is recommended to restart the module by first turning off the power supply and then powering up.
2. The module supports battery charging by default. If the above power supply design is adopted, disable the charging function by software, or connect VBAT to a Schottky diode in series to avoid the reverse current to the power supply IC.

3.4. Turn On/Off

3.4.1. Turn On with PWRKEY

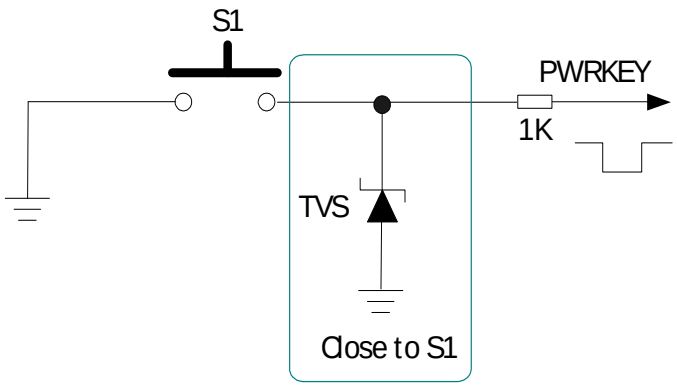
The module can be turned on by driving the PWRKEY pin low for at least 1.6 s. The PWRKEY pin is pulled up to 1.1 V internally. It is recommended to use an open collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

Figure 4: Turn On Module with Open Collector Driver



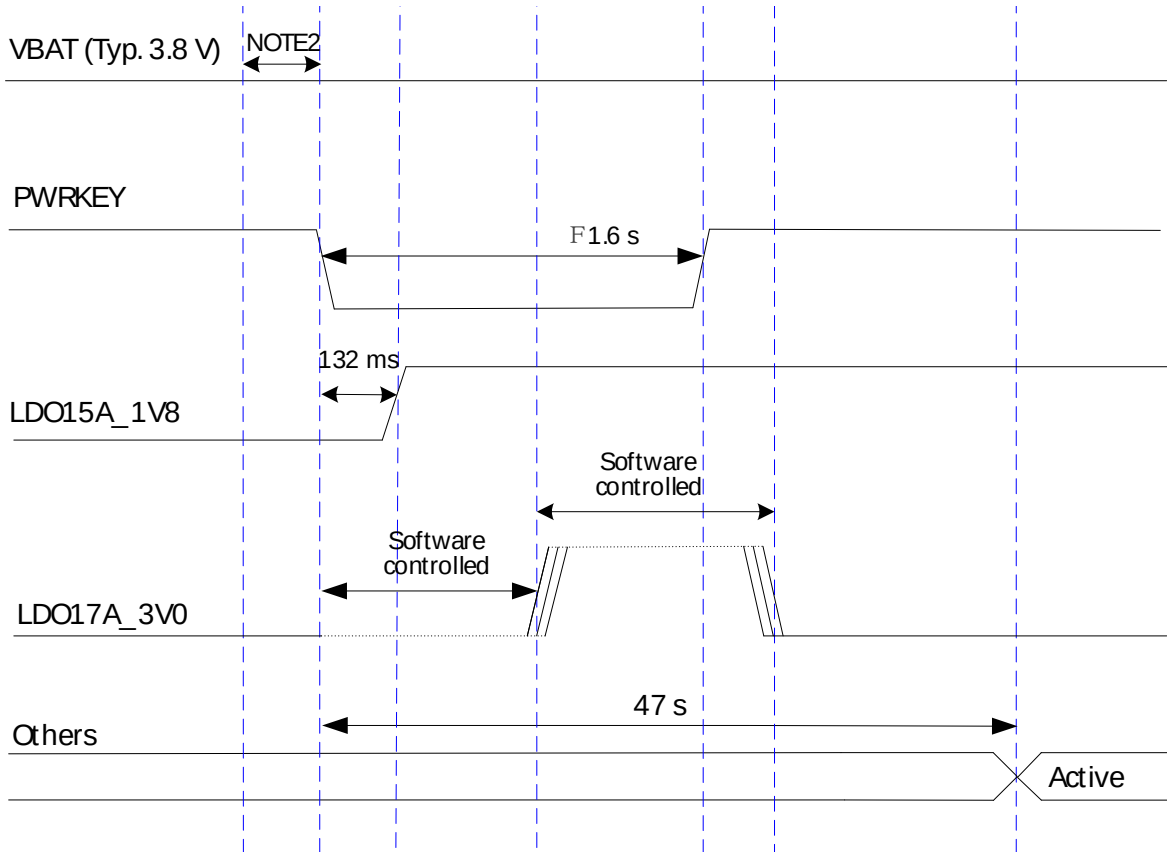
Another way to control PWRKEY is by using a button directly. You must place a TVS nearby the button for ESD protection. A reference circuit is shown by the following figure.

Figure 5: Turn On Module with Button



The turning-on scenario is illustrated in the following figure.

Figure 6: Turn-on Timing



NOTE

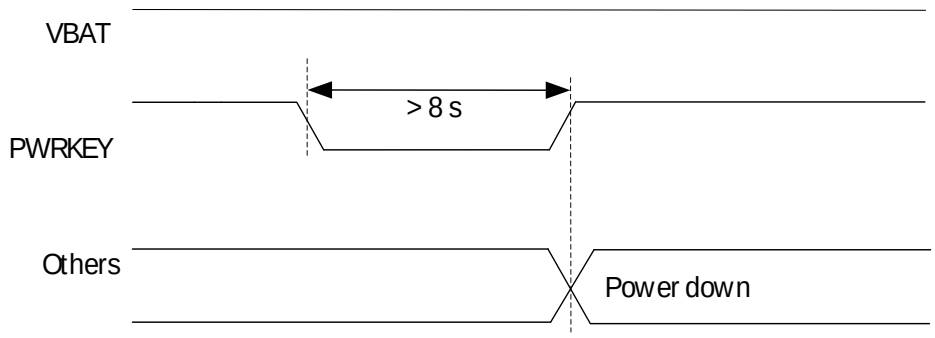
1. When the module is turned on for the first time, the turn-on timing may be different from that shown above.
2. Make sure that VBAT is stable before pulling down PWRKEY. It is recommended to wait until VBAT is stable at 3.8 V for at least 30 ms before pulling down PWRKEY. Additionally, do not keep pulling PWRKEY down all the time.

3.4.2. Turn Off

Drive the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.
oose to turn off the module when the prompt window comes up.

You can also force the module to turn off by driving PWRKEY low for more than 8 s. The forced turn-off timing is illustrated by the following figure.

Figure 7: Forced Turn-off Timing



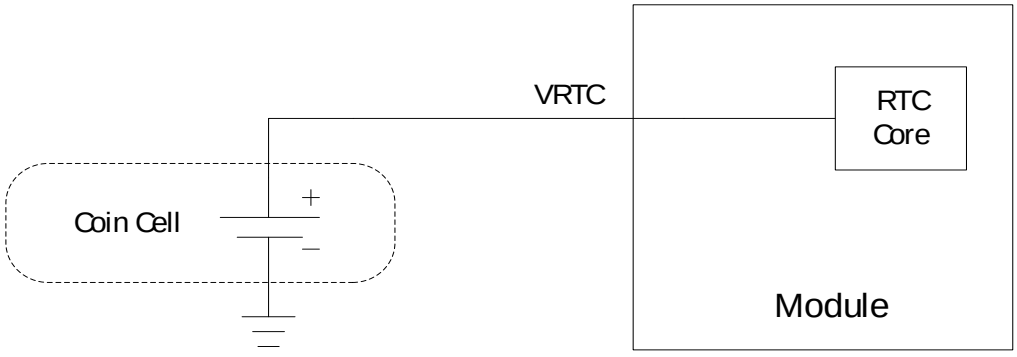
3.5. VRTC

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supplied to VBAT. The external power source can be a rechargeable battery (such as a coin cell) according to application demands. A reference circuit design is shown below.

Table 5: Pin definition of VRTC

Pin Name	Pin No.	I/O	Description	Comment
VRTC	126	PIO	Power supply for RTC	If unused, keep it open.

Figure 8: RTC Powered by Coin Cell



If RTC fails, the module can synchronize time over the network after being powering up. The recommended input voltage range for VRTC is 2.5–3.2 V and the recommended typical value is 3.0 V.

3.6. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In applications, it is recommended to use a 33 pF and a 10 pF capacitor in parallel in the circuit to suppress high-frequency

noise.

Table 6: Power Description

Pin Name	Pin No.	Default Voltage (V)	Driving Current (mA)	@ Idle State
LDO15A_1V8	111	1.8	200	Keeps ON
LDO_IOVDD	125	1.8	300	-
VDD_2V8	129	2.8	500	-
LDO17A_3V0	156	3.0	192	-

3.7. Charging Interface

The module supports battery charging. The battery charger IC in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- Trickle charging: There are two steps in this mode. When the battery voltage is below 2.1 V, a 90 mA trickle charging current is applied to the battery. When the battery voltage is charged up and is between 2.1 V and 3.4 V, the charging current can be set to 400 mA maximally.
- Constant current mode (CC mode): When the battery is increased to 3.4 to 4.35 V, the system will switch to CC mode. The maximum charging current is 1.85 A when an adapter is used for battery charging, and the maximum charging current is 450 mA for USB charging.
- Constant voltage mode (CV mode): When the battery voltage reaches the constant current charging cut-off voltage, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, charging is completed.

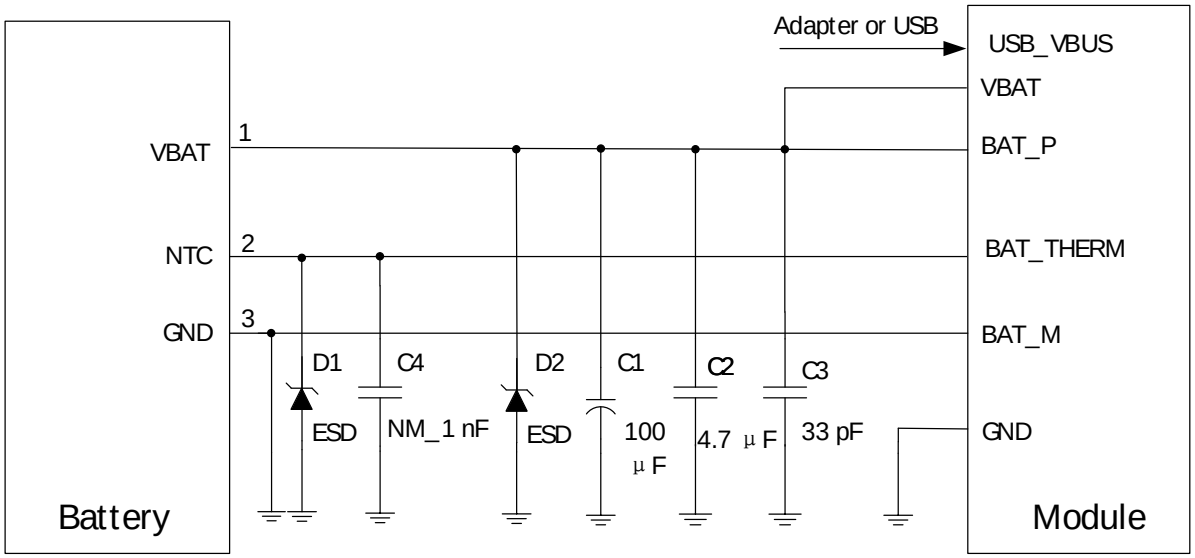
Table 7: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	133	AI	Battery voltage detect (+)	Cannot be kept open.
BAT_M	183	AI	Battery voltage detect (-)	
BAT_THERM	134	AI	Battery temperature detect	Internally pulled up by default. Supports 47 kΩ NTC thermistor by default. If unused, connect it to GND with a 47 kΩ resistor.
BAT_ID	185	AI	Battery type detect	Internally pulled down with a 100 kΩ resistor. If unused, keep it open.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (47 kΩ 1 % NTC thermistor with a B-constant of 4050 K by default) and the thermistor is connected to BAT_THERM pin. If the BAT_THERM pin is not connected, there will be malfunctions such as boot error, battery charging failure, and battery level display error. The battery charge temperature range varies with different types of batteries.

A reference design for the battery charging circuit is shown below.

Figure 9: Reference Design for Battery Charging Circuit



Mobile devices such as mobile phones or handheld POS systems are powered by batteries. For different batteries, you should modify the charging and discharging curve correspondingly to achieve the best performance.

If the thermistor is not available in the battery, or an adapter is utilized to power the module, you must connect BAT_THERM to GND via a 47 kΩ resistor. Otherwise, the system may mistakenly judge that the battery temperature is abnormal, and therefore cause battery charging failure.

BAT_P and BAT_M must be connected. Otherwise, exceptions in voltage detection will be caused, with associated problems of turn-on/off and battery charging/discharging.

3.8. USB Interface (Type-C)

The module provides one USB interface which complies with both USB 3.1 Gen 1 and USB 2.0 specifications and supports SuperSpeed (5 Gbps) and high-speed (480 Mbps), and full-speed (12 Mbps) modes. The USB interface supports USB OTG and is used for AT command transmission, data transmission, software debugging and firmware upgrade.

The module only supports USB Type-C. It provides one USB 2.0 compliant high-speed interface (USB_DP, USB_DM) and two USB 3.1 compliant SuperSpeed interfaces (USB_SS1_RX_P/M, USB_SS1_TX_P/M and USB_SS2_RX_P/M, USB_SS2_TX_P/M).

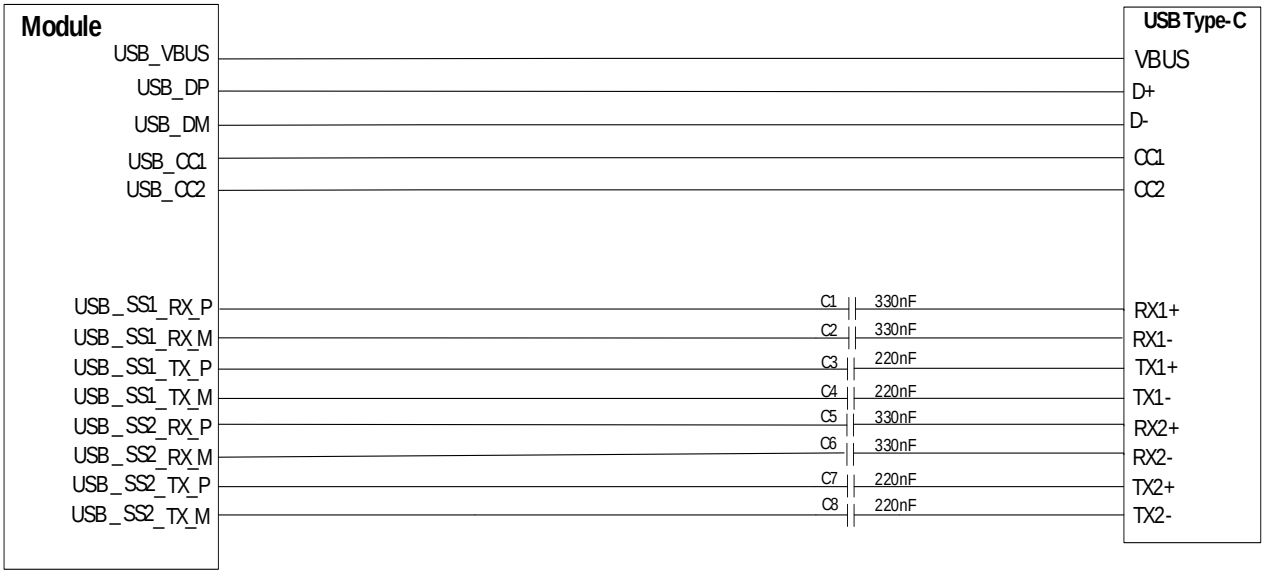
When Type-C is plugged in with one side up, the external device is detected by USB_CC1, and the data will be transmitted through USB_SS1; when it is plugged in with the other side up, the external device is detected by USB_CC2, and the data will be transmitted through USB_SS2. The following table shows the pin definition of USB interface.

Table 8: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	Maximum output current is 500 mA.

USB_DM	13	AIO	USB differential data (-)	90 Ω differential impedance. USB 2.0 standard compliant.
USB_DP	14	AIO	USB differential data (+)	
USB_SS1_RX_P	252	AI	USB 3.1 channel 1 super-speed receive (+)	90 Ω differential impedance. USB 3.1 standard compliant.
USB_SS1_RX_M	270	AI	USB 3.1 channel 1 super-speed receive (-)	
USB_SS1_TX_P	254	AO	USB 3.1 channel 1 super-speed transmit (+)	
USB_SS1_TX_M	253	AO	USB 3.1 channel 1 super-speed transmit (-)	
USB_SS2_RX_P	152	AI	USB 3.1 channel 2 super-speed receive (+)	
USB_SS2_RX_M	192	AI	USB 3.1 channel 2 super-speed receive (-)	
USB_SS2_TX_P	150	AO	USB 3.1 channel 2 super-speed transmit (+)	
USB_SS2_TX_M	151	AO	USB 3.1 channel 2 super-speed transmit (-)	
USB_CC1	249	AI	USB Type-C detect 1	
USB_CC2	246	AI	USB Type-C detect 2	

Figure 10: USB Interface Reference Design (OTG Supported)



In order to ensure USB performance, comply with the following principles when designing the USB interface.

- Route the USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace should be controlled to 90 Ω.
- Keep the ESD protection component as close as possible to the USB connector. Pay attention to the influence of junction capacitance of ESD protection component on USB data lines. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that

layer and with ground planes above and below.
- Make sure the intra-pair length difference within USB 2.0 differential pair does not exceed 2 mm, and that within USB 3.1 Rx or Tx differential pair does not exceed 0.7 mm.
- The spacing between USB 3.1 Rx and Tx signals should be at least 3 times the trace width and the spacing between USB 3.1 signals and other signals should be at least 4 times the trace width. The spacing between USB 2.0 signals and other signals should be at least 3 times the trace width.
- For USB 3.1, it is suggested to do simulation after the design is completed. If the cable is too long or there are too many vias, a redriver can be added to ensure the quality of signal transmission if necessary.

Table 9: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (P - M)
13	USB_DM	24.13	0.24
14	USB_DP	24.37	
252	USB_SS1_RX_P	16.33	-0.17
270	USB_SS1_RX_M	16.50	
254	USB_SS1_TX_P	10.07	-0.07
253	USB_SS1_TX_M	10.14	
152	USB_SS2_RX_P	17.74	-0.28
192	USB_SS2_RX_M	18.02	
150	USB_SS2_TX_P	20.84	0.30
151	USB_SS2_TX_M	20.54	

3.9. UART Interfaces

The module provides three UART interfaces:

- UART0: four-wire UART interface, supports RTS and CTS hardware flow control
- UART4 (debug UART): two-wire UART interface, dedicated for debugging
- UART1: two-wire UART interface

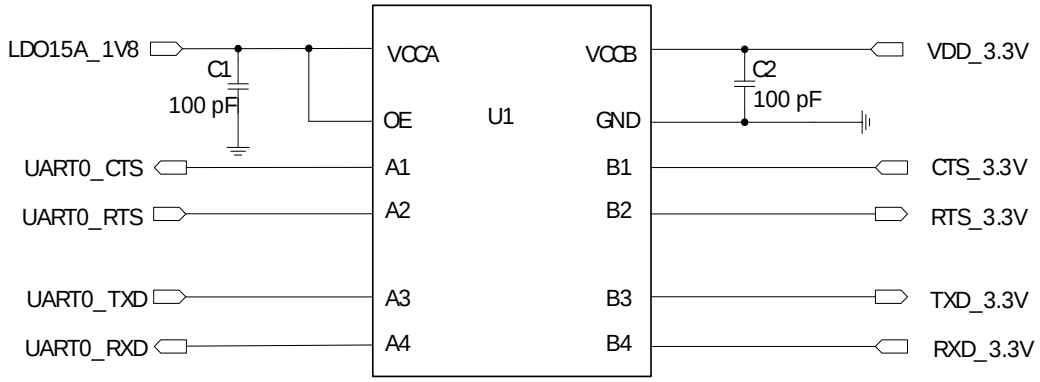
Table 10: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
UART0_TXD	34	DO	UART0 transmit	1.8 V power domain. If unused, keep it open.
UART0_RXD	35	DI	UART0 receive	
UART0_RTS	37	DO	Request to send signal from the module	

UART0_CTS	36	DI	Clear to send signal to the module
DBG_TXD	94	DO	Debug UART transmit
DBG_RXD	93	DI	Debug UART receive
UART1_TXD	154	DO	UART1 transmit
UART1_RXD	153	DI	UART1 receive

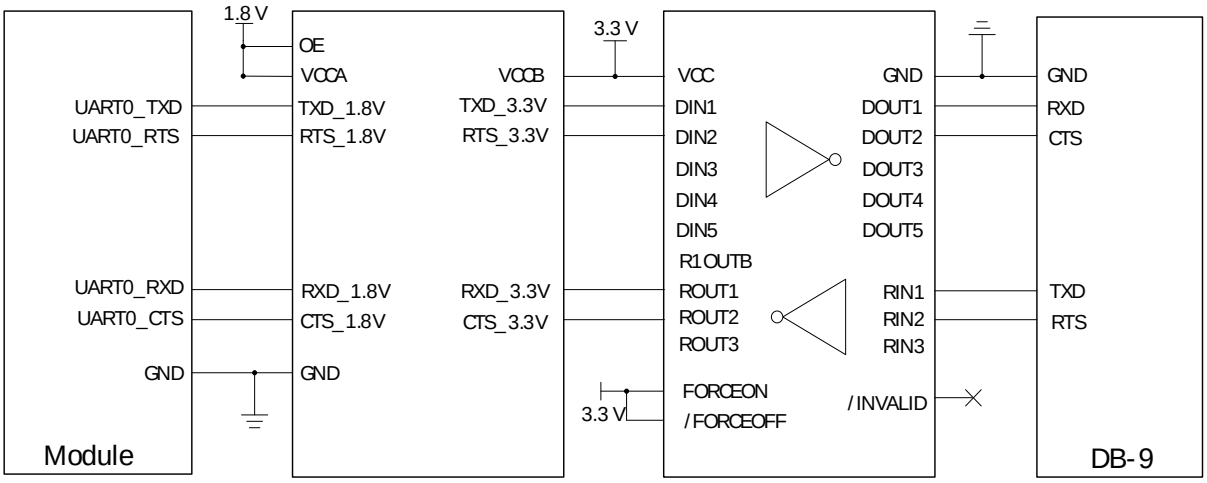
UART0 is a four-wire UART interface with 1.8 V power domain. You should use a level-shifting chip if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

Figure 11: Reference Circuit with Level-shifting Chip for UART0



The following figure presents an example of connection between the module and a PC. It is recommended to add a level-shifting chip and an RS-232 level-shifting chip between the module and the PC.

Figure 12: RS-232 Level Match Circuit for UART0



NOTE

UART4 (debug UART) and UART1 are similar to UART0. For the reference designs, refer to that of UART0.

3.10. (U)SIM Interfaces

The module provides two (U)SIM interfaces that meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card is powered by the internal power supply of the module.

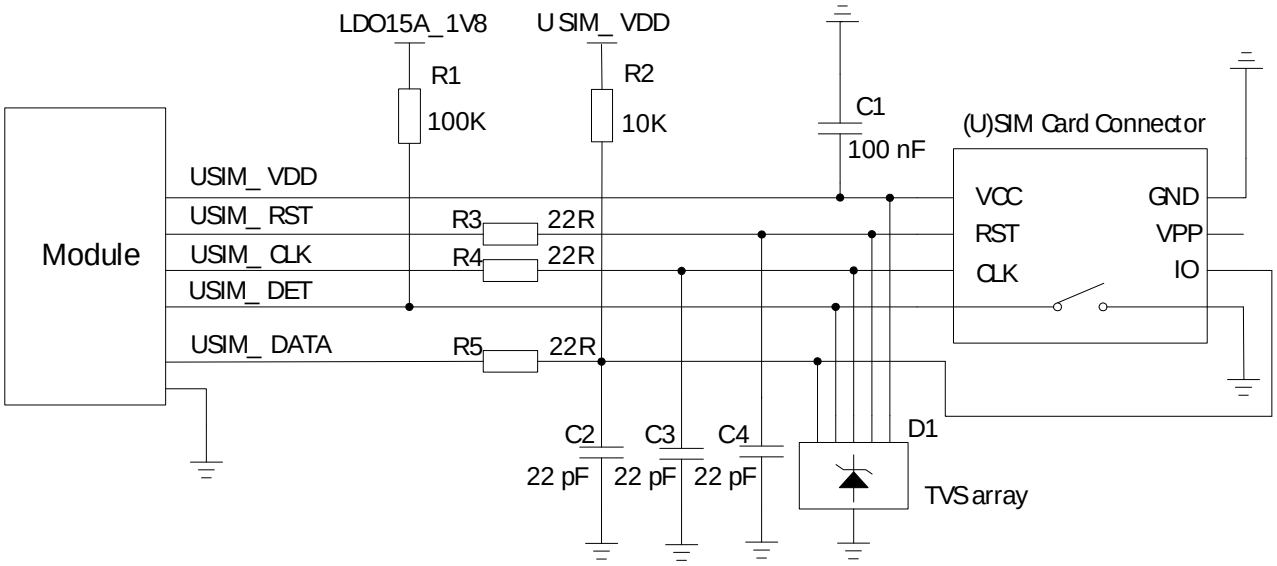
Table 11: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	25	DIO	(U)SIM1 card data	Externally pulled up to USIM1_VDD with a 10 kΩ resistor.
USIM1_CLK	24	DO	(U)SIM1 card clock	
USIM1_RST	23	DO	(U)SIM1 card reset	
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	Active low. Externally pulled up to 1.8 V. If unused, keep it open.
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	20	DIO	(U)SIM2 card data	Externally pulled up to USIM2_VDD with a 10 kΩ resistor.
USIM2_CLK	19	DO	(U)SIM2 card clock	
USIM2_RST	18	DO	(U)SIM2 card reset	
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	Active low. Externally pulled up to 1.8 V. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pins. This function is disabled by default via software. To enable it, contact Netprisma Technical Support to change the software configuration.

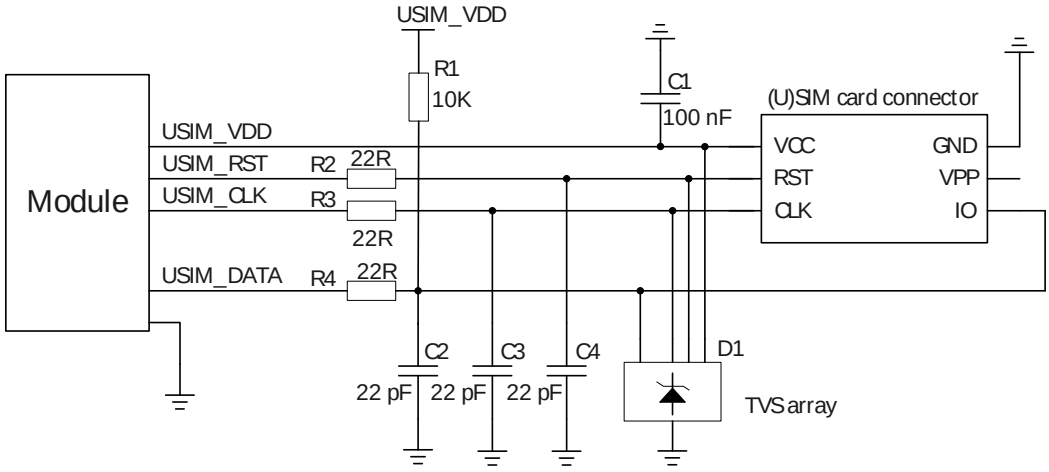
A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

Figure 13: Reference Circuit for (U)SIM Interface with an 8-pin (U)SIM Card Connector



If you do not need hot-plug detection, keep USIM1_DET and USIM2_DET pins open. The following is a reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector when hot-plug detection is not needed.

Figure 14: Reference Circuit for (U)SIM Interface with a 6-pin (U)SIM Card Connector



To enhance the reliability and availability of the (U)SIM card in applications, you should follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Reserve a filter capacitor for USIM_VDD, and its maximum capacitance should not exceed 1 μF. Additionally, place the capacitor near the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground. USIM_RST also needs ground protection.
- To ensure better ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 10 pF. Add 22 Ω resistors in series between the module and (U)SIM card to suppress EMI and improve ESD protection. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- Add 22 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter RF interference, and place them as close to the (U)SIM card connector as possible.

3.11. SD Card Interface

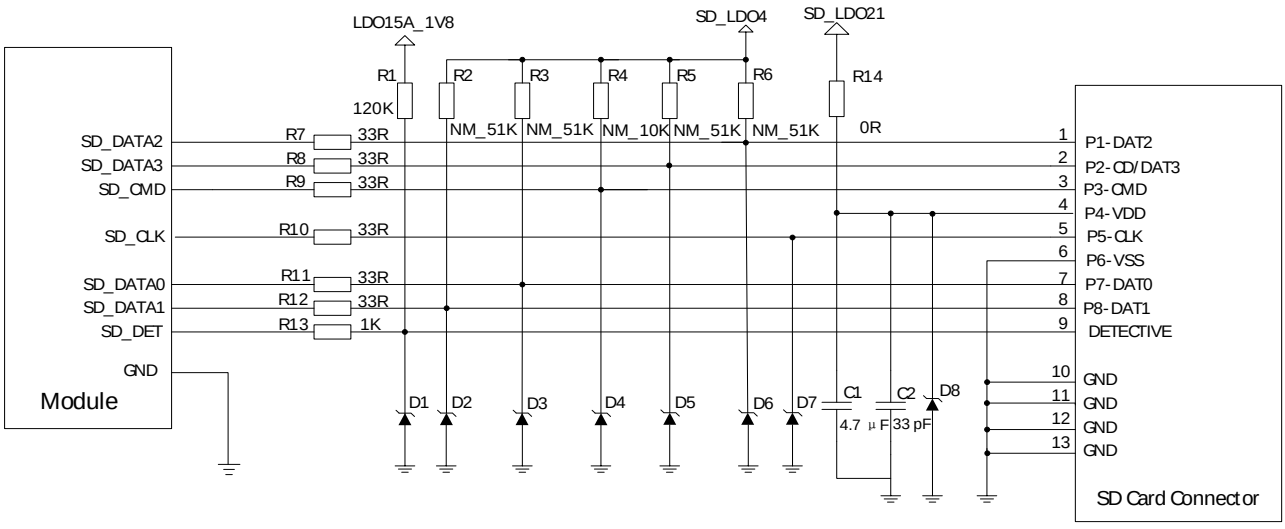
SD card interface of the module supports SD 3.0 protocol. The pin definition of SD card interface is shown below.

Table 12: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	39	DO	SD card clock	50 Ω characteristic impedance.
SD_CMD	40	DIO	SD card command	
SD_DATA0	41	DIO	SDIO data bit 0	
SD_DATA1	42	DIO	SDIO data bit 1	
SD_DATA2	43	DIO	SDIO data bit 2	
SD_DATA3	44	DIO	SDIO data bit 3	
SD_DET	45	DI	SD card hot-plug detect	Active low.
SD_LDO21	38	PO	SD card power supply	
SD_LDO4	32	PO	1.8/2.95 V output power for SD card pull-up circuits	

A reference circuit for the SD card interface is shown below.

Figure 15: Reference Circuit for the SD Card Interface



SD_LDO21 is the power supply for the SD card and can provide up to 841 mA output current. Due to the

high output current, it is recommended that the trace width should be at least 0.8 mm. To ensure output current stability, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2, and SD_DATA3 are all high-speed signal traces. In PCB design, control the characteristic impedance of them to 50 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of the PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control the impedance to 50 Ω ±10 % and add ground shielding.
- Keep the trace length difference between SD_CLK and SD_CMD/SD_DATA less than 2 mm.
- Spacing between signal traces should be 1.5 times the trace width.
- The load capacitance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 5 pF.

Table 13: SD Card Interface Trace Length Inside the Module

Pin No.	Signal	Length (mm)
39	SD_CLK	35.01
40	SD_CMD	35.12
41	SD_DATA0	34.98
42	SD_DATA1	35.04
43	SD_DATA2	34.98
44	SD_DATA3	35.10

3.12. GPIO Interfaces

The module has abundant GPIO interfaces with a power domain of 1.8 V. The pin definition is listed below.

Table 14: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_28	33	DIO	General-purpose input/output	
GPIO_31	97	DIO	General-purpose input/output	
GPIO_32	99	DIO	General-purpose input/output	
GPIO_33	108	DIO	General-purpose input/output	
GPIO_34	109	DIO	General-purpose input/output	
GPIO_35	107	DIO	General-purpose input/output	
GPIO_36	110	DIO	General-purpose input/output	

GPIO_55	100	DIO	General-purpose input/output	
GPIO_56	106	DIO	General-purpose input/output	
GPIO_57	112	DIO	General-purpose input/output	Cannot be pulled up during startup.
GPIO_58	113	DIO	General-purpose input/output	
GPIO_60	123	DIO	General-purpose input/output	
GPIO_86	182	DIO	General-purpose input/output	
GPIO_112	177	DIO	General-purpose input/output	
GPIO_111	267	DIO	General-purpose input/output	
GPIO_98	265	DIO	General-purpose input/output	
GPIO_99	105	DIO	General-purpose input/output	
GPIO_100	264	DIO	General-purpose input/output	
GPIO_101	239	DIO	General-purpose input/output	
GPIO_102	104	DIO	General-purpose input/output	
GPIO_103	103	DIO	General-purpose input/output	
GPIO_104	101	DIO	General-purpose input/output	
GPIO_105	102	DIO	General-purpose input/output	
GPIO_106	90	DIO	General-purpose input/output	
GPIO_107	98	DIO	General-purpose input/output	
GPIO_14	118	DIO	General-purpose input/output	
GPIO_15	119	DIO	General-purpose input/output	
GPIO_16	116	DIO	General-purpose input/output	
GPIO_17	117	DIO	General-purpose input/output	
PMU_GPIO03	124	DIO	General-purpose input/output	
PMU_GPIO04	115	DIO	General-purpose input/output	
PMU_GPIO08	127	DIO	General-purpose input/output	
PMU_GPIO07	201	DIO	General-purpose input/output	

NOTE

For more details about GPIO configuration, see ***document 1***.

3.13. I2C Interfaces

The module provides four I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. SENSOR_I2C only supports sensors of ADSP architecture. CAM0_I2C and CAM1_I2C signals are controlled by Linux Kernel code and support connection with video-output-related devices.

Table 15: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	47	OD	TP I2C clock	Need to be pulled up to 1.8 V externally. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data	
CAM0_I2C_SCL	83	OD	I2C clock of camera 0	For I2C application, these pins can only be used for camera I2C and can not be connected to other I2C devices.
CAM0_I2C_SDA	84	OD	I2C data of camera 0	
CAM1_I2C_SCL	166	OD	I2C clock of camera 1	
CAM1_I2C_SDA	205	OD	I2C data of camera 1	
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	For I2C application, these pins can only be used for sensor I2C and can not be connected to other I2C devices. SENSOR_I2C only supports sensors of ADSP architecture.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	

3.14. ADC Interface

The module supports one Analog-to-Digital Converter (ADC) interface. The ADC interface supports resolution of up to 15 bits. The pin definition is shown below.

Table 16: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC	128	AI	General-purpose ADC interface	The maximum input voltage is 1.875 V.

3.15. Vibration Motor Driver Interface

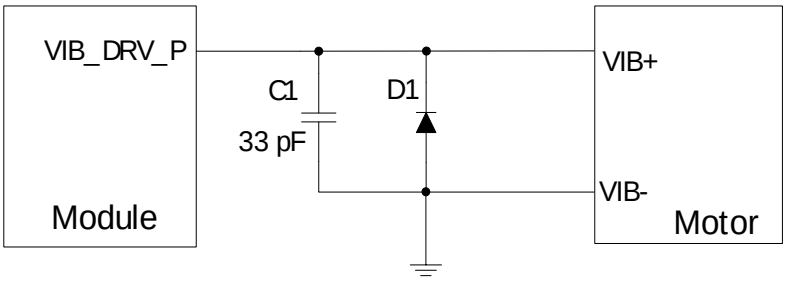
The pin definition of the vibration motor driver interface is listed below.

Table 17: Pin Definition of Vibration Motor Driver Interface

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV_P	28	PO	Vibration motor driver output control	Connect it to the positive pole of the motor.

The motor is driven by an exclusive circuit, and a reference circuit is shown below.

Figure 16: Reference Circuit for Motor Connection



When the motor stops working and the VIB_DRV_P is disconnected, the redundant electricity on the motor can be discharged from the circuit loop formed by diodes, thus avoiding damage to components.

3.16. LCM Interface

The module provides one LCM interface, which is MIPI DSI standard compliant. The interface supports high-speed differential data transmission and supports HD+ display (1680 × 720 @ 60 fps). The pin definition of the LCM interface is shown below.

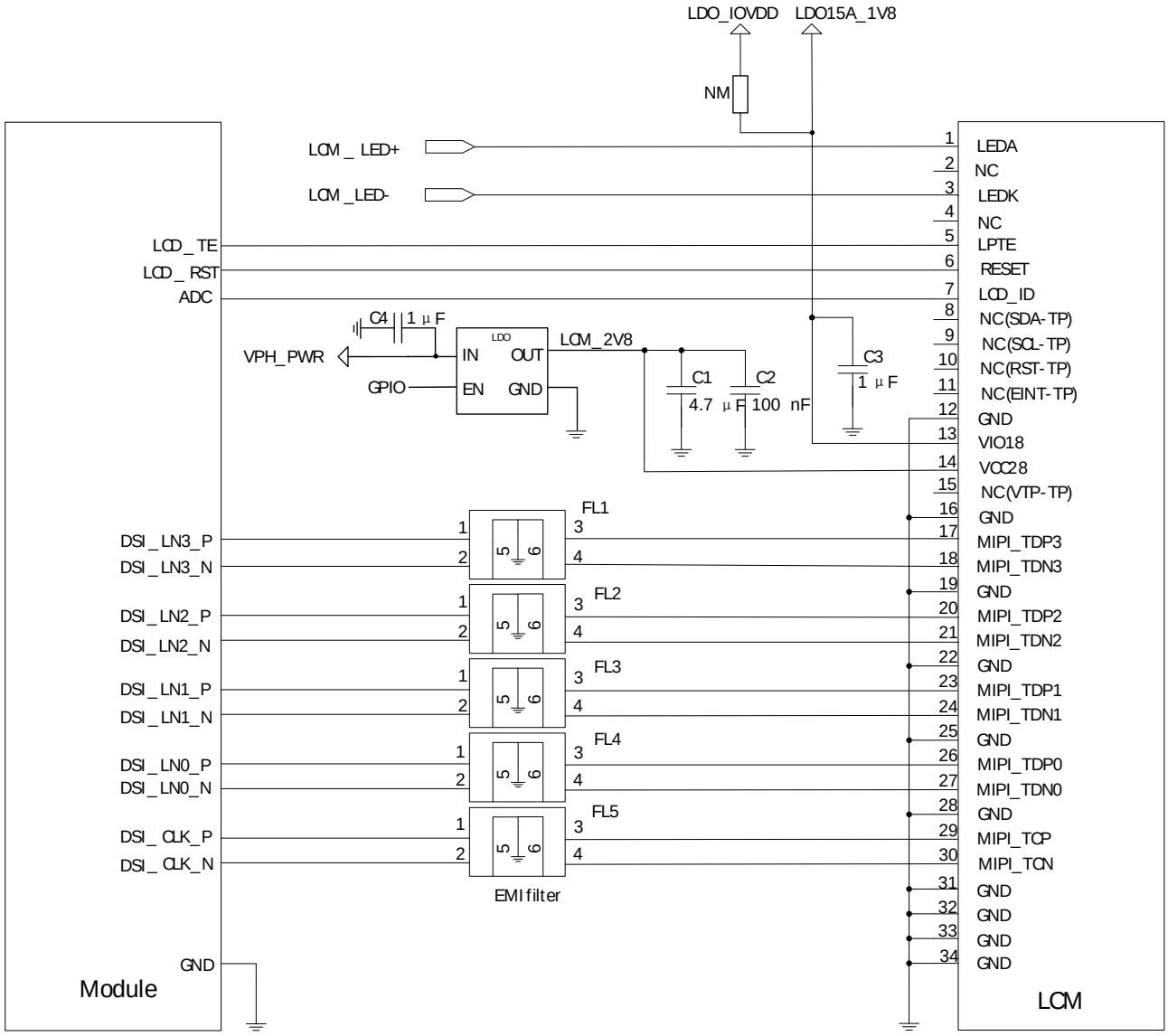
Table 18: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	1.8 V power domain.
LCD_TE	50	DI	LCD tearing effect	
DSI_CLK_N	52	AO	LCD MIPI clock (-)	
DSI_CLK_P	53	AO	LCD MIPI clock (+)	
DSI_LN0_N	54	AO	LCD MIPI lane 0 data (-)	
DSI_LN0_P	55	AO	LCD MIPI lane 0 data (+)	
DSI_LN1_N	56	AO	LCD MIPI lane 1 data (-)	

DSI_LN1_P	57	AO	LCD MIPI lane 1 data (+)	
DSI_LN2_N	58	AO	LCD MIPI lane 2 data (-)	
DSI_LN2_P	59	AO	LCD MIPI lane 2 data (+)	
DSI_LN3_N	60	AO	LCD MIPI lane 3 data (-)	
DSI_LN3_P	61	AO	LCD MIPI lane 3 data (+)	
PWM	29	DO	PWM output	1.8 V power domain.

A reference circuit for the LCM interface is shown below.

Figure 17: Reference Circuit Design for LCM Interface

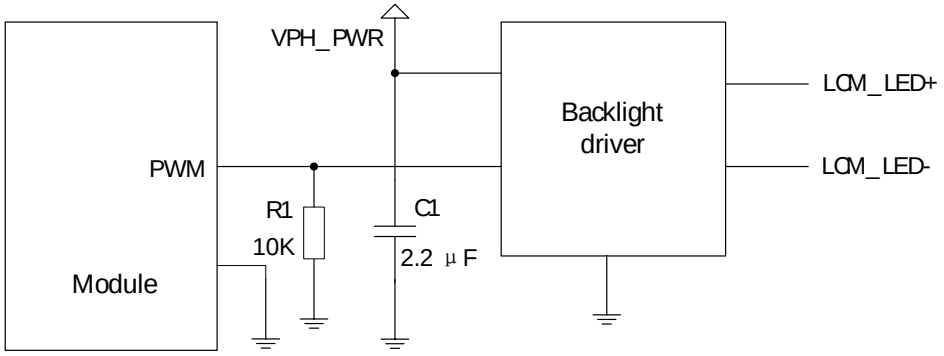


MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that the LCM factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but you need to make sure that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

You can design the external backlight driving circuit for LCM according to actual requirements. A reference circuit design is shown in the following figure, in which the PWM pin is used to adjust the backlight brightness.

Figure 18: Reference Design for LCM External Backlight Driving Circuit



For more details about the principles when designing LCM interface, see ***Chapter 3.19.1***.

3.17. Flash & Torch Interface

The module supports one flash LED driver, with maximum output current up to 1 A.

Table 19: Pin Definition of Flash & Torch Interface

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED	180	AO	Flash/torch driver output	Supports flash and torch modes.

NOTE

Flash current is programmable in step 12.5 mA (max. 1 A) or 5 mA (max. 640 mA).

3.18. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and also provides the

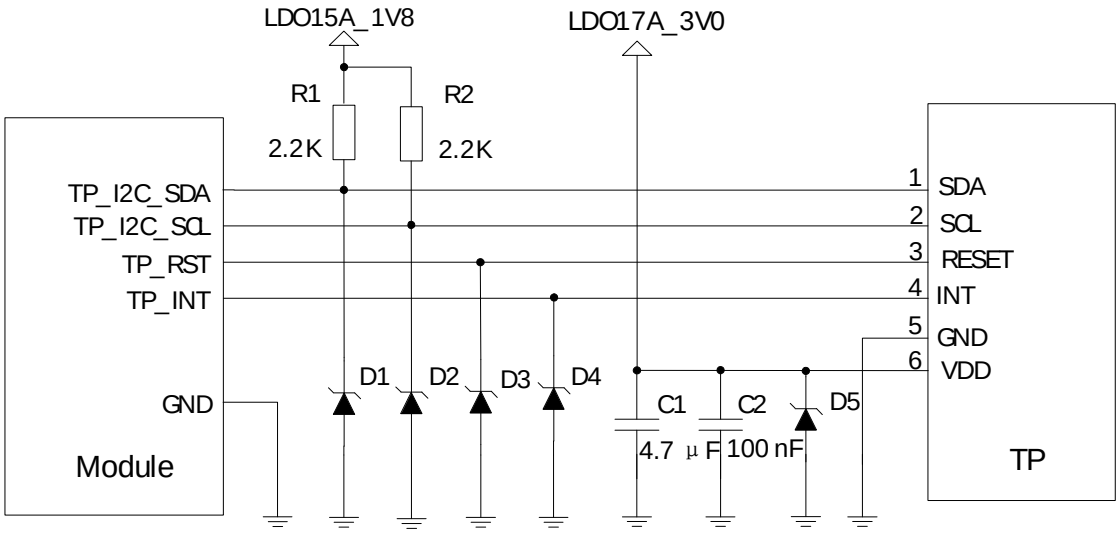
corresponding power supply and interrupt pins. The pin definition of TP interface is illustrated below.

Table 20: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	31	DO	TP reset	1.8 V voltage domain. Active low.
TP_INT	30	DI	TP interrupt	1.8 V voltage domain.
TP_I2C_SCL	47	OD	TP I2C clock	Need to be pulled up to 1.8 V externally. Can be used for other I2C devices.
TP_I2C_SDA	48	OD	TP I2C data	

A reference circuit for the TP interface is shown below.

Figure 19: Reference Circuit Design for the Touch Panel Interface



3.19. Camera Interfaces

Based on MIPI CSI standard, the module supports two cameras (4-lane + 4-lane) or three cameras (4-lane + 2-lane + 1-lane), and the maximum pixel of the camera can be up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor and camera lens specifications.

Table 21: Pin Definition of Camera Interfaces

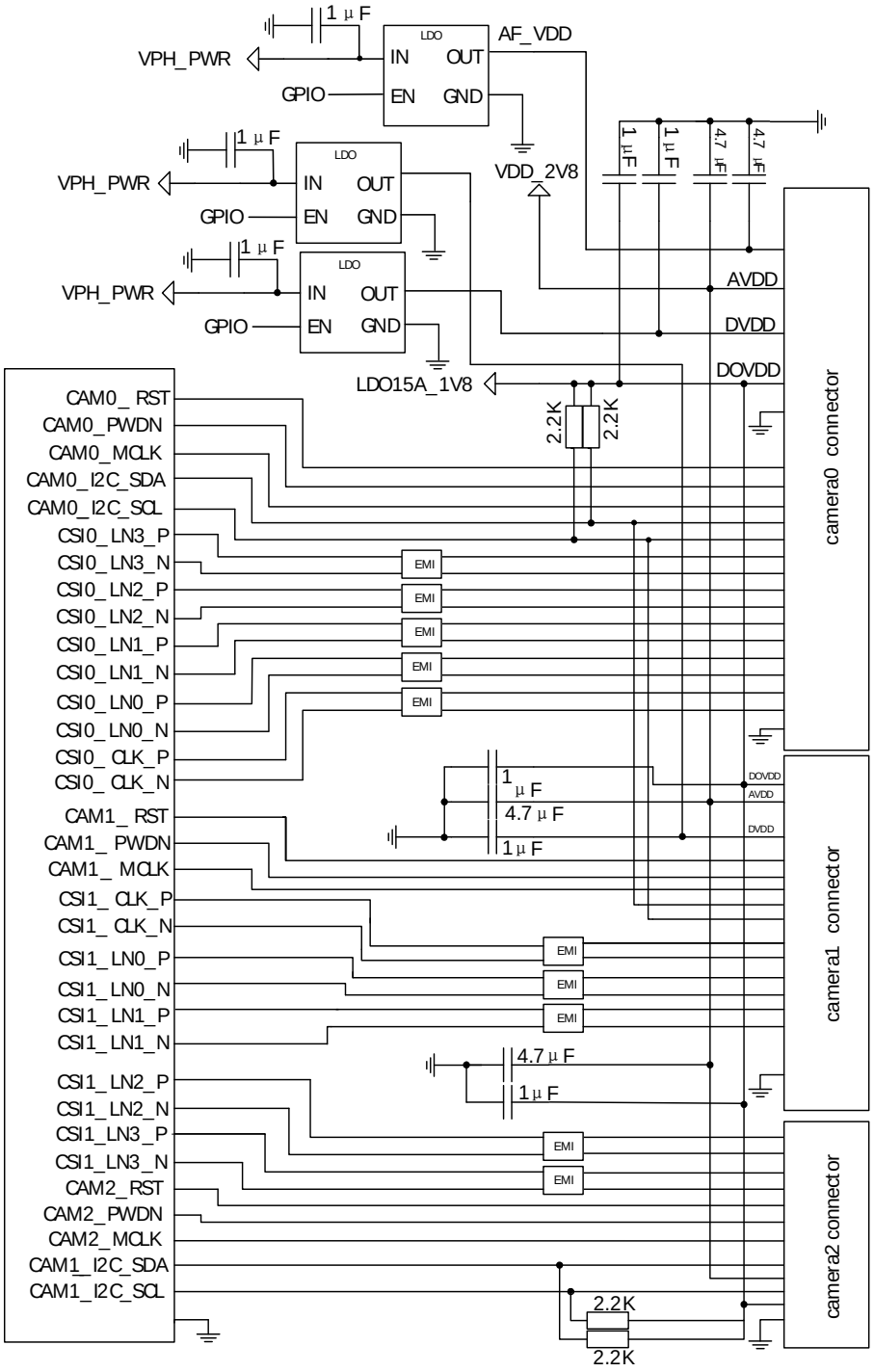
Pin Name	Pin No.	I/O	Description	Comment
CSI1_CLK_N	63	AI	MIPI CSI1 clock (-)	
CSI1_CLK_P	64	AI	MIPI CSI1 clock (+)	
CSI1_LN0_N	65	AI	MIPI CSI1 lane 0 data (-)	

CSI1_LN0_P	66	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN1_N	67	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN1_P	68	AI	MIPI CSI1 lane 1 data (+)	
CSI1_LN2_N	72	AI	MIPI CSI1 lane 2 data (-)	
CSI1_LN2_P	73	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN3_N	70	AI	MIPI CSI1 lane 3 data (-)	
CSI1_LN3_P	71	AI	MIPI CSI1 lane 3 data (+)	
CSI0_CLK_N	157	AI	MIPI CSI0 clock (-)	
CSI0_CLK_P	196	AI	MIPI CSI0 clock (+)	
CSI0_LN0_N	158	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN0_P	197	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN1_N	159	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN1_P	198	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN2_N	160	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN2_P	199	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN3_N	161	AI	MIPI CSI0 lane 3 data (-)	
CSI0_LN3_P	200	AI	MIPI CSI0 lane 3 data (+)	
CAM0_I2C_SCL	83	OD	I2C clock of camera 0	Need to be pulled up to 1.8 V externally. For I2C application, these pins can only be used for camera I2C and can not be connected to other I2C devices.
CAM0_I2C_SDA	84	OD	I2C data of camera 0	
CAM0_PWDN	80	DO	Power down of camera 0	1.8 V power domain.
CAM1_PWDN	82	DO	Power down of camera 1	
CAM2_PWDN	163	DO	Power down of camera 2	
CAM0_MCLK	74	DO	Master clock of camera 0	
CAM1_MCLK	75	DO	Master clock of camera 1	
CAM2_MCLK	165	DO	Master clock of camera 2	
CAM0_RST	79	DO	Reset of camera 0	
CAM1_RST	81	DO	Reset of camera 1	

CAM2_RST	164	DO	Reset of camera 2	
CAM1_I2C_SCL	166	OD	I2C clock of camera 1	Need to be pulled up to 1.8 V externally. For I2C application, these pins can only be used for camera I2C and can not be connected to other I2C devices.
CAM1_I2C_SDA	205	OD	I2C data of camera 1	

The following is a reference circuit design for 3-camera applications.

Figure 20: Reference Circuit Design for 3-Camera Applications



NOTE

In 3-camera applications, CSI1_LN3_P and CSI1_LN3_N are used as MIPI clock signals of camera 2. CSI1_LN2_P and CSI1_LN2_N are used as MIPI data signals of camera 2.

3.19.1. MIPI Design Considerations

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal tracs for DSI-supported maximum data rate of up to 1.5 Gbps and CSI-supported maximum data rate of up to 2.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, keep all the MIPI traces of the same length. To avoid crosstalk, keep a distance of 1.5 times the trace width among MIPI signal traces. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a low-capacitance TVS for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following rules:
  a) When the MIPI signal line rate is 1.5 Gbps/lane, the FPC trace length is 76.2 mm, and the insertion loss of the FPC cable is -0.9 dB, the PCB trace length should not exceed 135 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length difference within 0.7 mm;
  d) Control inter-lane length difference within 1.4 mm.

Table 22: MIPI Trace Length Inside the Module

Pin Name	Pin No.	Length (mm)	Length Difference (P - N)
DSI_CLK_N	52	38.53	-0.23
DSI_CLK_P	53	38.30	
DSI_LN0_N	54	38.59	-0.16
DSI_LN0_P	55	38.43	
DSI_LN1_N	56	38.22	0.25
DSI_LN1_P	57	38.47	
DSI_LN2_N	58	38.84	-0.28
DSI_LN2_P	59	38.56	
DSI_LN3_N	60	38.74	-0.26
DSI_LN3_P	61	38.48	
CSI1_CLK_N	63	18.87	-0.03
CSI1_CLK_P	64	18.84	
CSI1_LN0_N	65	19.42	-0.24
CSI1_LN0_P	66	19.18	
CSI1_LN1_N	67	19.02	0.26
CSI1_LN1_P	68	19.28	
CSI1_LN2_N	72	19.53	-0.3

CSI1_LN2_P	73	19.23		
CSI1_LN3_N	70	18.93	-0.11	
CSI1_LN3_P	71	18.82		
CSI0_CLK_N	157	20.94	-0.21	
CSI0_CLK_P	196	20.73		
CSI0_LN0_N	158	18.74	-0.34	
CSI0_LN0_P	197	18.40		
CSI0_LN1_N	159	17.18	0.19	
CSI0_LN1_P	198	17.37		
CSI0_LN2_N	160	8.28	-0.13	
CSI0_LN2_P	199	8.15		
CSI0_LN3_N	161	4.97	-0.27	
CSI0_LN3_P	200	4.70		

3.20. Sensor Interface

The module supports communication with sensors via I2C interfaces, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, and pressure sensor.

Table 23: Pin Definition of Sensor Interface

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	Need to be pulled up to 1.8 V externally. For I2C application, these pins can only be used for sensor I2C and can not be connected to other I2C devices. SENSOR_I2C only supports sensors of ADSP architecture.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	

3.21. Audio Interfaces

The module provides three analog input channels and three analog output channels. The following table

shows the pin definition.

Table 24: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS1	147	PO	Bias voltage 1 output for microphone	The rated output current is 3 mA. The default software setting output voltage is 1.8 V.
MIC1_P	4	AI	Microphone input for channel 1 (+)	
MIC1_M	5	AI	Microphone input for channel 1 (-)	
MIC2_P	6	AI	Microphone input for headset (+)	
MIC3_P	148	AI	Microphone input for channel 3 (+)	
MIC3_M	149	AI	Microphone input for channel 3 (-)	
MIC_BIAS3	155	PO	Bias voltage 3 output for microphone	The rated output current is 3 mA. The output voltage is fixed to 1.8 V and cannot be adjusted.
EAR_P	8	AO	Earpiece output (+)	
EAR_M	9	AO	Earpiece output (-)	
LINEOUT_P	10	AO	Audio line differential output (+)	The typical output voltage is 2 Vrms.
LINEOUT_M	11	AO	Audio line differential output (-)	
HPH_R	136	AO	Headphone right channel output	
HPH_GND	137	AO	Headphone reference ground	
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset hot-plug detect	High level by default.

- The module offers three audio input channels.
- The output voltage range of MIC_BIAS1 is programmable between 1.6 V and 2.85 V, and the maximum output current is 3 mA. MIC_BIAS3 supports 1.8 V pull-up output only and is not programmable.
- The earpiece interface uses differential output.
- The lineout interface uses differential output and lineout is used as audio PA input.
- The headphone interface features stereo left and right channel output, and supports headset insertion detection.

3.21.1. Reference Circuit Design for Microphone Interfaces

Figure 21: Reference Circuit Design for ECM Microphone Interface

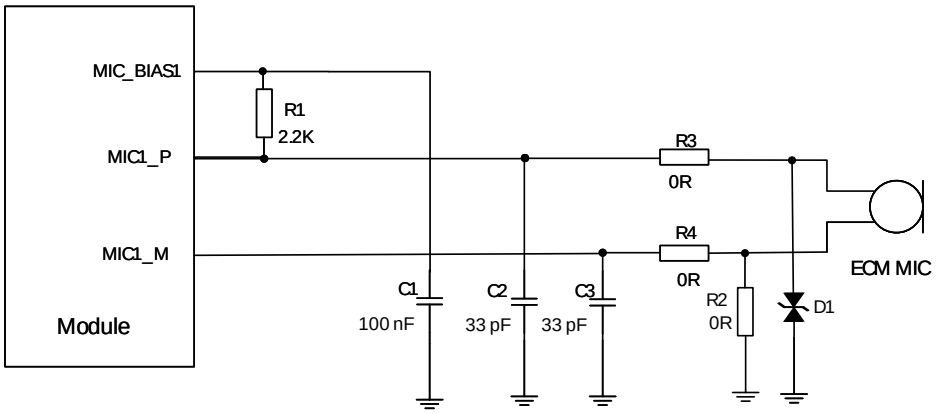
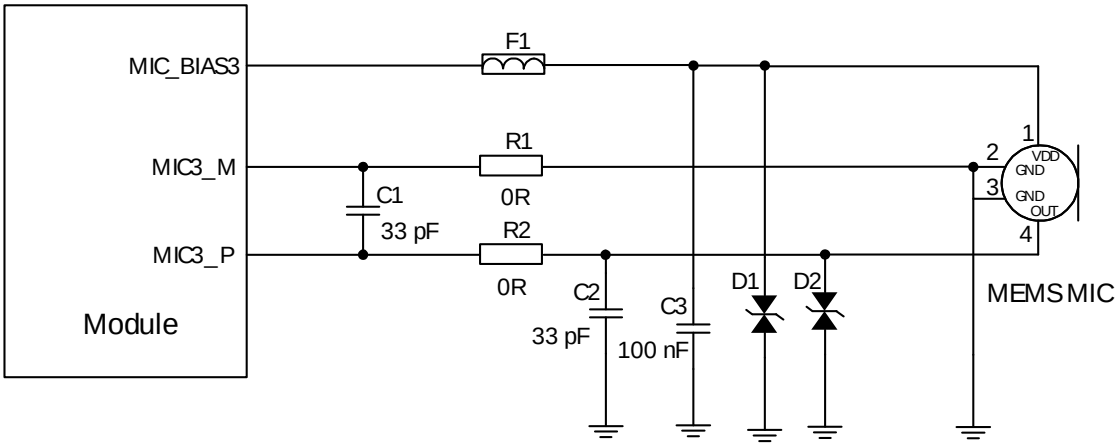
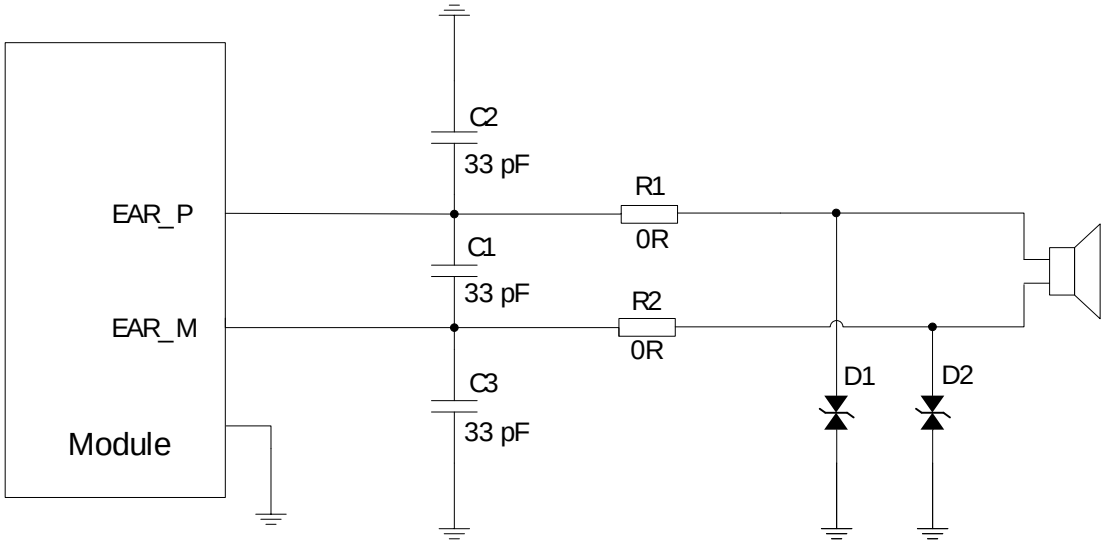


Figure 22: Reference Circuit Design for MEMS Microphone Interface



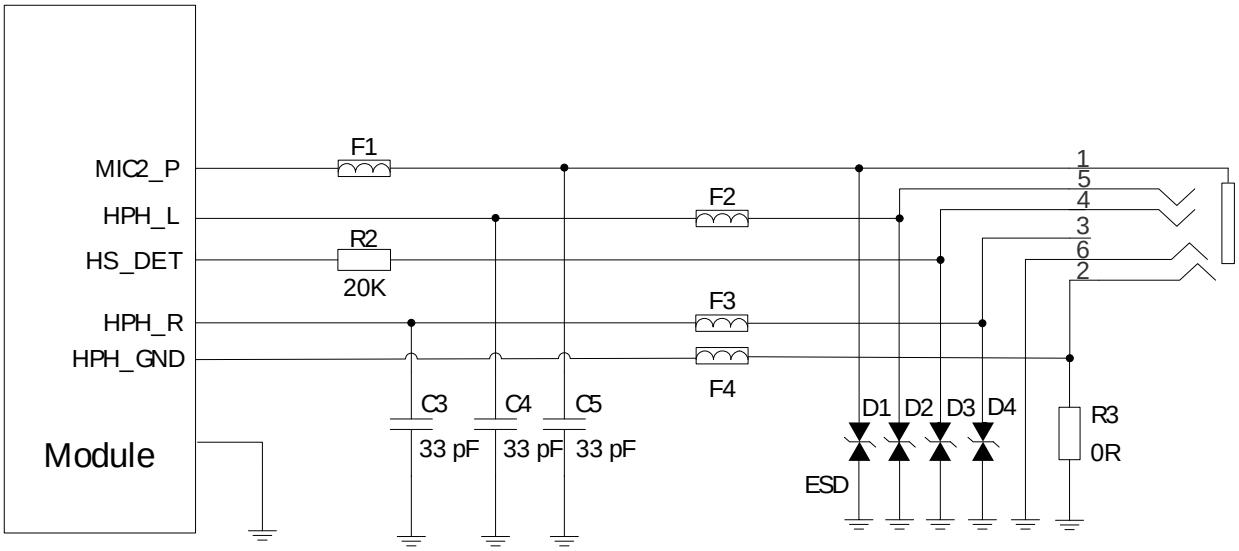
3.21.2. Reference Circuit Design for Earpiece Interface

Figure 23: Reference Circuit Design for Earpiece Interface



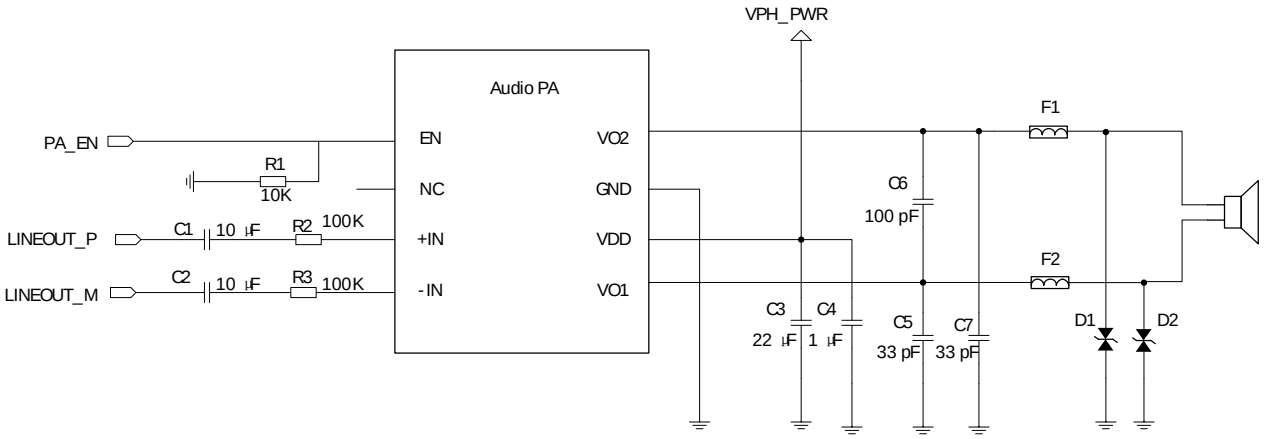
3.21.3. Reference Circuit Design for Headset Interface

Figure 24: Reference Circuit Design for Headset Interface



3.21.4. Reference Circuit Design for Lineout Interface

Figure 25: Reference Circuit Design for Lineout Interface



3.21.5. Audio Signal Design Considerations

It is recommended to use the ECM microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without these capacitors, TDD noise could be heard during voice calls. Note that the resonant frequency point of a capacitor largely depends on its material and manufacturing technique. Therefore, you should consult the capacitor vendors to choose the most suitable capacitor to filter out the high-frequency noises.

For models that support GSM, the severity degree of RF interference in the voice channel during GSM transmitting largely depends on the application design. Therefore, you should select a suitable capacitor according to the test results. Sometimes, even no RF filtering capacitor is required. The filter capacitors on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitors should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

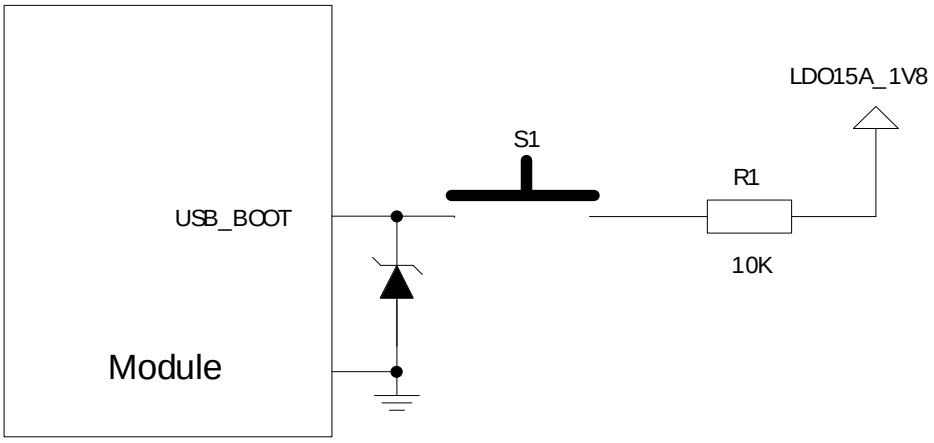
3.22. USB_BOOT Control Interface

USB_BOOT is a forced download interface. You can force the module to enter download mode by pulling it up to LDO15A_1V8 before turning on the module. This is a forced option when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Table 25: Pin Definition of USB_BOOT Control Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	46	DI	Force the module into download mode	Force the module to enter download mode by pulling this pin up to LDO15A_1V8 before turning on the module.

Figure 26: Reference Circuit Design for USB_BOOT Control Interface



4 Wi-Fi/Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance should be controlled to 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna, or ceramic antenna to the module via the interface to achieve Wi-Fi and Bluetooth functions. Bluetooth and WLAN (both 5 GHz and 2.4 GHz) are operating in TDD under coex mode.

4.1. Wi-Fi

The module supports 2.4 GHz and 5 GHz dual-band WLAN based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 150 Mbps in 2.4 GHz bands, and 433 Mbps in 5 GHz bands. The features are as below:

- Supports Wake-on-WLAN (WoWLAN)
- Supports ad hoc mode
- Supports WAPI SMS4 hardware encryption
- Supports AP and STA modes
- Supports Wi-Fi Direct
- Supports MCS 0–7 for HT20 and HT40
- Supports MCS 0–8 for VHT20
- Supports MCS 0–9 for VHT40 and VHT80

4.1.1. Wi-Fi Performance

The following tables list the Wi-Fi transmitting and receiving performance of the module.

Table 26: Wi-Fi Transmitting Performance

Frequency Bands	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	16.5 dBm ±3 dB
	802.11b	11 Mbps	16.5 dBm ±3 dB
	802.11g	6 Mbps	16.5 dBm ±3 dB
	802.11g	54 Mbps	14.5 dBm ±3 dB
	802.11n HT20	MCS0	15 dBm ±3 dB
	802.11n HT20	MCS7	14.5 dBm ±3 dB
	802.11n HT40	MCS0	15 dBm ±3 dB
	802.11n HT40	MCS7	13.5 dBm ±3 dB
5 GHz	802.11a	6 Mbps	15.5 dBm ±3 dB
	802.11a	54 Mbps	13 dBm ±3 dB
	802.11n HT20	MCS0	15.5 dBm ±3 dB

	802.11n HT20	MCS7	13 dBm ±3 dB
	802.11n HT40	MCS0	15.5 dBm ±3 dB
	802.11n HT40	MCS7	13 dBm ±3 dB
	802.11ac VHT20	MCS0	15.5 dBm ±3 dB
	802.11ac VHT20	MCS8	12.5 dBm ±3 dB
	802.11ac VHT40	MCS0	15 dBm ±3 dB
	802.11ac VHT40	MCS9	12 dBm ±3 dB
	802.11ac VHT80	MCS0	14.5 dBm ±3 dB
	802.11ac VHT80	MCS9	11 dBm ±3 dB

Table 27: Wi-Fi Receiving Performance

Frequency Bands	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-96 dBm
	802.11b	11 Mbps	-87 dBm
	802.11g	6 Mbps	-90 dBm
	802.11g	54 Mbps	-74 dBm
	802.11n HT20	MCS0	-88 dBm
	802.11n HT20	MCS7	-68 dBm
	802.11n HT40	MCS0	-85 dBm
	802.11n HT40	MCS7	-66 dBm
5 GHz	802.11a	6 Mbps	-89 dBm
	802.11a	54 Mbps	-72 dBm
	802.11n HT20	MCS0	-88 dBm
	802.11n HT20	MCS7	-68 dBm
	802.11n HT40	MCS0	-85 dBm
	802.11n HT40	MCS7	-66 dBm
	802.11ac VHT20	MCS0	-89 dBm
	802.11ac VHT20	MCS8	-66 dBm

802.11ac VHT40	MCS0	-85 dBm
802.11ac VHT40	MCS9	-61 dBm
802.11ac VHT80	MCS0	-82 dBm
802.11ac VHT80	MCS9	-58 dBm

Reference specifications are listed below:

- *IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
- *IEEE Std 802.11a*, *IEEE Std 802.11b*, *IEEE Std 802.11g: IEEE 802.11-2007 WLAN MAC and PHY, June 2007*

4.2. Bluetooth

The module supports Bluetooth 5.0 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally supports up to 7 wireless connections.
- Maximally supports up to 3.5 Piconets simultaneously.
- Supports one SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 28: Bluetooth Data Rate and Version

Version	Data Rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0 + EDR	3 Mbit/s	> 80 kbit/s
3.0 + HS	24 Mbit/s	Reference 3.0 + HS
4.0	24 Mbit/s	Reference 4.0 LE
5.0	24 Mbit/s	Reference 5.0 LE

Reference specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

4.2.1. Bluetooth Performance

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 29: Bluetooth Transmitting and Receiving Performance

Transmitting Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	7 dBm ±3 dB	6.5 dBm ±3 dB	6.5 dBm ±3 dB
Receiving Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-93 dBm	-90 dBm	-85 dBm

5 GNSS (Optional)

The module integrates an IZat™ GNSS engine (GEN 8C) which supports multiple positioning and navigation systems including GPS, GLONASS, Galileo, BDS, QZSS, SBAS. With an embedded LNA, the positioning accuracy of the module has been significantly improved.

5.1. GNSS Performance

The following table lists the GNSS performance of the module in conduction mode.

Table 30: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity	Acquisition	-147	dBm
	Reacquisition	-159	dBm
	Tracking	-159	dBm
TTFF	Cold start	31.2	s
	Warm start	24.7	s
	Hot start	1.32	s
Accuracy	CEP-50	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2. Reference Design

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. To avoid this, follow the reference design rules as below:

- Maximize the distance between GNSS RF part and the other RF part (including trace routing and antenna layout) to avoid mutual interference.

- In user systems, place GNSS RF signal traces and RF components far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with harsh electromagnetic environment or high ESD protection requirements, it is recommended to add ESD protection components for the antenna interface. The junction capacitance of the components should be less than 0.5 pF. Otherwise, it will influence the impedance characteristic of RF circuit loop, or cause attenuation of bypass RF signals.
- Control the impedance of feeder lines and PCB traces to 50 Ω, and keep the trace length as short as possible.
- See ***Chapter 6.3*** for reference circuit designs of GNSS antenna.

6 Antenna Interfaces

SUE200-LD and SUE209-LD provide four antenna interfaces for the main, Rx-diversity, Wi-Fi/Bluetooth, and GNSS antennas respectively. The impedance of the antenna ports should be controlled to 50 Ω.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

6.1. Main Antenna and Rx-diversity Antenna Interfaces

Table 31: Pin Definition of Main and Rx-diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	AIO	Main antenna interface	50 Ω impedance
ANT_DRX	131	AI	Diversity antenna interface	

6.1.1. Operating Frequency

The operating frequencies of the modules are listed in the following tables.

Table 32: SUE200-LD & SUE209-LD Operating Frequency

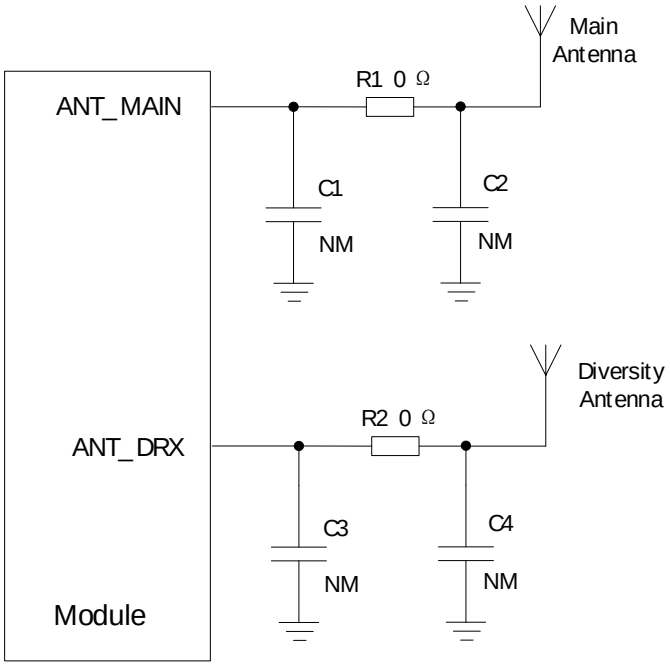
Operating Frequency	Receive	Transmit	Unit
LTE-FDD B2	1930–1990	1850–1910	MHz
LTE-FDD B4	2110–2155	1710–1755	MHz
LTE-FDD B5	869–894	824–849	MHz
LTE-FDD B7	2620–2690	2500–2570	MHz
LTE-FDD B12	729–746	699–716	MHz
LTE-FDD B13	746–756	777–787	MHz
LTE-FDD B14	758–768	788–798	MHz
LTE-FDD B17	734–746	704–716	MHz
LTE-FDD B25	1930–1995	1850–1915	MHz
LTE-FDD B26	859–894	814–849	MHz

LTE-FDD B66	2110–2180	1710–1780	MHz
LTE-FDD B71	617–652	663–698	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz

6.1.2. Reference Design

A reference circuit design for the main and Rx-diversity antenna interfaces is shown below. Reserve a π-type matching circuit for each antenna to achieve better RF performance, and place the π-type matching components (R1/C1/C2 and R2/C3/C4) as close to the antennas as possible. The capacitors are not mounted by default and the resistors are 0 Ω.

Figure 27: Reference Circuit Design for Main and Rx-diversity Antenna Interfaces



6.2. Wi-Fi/Bluetooth Antenna Interface

The following tables show the pin definition and frequency specification of the Wi-Fi/Bluetooth antenna interface.

Table 33: Pin Definition of Wi-Fi/Bluetooth Antenna Interface

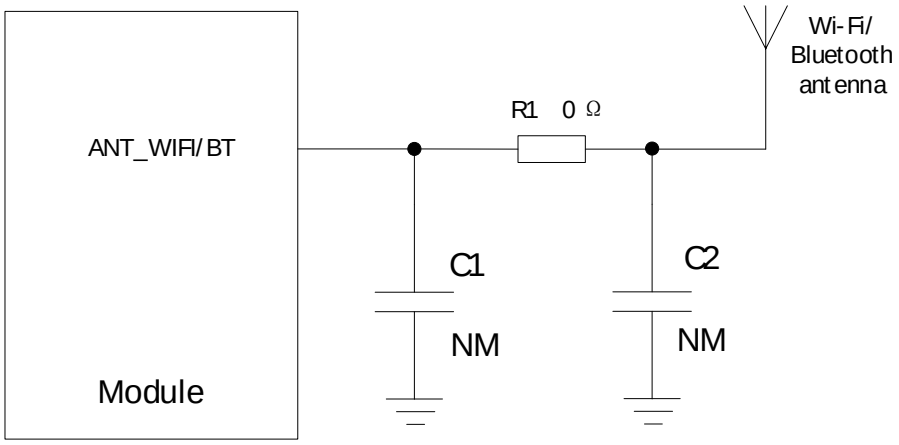
Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance

Table 34: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi (2.4 GHz)	2402–2482	MHz
Wi-Fi (5 GHz)	5180–5825	MHz
Bluetooth 5.0	2402–2480	MHz

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default and the resistor is 0 Ω.

Figure 28: Reference Circuit Design for Wi-Fi/Bluetooth Antenna



6.3. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 35: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	121	AI	GNSS antenna interface	50 Ω impedance

Table 36: GNSS Frequency

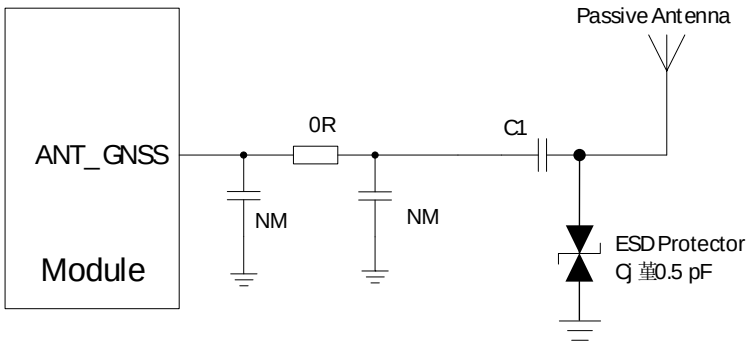
GNSS Constellation Type	Frequency	Unit
GPS L1	1575.42 ±1.023	MHz
GLONASS L1	1597.5–1605.8	MHz

BDS B1I	1561.098 ±2.046	MHz
Galileo E1	1575.42 ±2.046	MHz
QZSS L1	1575.42 ±1.023	MHz
SBAS L1	1575.42 ±1.023	MHz

6.3.1. Reference Circuit Design for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

Figure 29: Reference Circuit Design for Passive Antenna



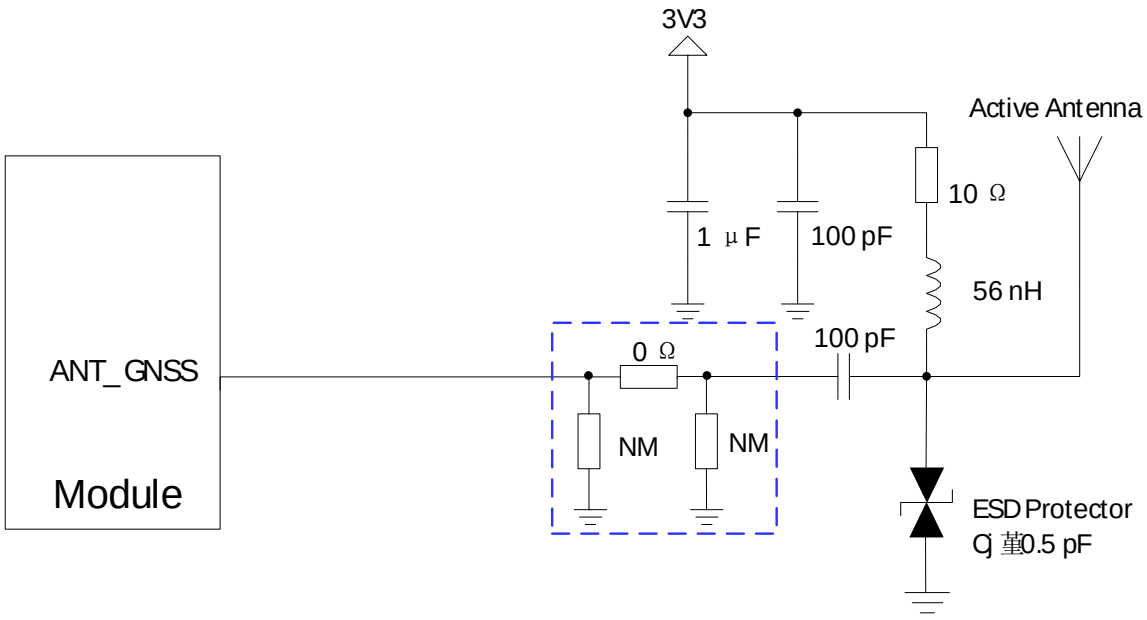
NOTE

It is not recommended to add an external LNA when using a passive antenna.

6.3.2. Reference Circuit Design for Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Despite its low power consumption, the active antenna still requires stable and clean power supplies. Therefore, it is recommended to use high-performance LDO as the power supply. A reference design for active antenna is shown below.

Figure 30: Reference Circuit Design for Active Antenna



NOTE

It is recommended to use a passive antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 31: Microstrip Design on a 2-layer PCB

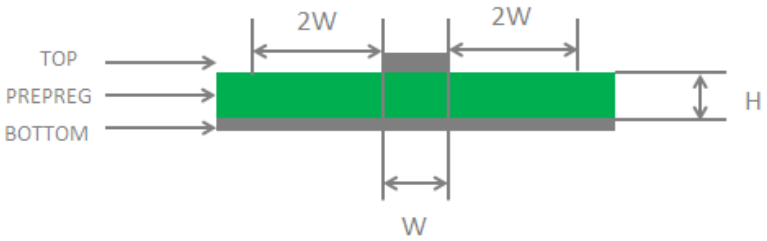


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

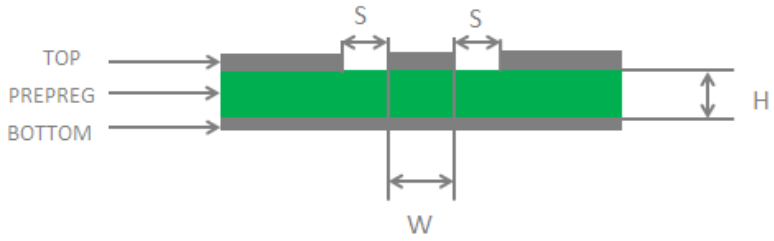


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

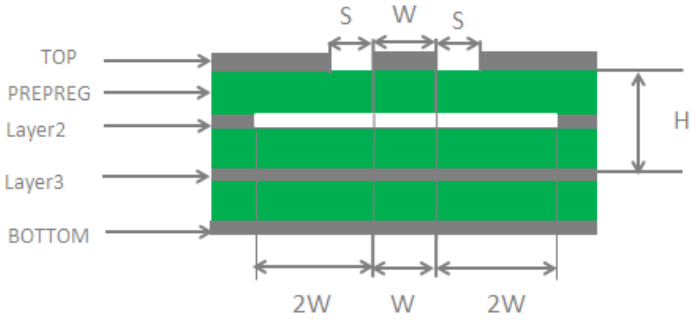
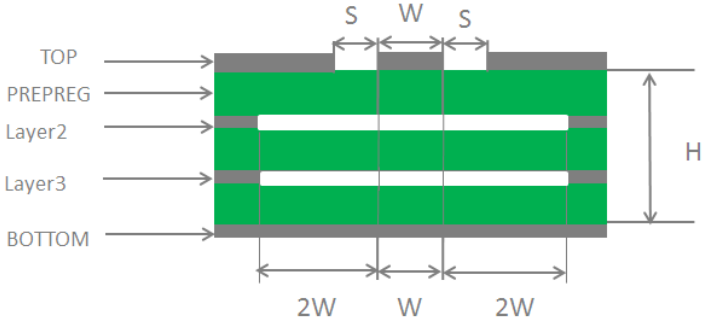


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between

traces on adjacent layers.

For more details about RF layout, see ***document 2***.

6.5. Antenna Installation

6.5.1. Antenna Design Requirements

The following table shows the requirements for the main antenna, Rx-diversity antenna, Wi-Fi/Bluetooth antenna, and GNSS antenna.

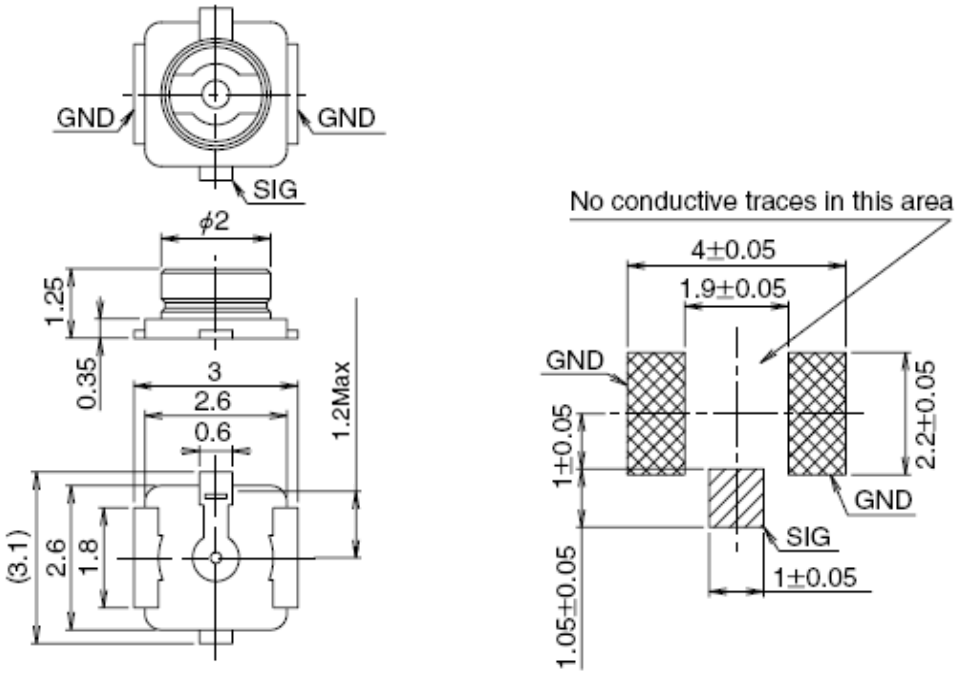
Table 37: Antenna Requirements

Type	Requirements
Cellular	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
Wi-Fi/Bluetooth	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical ● Cable Insertion Loss: < 1 dB
GNSS	● Frequency range: L1: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: Active antenna noise figure: < 1.5 dB (Typ.) Active antenna embedded LNA gain: < 17 dB (Typ.)

6.5.2. RF Connector Recommendation

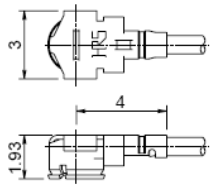
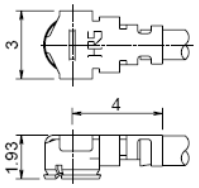
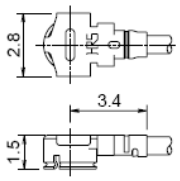
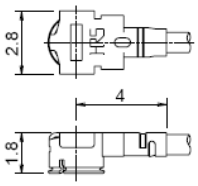
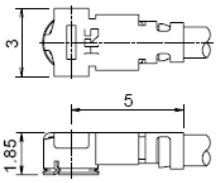
If you use an RF connector for antenna connection, it is recommended to use the U.FL-R-SMT receptacle provided by Hirose.

Figure 35: Dimensions of the Receptacle (Unit: mm)



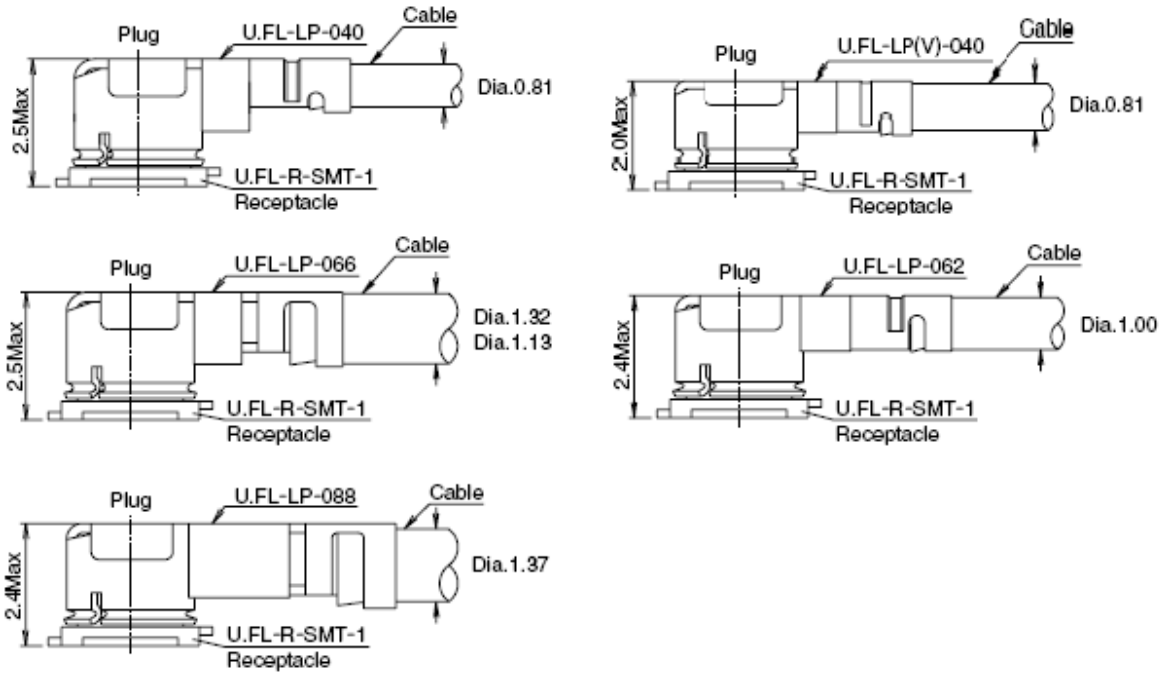
U.FL-LP series mated plugs listed in the following figure can be used to match U.FL-R-SMT.

Figure 36: Specifications of Mated Plugs

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated connectors.

Figure 37: Space Factor of Mated Connectors (Unit: mm)



For more details, visit http://www.hirose.com.

7 Electrical Characteristics and Reliability

7.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 38: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6	V
USB_VBUS	-0.5	16	V
Peak Current of VBAT	-	3	A
Voltage at Digital Pins	-0.3	2.16	V

7.2. Power Supply Ratings

Table 39: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must be kept between the minimum and maximum values	3.55	3.8	4.4	V
	Voltage drop during transmitting burst	At maximum power control level	-	-	400	mV
IVBAT	Peak supply current	At maximum power control level	-	1.8	3.0	A
USB_VBUS	Charging power input	-	4.0	5.0	6.0	V
VRTC	Power supply voltage of the backup battery	-	2.5	3.0	3.2	V

7.3. Digital I/O Characteristics

Table 40: 1.8 V Digital I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.17	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.63	V
V_{OH}	High-level output voltage	1.35	1.8	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 41: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.75	1.85	V
V_{IH}	High-level input voltage	1.26	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.36	V
V_{OH}	High-level output voltage	1.44	1.8	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 42: (U)SIM 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.8	3.1	V
V_{IH}	High-level input voltage	2.065	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.59	V
V_{OH}	High-level output voltage	2.36	2.95	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 43: SD Card 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.27	2	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	-	V

V_{OL}	Low-level output voltage	-	0.45	V

Table 44: SD Card 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.84	3.25	V
V_{IL}	Low-level input voltage	-0.3	0.74	V
V_{OH}	High-level output voltage	2.21	2.95	V
V_{OL}	Low-level output voltage	0	0.37	V

7.4. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 45: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating temperature range [4]	-35	+25	+75	ºC
Storage Temperature Range	-40	-	+90	ºC

7.5. Power Consumption

The values of current consumption are shown below.

Table 46: SUE200-LD & SUE209-LD Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power off	36	μA
LTE-FDD supply current	Sleep state (USB disconnected) @ DRX = 6	6.25	mA

[4] Within operating temperature range, the module meets 3GPP specifications.

	Sleep state (USB disconnected) @ DRX = 7	4.85	mA
	Sleep state (USB disconnected) @ DRX = 8	4.19	mA
	Sleep state (USB disconnected) @ DRX = 9	3.96	mA
LTE-TDD supply current	Sleep state (USB disconnected) @ DRX = 6	6.34	mA
	Sleep state (USB disconnected) @ DRX = 7	5.07	mA
	Sleep state (USB disconnected) @ DRX = 8	4.33	mA
	Sleep state (USB disconnected) @ DRX = 9	4.04	mA
LTE data transmission	LTE-FDD B2 @ max power	671	mA
	LTE-FDD B4 @ max power	649	mA
	LTE-FDD B5 @ max power	670	mA
	LTE-FDD B7 @ max power	822	mA
	LTE-FDD B12 @ max power	722	mA
	LTE-FDD B13 @ max power	742	mA
	LTE-FDD B14 @ max power	639	mA
	LTE-FDD B17@ max power	705	mA
	LTE-FDD B25 @ max power	707	mA
	LTE-FDD B26 @ max power	660	mA
	LTE-FDD B66 @ max power	673	mA
	LTE-FDD B71 @ max power	634	mA
	LTE-TDD B41 @ max power	423	mA

7.6. Tx Power

The following tables show the RF output power of the module.

Table 47: SUE200-LD & SUE209-LD RF Tx Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
LTE	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to 3GPP TS 51.010-1 subclause 13.16.

7.7. Rx Sensitivity

The following table shows the RF receiving sensitivity of the module.

Table 48: SUE200-LD & SUE209-LD RF Rx Sensitivity (Unit: dBm)

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	-97.0	-98.5	-101.0	-94.3
LTE-FDD B4 (10 MHz)	-97.0	-98.0	-100.5	-96.3
LTE-FDD B5 (10 MHz)	-99.0	-98.5	-102.0	-94.3
LTE-FDD B7 (10 MHz)	-96.0	-98.0	-100.0	-94.3
LTE-FDD B12 (10 MHz)	-98.5	-98.0	-101.5	-93.3
LTE-FDD B13 (10 MHz)	-98.0	-99.0	-101.5	-93.3
LTE-FDD B14 (10 MHz)	-97.5	-98.5	-101.0	-93.3
LTE-FDD B17 (10 MHz)	-97.0	-99.0	-101.0	-93.3
LTE-FDD B25 (10 MHz)	-97.0	-98.5	-101.0	-92.8
LTE-FDD B26 (10 MHz)	-98.5	-99.5	-102.0	-93.8
LTE-FDD B66 (10 MHz)	-97.0	-97.5	-100.5	-95.8
LTE-FDD B71 (10 MHz)	-99.0	-100.5	-103.0	-93.5
LTE-TDD B41 (10 MHz)	-96.5	-96.5	-99.5	-94.3

7.8. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatic discharge characteristics of the module.

Table 49: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

8 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

8.1. Mechanical Dimensions

Figure 38: Module Top and Side Dimensions

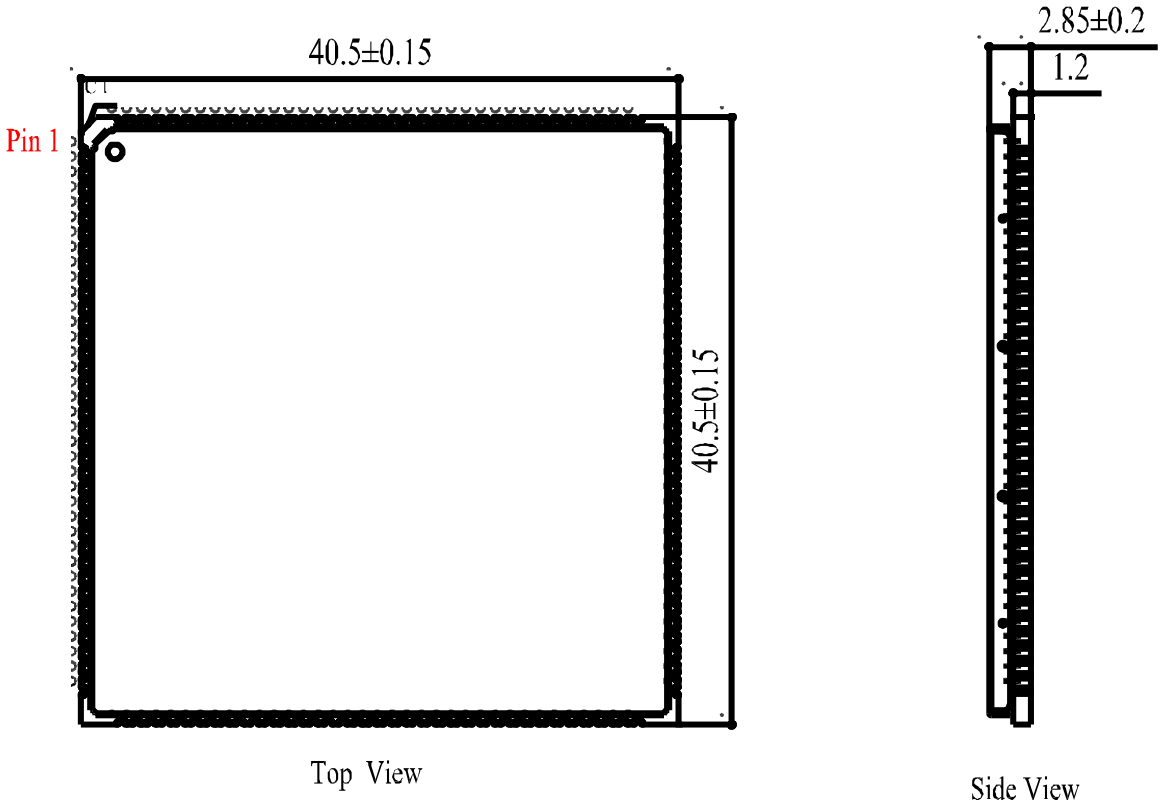
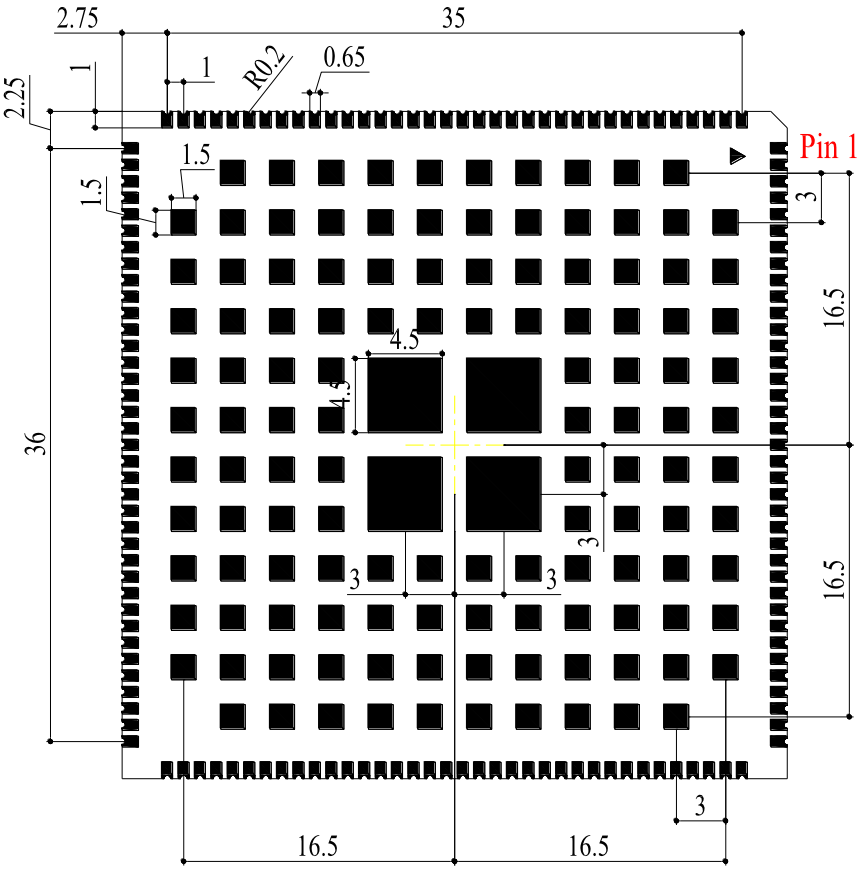


Figure 39: Module Bottom Dimensions (Bottom View)

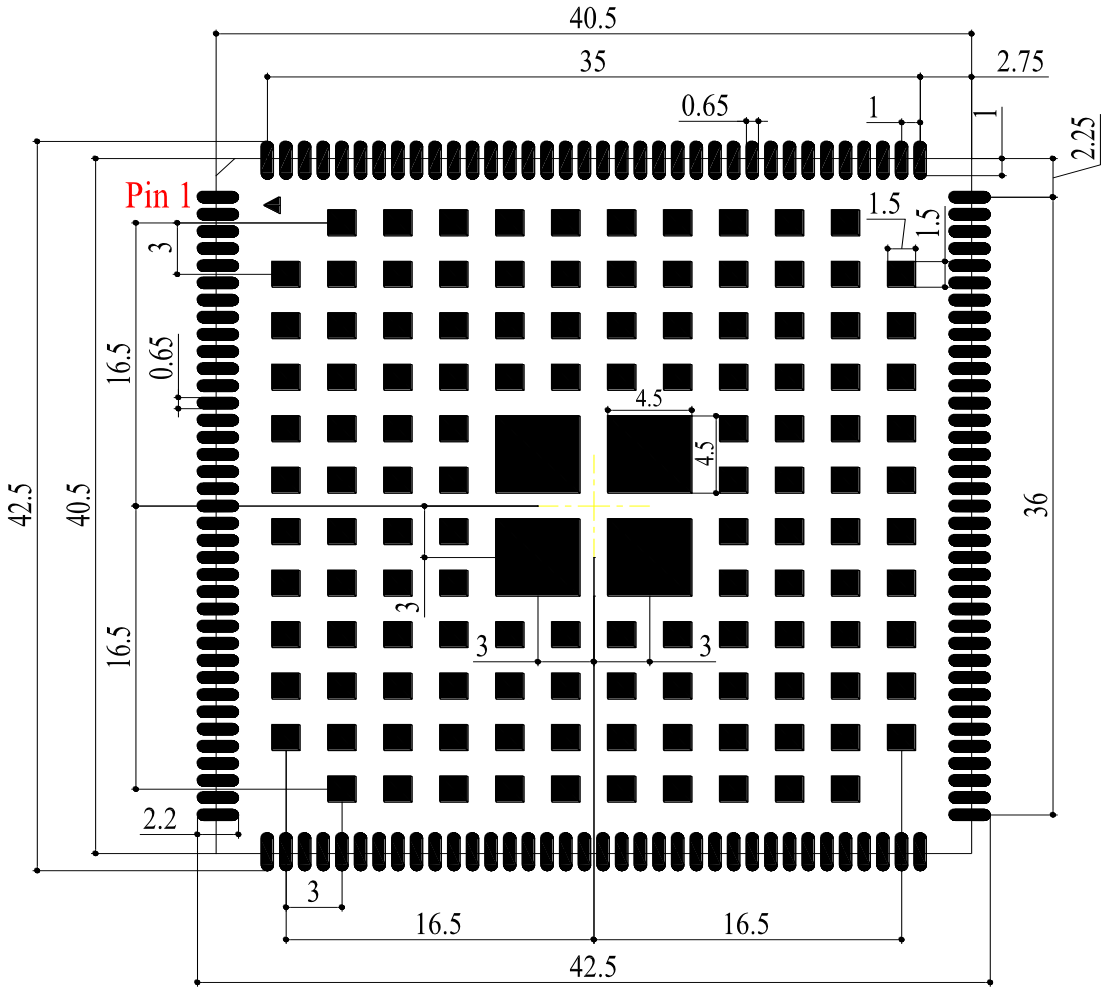


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

8.2. Recommended Footprint

Figure 40: Recommended Footprint



NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

8.3. Top and Bottom Views

Figure 41: Top and Bottom Views of SUE200-LD

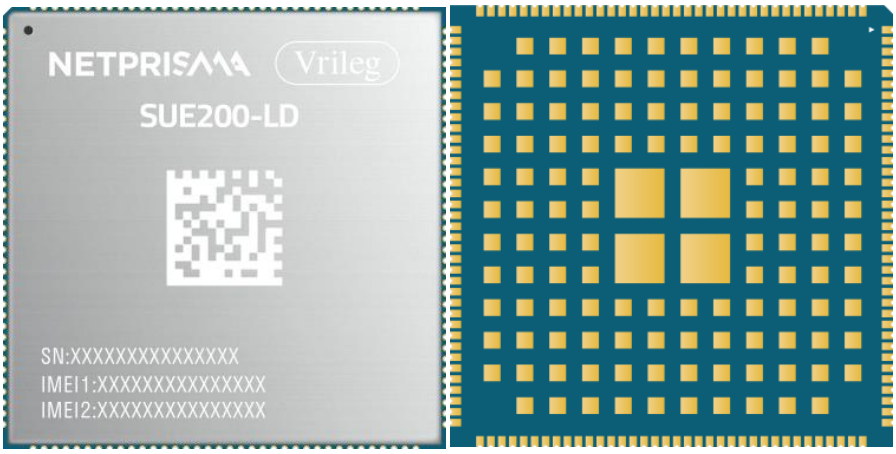
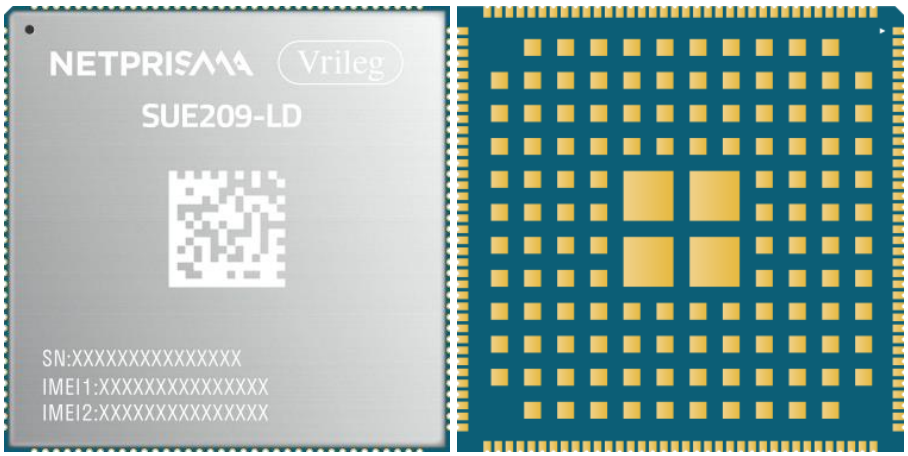


Figure 42: Top and Bottom Views of SUE209-LD



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Netprisma.

9 Storage, Manufacturing & Packaging

9.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours[5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see IPC/JEDEC J-STD-033 for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

9.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document 3***.

[5] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. Do not unpack the modules in large quantities until they are ready for soldering.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 43: Recommended Reflow Soldering Thermal Profile

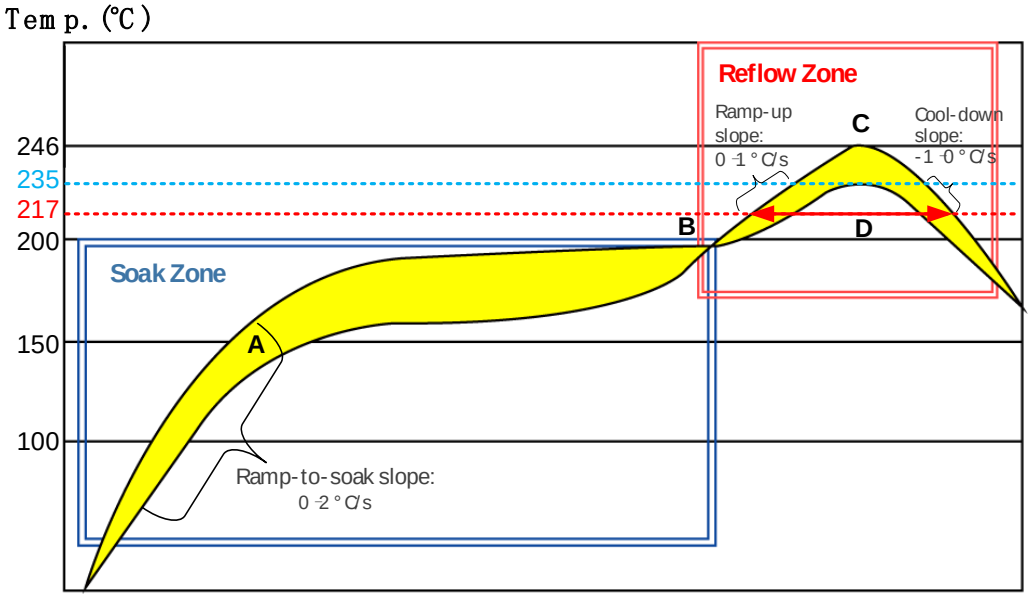


Table 50: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, to avoid excessive temperature change, which may cause excessive thermal deformation of the metal shielding frame and cover, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste. If possible, please choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. ide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact Netprisma Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document 4***.

9.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

9.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 44: Carrier Tape Dimension Drawing (Unit: mm)

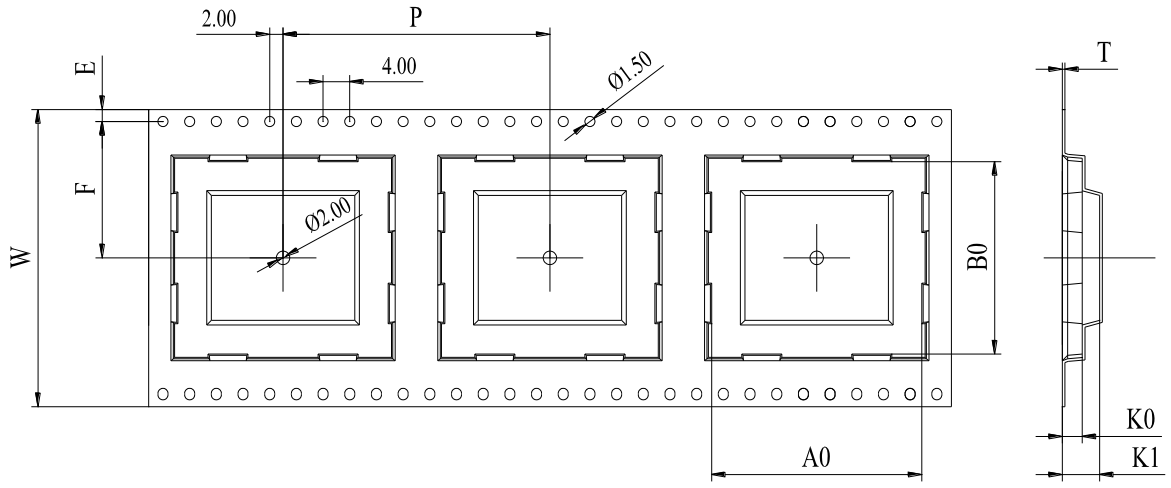


Table 51: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	41.2	41.2	4	4.6	34.2	1.75

9.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 45: Plastic Reel Dimension Drawing

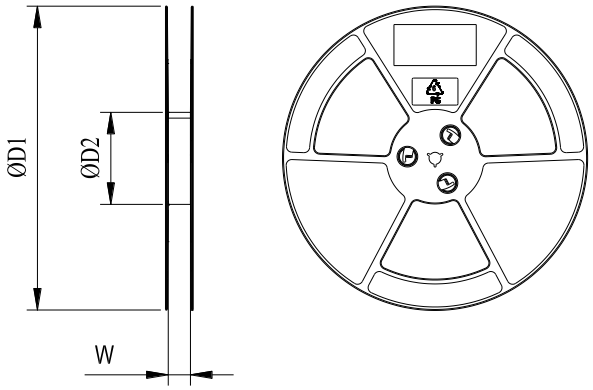
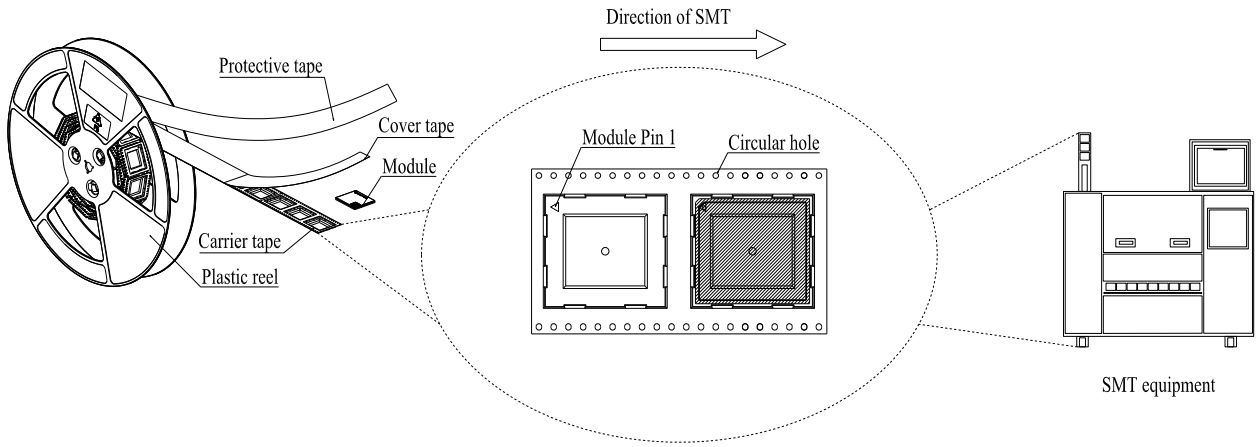


Table 52: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

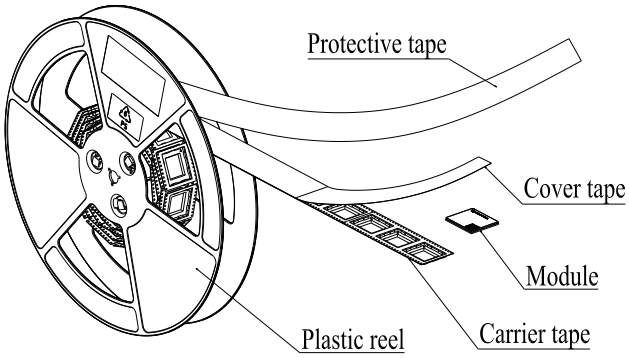
9.3.3. Mounting Direction

Figure 46: Mounting Direction



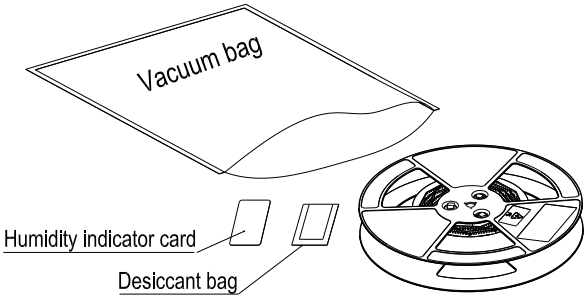
9.3.4. Packaging Process

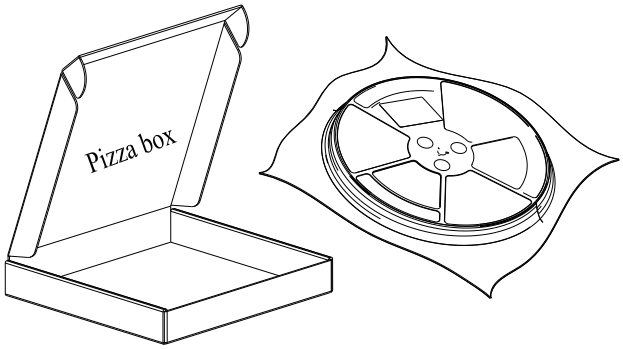
Figure 47: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

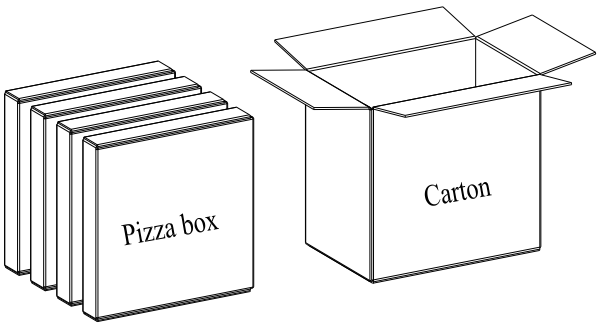
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.



10 Appendix References

Table 53: Related Documents

Document Name
1. Netprisma-SUE200-LD&SUE209-LD-GPIO-Configuration
2. Netprisma-RF-Layout-Application-Note
3. Netprisma-Module-Stencil-Design-Requirements
4. Netprisma-Module-SMT-Application-Note

Table 54: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
ADSP	Audio Digital Signal Processor
ALS	Ambient Light Sensor
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
AP	Access Point/Application Processor
ARM	Advanced RISC Machine
BDS	BeiDou Navigation Satellite System
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
CDMA	Code Division Multiple Access
CEP	Circular Error Probable
Cj	Junction Capacitance
CPE	Customer-Premise Equipment

CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear to Send
DC	Dual Carrier
DC-HSPA+	Dual Carrier High Speed Packet Access Plus
DCS	Digital Cellular System
DL	Downlink
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
DRX	Discontinuous Reception
DSI	Display Serial Interface
DSP	Digital Signal Processor
ECM	Electret Condenser Microphone
EDGE	Enhanced Data Rate for GSM Evolution
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM
eMMC	Embedded Multimedia Card
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
EVDO	Evolution-Data Optimized
EVRC	Enhanced Variable Rate Codec
FDD	Frequency Division Duplex
fps	Frame per Second

FR	Full Rate
Galileo	Galileo Satellite Navigation System (EU)
GFSK	Gaussian Frequency Shift Keying
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GRFC	Generic RF control
GSM	Global System for Mobile Communications
HR	Half Rate
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSPA+	High-Speed Packet Access+
HSUPA	High Speed Uplink Packet Access
HT	High Throughput
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IMT-2000	International Mobile Telecommunications for the year 2000
I/O	Input/Output
IImax	Maximum Input Load Current
IOmax	Maximum Output Load Current
ISP	Image Signal Processor/Internet Service Provider
LCC	Leadless Chip Carrier

LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LE	Low Energy
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low-Power Double Data Rate
LTE	Long-Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MEMS	Micro-Electro-Mechanical System
MIC	Microphone
MIMO	Multi-Input Multi-Output / Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSL	Moisture Sensitivity Levels
MT	Mobile Terminating/Terminated
NFC	Near Field Communication
NTC	Negative Temperature Coefficient
OTA	Over-the-Air Upgrade
OTG	On-The-Go
OTP	One Time Programable
PAM	Power Amplifier Module
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level

PCS	Personal Communication Service
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMU	Power Management Unit
POS	Point of Sale
PWM	Pulse Width Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SCO	Synchronous Connection Oriented
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mounting Device
SMS	Short Message Service
SMT	Surface Mount Technology
STA	Station
TDD	Time-Division Duplex
TP	Touch Panel
TTFF	Time to First Fix

TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
VHT	Very High Throughput
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
VImax	Absolute Maximum Input Voltage
VImin	Absolute Minimum Input Voltage
VIHmin	Minimum High-level Input Voltage
VILmax	Maximum Low-level Input Voltage
VOmax	Maximum Output Voltage
VOHmin	Minimum High-level Output Voltage
VOLmax	Maximum Low-level Output Voltage
Vrms	Root Mean Square Voltage
VSWR	Voltage Standing Wave Ratio
WAPI	WLAN Authentication and Privacy Infrastructure
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network

FCC ID: 2BEY3SUE200LDA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA INC. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

“Contains FCC ID: 2BEY3SUE200LDA”

“Contains IC: 32052-SUE200LDA”

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used

on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Band	Antenna Type	Max Gain Allowed (dBi)
LTE B2	External	8.00
LTE B4		5.00
LTE B5		13.41
LTE B7		8.00
LTE B12		11.92
LTE B13		11.92
LTE B14		11.92
LTE B17		11.92
LTE B25		8.00
LTE B26		13.36
LTE B41		8.00
LTE B66		5.00
LTE B71		11.92
Bluetooth		0.47
WiFi 2.4G		0.47
WiFi 5150-5250MHz		-0.67
WiFi 5250-5350MHz		-0.19
WiFi 5470-5725MHz		1.28
WiFi 5725-5850MHz		1.1

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 15 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IC: 32052-SUE200LDA

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

	Antenna Type	Max Gain Allowed (dBi)
Bluetooth	External	0.47
WiFi 2.4G		0.47
WiFi 5150-5250MHz		-0.67
WiFi 5250-5350MHz		-0.19
WiFi 5470-5725MHz		1.28
WiFi 5725-5850MHz		1.1

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.
Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 32052-SUE200LDA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 32052-SUE200LDA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon

d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Document History

Revision	Date	Changes
A	2025-02-21	The first revision.

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