SUC200-LD

Hardware Design

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1 Introduction

The document mainly introduces SUC200-LD and its hardware interfaces and air interfaces connected to your applications, which can help you quickly understand the hardware interface characteristics, RF characteristics, electrical characteristics, mechanical specifications and other relevant information of the module.

1.1. Text Conventions

Table 1: Text Conventions

NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

SUC200-LD is an industrial-grade 4G smart module, supporting Android operating system. It is an SMD module with compact packaging and it supports built-in high performance AdrenoTM 610 graphics processing unit (GPU), multiple audio and video codecs, and multiple audio and video input/output interfaces as well as abundant GPIOs.

Table 2: Basic Information

SUC200-LD	
Packaging type	LCC + LGA
Pin counts	278 pins
Dimensions	(40.5 ±0.15) mm × (40.5 ±0.15) mm × (2.85 ±0.2) mm
Weight	Approx. 10.16 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Function	SUC200-LD
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/B71
LTE-TDD	B41 (200M)
GNSS (optional)	GPS/GLONASS/BDS/Galileo/QZSS/SBAS
Wi-Fi 802.11a/b/g/n/ac	2.4 GHz; 5 GHz, 802.11a/b/g/n/ac
Bluetooth	Bluetooth 5.0 (BR/EDR + BLE)

2.2. Key Features

Table 4: Key Features

Categories	Description
Application Processor	● 8-core 64-bit ARM Kryo™ 260 CPU ● Kryo Gold: high performance quad-core @ 2.1 GHz with 1 MB L2 cache ● Kryo Silver: low power consumption quad-core @ 2.0 GHz with 512 KB L2 cache

DSP	Hexagon DSP, supporting Dual-HVX 512 MHz
GPU	Internal integrated with 64-bit Adreno™ 610 @ 1050 MHz 3D accelerated high-performance GPU
Memory	**eMMC + LPDDR4X:** ● 64 GB eMMC + 4 GB LPDDR4X (default)
Operating System	Android 13
Supply Voltage	● 3.55–4.4 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: module by default
USB Interface	● Complies with USB 3.1 Gen 1 and USB 2.0 specifications ● Data rate: up to 5 Gbps on USB 3.1 Gen 1 and 480 Mbps on USB 2.0 ● Support: USB OTG, USB Type-C and USB Hub expansion ● Use: AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB
(U)SIM Interfaces	● 2 groups of (U)SIM interfaces ● Support USIM/SIM card: 1.8 V and 2.95 V ● Support Dual SIM Dual Standby (supported by software by default)
SD Card Interface	● Compliant with SD 3.0 specification ● Supports 1.8/2.95 V SD card ● Supports SD card hot-plug
UART Interfaces [1]	● Support up to 5 groups of UART interfaces. 3 of them are configured by default, and 2 of them are multiplexed from other interfaces: – Debug UART: 2-wire UART, used for debugging only – UART0: 4-wire UART with the speed rate up to 4 Mbps, which supports RTS and CTS hardware flow control – UART1: 2-wire UART ● Other 2 groups of UART interfaces are multiplexed from other interfaces
SPI [1]	● Supports up to 5 groups of SPI, which are multiplexed from other interfaces ● Supports master mode only
I2C Interfaces [1]	● Support up to 8 groups of I2C interfaces: – 3 groups of dedicated I2C interfaces, used for camera and sensors – 1 group of TP I2C interface, used for touch panel or other peripherals ● 4 groups of I2C interfaces are multiplexed from other interfaces
I2S Interfaces [1]	Support up to 2 groups of I2S interfaces, which are multiplexed from other interfaces
Audio Interfaces	**Audio inputs:** 3 groups of analog microphone inputs, integrated with internal bias voltage in MIC2 **Audio outputs:** ● Class AB stereo headphone output ● Class AB earpiece differential output ● Class AB loudspeaker differential amplifier output, and an external power amplifier is required
Audio Codec	● EVS, EVRC, EVRC-B, EVRC-WB ● G.711, G.729A/ AB ● GSM-FR, GSM-EFR, GSM-HR ● AMR-NB, AMR-WB
ADC Interfaces	● 2 generic ADC interfaces ● Resolution: up to 15 bits
LCM Interface	● Supports 1 group of 4-lane MIPI_DSI with data rate up to 1.5 Gbps/lane ● Supports FHD + (1080 × 2520) @ 60 fps

[1] For details about the multiplexing and conflict relationships of UART, I2C, SPI and I2S interfaces, see ***Table 20***.

Camera Interfaces	● Support 3 groups of 4-lane MIPI_CSI with data rate up to 2.5 Gbps/lane ● Support 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) ● Support 3 groups of ISP: (13 MP + 13 MP) @ 30 fps, (25 MP + 5 MP) @ 30 fps, (16 MP + 16 MP) @ 24 fps ● Support up to 3 concurrently working cameras
Video Codec	● Encoding: 1080p @ 60 fps 8-bit HEVC (H.265), 1080p @ 60 fps 8-bit H.264 ● Decoding: 1080p @ 60 fps 8-bit H.264, 1080p @ 60 fps 8-bit HEVC (H.265), VP9 ● Encoding + Decoding: 1080p @ 30 fps + 1080p @ 30 fps
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DRX) ● GNSS antenna interface (ANT_GNSS) ● Wi-Fi & Bluetooth antenna interface (ANT_WIFI/BT) ● 50 Ω characteristic impedance
Transmitting Power	● LTE-TDD: Class 3 (23 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Complies with 3GPP Rel-10 FDD and TDD ● Max. LTE category: – DL CA: Cat 4 – UL CA: Cat 4 ● 1.4 MHz, 3 MHz, 5 MHz,10 MHz,15 MHz and 20 MHz RF bandwidths ● DL modulations: QPSK, 16QAM and 64QAM ● UL modulations: QPSK and 16QAM ● DL 2 × 2 MIMO ● LTE-FDD max. data rates: – DL: 150 Mbps – UL: 50 Mbps ● LTE-TDD max. data rates: – DL: 130 Mbps – UL: 30 Mbps
GNSS features (optional)	GPS, GLONASS, BDS, Galileo, QZSS and SBAS positioning systems
WLAN Features	● Operating modes: AP and STA ● Operating frequency: 2.4 GHz, 5 GHz ● Protocol features: IEEE 802.11a/b/g/n/ac ● Data rate: up to 150 Mbps (on 2.4 GHz) and 433 Mbps (on 5 GHz)
Bluetooth Features	● *Bluetooth Core Specification Version 5.0* ● Bluetooth Classic & Bluetooth Low Energy (BLE)
Real Time Clock	The module supports RTC function
Temperature Ranges	● Normal operating temperature [2]: -35 °C to +75 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 interface ● OTA
RoHS	All hardware components fully comply with EU RoHS directive

[2] Within this range, the module's indicators comply with 3GPP specification requirements.

2.3. Pin Definitions

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PU	Pull Up
PD	Pull Down

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply						
Pin Name	**Pin No.**	**I/O**	**Status After Reset**	**Description**	**DC Characteristics**	**Comment**
VBAT	1, 2, 145, 146	PI	-	Power supply for the module	Vmin = 3.55 V Vnom = 3.8 V Vmax = 4.4 V	It must be provided with sufficient current of at least 3.0 A. It is recommended to use a TVS to increase voltage surge withstand capability.
VPH_PWR	184	PI	-	Power supply for the module		Connect to VBAT internally.
LDO9A_1V8	111	PO	-	1.8 V output power for I/O of external cameras, LCM and sensors	Vnom = 1.8 V $I_O$max = 200 mA	Cannot be used as power supply for peripherals. An external capacitor is not required.
ELDO3_3V0	156	PO	-	3.0 V output power for TP and sensors	Vnom = 3.0 V $I_O$max = 300 mA	Add a 1.0–2.2 µF bypass capacitor if used.

						The voltage is not adjustable. Controlled by GPIO_54 and PMU_GPIO01 internally.
ELDO1_1V8	125	PO	-	1.8 V output power for IOVDD of external camera LCM	Vnom = 1.8 V $I_O$max = 300 mA	Add a 1.0–4.7 µF bypass capacitor if used. The voltage is not adjustable. Controlled by PMU_GPIO05 internally.
VRTC	126	PIO	-	Power supply for RTC	Vmin = 2.0 V Vnom = 3.0 V Vmax = 3.25 V	If unused, keep it open.
ELDO2_2V8	129	PO	-	2.8 V output power supply	Vnom = 2.8 V $I_O$max = 500 mA	Add a 1.0–2.2 µF bypass capacitor if used. The voltage is not adjustable. Controlled by PMU_GPIO06 internally.
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 162, 171, 172, 176, 187–191, 202–204, 206–224, 226–231, 233–238, 240, 241, 243–245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271–274					

Analog Audio Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
MIC_BIAS1	147	PO	-	Bias voltage output 1 for microphone	Vmin = 1.0 V Vmax = 2.85 V	The maximum output current is 6 mA. The default output voltage set by the software is 1.8 V.
MIC1_P	4	AI	-	Microphone input for channel 1 (+)		
MIC1_M	5	AI	-	Microphone input for channel 1 (-)		
MIC2_P	6	AI	-	Microphone input for headset (+)		
MIC3_P	148	AI	-	Microphone input for channel 2 (+)		
MIC3_M	149	AI	-	Microphone input for channel 2 (-)		
MIC_BIAS3	155	PO	-	Bias voltage output 3 for microphone	Vmin = 1.0 V Vmax = 2.85 V	The maximum output current is 6 mA. The default output voltage set by the software is 1.8 V.
EAR_P	8	AO	-	Earpiece output (+)		
EAR_M	9	AO	-	Earpiece output (-)		
LINEOUT_P	10	AO	-	Loudspeaker output (+)		An additional audio PA is required.

LINEOUT_M	11	AO	-	Loudspeaker output (-)		
HPH_R	136	AO	-	Headphone right channel output		
HPH_GND	137	AO	-	Headphone reference ground		
HPH_L	138	AO	-	Headphone left channel output		
HS_DET	139	AI	-	Headset hot-plug detect		High level by default.

USB Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USB_VBUS	141, 142	PI	-	USB/adaptor insertion detection	Vmax = 21.0 V Vnom = 5.0 V Vmin = 4.0 V	A test point must be reserved.
USB_DM	13	AIO	-	USB 2.0 differential data (-)		Tests points must be reserved. 90 Ω differential impedance.
USB_DP	14	AIO	-	USB 2.0 differential data (+)		
USB_SS1_RX_P	252	AI	-	USB 3.1 channel 1 SuperSpeed receive (+)		90 Ω differential impedance. USB 3.1 Gen 1 standard compliant.
USB_SS1_RX_M	270	AI	-	USB 3.1 channel 1 SuperSpeed receive (-)		
USB_SS1_TX_P	254	AO	-	USB 3.1 channel 1 SuperSpeed transmit (+)		
USB_SS1_TX_M	253	AO	-	USB 3.1 channel 1 SuperSpeed transmit (-)		
USB_SS2_RX_P	152	AI	-	USB 3.1 channel 2 SuperSpeed receive (+)		
USB_SS2_RX_M	192	AI	-	USB 3.1 channel 2 SuperSpeed receive (-)		
USB_SS2_TX_P	150	AO	-	USB 3.1 channel 2 SuperSpeed transmit (+)		
USB_SS2_TX_M	151	AO	-	USB 3.1 channel 2 SuperSpeed transmit (-)		
USB_CC1	249	AI	-	USB Type-C configuration channel 1		

USB_CC2	246	AI	-	USB Type-C configuration channel 2		
USB_ID	16	AI	-	USB ID detect		High level by default.

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USIM1_VDD	26	PO	-	(U)SIM1 card power supply	**Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.1 V Vnom = 2.95 V Vmin = 2.7 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DATA	25	DIO	-	(U)SIM1 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	It is internally pulled up to USIM1_VDD with a 20 kΩ resistor.
USIM1_CLK	24	DO	-	(U)SIM1 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM1_VDD	
USIM1_RST	23	DO	-	(U)SIM1 card reset		
USIM1_DET	22	DI	PD	(U)SIM1 card hot-plug detect	LDO9A_1V8	Active low. External pull-up to 1.8 V is required. If unused, keep it open. The function is disabled by default, and can be enabled by software configuration.
USIM2_VDD	21	PO	-	(U)SIM2 card power supply	**Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.1 V Vnom = 2.95 V Vmin = 2.7 V	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	20	DIO	-	(U)SIM2 card data	V_{IL}max = 0.2 × USIM1_VDD V_{IH}min = 0.7 × USIM1_VDD V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	It is internally pulled up to USIM2_VDD with a 20 kΩ resistor.
USIM2_CLK	19	DO	-	(U)SIM2 card clock	V_{OL}max = 0.4 V V_{OH}min = 0.8 × USIM2_VDD	
USIM2_RST	18	DO	-	(U)SIM2 card reset		
USIM2_DET	17	DI	PD	(U)SIM2 card hot-plug detect	LDO9A_1V8	Active low. External pull-up to 1.8 V is required.

						If unused, keep it open. The function is disabled by default, and can be enabled by software configuration.

SD Card Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
SD_CLK	39	DO	-	SD card clock	**Low-voltage:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **High-voltage:** V_{OL}max = 0.37 V V_{OH}min = 2.2 V	50 Ω impedance.
SD_CMD	40	DIO	-	SD card command	**Low-voltage:** V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{OL}max = 0.45 V V_{OH}min = 1.4 V **High-voltage:** V_{IL}max = 0.73 V V_{IH}min = 1.84 V V_{OL}max = 0.37 V V_{OH}min = 2.2 V	
SD_DATA0	41	DIO	-	SDIO data bit 0		
SD_DATA1	42	DIO	-	SDIO data bit 1		
SD_DATA2	43	DIO	-	SDIO data bit 2		
SD_DATA3	44	DIO	-	SDIO data bit 3		
SD_DET	45	DI	PD	SD card hot-plug detect	LDO9A_1V8	Active low.
SD_VDD	38	PO	-	SD card Power Supply	Vnom = 2.96 V $I_O$max = 600 mA	
SD_PU_VDD	32	PO	-	1.8/2.95 V output power for SD card pull-up circuits	**Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.1 V Vnom = 2.95 V Vmin = 2.7 V	

Touch Panel Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
TP_RST	31	DO	PD	TP reset	LDO9A_1V8	Active low.
TP_INT	30	DI	PD	TP interrupt		
TP_I2C_SCL	47	OD	PD	TP I2C clock		External pull-up to 1.8 V is required. These pins can be connected with other I2C peripherals when they are not
TP_I2C_SDA	48	OD	PD	TP I2C data		

						used for TP interface.

LCM Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
LCD_RST	49	DO	PD	LCD reset	LDO9A_1V8	
LCD_TE	50	DI	PD	LCD tearing effect		
DSI_CLK_N	52	AO	-	LCD MIPI clock (-)		85 Ω differential impedance.
DSI_CLK_P	53	AO	-	LCD MIPI clock (+)		
DSI_LN0_N	54	AO	-	LCD MIPI data 0 (-)		
DSI_LN0_P	55	AO	-	LCD MIPI data 0 (+)		
DSI_LN1_N	56	AO	-	LCD MIPI data 1 (-)		
DSI_LN1_P	57	AO	-	LCD MIPI data 1 (+)		
DSI_LN2_N	58	AO	-	LCD MIPI data 2 (-)		
DSI_LN2_P	59	AO	-	LCD MIPI data 2 (+)		
DSI_LN3_N	60	AO	-	LCD MIPI data 3 (-)		
DSI_LN3_P	61	AO	-	LCD MIPI data 3 (+)		
PWM	29	DO	IN/PD	PWM output	VBAT	

Camera Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
CSI1_CLK_N	63	AI	-	MIPI CSI1 clock (-)		85 Ω differential impedance.
CSI1_CLK_P	64	AI	-	MIPI CSI1 clock (+)		
CSI1_LN0_N	65	AI	-	MIPI CSI1 data 0 (-)		
CSI1_LN0_P	66	AI	-	MIPI CSI1 data 0 (+)		
CSI1_LN1_N	67	AI	-	MIPI CSI1 data 1 (-)		
CSI1_LN1_P	68	AI	-	MIPI CSI1 data 1 (+)		
CSI1_LN2_N	72	AI	-	MIPI CSI1 data 2 (-)		
CSI1_LN2_P	73	AI	-	MIPI CSI1 data 2 (+)		
CSI1_LN3_N	70	AI	-	MIPI CSI1 data 3 (-)		
CSI1_LN3_P	71	AI	-	MIPI CSI1 data 3 (+)		

CSI0_CLK_N	157	AI	-	MIPI CSI0 clock (-)		
CSI0_CLK_P	196	AI	-	MIPI CSI0 clock (+)		
CSI0_LN0_N	158	AI	-	MIPI CSI0 data 0 (-)		
CSI0_LN0_P	197	AI	-	MIPI CSI0 data 0 (+)		
CSI0_LN1_N	159	AI	-	MIPI CSI0 data 1 (-)		
CSI0_LN1_P	198	AI	-	MIPI CSI0 data 1 (+)		
CSI0_LN2_N	160	AI	-	MIPI CSI0 data 2 (-)		
CSI0_LN2_P	199	AI	-	MIPI CSI0 data 2 (+)		
CSI0_LN3_N	161	AI	-	MIPI CSI0 data 3 (-)		
CSI0_LN3_P	200	AI	-	MIPI CSI0 data 3 (+)		
CSI2_CLK_N	257	AI	-	MIPI CSI2 clock (-)		
CSI2_CLK_P	232	AI	-	MIPI CSI2 clock (+)		
CSI2_LN0_N	167	AI	-	MIPI CSI2 data 0 (-)		
CSI2_LN0_P	168	AI	-	MIPI CSI2 data 0 (+)		
CSI2_LN1_N	169	AI	-	MIPI CSI2 data 1 (-)		
CSI2_LN1_P	170	AI	-	MIPI CSI2 data 1 (+)		
CSI2_LN2_N	178	AI	-	MIPI CSI2 data 2 (-)		
CSI2_LN2_P	179	AI	-	MIPI CSI2 data 2 (+)		
CSI2_LN3_N	174	AI	-	MIPI CSI2 data 3 (-)		
CSI2_LN3_P	175	AI	-	MIPI CSI2 data 3 (+)		
CAM_I2C0_SCL	83	OD	PD	I2C0 clock of camera	LDO9A_1V8	The flash driver chip in the module occupies the 0x63 address of the I2C bus. Cannot be used for generic GPIO. An external 2.2 kΩ resistor is required to pull it up to 1.8 V. This pin is dedicated to CAM_I2C and cannot be used for other I2C devices.
CAM_I2C0_SDA	84	OD	PD	I2C0 data of camera		
CAM0_PWDN	80	DO	PD	Power down of camera 0	LDO9A_1V8	
CAM1_PWDN	82	DO	PD	Power down of camera 1		
CAM2_PWDN	163	DO	PD	Power down of camera 2		

CAM0_MCLK	74	DO	PD	Master clock of camera 0		
CAM1_MCLK	75	DO	PD	Master clock of camera 1		
CAM2_MCLK	165	DO	PD	Master clock of camera 2		
CAM3_MCLK	33	DO	PD	Master clock of camera 3		
CAM0_RST	79	DO	PD	Reset of camera 0		
CAM1_RST	81	DO	PD	Reset of camera 1		
CAM2_RST	164	DO	PD	Reset of camera 2		
CAM_I2C1_SCL	166	OD	PD	I2C1 clock of camera		An external 2.2 kΩ resistor is required to pull it up to 1.8 V. This pin is dedicated to CAM_I2C and cannot be used for other I2C devices.
CAM_I2C1_SDA	205	OD	PD	I2C1 data of camera		

Flash & Torch Interface

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
FLASH_LED	180	AO	-	Flash/torch driver output	**Flash:** Imax = 1.5 A **Torch:** Imax = 375 mA	The built-in flash driver chip should be used with CAM_I2C0. Torch and flash mode is supported.

Keypad Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
PWRKEY	114	DI	-	Turn on/off the module		Pull it up to 1.1 V internally. Active low.
VOL_UP	95	DI	PD	Volume up	LDO9A_1V8	If unused, keep it open.
VOL_DOWN	96	DI	PD	Volume down		
RESET_N	225	DI	-	Reset the module		The function is disabled by default, and can be enabled by software configuration. A test point is recommended to be reserved if unused.

UART Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
DBG_TXD	94	DO	PD	Debug UART Transmit	LDO9A_1V8	If unused, keep them open.

DBG_RXD	93	DI	PD	Debug UART Receive		Test points must be reserved.
UART0_TXD	34	DO	PD	UART0 transmit		
UART0_RXD	35	DI	PD	UART0 receive		
UART0_RTS	37	DO	PD	Request to send signal from the module		If unused, keep them open.
UART0_CTS	36	DI	PD	Clear to send signal to the module		
UART1_TXD	154	DO	PD	UART1 transmit		
UART1_RXD	153	DI	PD	UART1 receive		

Sensor Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
SENSOR_I2C_SCL	91	OD	PD	I2C clock for external sensor	LDO9A_1V8	An external 2.2 kΩ resistor is required to pull it up to 1.8 V. SENSOR_I2C only supports sensors in the ADSP architecture.
SENSOR_I2C_SDA	92	OD	PD	I2C data for external sensor		
ALPS_INT	107	DI	PD	Light/proximity sensor interrupt		
GYRO_INT	108	DI	PD	Gyroscopic sensor interrupt		
MAG_INT	109	DI	PD	Magnetic sensor interrupt		
ACCEL_INT	110	DI	PD	Acceleration sensor interrupt		

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
ANT_MAIN	87	AIO	-	Main antenna interface		50 Ω characteristic impedance.
ANT_GNSS	121	AI	-	GNSS antenna interface		
ANT_DRX	131	AI	-	Diversity antenna interface		
ANT_WIFI/BT	77	AIO	-	Wi-Fi/ Bluetooth antenna interface		

Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Status	Description	DC Characteristics	Comment

			After Reset			
GRFC_0	173	DIO	-	Generic RF Controller		Only used for RF tuner control.
GRFC_1	260	DIO	-	Generic RF Controller		
GRFC_9	262	DIO	-	Generic RF Controller		

ADC Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
ADC0	128	AI	IN/PD	General-purpose ADC interface		The maximum input voltage is 1.875 V.
ADC1	185	AI	IN/PD			

Other Interfaces

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
USB_BOOT	46	DI	-	Force the module into download mode		Pull it up to LDO9A_1V8 will force the module to download mode. A test point is recommended to be reserved.
GNSS_LNA_EN	194	DO	-	GNSS LNA enable control		Only used for the internal testing. Keep it open.
NFC_CLK	181	DO	-			
CBL_PWR_N	186	DI	-	Cable power-on; Initiates power on when grounded		If unused, keep it open.

GPIOs

Pin Name	Pin No.	I/O	Status After Reset	Description	DC Characteristics	Comment
GPIO_106	90	DIO	PD	General-purpose input/output	LDO9A_1V8	
GPIO_31	97					
GPIO_107	98					
GPIO_25	99					
GPIO_93	100					
GPIO_104	101					
GPIO_105	102					

GPIO_103	103		
GPIO_102	104		
GPIO_99	105		
GPIO_56	106		
GPIO_26	112		
GPIO_68	113		
GPIO_36	115		
GPIO_16	116		
GPIO_17	117		
GPIO_14	118		
GPIO_15	119		
GPIO_83	123		
GPIO_84	124		
GPIO_67	127		
GPIO_112	177		
GPIO_86	182		
GPIO_60	201		
GPIO_101	239		
GPIO_100	264		
GPIO_98	265		
GPIO_111	267		
Reserved Pins			
Pin Name	**Pin No.**		
RESERVED	28, 133, 134, 183, 193, 195, 242, 263, 275, 276, 277, 278		

2.4. EVB Kit

NetPrisma supplies an evaluation board (Smart EVB G5) with accessories to develop and test the module. For more details, see ***document 1***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Interface

The module provides four VBAT pins dedicated to connecting with the external power supply. The power supply range of the module is 3.55–4.4 V, and the recommended value is 3.8 V.

Table 7: VBAT and GND Pins

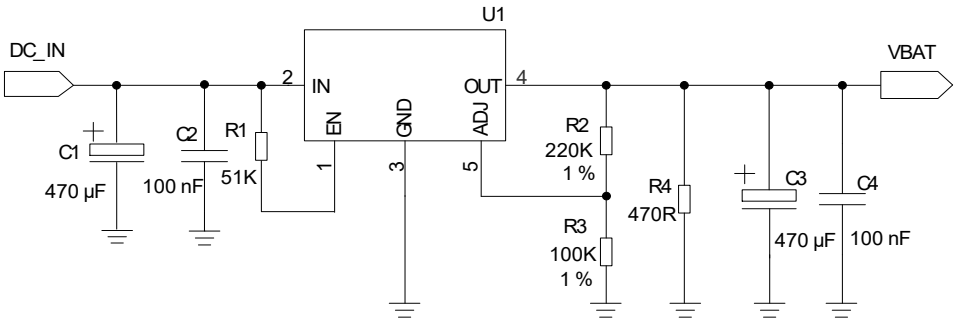
Pin Name	Pin No.	I/O	Description	Comment
VBAT	1, 2, 145, 146	PI	Power supply for the module	It must be provided with sufficient current of at least 3.0 A. It is recommended to use a TVS to increase voltage surge withstand capability.
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 162, 171, 172, 176, 187–191, 202–204, 206–224, 226–231, 233–238, 240, 241, 243–245, 247, 248, 250, 251, 255, 256, 258, 259, 261, 266, 268, 269, 271–274			

3.1.2. Reference Design for Power Supply

The power source is critical to the module's performance. The power supply of the module should be able to provide sufficient current of at least 3 A. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for 5 V input power supply.

Figure 1: Reference Design of Power Input



NOTE

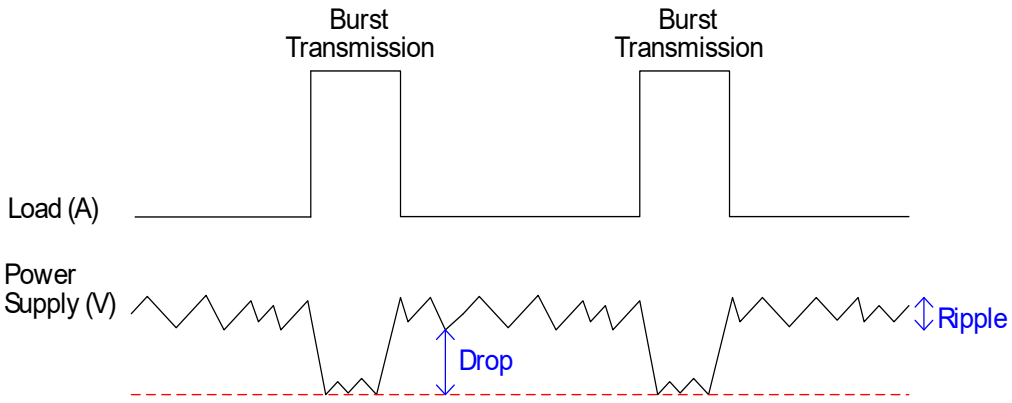
To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. It is essential to first shut down the module using PWRKEY before safely cutting off the power supply.

3.1.3. Requirements for Voltage Stability

The recommended power supply voltage of the module is 3.8 V. The power supply performance, such as load capacity, voltage ripple will directly influence the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3 A. If the power supply capability is not

sufficient, there will be voltage drops, and if the voltage drops below 3.3 V, the module will turn off automatically. Therefore, ensure the input voltage never drops below 3.3 V.

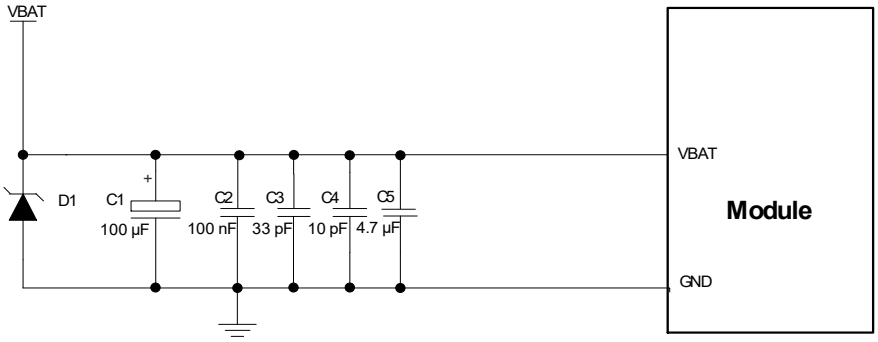
Figure 2: Power Supply Limits During Burst Transmission



To prevent the voltage from dropping below 3.3 V, it is recommended to connect a 100 µF bypass capacitor with low ESR as well as 100 nF, 33 pF and 10 pF and 4.7µF filter capacitors in parallel near the VBAT pins of the module. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power. The width of VBAT trace should be at least 3 mm. As per design rules, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

To suppress the impact of power fluctuations and ensure the stability of the output power supply, it is suggested to add a TVS component and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows a reference circuit:

Figure 3: Reference Design of Power Supply



3.2. Turn On

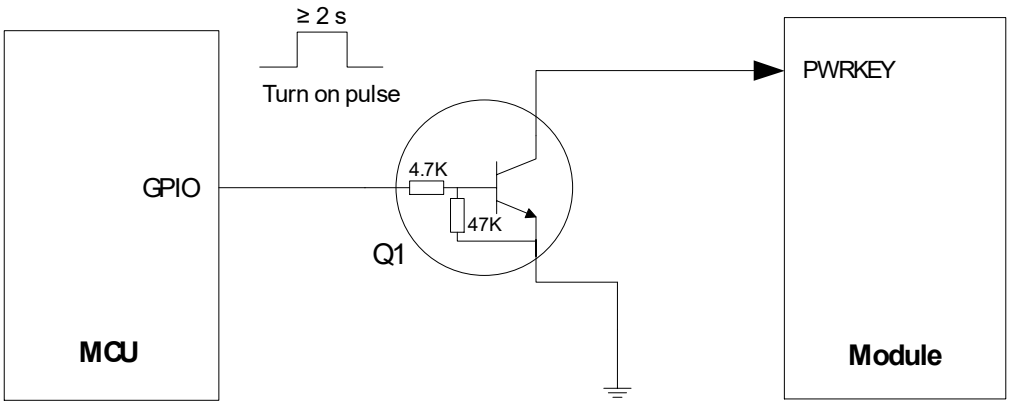
3.2.1. Turn On with PWRKEY

Table 8: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	114	DI	Turn on/off the module	Pull it up to 1.1 V internally. Active low.

When powering up the VBAT, the module can be turned on by driving PWRKEY low for at least 2 s. It is recommended to use an open drain/collector driver to control PWRKEY. PWRKEY is pulled up to VBAT internally.

Figure 4: Reference Design of Turn-on with Driving Circuit



Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

Figure 5: Reference Design of Turn-on with Keystroke

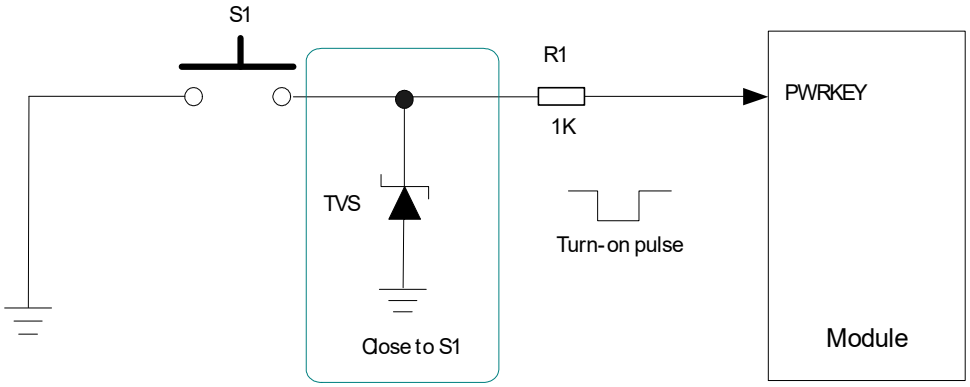
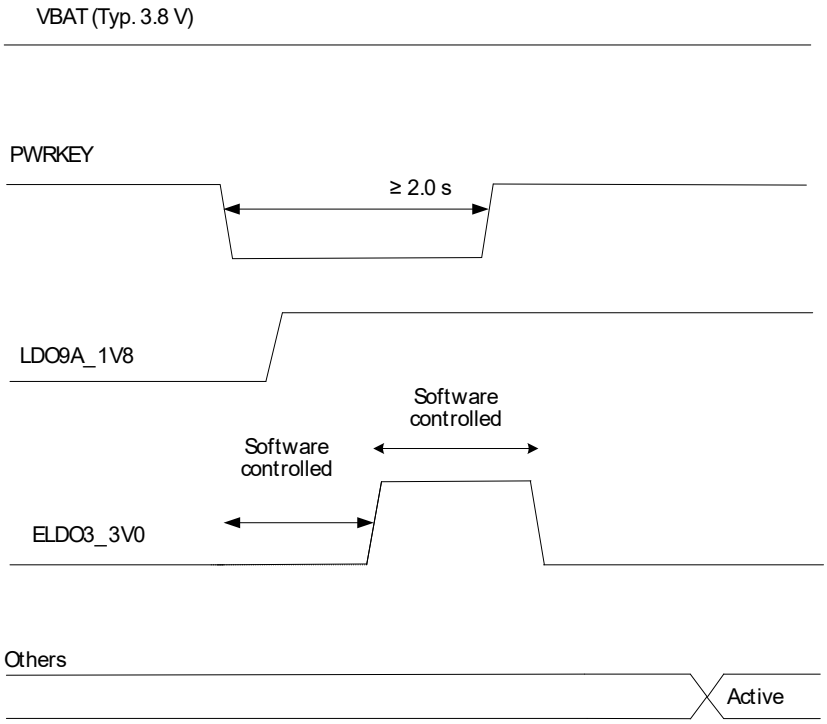


Figure 6: Timing of Turn On with PWRKEY



NOTE

1. When the module is powered up for the first time, its turn on timing may be different from that shown in the figure above.
2. Ensure the voltage of VBAT is stable before driving PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 3.8 V and remains stable for 30 ms. PWRKEY cannot be driven low all the time.

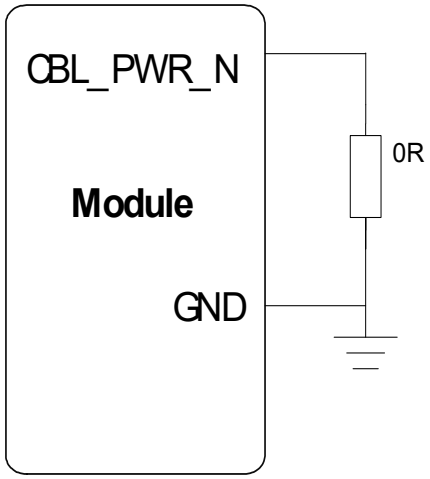
3.2.2. Turn On Automatically with CBL_PWR_N

Table 9: Pin Description of CBL_PWR_N

Pin Name	Pin No.	I/O	Description	Comment
CBL_PWR_N	186	DI	Cable power-on; Initiates power on when grounded	If unused, keep it open.

The module can turn on automatically through CBL_PWR_N:

Figure 7: Reference Circuit of Automatically Turn-on with CBL_PWR_N



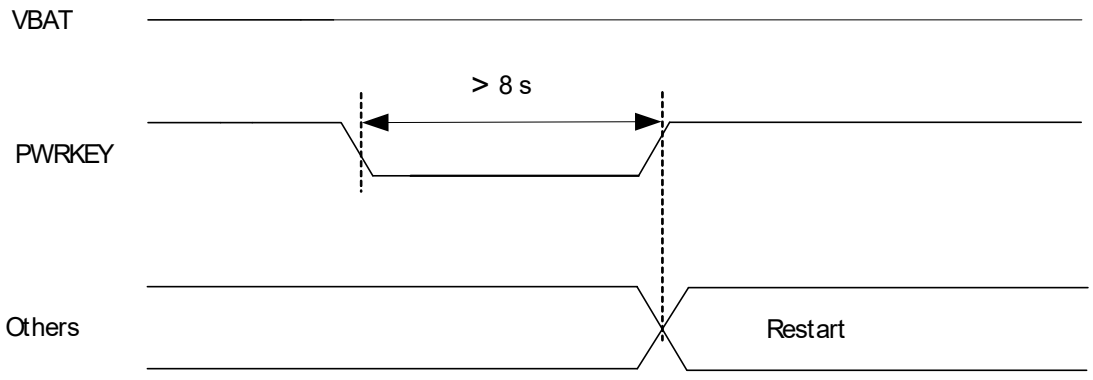
NOTE

If the module turns on automatically through CBL_PWR_N, it cannot be turned off manually. In such case, it can be turned off only by cutting off the power supply of system.

3.3. Restart/Turn Off

The module can be turned off by driving PWRKEY low for at least 1 s, and then choose to turn off or to restart the module when the prompt window comes up. In addition, you can execute the forced restart by driving PWRKEY low for more than 8 s.

Figure 8: Timing of Restart



3.4. VRTC

Table 10: Pin Description of VRTC

Pin Name	Pin No.	I/O	Description	Comment

VRTC	126	PIO	Power supply for RTC	If unused, keep it open.

The RTC of the module can be powered by an external power supply pin VRTC. When VBAT is disconnected and you need to reserve RTC function, VRTC cannot be kept open. The RTC can be powered by an external power source when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

Figure 9: RTC Powered by Rechargeable Cell Battery

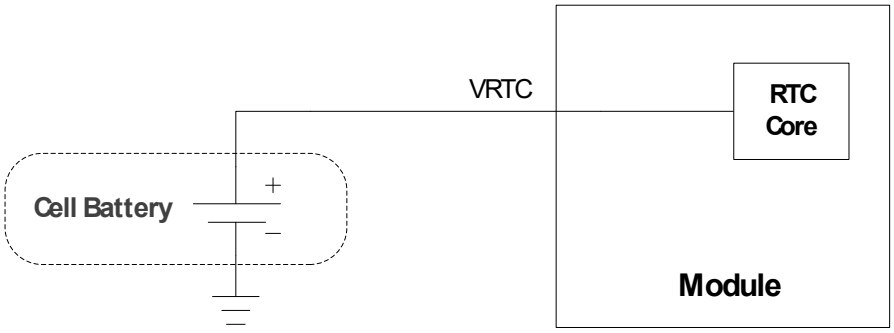
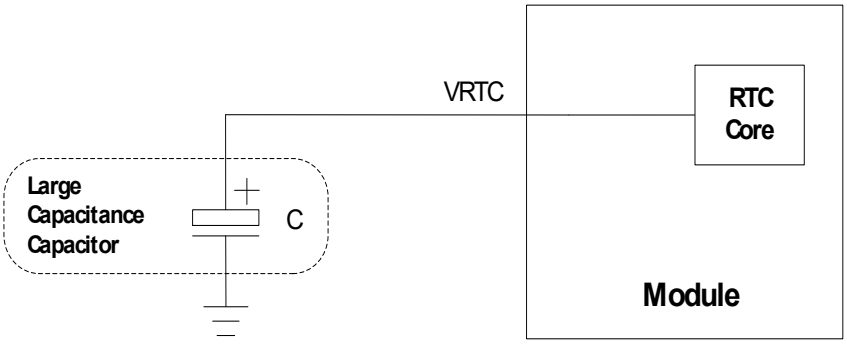


Figure 10: RTC Powered by Large Capacitance Capacitor



If RTC fails, the module can synchronize time over the network after being powered up.

- The recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V. The average power consumption is 10 μA when VBAT is disconnected.
- When powered by VBAT, the deviation of RTC is 50 ppm; When powered by VRTC, the deviation of RTC is 200 ppm.
- If a rechargeable button battery is used, ESR of the battery should be less than 2 kΩ. It is recommended to use MS621FE FL11E of SEIKO.
- If RTC function is not required, a 4.7 μF capacitor should be connected to VRTC.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to use a 10 pF and a 33 pF capacitor in parallel to suppress high-frequency noise.

Table 11: Power Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
LDO9A_1V8	1.8	200	Keeps On
ELDO1_1V8	1.8	300	-
ELDO2_2V8	2.8	500	-
ELDO3_3V0	3.0	300	-

4 Application Interfaces

4.1. USB Interface

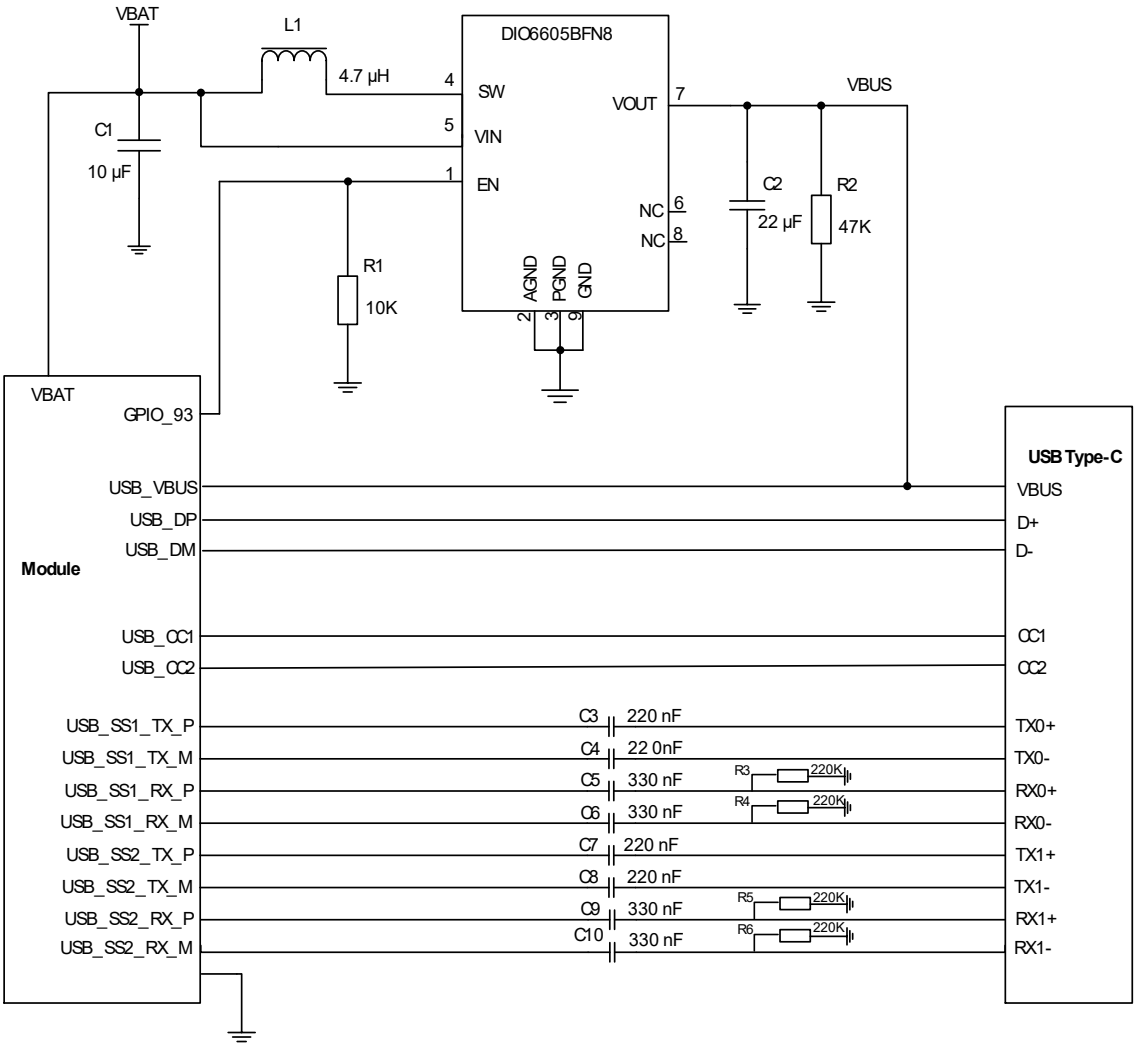
The module provides one USB interface which complies with USB 3.1 Gen 1 and USB 2.0 specifications and supports USB OTG, USB Type-C interface and Micro USB interface. It also supports SuperSpeed mode (5 Gbps) for USB 3.1 Gen 1, high-speed (480 Mbps) and full-speed (12 Mbps) modes for USB 2.0. The USB interface is used for AT command transmission, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

4.1.1. Type-C Interface

Table 12: Pin Description of USB Type-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	USB/adaptor insertion detection	A test point must be reserved.
USB_DM	13	AIO	USB 2.0 differential data (-)	Test points must be reserved. 90 Ω differential impedance.
USB_DP	14	AIO	USB 2.0 differential data (+)	
USB_SS1_RX_P	252	AI	USB 3.1 channel 1 SuperSpeed receive (+)	90 Ω differential impedance. USB 3.1 Gen 1 standard compliant.
USB_SS1_RX_M	270	AI	USB 3.1 channel 1 SuperSpeed receive (-)	
USB_SS1_TX_P	254	AO	USB 3.1 channel 1 SuperSpeed transmit (+)	
USB_SS1_TX_M	253	AO	USB 3.1 channel 1 SuperSpeed transmit (-)	
USB_SS2_RX_P	152	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB_SS2_RX_M	192	AI	USB 3.1 channel 2 SuperSpeed receive (-)	
USB_SS2_TX_P	150	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB_SS2_TX_M	151	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB_CC1	249	AI	USB Type-C configuration channel 1	
USB_CC2	246	AI	USB Type-C configuration channel 2	
USB_ID	16	AI	USB ID detect	High level by default.

Figure 11: Reference Design of USB Type-C Mode



4.1.2. Micro USB Interface

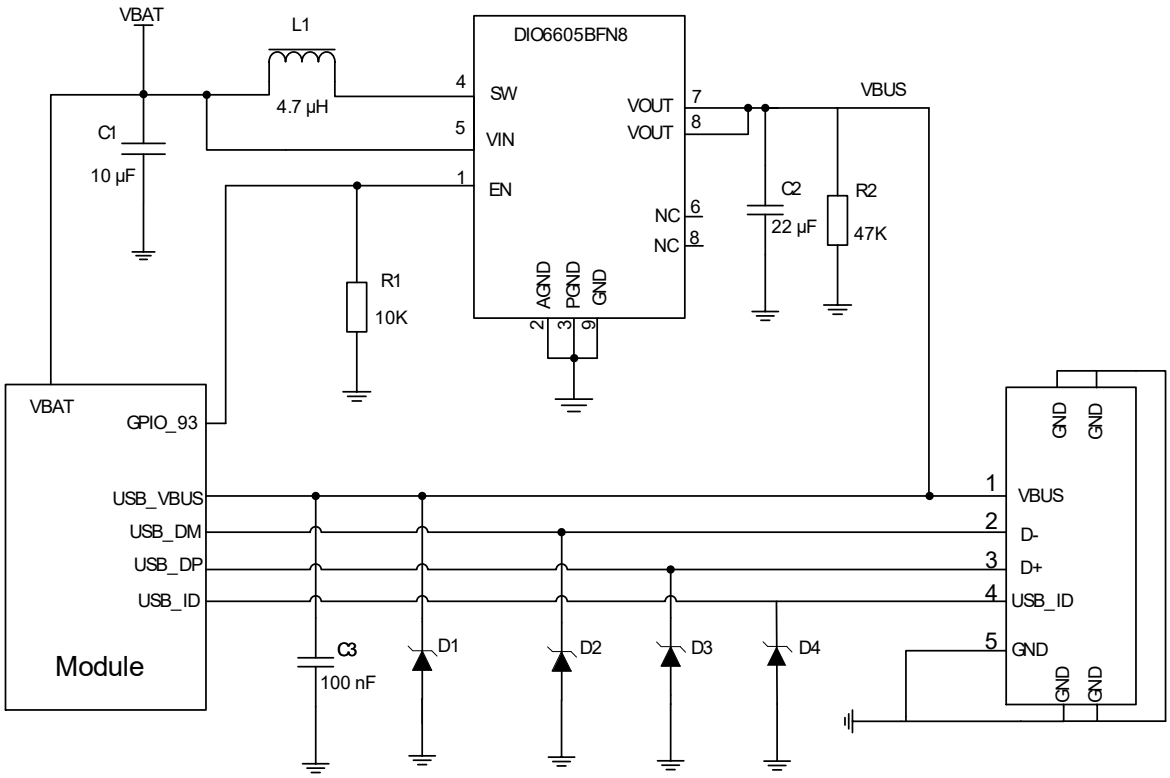
The module supports USB Type-C interface by default. Micro USB interface can be used via hardware configuration.

Table 13: Pin Description of Micro USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	141, 142	PI	USB/adaptor insertion detection	A test point must be reserved.
USB_DM	13	AIO	USB 2.0 differential data (-)	Test points must be reserved. 90 Ω differential impedance.
USB_DP	14	AIO	USB 2.0 differential data (+)	
USB_ID	16	DI	USB ID detect	High level by default.

The reference design of Micro USB interface configured with USB is shown below:

Figure 12: Reference Design of Micro USB Interface



4.1.3. USB Interface Design Considerations

Table 14: USB Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
13	USB_DM	32.74	0.06
14	USB_DP	32.68	
270	USB_SS1_RX_M	23.82	0.18
252	USB_SS1_RX_P	23.64	
253	USB_SS1_TX_M	13.55	0.03
254	USB_SS1_TX_P	13.58	
192	USB_SS2_RX_M	17.94	0.33
152	USB_SS2_RX_P	17.61	
151	USB_SS2_TX_M	23.56	0.08
150	USB_SS2_TX_P	23.64	

To ensure performance, you should follow the following principles when designing USB interfaces:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on

that layer and ground planes above and below. For signal traces, provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.

- The reference ground plane under the USB signal traces must be continuous without any cuts or vias to ensure impedance continuity.
- Pay attention to the impact caused by parasitic capacitance of the ESD protection component on USB data traces. Typically, parasitic capacitance should be less than 2 pF for USB 2.0, and less than 0.5 pF for USB 3.1 Gen 1.
- Do not route USB 3.1 Gen 1 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden. Isolation between USB 3.1 Gen 1 signals and RF signals should be over 90 dB. Otherwise, the RF signals will be seriously affected.
- For USB 3.1 Gen 1 signal traces, length matching of TX_P and TX_M, RX_P and RX_M should be less than 0.7 mm. While the inter-pair length matching (TX/RX) should be less than 10 mm.
- For USB 3.1 Gen 1, the spacing between RX and TX signal traces should be 3 times the signal trace width. The spacing between USB 3.1 Gen1 signal traces and other signal traces should be 4 times the signal trace width.
- For USB 2.0 signal traces, the differential data pair matching (DP/DM) should be less than 2 mm.
- For USB 2.0, the spacing between DP-DM signal traces and other signal traces should be 3 times the signal trace width.

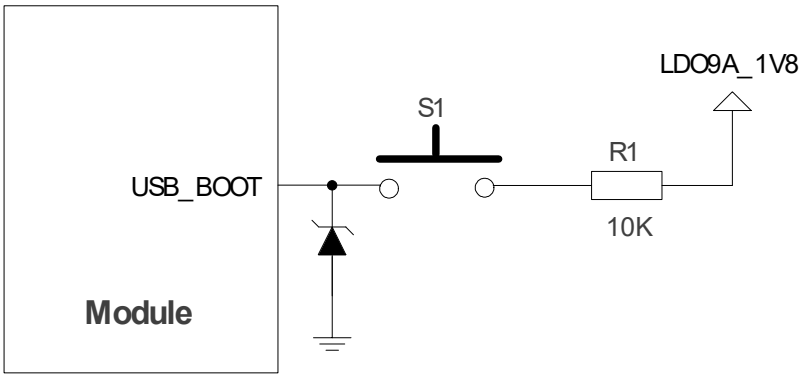
4.2. USB_BOOT

The module provides a USB_BOOT for forced download. Pull up USB_BOOT to LDO9A_1V8 before turning on the module, and then the module enters the forced download mode. This is a final approach when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Table 15: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	46	DI	Force the module into download mode	Pull it up to LDO9A_1V8 will force the module to download mode. A test point is recommended to be reserved.

Figure 13: Reference Design of USB_BOOT



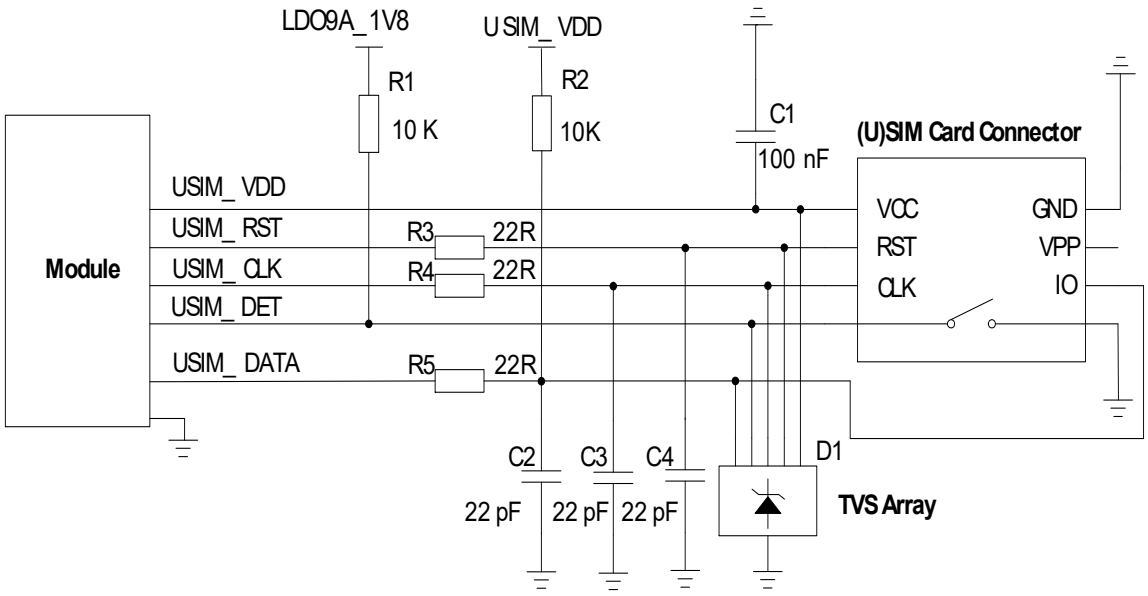
4.3. (U)SIM Interfaces

The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby function is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM card is powered by the internal power supply of the module.

Table 16: Pin Description of (U)SIM Interfaces

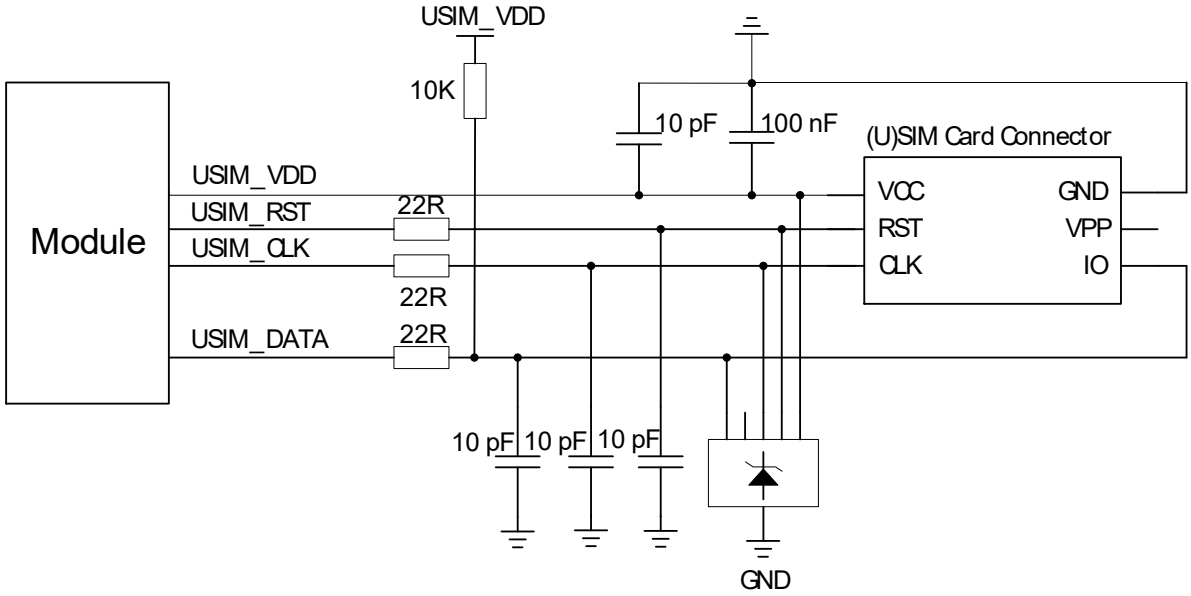
Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	26	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DATA	25	DIO	(U)SIM1 card data	It is internally pulled up to USIM1_VDD with a 20 kΩ resistor.
USIM1_CLK	24	DO	(U)SIM1 card clock	
USIM1_RST	23	DO	(U)SIM1 card reset	
USIM1_DET	22	DI	(U)SIM1 card hot-plug detect	Active low. External pull-up to 1.8 V is required. If unused, keep it open. The function is disabled by default, and can be enabled by software configuration.
USIM2_VDD	21	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	20	DIO	(U)SIM2 card data	It is internally pulled up to USIM2_VDD with a 20 kΩ resistor.
USIM2_CLK	19	DO	(U)SIM2 card clock	
USIM2_RST	18	DO	(U)SIM2 card reset	
USIM2_DET	17	DI	(U)SIM2 card hot-plug detect	Active low. External pull-up to 1.8 V is required. If unused, keep it open. The function is disabled by default, and can be enabled by software configuration.

Figure 14: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector



If the function of (U)SIM card hot-plug is not needed, keep USIM_DET open.

Figure 15: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector



To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Route (U)SIM card traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC.
- Ensure the tracing between the (U)SIM card connector and the module is short and wide. Keep the trace width of GND and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 30 pF. Add 22 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 22 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.
- For USIM_DATA, it is recommended to add a 10 kΩ pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U)SIM card.

4.4. SD Card Interface

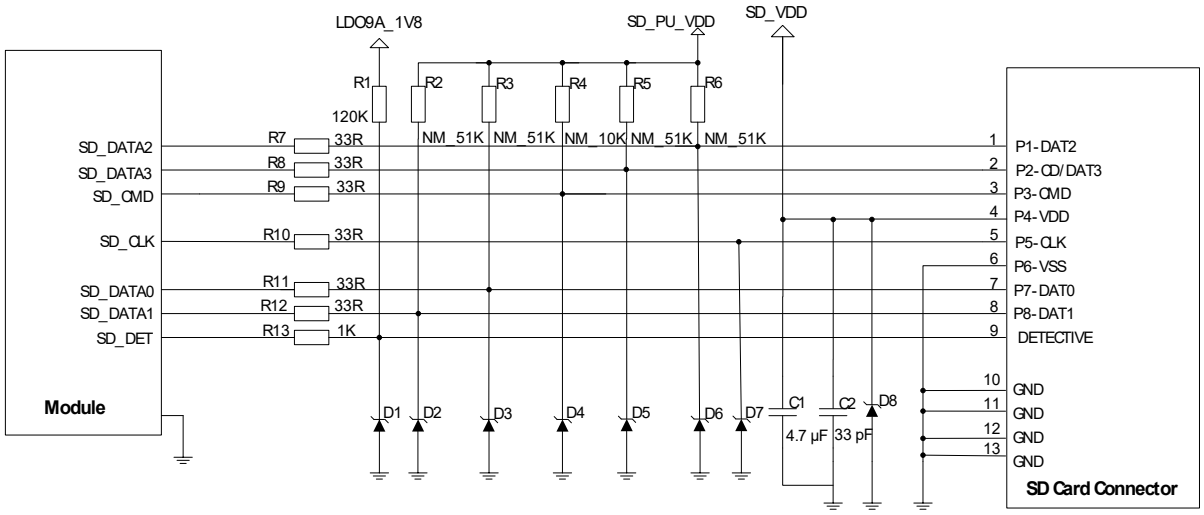
SD card interface of the module complies with SD 3.0 specifications:

Table 17: Pin Description of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	39	DO	SD card clock	50 Ω impedance.
SD_CMD	40	DIO	SD card command	
SD_DATA0	41	DIO	SDIO data bit 0	

SD_DATA1	42	DIO	SDIO data bit 1	
SD_DATA2	43	DIO	SDIO data bit 2	
SD_DATA3	44	DIO	SDIO data bit 3	
SD_DET	45	DI	SD card hot-plug detect	Active low.
SD_VDD	38	PO	SD card power supply	
SD_PU_VDD	32	PO	1.8/2.95 V output power for SD card pull-up circuits	

Figure 16: Reference Design of SD Card Interface



SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 800 mA. Because of the high drive current, it is recommended to keep the trace width as at least 0.8 mm. To ensure the stability of drive power, you should add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.
SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 50 Ω, shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- Trace length matching between SD_CLK and SD_CMD/SD_DATA should be less than 2 mm.
- The trace length should be less than 150 mm in SDR50 mode. Trace length matching between SD_CMD/SD_DATA[0:3] and SD_CLK should not exceed 6 mm.
- The spacing between signal traces should be 1.5 times the trace width.
- The load capacitance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 5 pF.

Table 18: SD Card Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length
39	SD_CLK	69.35

40	SD_CMD	69.38
41	SD_DATA0	69.14
42	SD_DATA1	69.24
43	SD_DATA2	69.08
44	SD_DATA3	68.93

4.5. UART Interfaces

The module supports up to five groups of UART. Three groups are configured by default, see ***Table 19*** for details. and two of them are multiplexed from other interfaces, see ***Table 20***.

Three groups of UART:

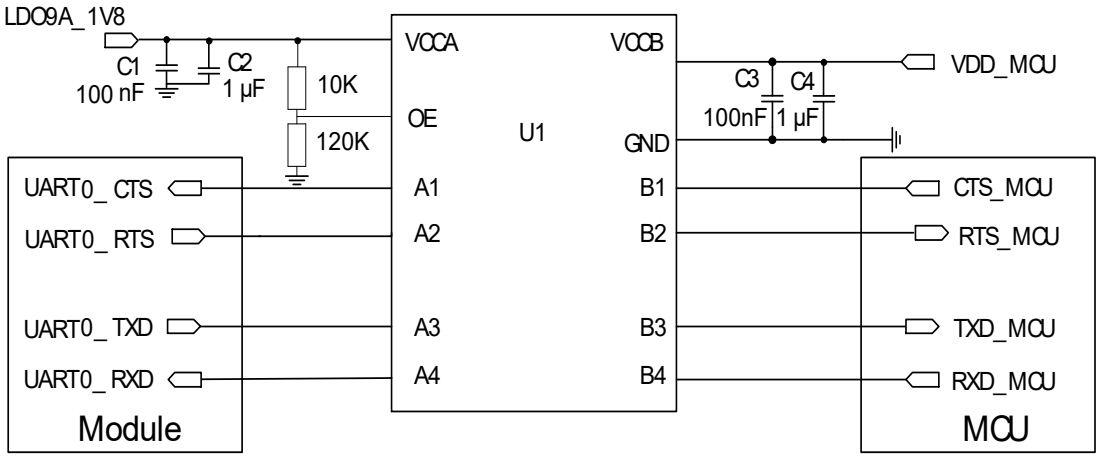
- UART0: 4-wire UART with the speed rate up to 4 Mbps, which supports RTS and CTS hardware flow control.
- UART1: 2-wire UART.
- Debug UART: 2-wire UART, used for debugging only.

Table 19: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	94	DO	Debug UART transmit	If unused, keep them open. Test points must be reserved.
DBG_RXD	93	DI	Debug UART receive	
UART0_TXD	34	DO	UART0 transmit	If unused, keep them open.
UART0_RXD	35	DI	UART0 receive	
UART0_RTS	37	DO	Request to send signal from the module	
UART0_CTS	36	DI	Clear to send signal to the module	
UART1_TXD	154	DO	UART1 transmit	
UART1_RXD	153	DI	UART1 receive	

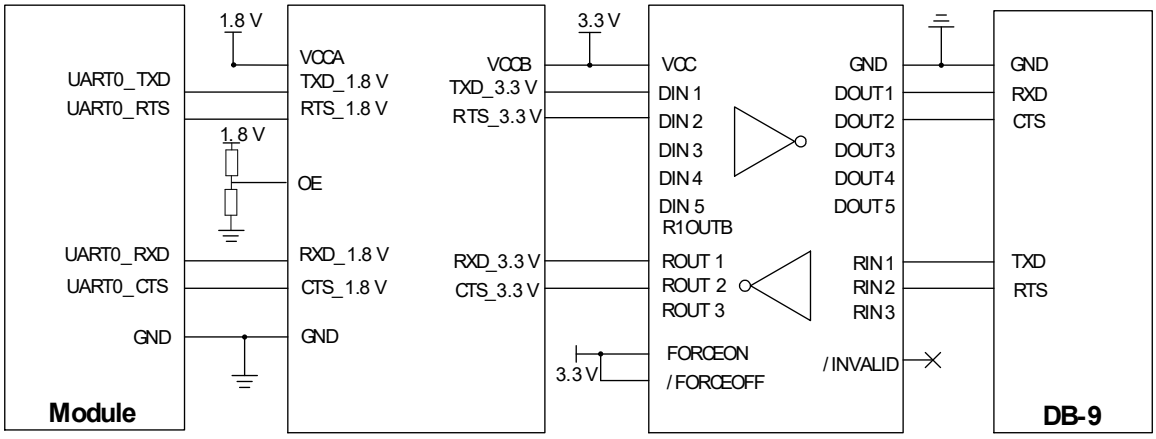
UART0 is a 4-wire UART with 1.8 V power domain. You can use a level-shifting chip between the module and MCU's UART if the MCU is equipped with a 3.3 V UART:

Figure 17: Reference Design of UART with Level-shifting Chip (UART0)



The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 level-shifting chip.

Figure 18: Reference Design of UART with RS-232 Level-shifting Chip (UART0)



NOTE

Debug UART is similar to UART0 and UART1. For the reference designs, refer to that of UART0.

4.6. SPI

The module supports up to five groups of SPI, which are multiplexed from other interfaces. SPI supports master mode only, and can be used for fingerprint recognition.

4.7. I2C Interfaces

The module supports up to eight groups of I2C interfaces. Three of them are dedicated I2C interfaces, used for cameras and sensors. One TP I2C interface is used for touch panel or other peripherals, and four are multiplexed from other interfaces, see ***Table 20*** for details. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. SENSOR_I2C only supports sensors of ADSP architecture. CAM_I2C/DCAM_I2C signals are controlled by Linux Kernel code and supports connection with video output related devices.

4.8. I2S Interfaces

The module supports up to two groups of I2S interfaces with 1.8 V power domain. Two of them are multiplexed from other interfaces, see ***Table 20***.

4.9. UART/SPI/I2C/I2S Multiplexing Relationship

The module supports up to five groups of configurable interfaces, which can be configured as UART, SPI, I2C or I2S interfaces. Specific multiplexing relationship is shown in the following table (dedicated I2C interfaces, dedicated debug UART and interfaces already used inside the module are not included):

Table 20: UART/SPI/I2C/I2S Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplexing Function			
				UART	SPI	I2C	I2S
QUP SE0	36	UART0_CTS	GPIO_0	UART_CTS	SPI_MISO	I2C_SDA	-
	37	UART0_RTS	GPIO_1	UART_RTS	SPI_MOSI	I2C_SCL	-
	34	UART0_TXD	GPIO_2	UART_TX	SPI_SCLK	-	-
	35	UART0_RXD	GPIO_3	UART_RX	SPI_CS_N_0	-	-
	49	LCD_RST	GPIO_82	-	SPI_CS_N_1	-	-
QUP SE1	80	CAM0_PWDN	GPIO_4	UART_CTS	SPI_MISO	I2C_SDA	-
	82	CAM1_PWDN	GPIO_5	UART_RTS	SPI_MOSI	I2C_SCL	-
	154	UART1_TXD	GPIO_69	UART_TX	SPI_SCLK	-	-
	153	UART1_RXD	GPIO_70	UART_RX	SPI_CS_N	-	-
QUP SE2	48	TP_I2C_SDA	GPIO_6	UART_CTS	SPI_MISO	I2C_SDA	-
	47	TP_I2C_SCL	GPIO_7	UART_RTS	SPI_MOSI	I2C_SCL	-
	31	TP_RST	GPIO_71	UART_TX	SPI_SCLK	-	-
	30	TP_INT	GPIO_80	UART_RX	SPI_CS_N	-	-

QUP SE4	95	VOL_UP	GPIO_96	UART_CTS	SPI_MISO	I2C_SDA	-
	96	VOL_DOWN	GPIO_97	UART_RTS	SPI_MOSI	I2C_SCL	-
	94	DBG_TXD	GPIO_12	UART_TX	SPI_SCLK	-	-
	93	DBG_RXD	GPIO_13	UART_RX	SPI_CS_N	-	-
QUP SE5	118	GPIO_14	GPIO_14	UART_CTS	SPI_MISO	I2C_SDA	-
	119	GPIO_15	GPIO_15	UART_RTS	SPI_MOSI	I2C_SCL	-
	116	GPIO_16	GPIO_16	UART_TX	SPI_SCLK	-	-
	117	GPIO_17	GPIO_17	UART_RX	SPI_CS_N	-	-
	265	GPIO_98	GPIO_98	-	-	-	LPI_MI2S0_CLK
	105	GPIO_99	GPIO_99	-	-	-	LPI_MI2S0_WS
	264	GPIO_100	GPIO_100	-	-	-	LPI_MI2S0_DATA0
	239	GPIO_101	GPIO_101	-	-	-	LPI_MI2S0_DATA1 /MI2S_MCLK1_B
	163	CAM2_PWDN	GPIO_108	-	-	-	MI2S_MCLK1_A
	104	GPIO_102	GPIO_102	-	-	-	LPI_MI2S1_CLK
	103	GPIO_103	GPIO_103	-	-	-	LPI_MI2S1_WS
	101	GPIO_104	GPIO_104	-	-	-	LPI_MI2S1_DATA0
	102	GPIO_105	GPIO_105	-	-	-	LPI_MI2S1_DATA1 /MI2S_MCLK0_A
	98	GPIO_107	GPIO_107	-	-	-	MI2S_MCLK1_C

NOTE

1. QUP-SE is flexible and supports four types of interfaces: UART, SPI, I2C and I2S.
2. Note that the same set of QUP-SE cannot support two protocols at the same time. For example: the same set of QUP cannot support UART and I2C at the same time. If a protocol only occupies part of the pins of this group of QUP, other pins can only be used for GPIO.

4.10. Analog Audio Interfaces

The module provides three groups of analog input channels and three groups of analog output channels:

Table 21: Pin Description of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MIC_BIAS1	147	PO	Bias voltage output 1 for microphone	The maximum output current is 6 mA. The default output voltage set by the software is 1.8 V.
MIC1_P	4	AI	Microphone input for channel 1 (+)	
MIC1_M	5	AI	Microphone input for channel 1 (-)	
MIC2_P	6	AI	Microphone input for headset (+)	
MIC3_P	148	AI	Microphone input for channel 2 (+)	
MIC3_M	149	AI	Microphone input for channel 2 (-)	
MIC_BIAS3	155	PO	Bias voltage output 3 for microphone	The maximum output current is 6 mA. The default output voltage set by the software is 1.8 V.
EAR_P	8	AO	Earpiece output (+)	
EAR_M	9	AO	Earpiece output (-)	
LINEOUT_P	10	AO	Loudspeaker output (+)	Additional audio PA is required.
LINEOUT_M	11	AO	Loudspeaker output (-)	
HPH_R	136	AO	Headphone right channel output	
HPH_GND	137	AO	Headphone reference ground	
HPH_L	138	AO	Headphone left channel output	
HS_DET	139	AI	Headset hot-plug detect detect	High level by default.

- The module offers three audio input channels, including two differential input pair and one single-ended input channels.
- The output voltage range of two MIC_BIAS is programmable from 1.0 V to 2.85 V, and the maximum output current is 6 mA.
- The earpiece interface uses the differential output.
- The loudspeaker interface uses the differential output, and an additional audio PA is required.
- The headset interface features stereo left and right channel output, and headset insert detection function is supported.

4.10.1. Microphone Interface Reference Design

Figure 19: Reference Design of ECM Microphone Interface

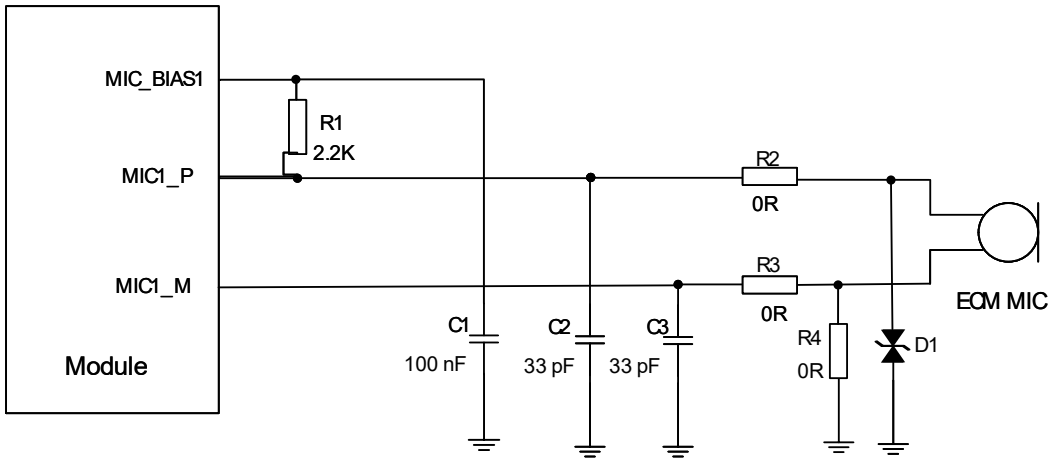
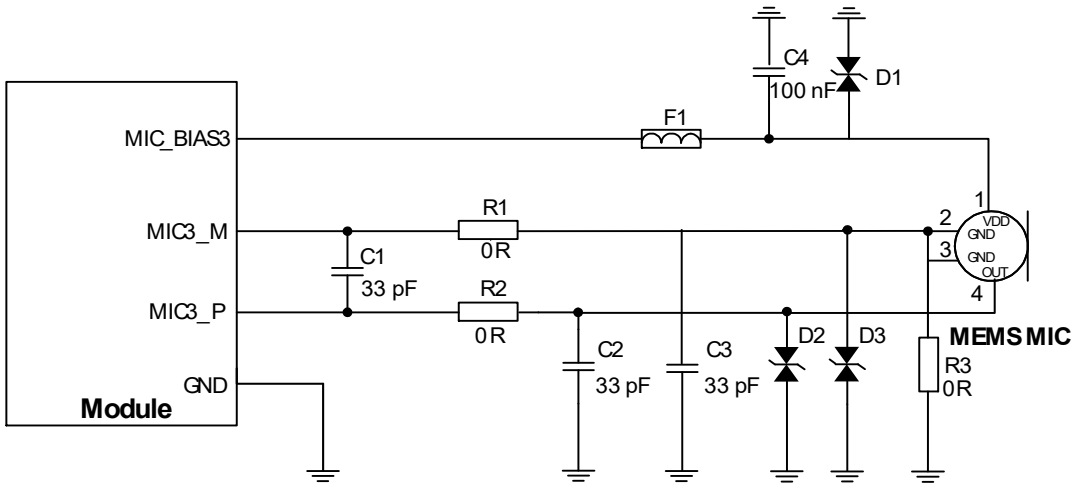
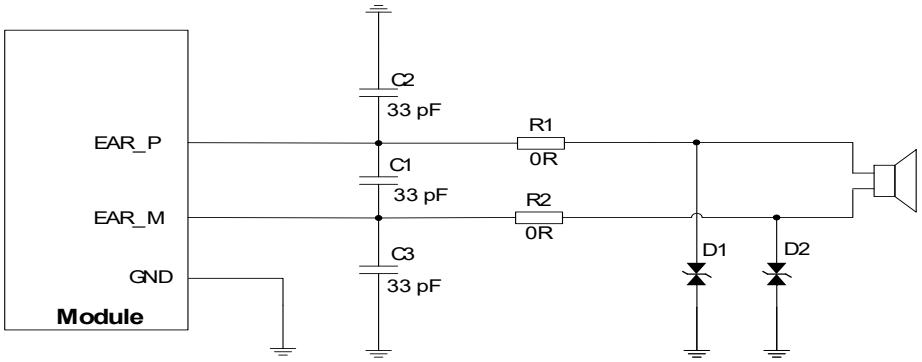


Figure 20: Reference Design of MEMS Microphone Interface



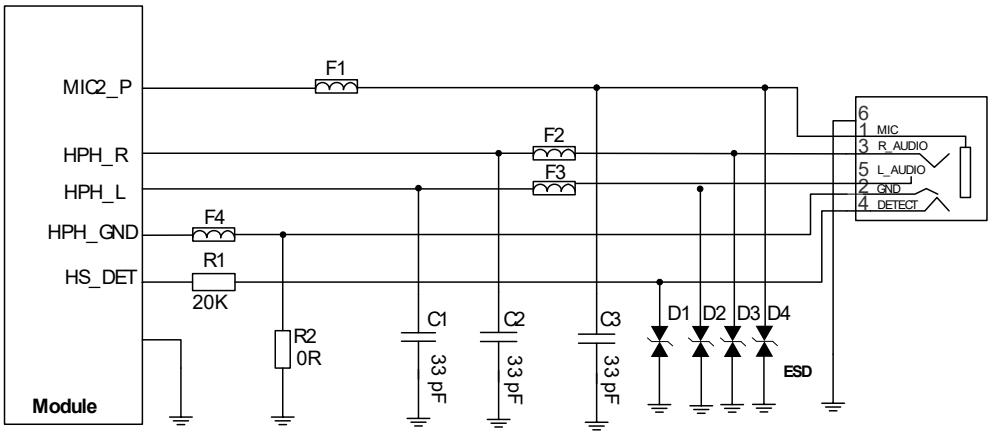
4.10.2. Earpiece Interface Reference Design

Figure 21: Reference Design of Earpiece Interface



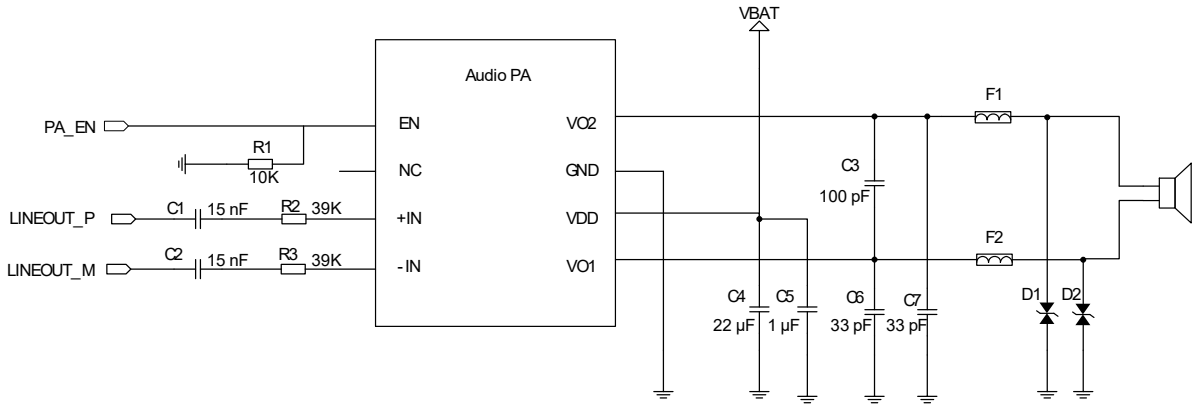
4.10.3. Headset Interface Reference Design

Figure 22: Reference Design of Headset Interface



4.10.4. Loudspeaker Interface Reference Design

Figure 23: Reference Design of Loudspeaker Interface



4.10.5. Audio Interface Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. Without this capacitor, TDD noise could be heard during the call. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises.

The filter capacitors on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. They should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.11. ADC Interfaces

The module provides two ADC interfaces which support up to 15-bit resolution.

Table 22: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment

ADC0	128	AI	General-purpose ADC interface	The maximum input voltage is 1.875 V.
ADC1	185	AI		

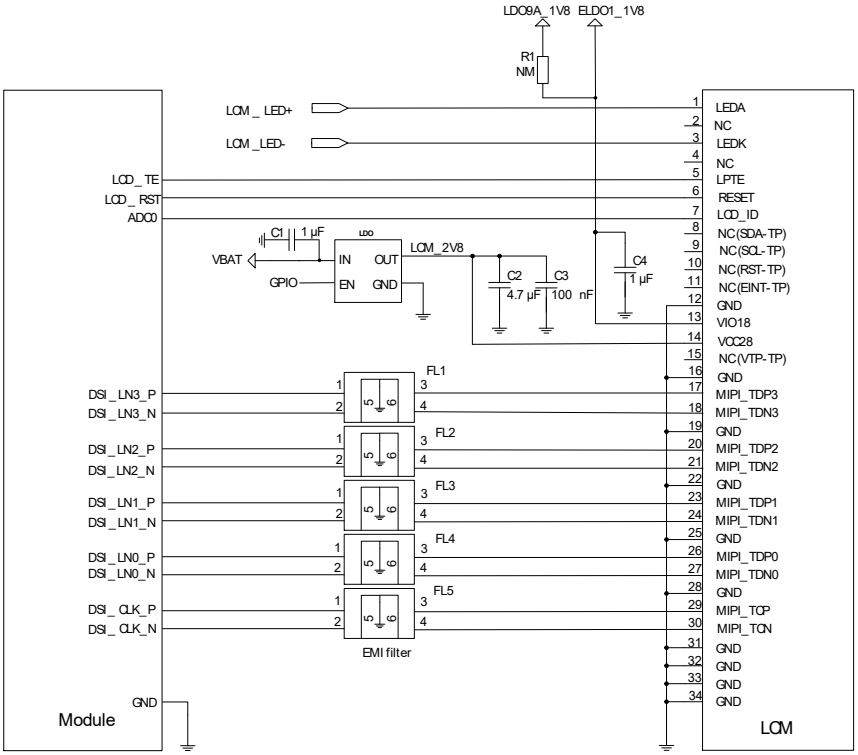
4.12. LCM Interface

The module provides one LCM interface, which is MIPI_DSI standard compliant. The interface supports 4-lane high-speed differential data transmission. The data rate can reach up to 1.5 Gbps per lane. The interface supports FHD+ display (1080 × 2520 @ 60 fps).

Table 23: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LCD_RST	49	DO	LCD reset	
LCD_TE	50	DI	LCD tearing effect	
DSI_CLK_N	52	AO	LCD MIPI clock (-)	85 Ω differential impedance.
DSI_CLK_P	53	AO	LCD MIPI clock (+)	
DSI_LN0_N	54	AO	LCD MIPI data 0 (-)	
DSI_LN0_P	55	AO	LCD MIPI data 0 (+)	
DSI_LN1_N	56	AO	LCD MIPI data 1 (-)	
DSI_LN1_P	57	AO	LCD MIPI data 1 (+)	
DSI_LN2_N	58	AO	LCD MIPI data 2 (-)	
DSI_LN2_P	59	AO	LCD MIPI data 2 (+)	
DSI_LN3_N	60	AO	LCD MIPI data 3 (-)	
DSI_LN3_P	61	AO	LCD MIPI data 3 (+)	
PWM	29	DO	PWM output	

Figure 24: Reference Design of LCM Interface

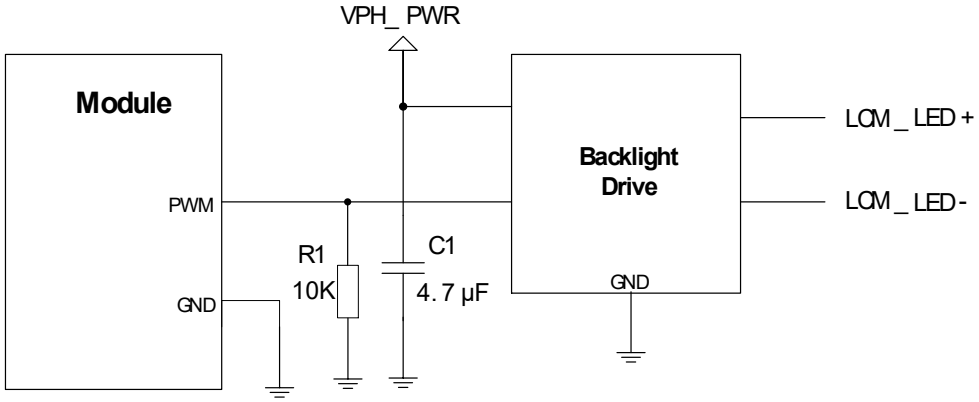


MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID of LCM to the GPIO of the module to distinguish different screens by high/low level detection. But note that the output voltage of LCD_ID should not exceed the voltage range of the GPIOs.

You can design an external backlight driver circuit for LCM according to the actual requirement. PWM can be used for backlight brightness adjustment.

Figure 25: Reference Design of LCM Interface External Backlight Driver



4.13. Camera Interfaces

Based on MIPI_CSI standard, the module supports three cameras (4-lane + 4-lane + 4-lane) or four cameras (4-lane + 4-lane + 2-lane + 1-lane). The maximum data rate is up to 2.5 Gbps/lane. The maximum pixel of the camera is up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor and camera lens specifications.

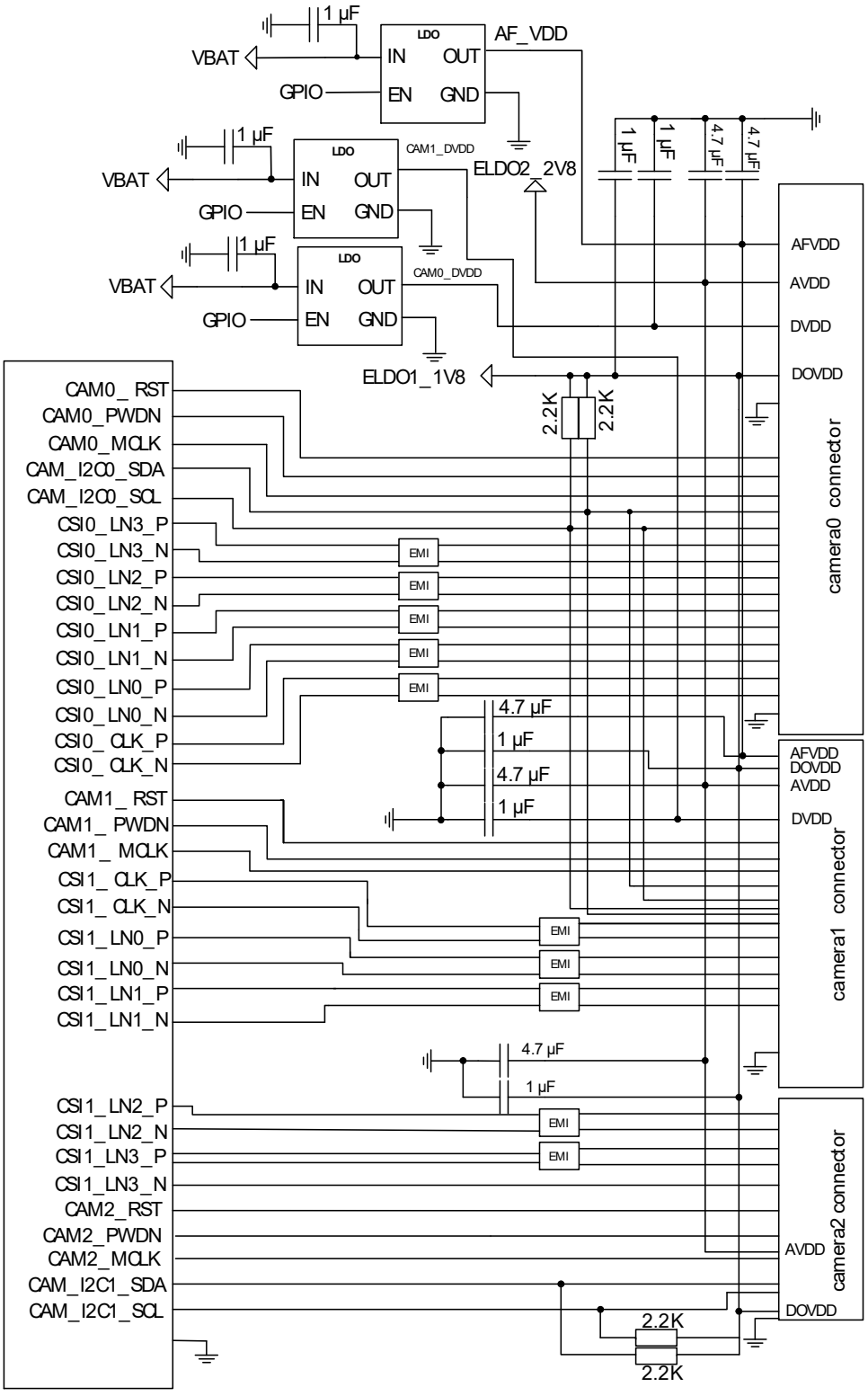
Table 24: Pin Description of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI1_CLK_N	63	AI	MIPI CSI1 clock (-)	
CSI1_CLK_P	64	AI	MIPI CSI1 clock (+)	
CSI1_LN0_N	65	AI	MIPI CSI1 data 0 (-)	
CSI1_LN0_P	66	AI	MIPI CSI1 data 0 (+)	
CSI1_LN1_N	67	AI	MIPI CSI1 data 1 (-)	
CSI1_LN1_P	68	AI	MIPI CSI1 data 1 (+)	
CSI1_LN2_N	72	AI	MIPI CSI1 data 2 (-)	
CSI1_LN2_P	73	AI	MIPI CSI1 data 2 (+)	
CSI1_LN3_N	70	AI	MIPI CSI1 data 3 (-)	
CSI1_LN3_P	71	AI	MIPI CSI1 data 3 (+)	
CSI0_CLK_N	157	AI	MIPI CSI0 clock (-)	
CSI0_CLK_P	196	AI	MIPI CSI0 clock (+)	
CSI0_LN0_N	158	AI	MIPI CSI0 data 0 (-)	85 Ω differential impedance.
CSI0_LN0_P	197	AI	MIPI CSI0 data 0 (+)	
CSI0_LN1_N	159	AI	MIPI CSI0 data 1 (-)	
CSI0_LN1_P	198	AI	MIPI CSI0 data 1 (+)	
CSI0_LN2_N	160	AI	MIPI CSI0 data 2 (-)	
CSI0_LN2_P	199	AI	MIPI CSI0 data 2 (+)	
CSI0_LN3_N	161	AI	MIPI CSI0 data 3 (-)	
CSI0_LN3_P	200	AI	MIPI CSI0 data 3 (+)	
CSI2_CLK_N	257	AI	MIPI CSI2 clock (-)	
CSI2_CLK_P	232	AI	MIPI CSI2 clock (+)	
CSI2_LN0_N	167	AI	MIPI CSI2 data 0 (-)	
CSI2_LN0_P	168	AI	MIPI CSI2 data 0 (+)	
CSI2_LN1_N	169	AI	MIPI CSI2 data 1 (-)	
CSI2_LN1_P	170	AI	MIPI CSI2 data 1 (+)	

CSI2_LN2_N	178	AI	MIPI CSI2 data 2 (-)	
CSI2_LN2_P	179	AI	MIPI CSI2 data 2 (+)	
CSI2_LN3_N	174	AI	MIPI CSI2 data 3 (-)	
CSI2_LN3_P	175	AI	MIPI CSI2 data 3 (+)	
CAM_I2C0_SCL	83	OD	I2C0 clock of camera	The flash driver chip in the module occupies the 0x63 address of the I2C bus. Cannot be used for generic GPIO. An external 2.2 kΩ resistor is required to pull it up to 1.8 V. This pin is dedicated to CAM_I2C and cannot be used for other I2C devices.
CAM_I2C0_SDA	84	OD	I2C0 data of camera	
CAM0_PWDN	80	DO	Power down of camera 0	
CAM1_PWDN	82	DO	Power down of camera 1	
CAM2_PWDN	163	DO	Power down of camera 2	
CAM0_MCLK	74	DO	Master clock of camera 0	
CAM1_MCLK	75	DO	Master clock of camera 1	
CAM2_MCLK	165	DO	Master clock of camera 2	
CAM3_MCLK	33	DO	Master clock of camera 3	
CAM0_RST	79	DO	Reset of camera 0	
CAM1_RST	81	DO	Reset of camera 1	
CAM2_RST	164	DO	Reset of camera 2	
CAM_I2C1_SCL	166	OD	I2C1 clock of camera	An external 2.2 kΩ resistor is required to pull it up to 1.8 V. This pin is dedicated to CAM_I2C and cannot be used for other I2C devices.
CAM_I2C1_SDA	205	OD	I2C1 data of camera	

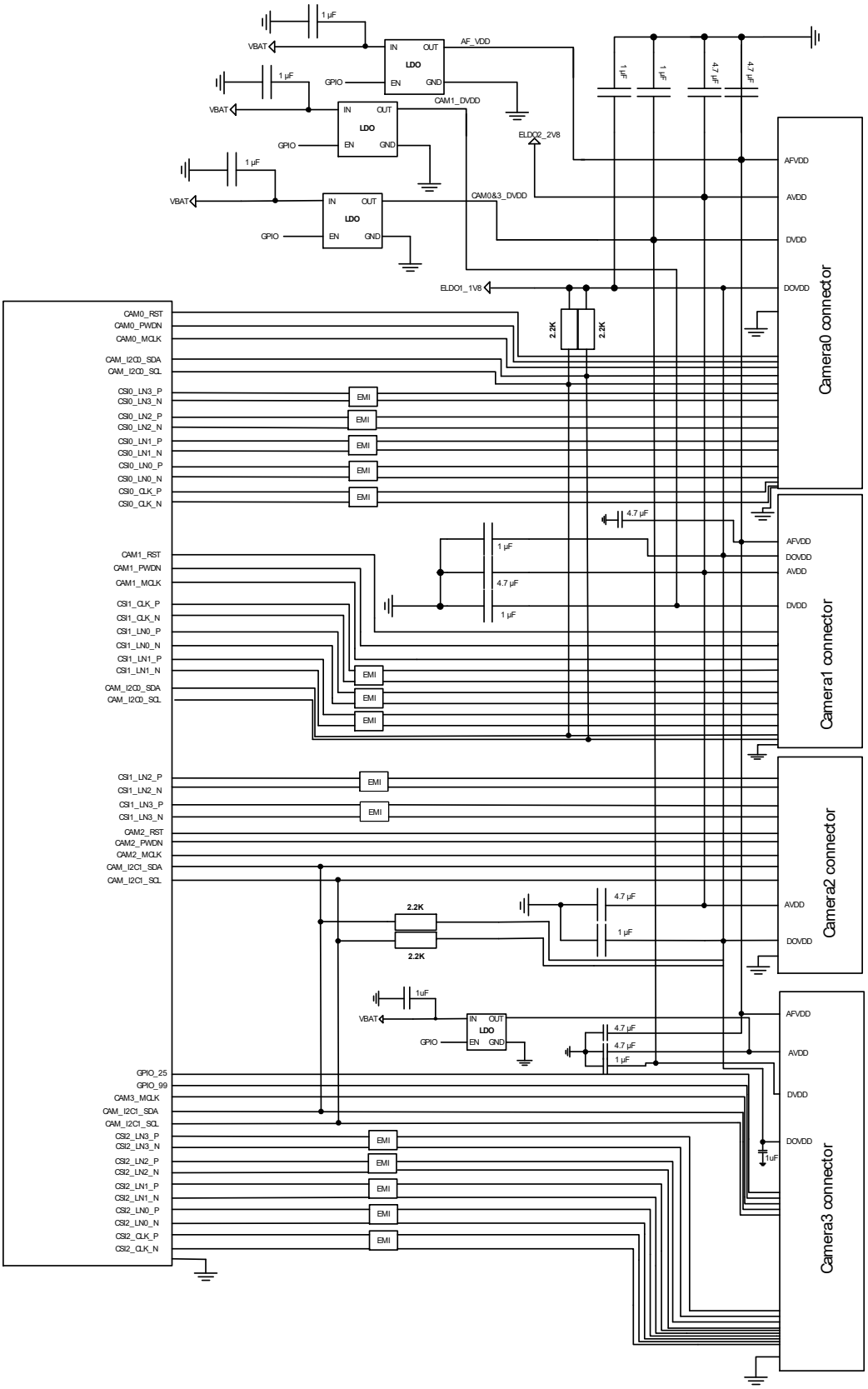
The following is a reference design of triple-camera application:

Figure 26: Reference Design of Triple-Camera Application



The following is a reference design of quad-camera application:

Figure 27: Reference Design of Quad-Camera Application



To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Pay attention to the pin description of LCM and camera interfaces. Different video devices may vary in the definitions of their connectors. Ensure that the devices and the connectors are correctly

connected.

- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps for CSI, and 1.5 Gbps for DSI. The differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same video device, keep all the MIPI traces be of the same length. To avoid crosstalk, a spacing of 1.5 times the trace width is recommended among MIPI signal traces. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following requirements:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 85 Ω ±10 %;
  c) Control intra-lane length matching within 0.7 mm;
  d) Control inter-lane length matching within 1.4 mm.

Table 25: MIPI Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
52	DSI_CLK_N	45.56	0.03
53	DSI_CLK_P	45.59	
54	DSI_LN0_N	45.67	0.10
55	DSI_LN0_P	45.77	
56	DSI_LN1_N	45.76	0.05
57	DSI_LN1_P	45.71	
58	DSI_LN2_N	45.72	0.10
59	DSI_LN2_P	45.82	
60	DSI_LN3_N	45.68	0.12
61	DSI_LN3_P	45.80	
157	CSI0_CLK_N	30.97	0.10
196	CSI0_CLK_P	30.87	
158	CSI0_LN0_N	31.37	0.02
197	CSI0_LN0_P	31.35	
159	CSI0_LN1_N	30.89	0.12
198	CSI0_LN1_P	31.01	
199	CSI0_LN2_P	31.65	0.19
160	CSI0_LN2_N	31.46	

200	CSI0_LN3_P	30.77	0.00
161	CSI0_LN3_N	30.77	
63	CSI1_CLK_N	46.92	0.03
64	CSI1_CLK_P	46.95	
65	CSI1_LN0_N	44.78	0.03
66	CSI1_LN0_P	44.81	
67	CSI1_LN1_N	43.29	0.01
68	CSI1_LN1_P	43.28	
72	CSI1_LN2_N	34.32	0.04
73	CSI1_LN2_P	34.28	
70	CSI1_LN3_N	30.95	0.00
71	CSI1_LN3_P	30.95	
257	CSI2_CLK_N	28.06	0.09
232	CSI2_CLK_P	28.15	
167	CSI2_LN0_N	28.70	0.13
168	CSI2_LN0_P	28.57	
169	CSI2_LN1_N	27.90	0.11
170	CSI2_LN1_P	27.79	
178	CSI2_LN2_N	28.03	0.12
179	CSI2_LN2_P	27.91	
174	CSI2_LN3_N	28.02	0.06
170	CSI2_LN3_P	28.08	

Table 26: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rate	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/lane	76.2	-0.7	< 210

	152.4	-1.15	< 155
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 125
1.5 Gbps/lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/lane	76.2	-1.3	< 170
	152.4	-2.3	< 90
2.5 Gbps/lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 27: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rate	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	3	-0.8	< 280
	6	-1.4	< 210
750 Mbps/lane	3	-1	< 210
	6	-1.5	< 150
1.0 Gbps/lane	3	-1.1	< 200
	6	-1.7	< 100
1.5 Gbps/lane	3	-1.2	< 135
	6	-2.2	< 40
2.1 Gbps/lane	3	-1.6	< 110
	6	-2.8	< 80
2.5 Gbps/lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

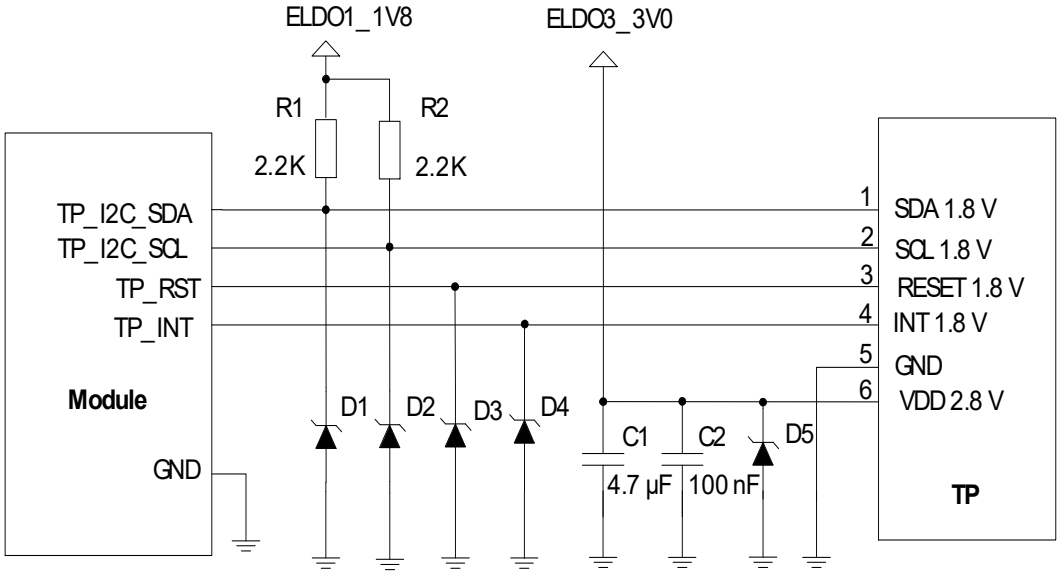
4.14. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins.

Table 28: Pin Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	31	DO	TP reset	Active low.
TP_INT	30	DI	TP interrupt	
TP_I2C_SCL	47	OD	TP I2C clock	External pull-up to 1.8 V is required. These pins can be connected with other I2C peripherals when they are not used for TP interface.
TP_I2C_SDA	48	OD	TP I2C data	

Figure 28: Reference Design of Touch Panel Interface



The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, pressure sensor.

Table 29: Pin Description of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	91	OD	I2C clock for external sensor	An external 2.2 kΩ resistor is required to pull it up to 1.8 V. SENSOR_I2C only supports sensors in the ADSP architecture.
SENSOR_I2C_SDA	92	OD	I2C data for external sensor	
ALPS_INT	107	DI	Light/proximity sensor interrupt	
GYRO_INT	108	DI	Gyroscopic sensor interrupt	
MAG_INT	109	DI	Magnetic sensor interrupt	
ACCEL_INT	110	DI	Acceleration sensor interrupt	

4.15. GPIOs

The module provides twenty-eight GPIOs with the power domain of 1.8 V.

Table 30: Pin Description of GPIOs

Pin Name	Pin No.	I/O	Description
GPIO_106	90	DIO	General-purpose input/output
GPIO_31	97	DIO	General-purpose input/output
GPIO_107	98	DIO	General-purpose input/output
GPIO_25	99	DIO	General-purpose input/output
GPIO_93	100	DIO	General-purpose input/output
GPIO_104	101	DIO	General-purpose input/output
GPIO_105	102	DIO	General-purpose input/output
GPIO_103	103	DIO	General-purpose input/output
GPIO_102	104	DIO	General-purpose input/output
GPIO_99	105	DIO	General-purpose input/output
GPIO_56	106	DIO	General-purpose input/output
GPIO_26	112	DIO	General-purpose input/output
GPIO_68	113	DIO	General-purpose input/output
GPIO_36	115	DIO	General-purpose input/output
GPIO_16	116	DIO	General-purpose input/output
GPIO_17	117	DIO	General-purpose input/output
GPIO_14	118	DIO	General-purpose input/output
GPIO_15	119	DIO	General-purpose input/output
GPIO_83	123	DIO	General-purpose input/output
GPIO_84	124	DIO	General-purpose input/output
GPIO_67	127	DIO	General-purpose input/output
GPIO_112	177	DIO	General-purpose input/output
GPIO_86	182	DIO	General-purpose input/output
GPIO_60	201	DIO	General-purpose input/output
GPIO_101	239	DIO	General-purpose input/output
GPIO_100	264	DIO	General-purpose input/output

GPIO_98	265	DIO	General-purpose input/output
GPIO_111	267	DIO	General-purpose input/output

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

The pin definition is shown below:

Table 31: Pin Definition of Cellular Network Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	87	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DRX	131	AI	Diversity antenna interface	

NOTE

Only passive antennas are supported.

Table 32: Operating Frequency

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B14	788–798	758–768
LTE-FDD B17	704–716	734–746
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–849	859–894

LTE-FDD B66	1710–1780	2110–2200
LTE-FDD B71	663–698	617–652
LTE-TDD B41 (200M)	2496–2690	2496–2690

5.1.2. Transmitting Power

Table 33: RF Transmitting Power

Operating Frequency	Max.	Min.
LTE	23 dBm ±2 dB	< -39 dBm

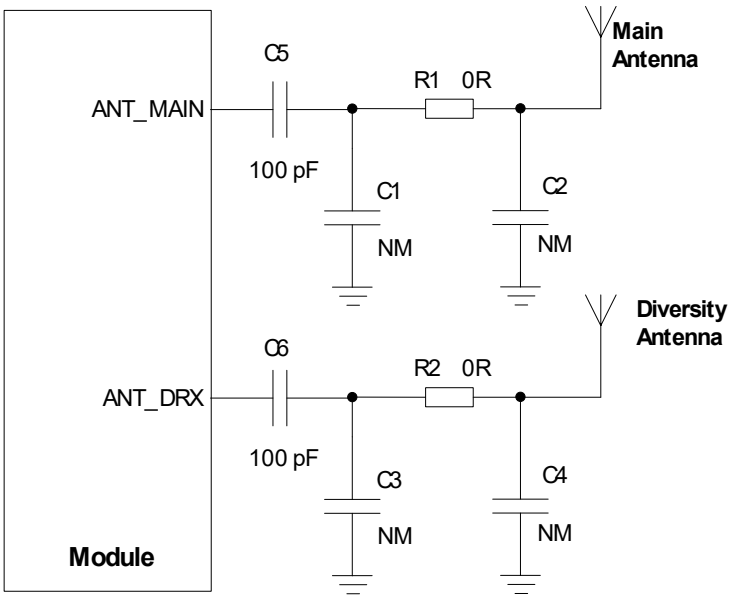
5.1.3. Receiver Sensitivity

Table 34: Conducted RF Receiver Sensitivity (Unit: dBm)

Operating Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	-97.8	-97.1	-100.7	-94.3
LTE-FDD B4 (10 MHz)	-97.1	-97.7	-100.4	-96.3
LTE-FDD B5 (10 MHz)	-98.9	-99.7	-102.5	-94.3
LTE-FDD B7 (10 MHz)	-95.3	-96.6	-99.1	-94.3
LTE-FDD B12 (10 MHz)	-98.1	-98.9	-101.7	-93.3
LTE-FDD B13 (10 MHz)	-97.5	-98.9	-101.5	-93.3
LTE-FDD B14 (10 MHz)	-97.6	-98.8	-101.3	-93.3
LTE-FDD B17 (10 MHz)	-98.1	-99.1	-101.8	-93.3
LTE-FDD B25 (10 MHz)	-97.6	-96.9	-100.5	-92.8
LTE-FDD B26 (10 MHz)	-98.8	-99.6	-102.4	-93.8
LTE-FDD B66 (10 MHz)	-96.9	-97.4	-100.1	-95.8
LTE-FDD B71 (10 MHz)	-98.8	-98.2	-101.6	-93.5
LTE-TDD B41 (10 MHz)	-96.3	-96.3	-99.4	-94.3

5.1.4. Reference Design

Figure 29: Reference Design of Main Antenna and Diversity Antenna



NOTE

1. To improve receiver sensitivity, ensure that the spacing among antennas is appropriate.
2. Use a dual L-type circuit for all the antenna interfaces for better cellular performance and easy debugging.
3. Capacitors(C1/C2/C3/C4) are not mounted by default.
4. Place the dual L-type components (C5 & C1 & R1 & C2, C6 & C3 & R2 & C4) to antennas as close as possible.
5. Notes on C5 and C6:
   1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C5 and C6.
      b) If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.

5.2. GNSS (Optional)

The module integrates the IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems, including GPS, GLONASS, BDS, Galileo, QZSS and SBAS. With an embedded LNA, the positioning accuracy of the module can be greatly improved.

5.2.1. Antenna Interface & Frequency Bands

The following table lists the GNSS performance of the module in conduction mode:

Table 35: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment

ANT_GNSS	121	AI	GNSS antenna interface	50 Ω characteristic impedance.

Table 36: GNSS Frequency (Unit: MHz)

GNSS Constellation Type	Operating Frequency
GPS	1575.42 ±1.023 (L1)
GLONASS	1597.5–1605.8 (L1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1)
QZSS	1575.42 ±1.023 (L1)
SBAS	1575.42 ±1.023 (L1)

5.2.2. GNSS Performance

Table 37: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition		TBD	
	Tracking		TBD	
TTFF	Cold start @ open sky	Autonomous	TBD	s
		XTRA start	TBD	
	Warm start @ open sky	Autonomous	TBD	
		XTRA start	TBD	
	Hot start @ open sky	Autonomous	TBD	
		XTRA start	TBD	
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

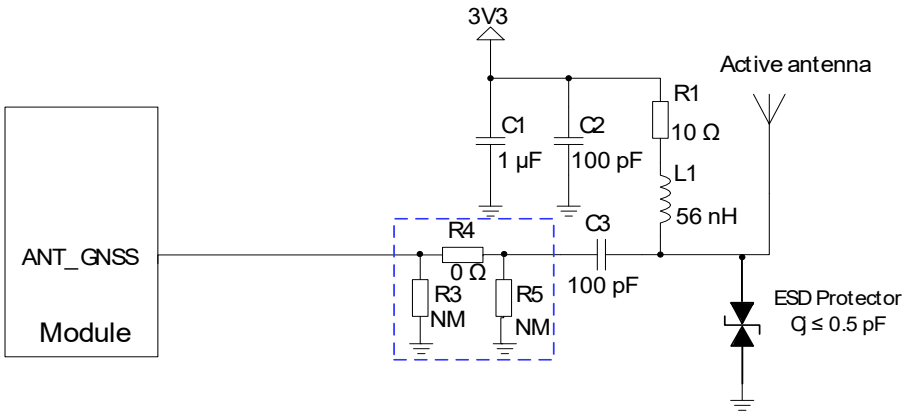
1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56-nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies, it is recommended to use a high-performance LDO:

Figure 30: Reference Design of Active Antenna



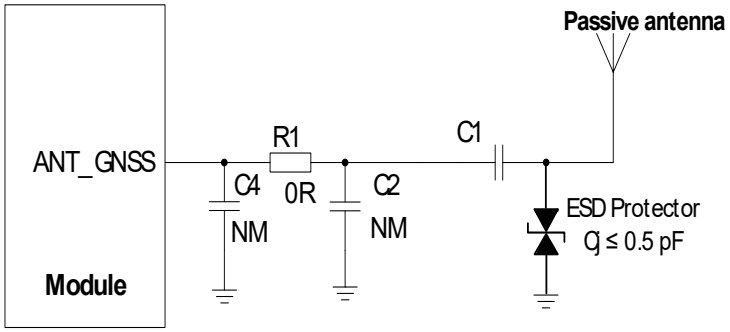
NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.2.3.2. Passive Antenna

You can also use passive ceramic antennas or other types of passive antennas:

Figure 31: Reference Design of Passive Antenna



NOTE

1. It is not recommended to add an external LNA when using a passive antenna.
2. Notes on C1:

1) If there is DC power at the antenna port, place capacitor on C1 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
2) If there is no DC power in the peripheral design:
   a) Do not reserve C1.
   b) If C1 has already been reserved, they should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.

5.2.3.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. In order to avoid this, follow the reference design rules as below:

- Maximize the distance between the GNSS part and the other RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal traces and RF components should be placed far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection components for the antenna interface. Only components with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Keep the impedance of either feeder line or PCB trace as 50 Ω, and keep the trace length as short as possible.

5.3. Wi-Fi & Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 38: Pin Description of Wi-Fi & Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_WIFI/BT	77	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω characteristic impedance.

Table 39: Wi-Fi & Bluetooth Frequency (Unit: MHz)

Type	Frequency
Wi-Fi 802.11	2402–2482 5180–5825
Bluetooth	2402–2480

5.3.1. Wi-Fi Overview

The module supports 2.4 GHz & 5 GHz dual-band Wi-Fi wireless communication based on Wi-Fi 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 150 Mbps for 2.4 GHz, and 433 Mbps for 5 GHz. It supports following features:

- Wake-on-WLAN (WoWLAN)
- ad hoc mode
- WAPI SMS4 hardware encryption
- AP and STA modes
- Wi-Fi Direct
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 8: VHT20
- MCS 0–MCS 9: VHT40 and VHT80

Table 40: Wi-Fi Transmitting Performance

Operating Frequency	Modulation	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB
	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n @ HT20	MCS 0	15 dBm ±2.5 dB
	802.11n @ HT20	MCS 7	13 dBm ±2.5 dB
	802.11n @ HT40	MCS 0	15 dBm ±2.5 dB
	802.11n @ HT40	MCS 7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	15 dBm ±2.5 dB
	802.11a	54 Mbps	13 dBm ±2.5 dB
	802.11n @ HT20	MCS 0	15 dBm ±2.5 dB
	802.11n @ HT20	MCS 7	13 dBm ±2.5 dB
	802.11n @ HT40	MCS 0	15 dBm ±2.5 dB
	802.11n @ HT40	MCS 7	13 dBm ±2.5 dB
	802.11ac @ VHT20	MCS 0	14 dBm ±2.5 dB
	802.11ac @ VHT20	MCS 8	13 dBm ±2.5 dB
	802.11ac @ VHT40	MCS 0	14 dBm ±2.5 dB
	802.11ac @ VHT40	MCS 9	12 dBm ±2.5 dB
	802.11ac @ VHT80	MCS 0	13 dBm ±2.5 dB

	802.11ac @ VHT80	MCS 9	12 dBm ±2.5 dB

Table 41: Wi-Fi Receiving Performance

Operating Frequency	Modulation	Rate	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	TBD
	802.11b	11 Mbps	TBD
	802.11g	6 Mbps	TBD
	802.11g	54 Mbps	TBD
	802.11n @ HT20	MCS 0	TBD
	802.11n @ HT20	MCS 7	TBD
	802.11n @ HT40	MCS 0	TBD
	802.11n @ HT40	MCS 7	TBD
5 GHz	802.11a	6 Mbps	TBD
	802.11a	54 Mbps	TBD
	802.11n @ HT20	MCS 0	TBD
	802.11n @ HT20	MCS 7	TBD
	802.11n @ HT40	MCS 0	TBD
	802.11n @ HT40	MCS 7	TBD
	802.11ac @ VHT20	MCS 0	TBD
	802.11ac @ VHT20	MCS 8	TBD
	802.11ac @ VHT40	MCS 0	TBD
	802.11ac @ VHT40	MCS 9	TBD
	802.11ac @ VHT80	MCS 0	TBD
	802.11ac @ VHT80	MCS 9	TBD

NOTE

The module complies with the IEEE specifications.

5.3.2. Bluetooth Overview

Models with built-in Bluetooth function provide Bluetooth antenna interface. The module supports Bluetooth 5.0 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulations. It supports following features:

- Up to 7-lane wireless connections.
- Up to 3.5 Piconets simultaneously.
- One SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 42: Bluetooth Data Rates and Versions

Version	Data Rate (Mbit/s)	Maximum Application Throughput
1.2	1	> 80 kbit/s
2.0 + EDR	3	> 80 kbit/s
3.0 + HS	24	Refer to 3.0 + HS
4.0	24	Refer to 4.0 LE
5.0	48	Refer to 5.0 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016

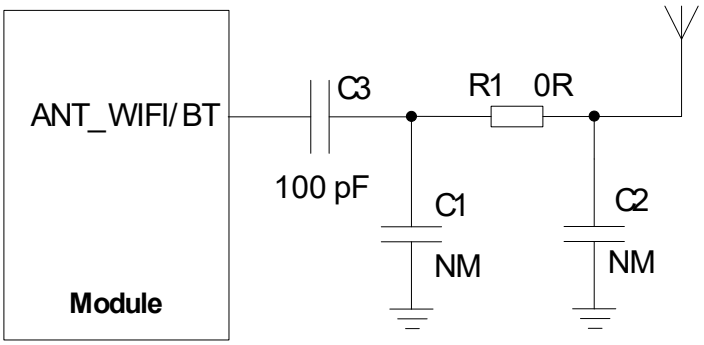
Table 43: Bluetooth Transmitting and Receiving Performance (Unit: dBm)

Condition (VBAT = 3.8 V; Temp.: 25 °C)	Transmitting power	Receiver sensitivity
BR	8 ±2.5 dB	TBD
EDR (π/4-DQPSK)	6 ±2.5 dB	TBD
EDR (8-DQPSK)	6 ±2.5 dB	TBD
BLE (1 Mbps)	TBD	TBD
BLE (2 Mbps)	TBD	TBD

5.3.3. Reference Design

A reference design of Wi-Fi & Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1.

Figure 32: Reference Design for Wi-Fi/Bluetooth Antenna



NOTE

Notes on C3:

1) If there is DC power at the antenna port, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
2) If there is no DC power in the peripheral design:
   a) Do not reserve C3.
   b) If C3 has already been reserved, they should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.

5.4. RF Routing Guidelines

When designing PCB, characteristic impedance of all RF traces should be controlled to 50 Ω. Generally, the impedance of RF traces is determined by materials' dielectric constant, trace width (W), spacing between RF traces and grounds (S) and height from the reference ground to the signal layer (H). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures when characteristic impedance of RF traces is controlled to 50 Ω.

Figure 33: Microstrip Design on a 2-layer PCB

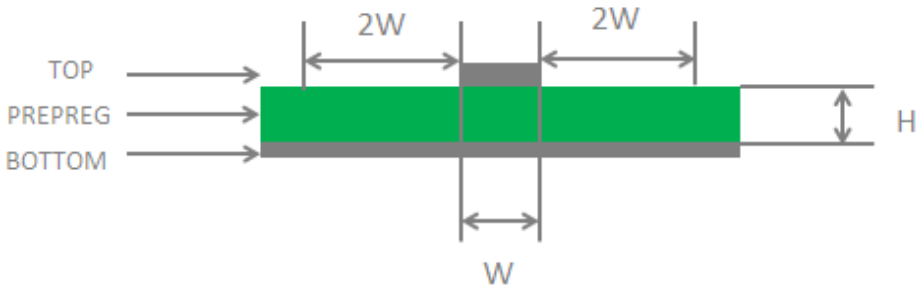


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

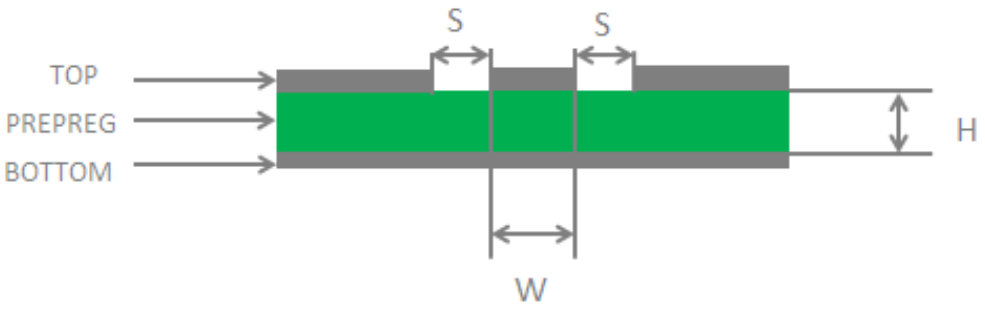


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

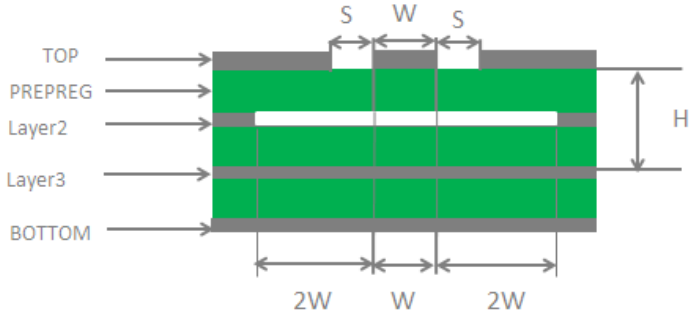
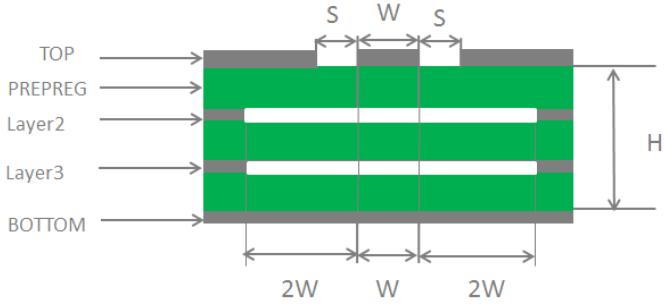


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- Clearance between RF pins and RF connector should be as short as possible, and all right-angle (90°) traces should be changed to the ones with the angle of 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground can improve RF performance. The clearance between ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document 3***.

5.5. Requirements for Antenna Design

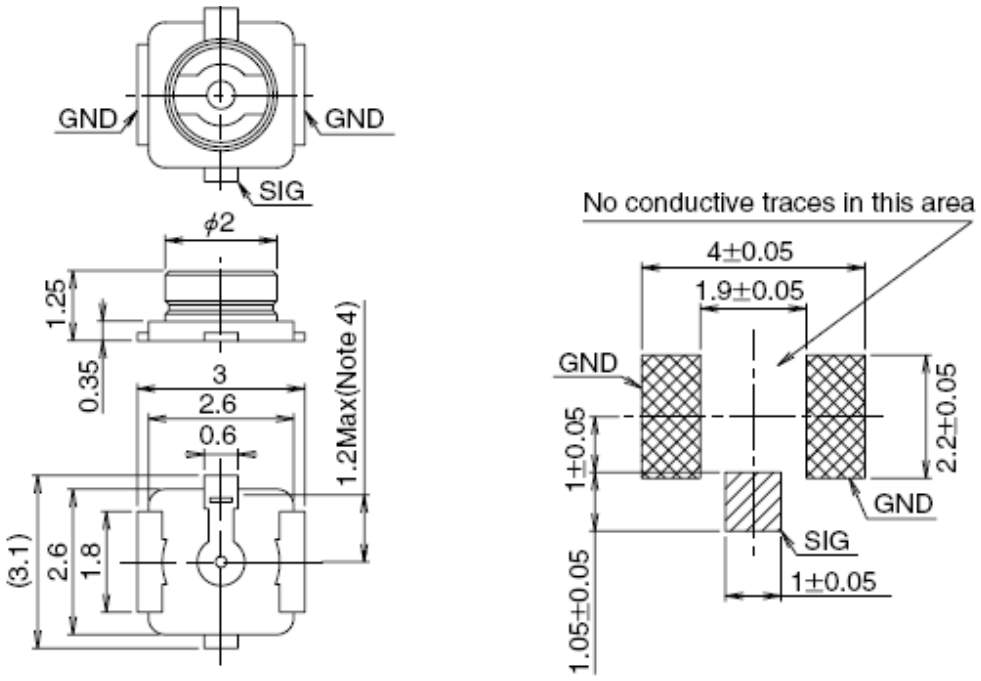
Table 44: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	**Frequency range:** ● L1: 1559–1609 MHz RHCP or linear polarization VSWR: ≤ 2 (typ.)
	For passive antenna application: Passive antenna gain: > 0 dBi
	For active antenna application: Active antenna noise coefficient: < 1.5 dB (typ.) Active antenna embedded LNA gain: < 17 dB (typ.)
Cellular Network	VSWR: ≤ 2 Gain: 1 dBi Max. input power: 50 W Input impedance: 50 Ω Vertical polarization **Cable insertion loss:** ● < 1 dB: LB (< 1 GHz) ● < 1.5 dB: MB (1–2.3 GHz) ● < 2 dB: HB (> 2.3 GHz)
Wi-Fi & Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max. input power: 50 W Input impedance: 50 Ω Vertical polarization Cable insertion loss: < 1 dB

5.6. RF Connector Recommendation

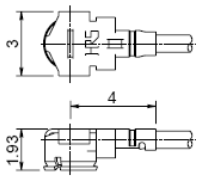
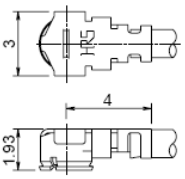
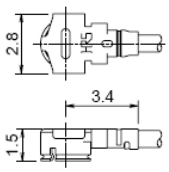
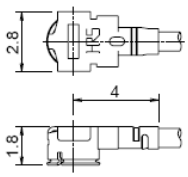
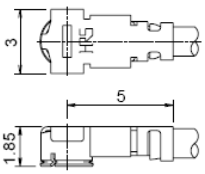
If you use an RF connector for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

Figure 37: Dimensions of the Receptacle (Unit: mm)



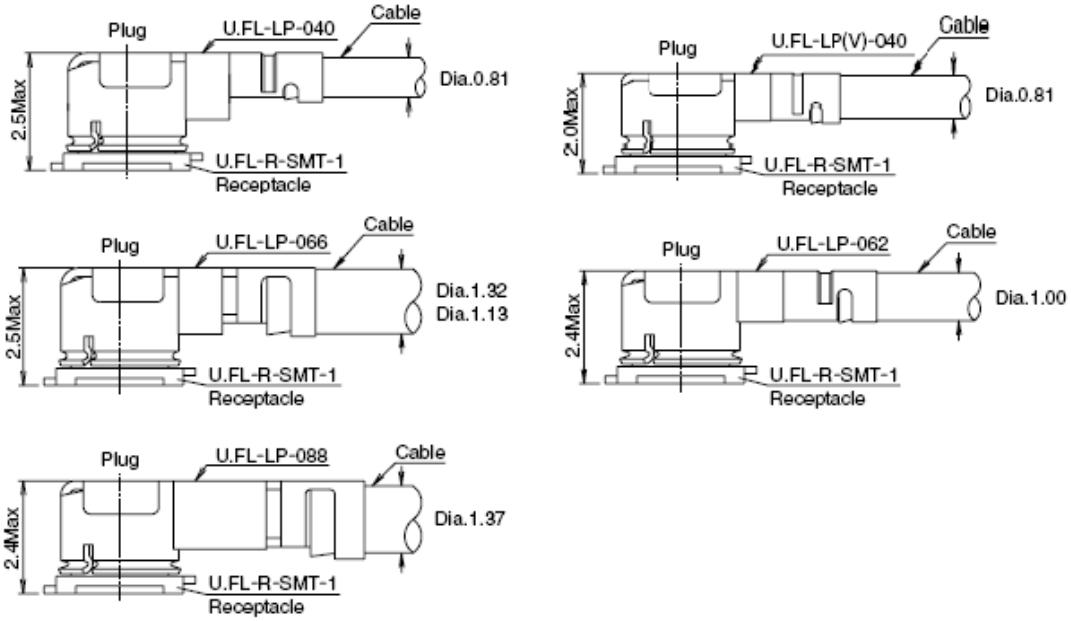
U.FL-LP series connectors listed in the following figure can be used to match the U.FL-R-SMT.

Figure 38: Specifications of Mated Plugs (Unit: mm)

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated connectors.

Figure 39: Space Factor of Mated Connectors (Unit: mm)



Please visit http://www.hirose.com for more information.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 45: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	-0.3	4.75	V
Voltage at USB_VBUS	-0.3	16	V
Voltage at digital pins	-0.3	2.2	V
Current at VBAT	-	3	A

6.2. Power Supply Ratings

Table 46: Module Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values	3.55	3.8	4.4	V
I_{VBAT}	Peak supply current	At maximum power control level	-	1.8	3.0	A
USB_VBUS	USB connection detection	-	4.0	5.0	21	V
VRTC	Supply voltage of the backup battery	-	2.0	3.0	3.25	V

6.3. Power consumption

Table 47: Power Consumption

Mode	Condition	Typ.	Unit
Power Down Mode	Power off	100	μA
Sleep state	Screen off	4.6	mA
LTE-FDD Sleep State Power supply	LTE-FDD PF = 32	TBD	mA

(USB disconnected)	LTE-FDD PF = 64	TBD	mA
	LTE-FDD PF = 128	TBD	mA
	LTE-FDD PF = 256	TBD	mA
LTE-TDD Sleep State Power supply (USB disconnected)	LTE-TDD PF = 32	TBD	mA
	LTE-TDD PF = 64	TBD	mA
	LTE-TDD PF = 128	TBD	mA
	LTE-TDD PF = 256	TBD	mA
LTE data transmission	LTE-FDD B2 @ max. power	TBD	mA
	LTE-FDD B4 @ max. power	TBD	mA
	LTE-FDD B5 @ max. power	TBD	mA
	LTE-FDD B7 @ max. power	TBD	mA
	LTE-FDD B12 @ max. power	TBD	mA
	LTE-FDD B13 @ max. power	TBD	mA
	LTE-FDD B14 @ max. power	TBD	mA
	LTE-FDD B17 @ max. power	TBD	mA
	LTE-FDD B25 @ max. power	TBD	mA
	LTE-FDD B26 @ max. power	TBD	mA
	LTE-FDD B66 @ max. power	TBD	mA
	LTE-FDD B71 @ max. power	TBD	mA
	LTE-TDD B41 @ max. power	TBD	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact NetPrisma Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 48: LDO9A_1V8 I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.

V_{IH}	High-level Input Voltage	1.17	2.09
V_{IL}	Low-level Input Voltage	-0.3	0.63
V_{OH}	High-level output voltage	1.35	1.8
V_{OL}	Low-level output voltage	0	0.45

Table 49: SD Card Interface High-Voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level Input Voltage	1.84	3.25
V_{IL}	Low-level Input Voltage	-0.3	0.74
V_{OH}	High-level output voltage	2.21	2.95
V_{OL}	Low-level output voltage	0	0.37

Table 50: SD Card Interface Low-Voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level Input Voltage	1.27	2
V_{IL}	Low-level Input Voltage	-0.3	0.58
V_{OH}	High-level output voltage	1.4	1.8
V_{OL}	Low-level output voltage	0	0.45

Table 51: (U)SIM Interface High-/Low-Voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	2.065	3.25
V_{IL}	Low-level input voltage	-0.3	0.59
V_{OH}	High-level output voltage	2.36	2.95
V_{OL}	Low-level output voltage	0	0.4

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the

development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 52: ESD Characteristics (Temperature: 25 °C–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
Antenna Interfaces	±5	±10
Other Interfaces	±0.25	±1

6.6. Operating and Storage Temperatures

Table 53: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Normal Operating Temperature [3]	-35	+25	+75
Storage Temperature	-40	-	+90

[3] Within the operating temperature range, the module meets 3GPP specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

Figure 40: Top and Side Dimensions

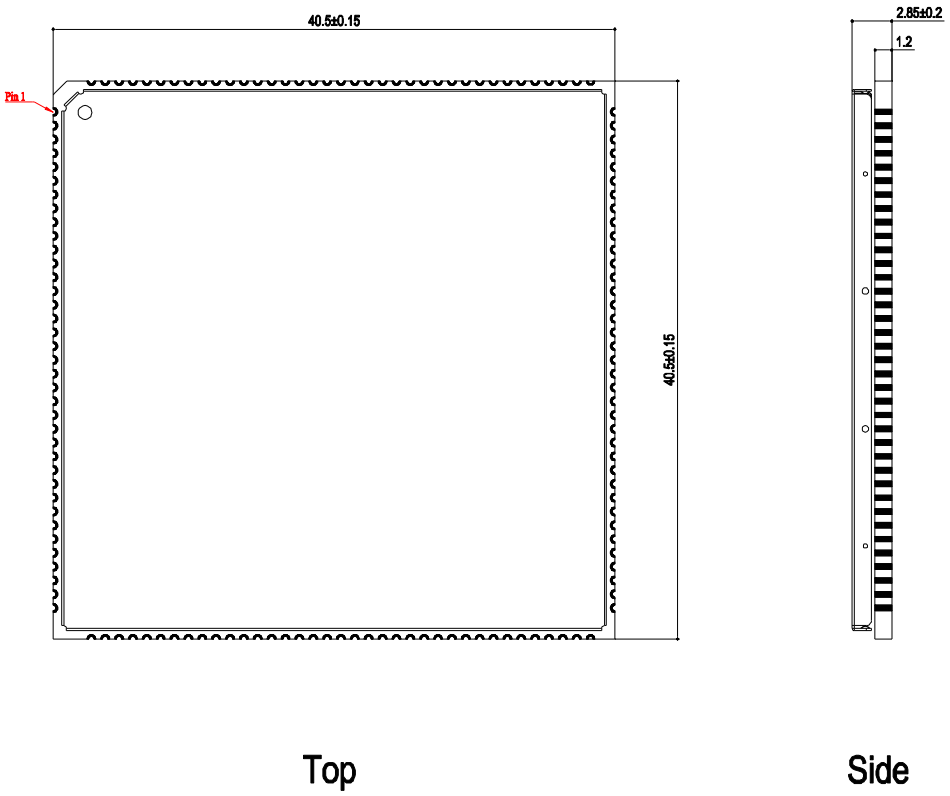
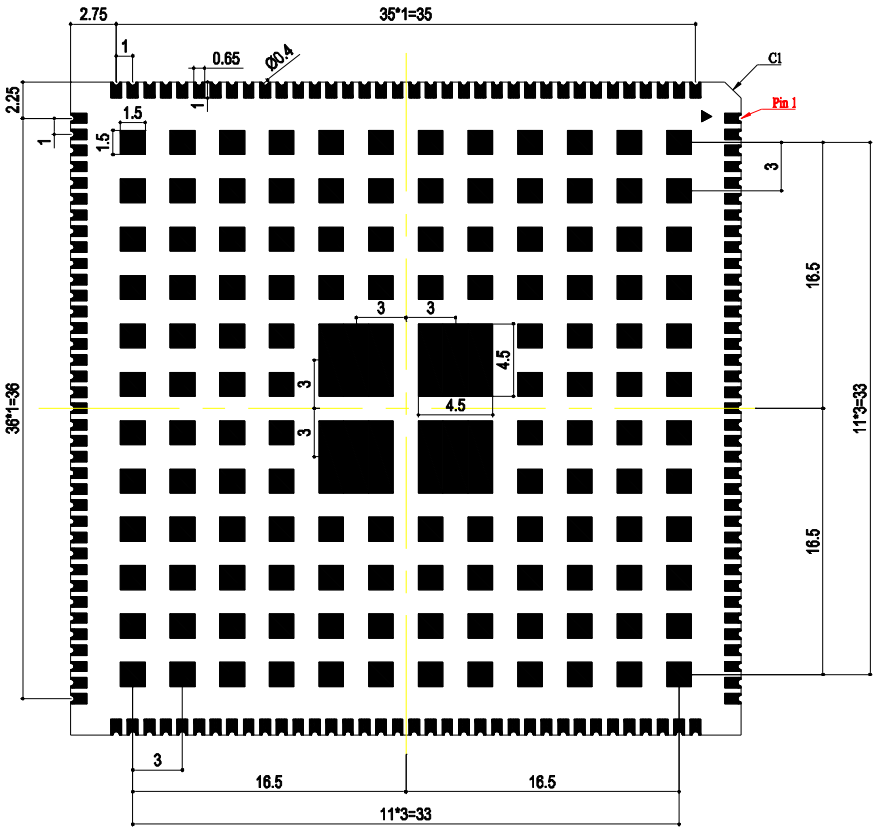


Figure 41: Bottom Dimensions (Bottom View)



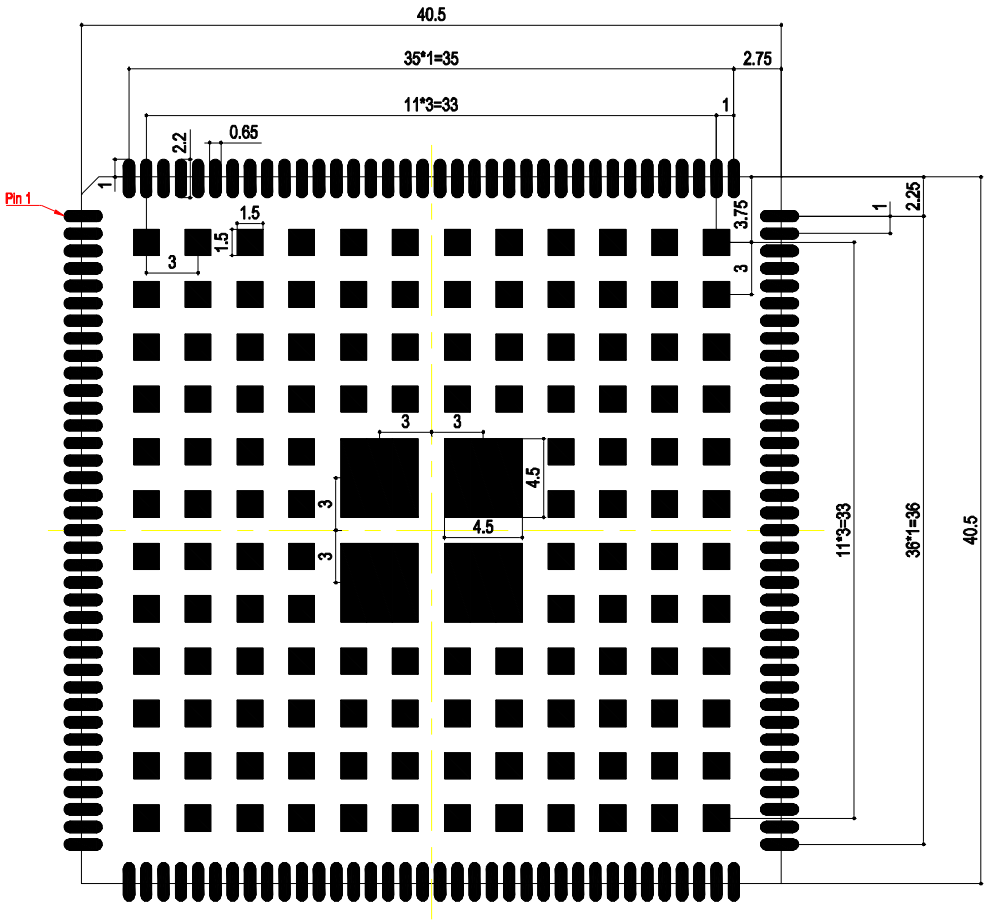
Bot

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

Figure 42: Recommended Footprint

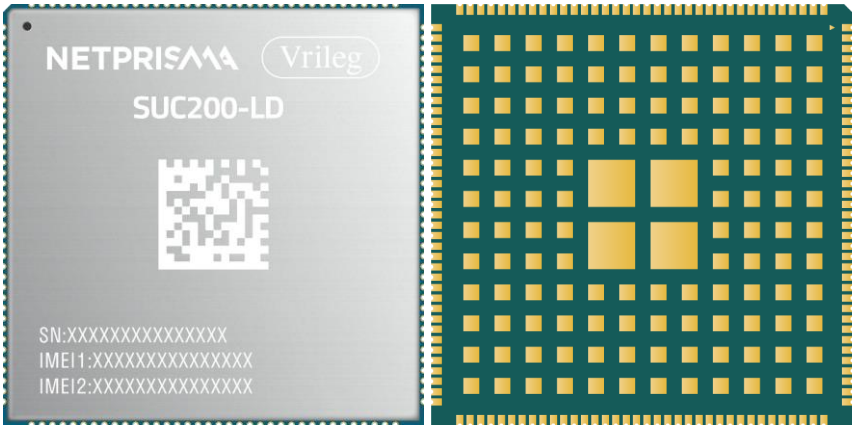


NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 43: Top and Bottom Views



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [4] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document 4***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB

[4] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to IPC/JEDEC J-STD-033. And do not unpack the modules in large quantities until they are ready for soldering.

has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 44: Recommended Reflow Soldering Thermal Profile

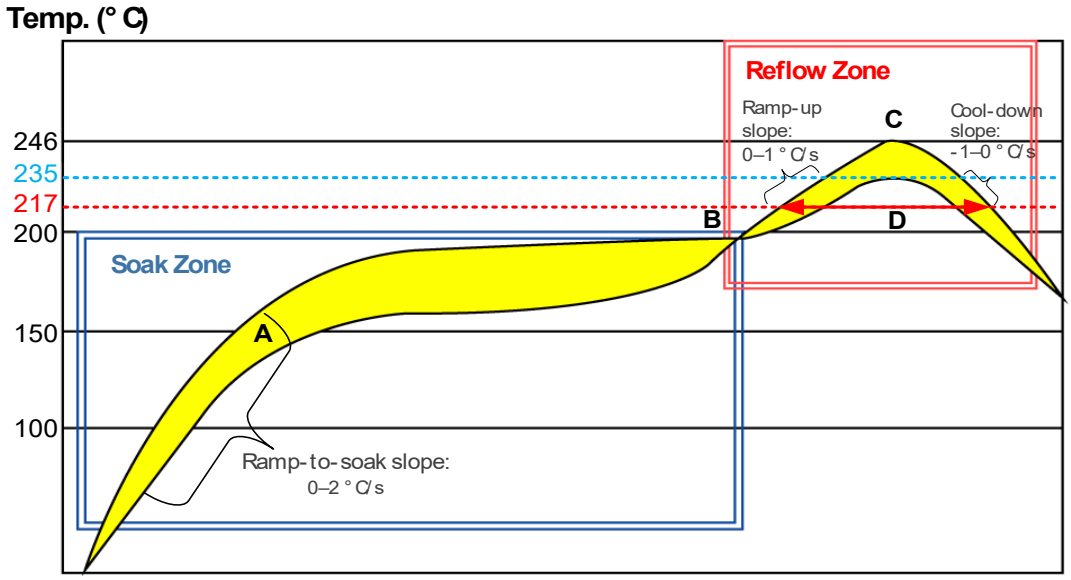


Table 54: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max. temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, an excessive temperature change may cause excessive thermal

deformation of the metal shielding frame and cover. Thus, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.

3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document 5***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 45: Carrier Tape Dimension Drawing (Unit: mm)

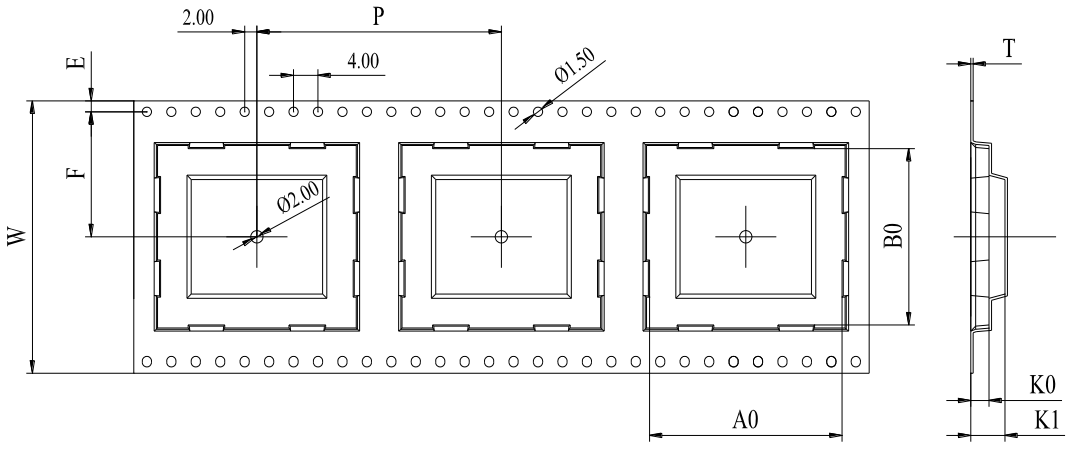


Table 55: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	41.2	41.2	4	4.6	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 46: Plastic Reel Dimension Drawing

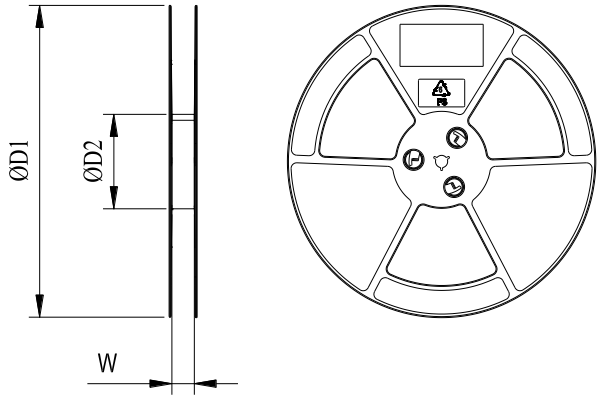
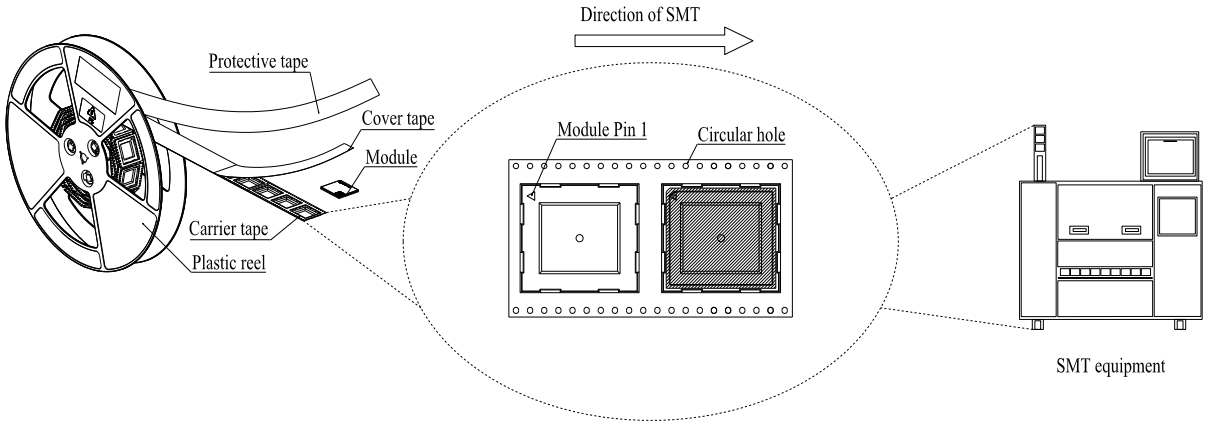


Table 56: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

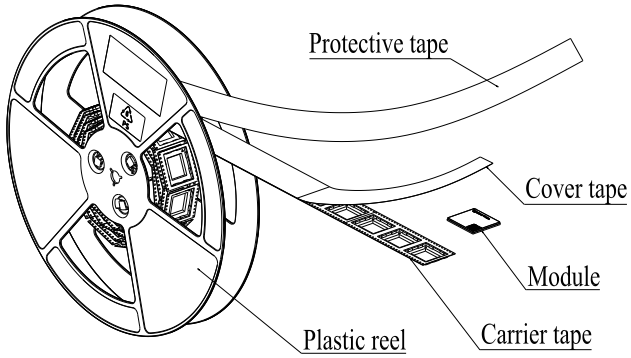
8.3.3. Mounting Direction

Figure 47: Mounting Direction



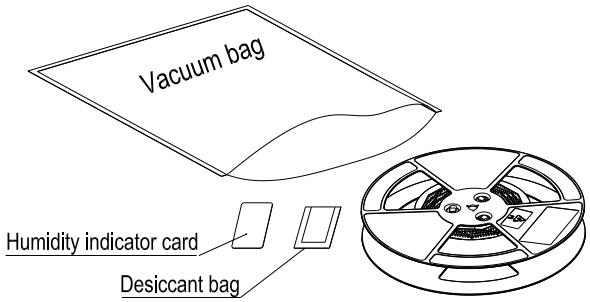
8.3.4. Packaging Process

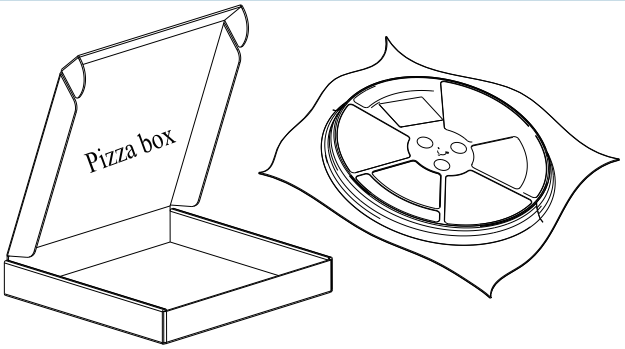
Figure 48: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

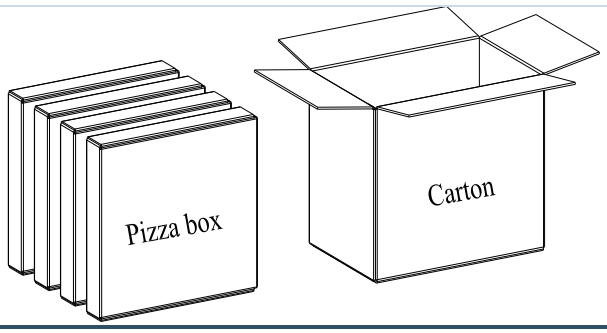
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.



9 Appendix References

Table 57: Related Documents

Document Name
1. NetPrisma-Smart-EVB-G5-User-Guide
2. NetPrisma-SUC200-LD-GPIO-Configuration
3. NetPrisma-RF-Layout-Application-Note
4. NetPrisma-Module-Stencil-Design-Requirements
5. NetPrisma-Module-SMT-Application-Note

Table 58: List of Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
ADSP	Audio Digital Signal Processor
ALS	Ambient Light Sensor
AMR-NB	Adaptive Multi Rate-Narrow Band Speech Codec
AMR-WB	Adaptive Multi-Rate Wideband
AP	Access Point
ARM	Advanced RISC Machine
BDS	BeiDou Navigation Satellite System
BLE	Bluetooth Low Energy
bps	Bits per Second
BR	Basic Rate
CDMA	Code Division Multiple Access
CEP	Circular Error Probable
CPE	Customer-Premise Equipment
CS	Coding Scheme

CSD	Circuit Switched Data
CSI	Camera Serial Interface
CTS	Clear To Send
DC	Dual Carrier
DC-HSPA+	Dual Carrier High Speed Packet Access+
DCS	Digital Cellular System
DL	Downlink
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Reference Phase Shift Keying
DRX	Discontinuous Reception
DSI	Display Serial Interface
DSP	Digital Signal Processor
ECM	Electret Condenser Microphone
EDGE	Enhanced Data Rate for GSM Evolution
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EGSM	Extended GSM
eMMC	Embedded Multimedia Card
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
EVDO	Evolution-Data Optimized
EVRC	Enhanced Variable Rate Codec
FDD	Frequency Division Duplex
FPC	Flexible Printed Circuit
fps	Frame per Second

FR	Full Rate
Galileo	Galileo Satellite Navigation System (EU)
GFSK	Gaussian Frequency Shift Keying
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GRFC	Generic RF control
GSM	Global System for Mobile Communications
HR	Half Rate
HS	High Speed
HSDPA	High Speed Downlink Packet Access
HSPA+	High-Speed Packet Access+
HSUPA	High Speed Uplink Packet Access
HT	High Throughput
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IMT-2000	International Mobile Telecommunications for the year 2000
I/O	Input/Output
$I_I$max	Maximum Input Load Current
$I_O$max	Maximum Output Load Current
ISP	Image Signal Processor/Internet Service Provider
LCC	Leadless Chip Carrier

LCD	Liquid Crystal Display
LCM	LCD Module
LDO	Low Dropout Regulator
LE	Low Energy
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low-Power Double Data Rate
LTE	Long-Term Evolution
M2M	Machine to Machine
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MEMS	Micro-Electro-Mechanical System
MIC	Microphone
MIMO	Multi-Input Multi-Output / Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSL	Moisture Sensitivity Levels
NFC	Near Field Communication
NTC	Negative Temperature Coefficient
OTA	Over-the-Air Upgrade
OTG	On-The-Go
OTP	One Time Programmable
PA	Power Amplifier
PAM	Power Amplifier Module
PC	Personal Computer
PCB	Printed Circuit Board
PCL	Power Control Level

PCS	Personal Communication Service
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMU	Power Management Unit
POS	Point of Sale
PWM	Pulse Width Modulation
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SCO	Synchronous Connection Oriented
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mounting Device
SMS	Short Message Service
SMT	Surface Mount Technology
STA	Station
TDD	Time-Division Duplex
TP	Touch Panel
TTFF	Time to First Fix

TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
VHT	Very High Throughput
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
$V_O$max	Maximum Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
Vrms	Root Mean Square Voltage
VSWR	Voltage Standing Wave Ratio
WAPI	WLAN Authentication and Privacy Infrastructure
WCDMA	Wideband Code Division Multiple Access
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network

FCC ID: 2BEY3SUC200LDA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA INC. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: 2BEY3SUC200LDA”
“Contains IC: 32052-SUC200LDA”
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Band	Antenna Type	Max Gain Allowed (dBi)
LTE B2	External	8.00
LTE B4		5.00
LTE B5		13.41
LTE B7		8.00
LTE B12		11.92
LTE B13		11.92
LTE B14		11.92
LTE B17		11.92
LTE B25		8.00
LTE B26		13.36
LTE B41		8.00
LTE B66		5.00
LTE B71		11.92
Bluetooth		0.47
WiFi 2.4G		0.47
WiFi 5150-5250MHz		-0.67
WiFi 5250-5350MHz		-0.19
WiFi 5470-5725MHz		1.28
WiFi 5725-5850MHz		1.1

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 15 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC: 32052-SUC200LDA

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 32052-SUC200LDA".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne

peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 32052-SUC200LDA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Document History

Revision	Date	Changes
A	2025-02-21	The first revision.

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