LUH33-LDX

Hardware Design

Rev.A– Preview – 2025-02-11

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1 Introduction

This document defines LUH33-LDX and describes its air interfaces and hardware interfaces which are connected with your applications

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate its application in different fields, relevant reference design is also provided for your reference. Associated with application note and user guide, you can use LUH33-LDX to design and set up mobile applications easily.

1.1. Text Conventions

Table 1: Text Conventions

NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

LUH33-LDX is an LTE/WCDMA wireless communication module featuring Rx-diversity. It supports data connectivity across LTE-FDD and WCDMA networks. Additionally, it provides GNSS [1] to meet the needs of your specific applications.

The following table shows the frequency bands and GNSS function of the module.

Table 2: Supported Frequency Bands and Function

Module	LTE Band	WCDMA Band	GNSS [1]
LUH33-LDX	FDD: B2/B4/B5/B12/B13/B14/B66/B71	B2/B4/B5	GPS, GLONASS, BDS, Galileo, QZSS

It is an SMD-type module designed for integration into applications using its 144 pins, which include 80 LCC pins and 64 LGA pins. With its compact size of 29.0 mm × 32.0 mm × 2.4 mm, the module is well-suited for most M2M and IoT applications.

2.1. Key Features

The table provides detailed information about the features of the module.

Table 3: Key Features

Feature	Description
Power Supply	● Operating voltage range: 3.3–4.3 V ● Nominal supply voltage: 3.8 V
Transmitting Power	● WCDMA bands: Class 3 (23 dBm ±2 dB) ● LTE bands: Class 3 (23 dBm ±2 dB)
LTE Features	● Support non-CA Cat 4 FDD ● RF bandwidth: 1.4/3/5/10/15/20 MHz ● MIMO supported in downlink ● DL modulations: QPSK, 16QAM, 64QAM ● UL modulations: QPSK, 16QAM ● LTE-FDD: Max. 150 Mbps (DL)/Max. 50 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● DL modulations: QPSK, 16QAM, 64QAM ● UL modulations: QPSK ● DC-HSDPA: Max 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/Max. 384 kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/FTP/FTPS/HTTP/HTTPS/NTP/PING/QMI/NITZ/SMTP/SSL/MQTT/FILE/CMUX/SMTPS/MMS protocols ● Support PAP and CHAP protocols for PPP connections
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default

[1] GNSS function is optional.

(U)SIM Interface	Support 1.8 V and 3.0 V (U)SIM cards
Audio Features	● Support one digital audio interface: PCM interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB
PCM Interface	● Support audio with an external codec ● 16-bit linear data format ● Long and short frame synchronization ● Master and slave modes (must be master for long frame sync)
USB Interface	● USB 2.0 compliant (slave mode, up to 480 Mbps) ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade ● Support USB serial drivers for: Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate up to 921600 bps (default: 115200 bps) ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	● Support 10/100/1000 Mbps Ethernet mode ● Support Max. 150 Mbps (DL)/50 Mbps (UL) for 4G network
WLAN and Bluetooth Application Interfaces	● Support an SDIO 3.0 interface for WLAN function ● Support UART and PCM interfaces for Bluetooth function
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features (Optional)	● Protocol: NMEA 0183 ● Default data update rate: 1 Hz by default ● Supports AGNSS. For more details, see ***document 1***
AT Commands	Compliant with *3GPP TS 27.007*, *3GPP TS 27.005*
Network Indication	NET_MODE and NET_STATUS indicate network connectivity status
Antenna Interfaces	● Main antenna interface: ANT_MAIN ● Diversity antenna interface: ANT_DIV ● GNSS antenna interface: ANT_GNSS
Physical Characteristics	● Size: (29.0 ±0.15) mm × (32.0 ±0.15) mm × (2.4 ±0.2) mm ● Package: LCC + LGA ● Weight: approx. 4.9 g
Temperature Ranges	● Operating temperature: -35 to +75 °C [2] ● Extended temperature: -40 to +85 °C [3] ● Storage temperature: -40 to +90 °C
Firmware Upgrade	USB 2.0 interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[2] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[3] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.2. EVB Kit

NetPrisma supplies an evaluation board (UMTS&LTE EVB) with accessories to develop and test the module. For more details, see ***document 2***

3 Application Interfaces

3.1. General Description

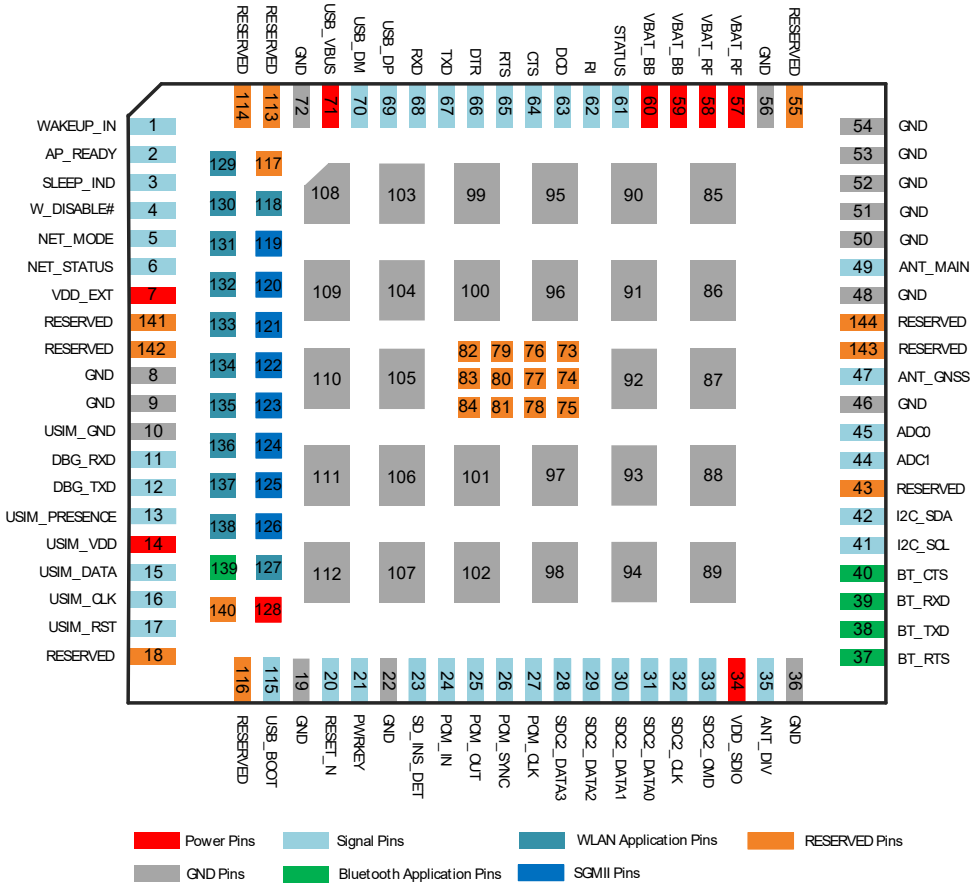
The module includes 80 LCC pins and 64 LGA pins for connection to a cellular application platform. The following chapters will provide detailed explanations of its interfaces/functions.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- WLAN and Bluetooth application interfaces
- ADC interfaces
- SGMII interface
- Indication signals
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment.

Figure 1: Pin Assignment (Top View)



NOTE

1. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact NetPrisma Technical Support.
2. Do not pull up the USB_BOOT pin or BOOT_CONFIG pins (WAKEUP_IN, NET_MODE, WLAN_EN, COEX_UART_RX, COEX_UART_TX, and BT_CTS) before startup.
3. Keep all RESERVED and unused pins unconnected.
4. Connect GND pins 85–112 to ground. Keep RESERVED pins 73–84 as a keepout area and do not include them in the schematic or PCB layout.
5. The module supports the antenna tuner function. Contact NetPrisma Technical Support for details.

3.3. Pin Description

The following tables show the pin definition.

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output

DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A. A test point is recommended to be reserved.
VBAT_RF	57, 58	PI	Power supply for module's RF part		It must be provided with sufficient current up to 1.8 A in a burst transmission. A test point is recommended to be reserved.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved. If unused, keep it open.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.
RESET_N	20	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	1.8 V power domain. A test point is recommended to be reserved if unused.
Status Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	61	OD	Indicate the module's operation status		The driving current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.

NET_MODE	5	DO	Indicate the module's network registration mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status		1.8 V power domain. If unused, keep it open.
SLEEP_IND	3	DO	Indicate the module's sleep mode		1.8 V power domain. If unused, keep it open.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	71	AI	USB connection detection	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved. If unused, keep it open.
USB_DP	69	AIO	USB differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)		

(U)SIM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	10	-	Specified ground for (U)SIM card		
USIM_PRESENCE	13	DI	(U)SIM card hot-plug detected	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM_VDD	14	PO	(U)SIM card power supply	$I_O$max = 50 mA **1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	**1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM_CLK	16	DO	(U)SIM card clock	**1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **3.0 V (U)SIM:**	
USIM_RST	17	DO	(U)SIM card reset		

				V_{OL}max = 0.45 V V_{OH}min = 2.55 V	

Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	62	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.
DCD	63	DO	Main UART data carrier detect		
CTS	64	DO	Clear to send signal from the module		1.8 V power domain. Connect to MCU's CTS. If unused, keep it open.
RTS	65	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
DTR	66	DI	Main UART data terminal ready; Sleep mode control		1.8 V power domain. Pulled up by default. When remains at low level, it can wake up the module. If unused, keep it open.
RXD	68	DI	Main UART receive		
TXD	67	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep them open.

Debug UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	12	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Test points must be reserved. If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	

ADC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	45	AI	General-purpose ADC interface	Input voltage range: 0.3 V to VBAT_BB	If unused, keep them open.
ADC1	44	AI	General-purpose ADC interface		

PCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM_IN	24	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
PCM_OUT	25	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35	

				V	
PCM_SYNC	26	DIO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Functions as an output when the module is in master mode and as an input when in slave mode. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	41	OD	I2C serial clock (for external codec)		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data (for external codec)		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC2_DATA3	28	DIO	SDIO data bit 3	**1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}min = -0.3 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V V_{IH}max = 2.0 V **3.0 V:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V V_{IL}min = -0.3 V V_{IL}max = 0.76 V V_{IH}min = 1.72 V V_{IH}max = 3.34 V	The SDIO signal output voltage can be adjusted to match the SD card's supported signal voltage. Refer to the SD 3.0 protocol for details. If unused, keep them open.
SDC2_DATA2	29	DIO	SDIO data bit 2		
SDC2_DATA1	30	DIO	SDIO data bit 1		
SDC2_DATA0	31	DIO	SDIO data bit 0		
SDC2_CMD	33	DIO	SDIO command		
SDC2_CLK	32	DO	SDIO clock	**1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **3.0 V:** V_{OL}max = 0.38 V V_{OH}min = 2.01 V	
SD_INS_DET	23	DI	SD card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Keep it open if the SD card is not used. Otherwise, it must be connected.
VDD_SDIO	34	PO	SD card SDIO pull-up power	$I_O$max = 50 mA	1.8/2.85 V configurable. Cannot be used for SD card power supply. If unused, keep it open.
SGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**

				s	
EPHY_RST_N	119	DO	Ethernet PHY reset	**1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.85 V:** V_{OL}max = 0.35 V V_{OH}min = 2.14 V	1.8/2.85 V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	DIO	SGMII management data	**1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V V_{IL}max = 0.58 V V_{IH}min = 1.27 V **2.85 V:** V_{OL}max = 0.35 V V_{OH}min = 2.14 V V_{IL}max = 0.71 V V_{IH}min = 1.78 V	1.8/2.85 V power domain. If unused, keep them open.
SGMII_MCLK	122	DO	SGMII management data clock	**1.8 V:** V_{OL}max = 0.45 V V_{OH}min = 1.4 V **2.85 V:** V_{OL}max = 0.35 V V_{OH}min = 2.14 V	
SGMII_TX_M	123	AO	SGMII transmit (-)		Connect this pin to a 0.1 µF capacitor near the PHY. If unused, keep them open.
SGMII_TX_P	124	AO	SGMII transmit (+)		
SGMII_RX_P	125	AI	SGMII receive (+)		Connect this pin to a 0.1 µF capacitor near the module. If unused, keep them open.
SGMII_RX_M	126	AI	SGMII receive (-)		
USIM2_VDD	128	PO	SGMII_MDATA pull-up power supply		Configurable power supply. 1.8/2.85 V power domain. If unused, keep it open.

WLAN and Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SDC1_DATA3	129	DIO	WLAN SDIO data bit 3	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
SDC1_DATA2	130	DIO	WLAN SDIO data bit 2		
SDC1_DATA1	131	DIO	WLAN SDIO data bit 1		
SDC1_DATA0	132	DIO	WLAN SDIO data bit 0		

SDC1_CMD	134	DIO	WLAN SDIO command		
SDC1_CLK	133	DO	WLAN SDIO clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PM_ENABLE	127	DO	WLAN power supply enable		1.8 V power domain. Active high. If unused, keep it open.
WAKE_ON_WIRELESS	135	DI	WLAN wake up the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Active low. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Active high. Cannot be pulled up before startup. If unused, keep it open.
COEX_UART_RX	137	DI	LTE & WLAN/ Bluetooth coexistence receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
COEX_UART_TX	138	DO	LTE & WLAN/ Bluetooth coexistence transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
BT_RXD	39	DI	Bluetooth UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep them open.
BT_TXD	38	DO	Bluetooth UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
BT_RTS	37	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
BT_CTS	40	DO	Clear to send signal from the module	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
BT_EN	139	DO	Bluetooth function enable		1.8 V power domain. Active high. If unused, keep it open.

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_DIV	35	AI	Diversity antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.

Other Interface Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WAKEUP_IN	1	DI	Sleep mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. Cannot be pulled up before

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	startup. Active low. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control		1.8 V power domain. Pulled up by default. When this pin is at low level, the module will enter airplane mode. If unused, keep it open.
AP_READY	2	DI	Application processor sleep state detection		1.8 V power domain. If unused, keep it open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	115	DI	Force the module to enter download mode	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Cannot be pulled up before startup. Active high. A test point is recommended to be reserved.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	18, 43, 55, 73–84, 113, 114, 116, 117, 140–144				Keep them unconnected.

3.4. Operating Modes

The table highlights the operating modes that will be detailed in the following sections.

Table 6: Overview of Operating Modes

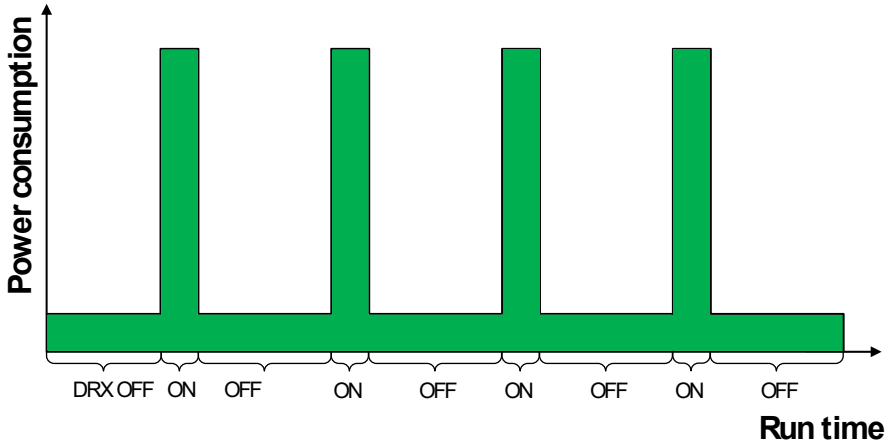
Mode	Details	
Full Functionality Mode	Idle	The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active.
	Data	The module is connected to network. Its power consumption varies with the network setting and data transmission rate.
Airplane Mode	**AT+CFUN=4** or pulling down W_DISABLE# pin can set the module to airplane mode. In this mode, the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption of the module is reduced to an ultra-low level.	
Power Down Mode	The module's power supply is cut off by its power management unit. In this mode, the software is inactive and UART is inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

For details of the commands, see ***document 3***.

3.5. Sleep Mode

The module minimizes power consumption to an ultra-low level in sleep mode.

Figure 2: Module Power Consumption in Sleep Mode



NOTE

DRX cycle values are transmitted over the wireless network.

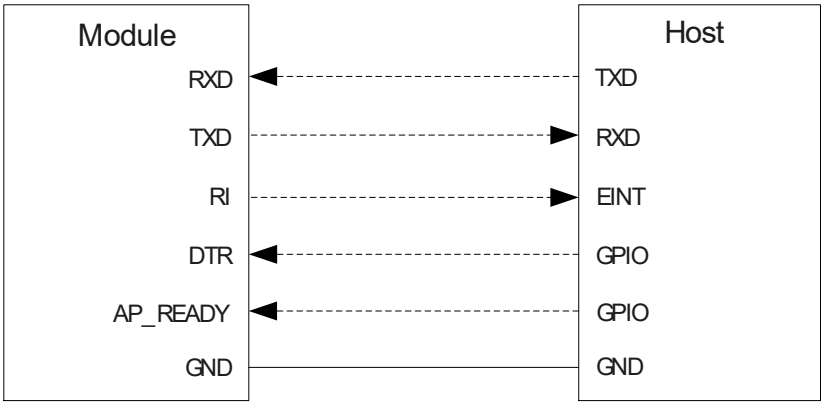
3.5.1. UART Application Scenario

If the MCU communicates with the module via UART interface, the following preconditions can make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. See ***document 3*** or details.
- Drive DTR to high level.

The following figure shows the connection between the module and the MCU.

Figure 3: Sleep Mode Application via UART



- Driving the module's DTR to low level will wake up the module.
- When the module has a URC to report, RI signal will wake up the MCU. See ***Chapter 3.19.4*** for details about RI behaviors.
- AP_READY will detect the sleep state of the MCU (This pin can be configured to high-level or

low-level detection). See ***document 4*** for details about **AT+QCFG="apready"**.

NOTE

Ensure proper level matching between the module and the MCU, as indicated by the dotted line.

3.5.2. USB Application Scenario

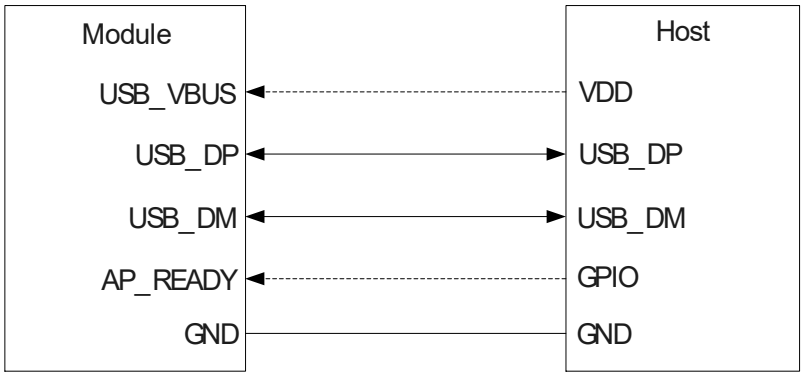
3.5.2.1. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure DTR is held at high level or keep it open.
- Ensure the host's USB bus, connected to the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

Figure 4: Sleep Mode Application with USB Remote Wakeup



- Sending data via USB wakes up the module.
- When the module has a URC to report, it will send remote wakeup signals via USB bus to wake up the host.

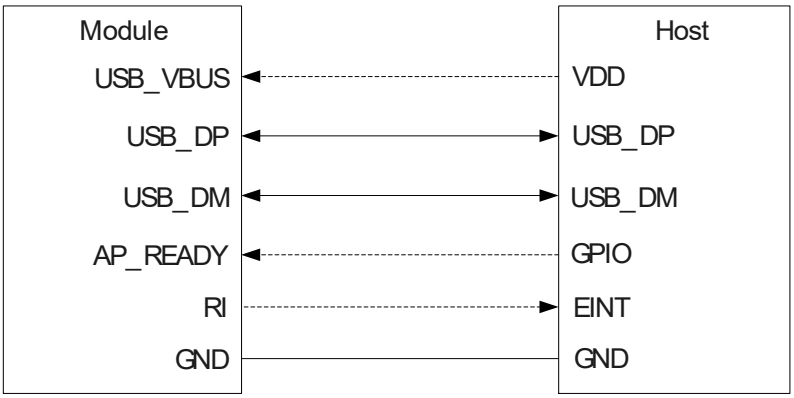
3.5.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB Suspend/Resume but not remote wakeup, the RI signal wakes up the host. Three conditions are needed for the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Ensure the host's USB bus, connected to the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

Figure 5: Sleep Mode Application with RI



- Sending data via USB wakes up the module.
- When the module has a URC to report, RI signal will wake up the host.

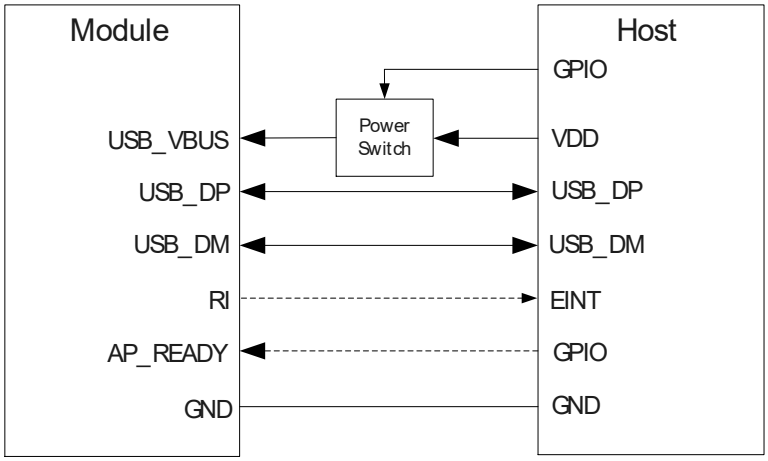
3.5.2.3. USB Application without USB Suspend Function

If the host does not support USB Suspend function, an additional control circuit should disconnect USB_VBUS to allow the module to enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

Figure 6: Sleep Mode Application Without Suspend Function



Resuming the power supply to USB_VBUS will wake up the module.

NOTE

1. Ensure proper level matching between the module and the host, as indicated by the dotted line.
2. For more details on module power management, see ***document 5***.

3.6. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be activated via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level activates airplane mode.

Software:

AT+CFUN provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4. For more details about the AT conmmand, see ***document 3***.

- **AT+CFUN=0:** Minimum functionality mode: Disables both (U)SIM and RF functions.
- **AT+CFUN=1:** Full functionality mode (by default): Enables all functions.
- **AT+CFUN=4:** Airplane mode: Disables RF functions.

NOTE

1. The W_DISABLE# control function is disabled by default in firmware. It can be enabled by **AT+QCFG="airplanecontrol"**. See ***document 4*** for more details.
2. Executing **AT+CFUN** does not affect the GNSS function.

3.7. Power Supply

3.7.1. Power Supply Pins

The module provides four VBAT pins for connecting to an external power supply, divided into two separate voltage domains.

- Two VBAT_RF pins power for the module's RF part.
- Two VBAT_BB pins power for the module's BB part.

The following table shows the details on VBAT and ground pins.

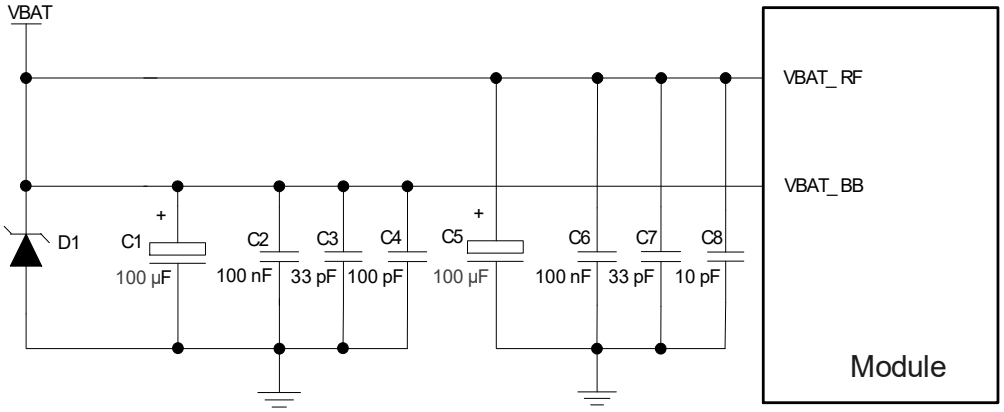
Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's BB part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112					

To reduce voltage drop, use a 100 µF filter capacitor with low ESR (0.7 Ω) and reserve a multi-layer ceramic chip (MLCC) capacitor array due to its ultra-low ESR for VBAT_BB and VBAT_RF. For the MLCC array, it is recommended to use three ceramic capacitors: 100 nF, 33 pF, and 100 pF for VBAT_BB, and 100 nF, 33 pF, and 10 pF for VBAT_RF. Place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from the external application should be a single voltage source, split into two sub-paths using a star structure. The VBAT_BB trace width should be at least 1 mm, and the VBAT_RF trace width at least 2 mm. As a general rule, longer VBAT traces should be made wider.

To prevent damage from electrical surges and ESD, it is recommended to use a TVS component with a low reverse stand-off voltage (V_{RWM}) of 4.5 V, low clamping voltage (V_C), and high reverse peak pulse current (I_{PP}). The following figure shows the star structure of the power supply.

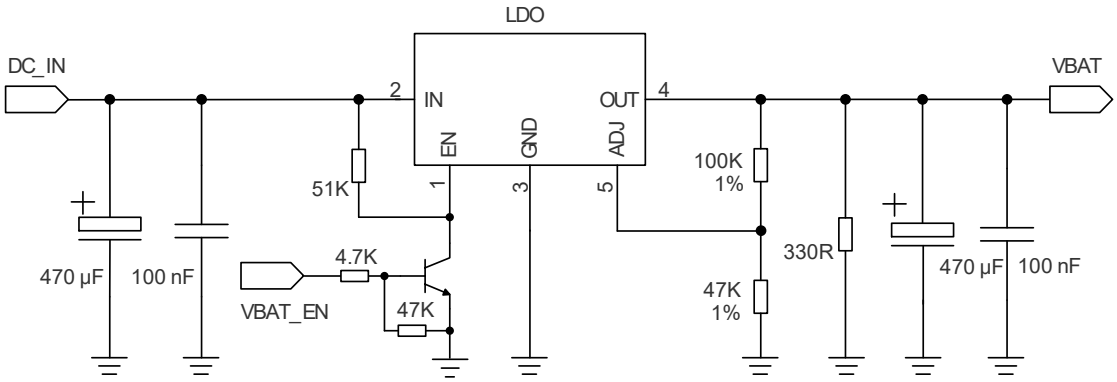
Figure 7: Star Structure of the Power Supply



3.7.2. Reference Design for Power Supply

The performance of the module heavily relies on the power source. The power supply must provide a minimum current of 1.5 A. If the voltage drop between the input and output is minimal, using an LDO is recommended for powering the module. However, if there is a large voltage difference between the input source and the required output (VBAT), a buck converter is the preferred option for the power supply.
The following figure shows a reference design for a +5.0 V input power source. The power supply provides a typical output of around 3.8 V with a maximum load current of 3.0 A.

Figure 8: Reference Circuit of Power Supply



NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.7.3. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document 3***.

3.8. Turn On

3.8.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

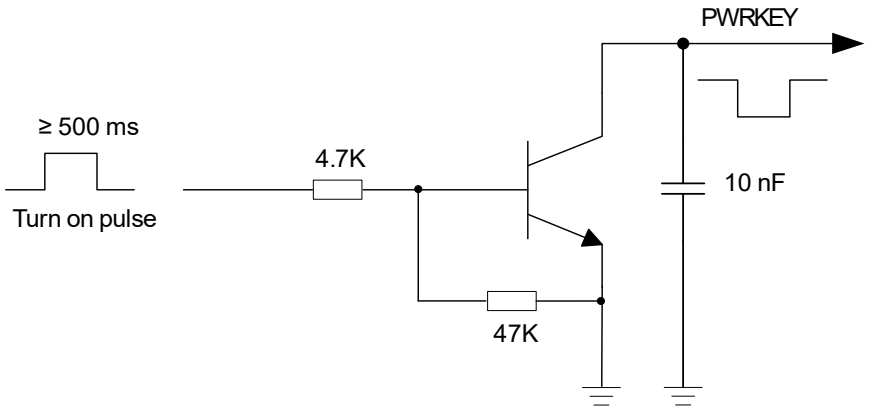
Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.

To turn on the module from power-down mode, drive the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY and release it once the STATUS pin (requiring an external pull-up resistor) outputs a low level. The STATUS pin acts as an indicator to show that the module has been turned on normally.

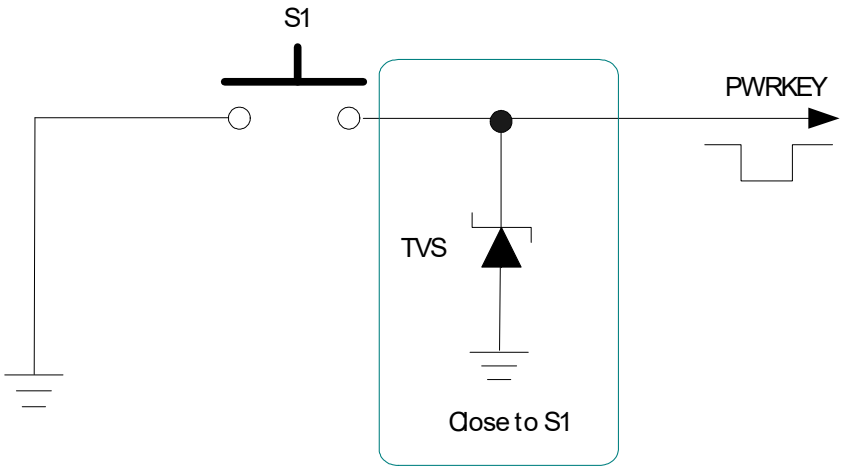
The reference circuit is illustrated in the following figure.

Figure 9: Turn On the Module by Using Driving Circuit



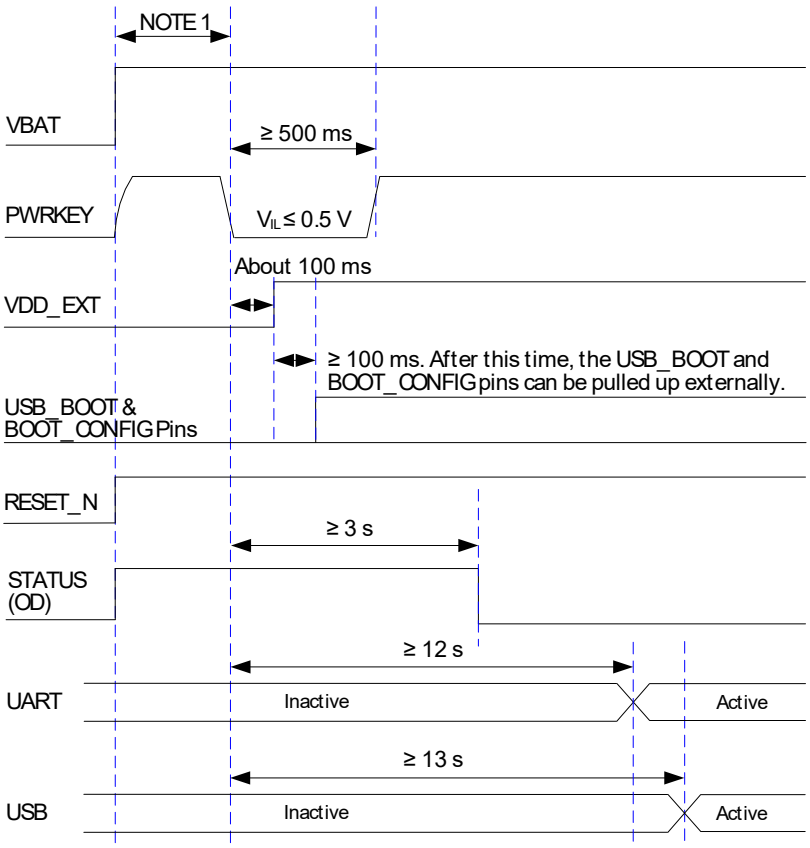
Another way to control the PWRKEY is by using a button directly. Since pressing the button may generate electrostatic discharge (ESD) from fingers, it is essential to place a TVS component near the button for ESD protection. A reference circuit is shown in the following figure.

Figure 10: Turn On the Module by Using a Button



The turn-on timing is illustrated in the following figure.

Figure 11: Turn-on Timing



NOTE

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to wait at least 30 ms after powering up VBAT before pulling down the PWRKEY pin.
2. For automatic module startup without requiring a shutdown, connect PWRKEY directly to GND with a recommended 10 kΩ resistor.
3. Do not pull up the USB_BOOT pin and BOOT_CONFIG pins (WAKEUP_IN, NET_MODE, WLAN_EN, COEX_UART_RX, COEX_UART_TX and BT_CTS) before statup.

3.9. Turn Off

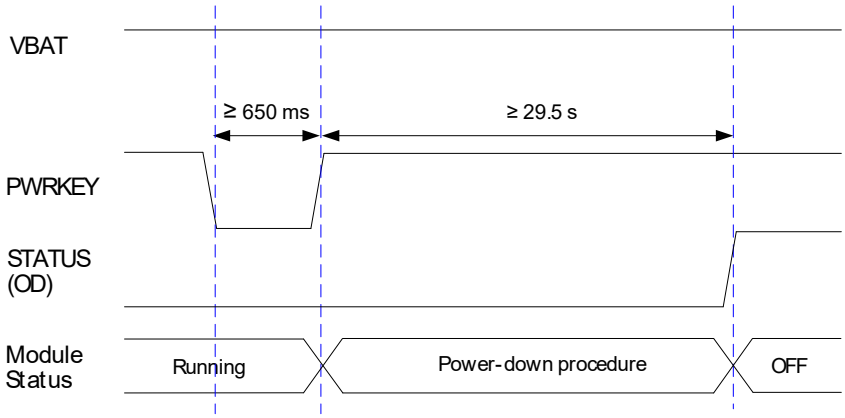
The module can be turned off normally using the following methods:

- Use the PWRKEY pin.
- Use **AT+QPOWD**. For details of the command, see ***document 3***.

3.9.1. Turn Off with PWRKEY

To power down the module, drive the PWRKEY pin to a low level for at least 650 ms. The module will begin the shutdown process once the PWRKEY pin is released. The turn-off timing is shown in the following figure.

Figure 12: Turn-off Timing



3.9.2. Turn Off with AT Command

Using the **AT+QPOWD** command is another safe method to turn off the module, similar to turning it off via the PWRKEY pin.

NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after the module is turned off by PWRKEY or AT command can the power supply be cut off.
When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after a successful turn-off.

3.10. Reset

The module can be reset by driving RESET_N low for 150–460 ms.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8 V power domain. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a button can be used to control the RESET_N.

Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

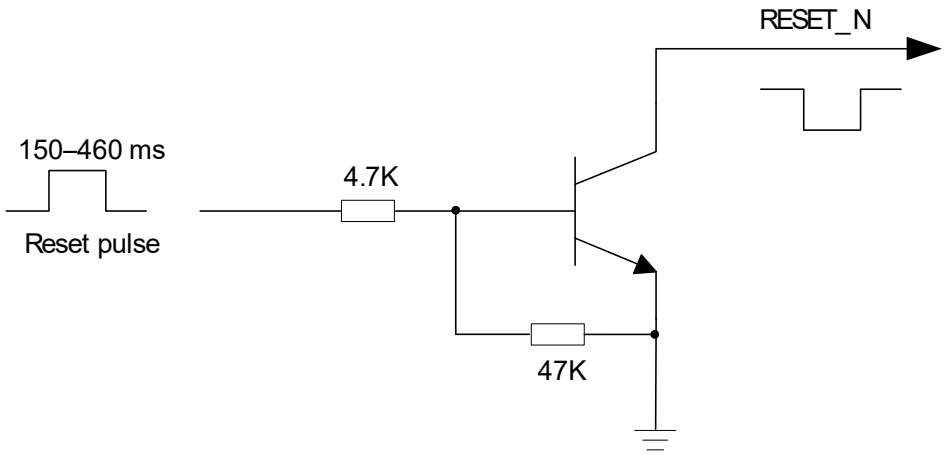
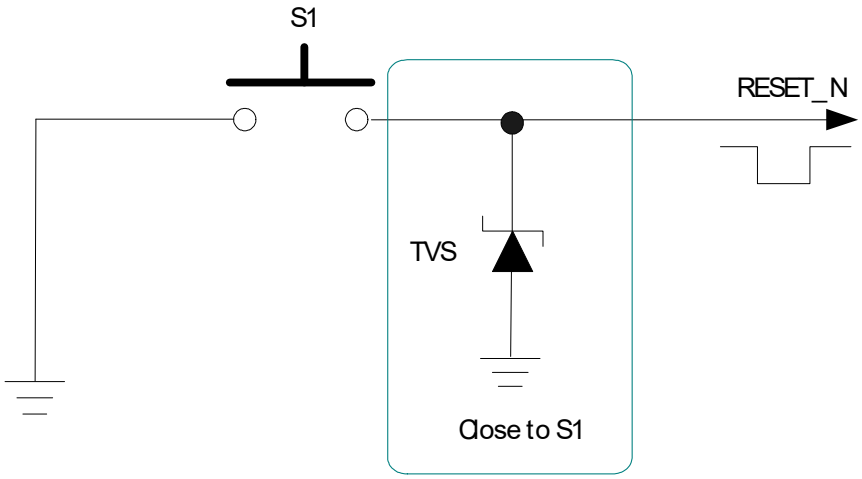
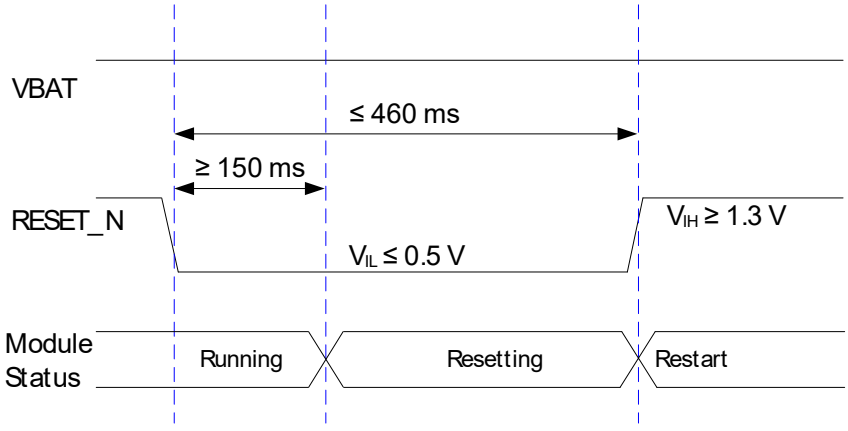


Figure 14: Reference Circuit of RESET_N by Using a Button



The reset timing is illustrated in the following figure.

Figure 15: Reset Timing



NOTE

1. Use the RESET_N pin only if the module cannot be turned off using the **AT+QPOWD** command or the PWRKEY pin.
2. Ensure there are no large capacitors connected to the PWRKEY and RESET_N pins.

3.11. (U)SIM Interfaces

The (U)SIM interface of the module complies with ETSI and IMT-2000 standards, supporting both 1.8 V and 3.0 V (U)SIM cards.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_PRESENCE	13	DI	(U)SIM card hot-plug detection	1.8 V power domain. If unused, keep it open.
USIM_GND	10	-	Specified ground for (U)SIM card	

The (U)SIM2 interface can be configured with pins 119–122 and 128 via **AT+QDSIM=1**. For more details about the AT command, please contact NetPrisma Technical Support.

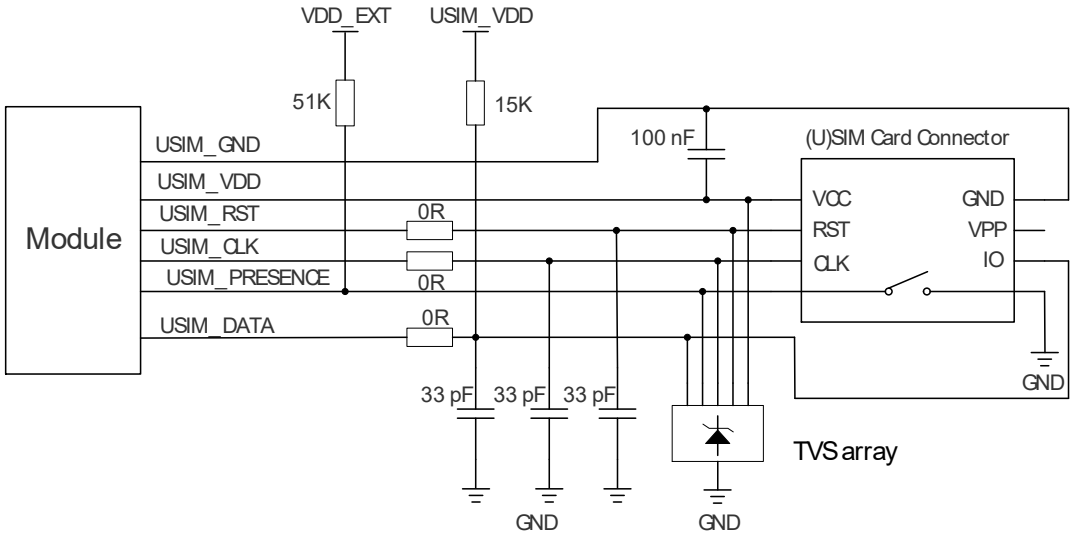
Table 11: Pin Definition of (U)SIM2 Interface

Pin Name	Pin No.	(U)SIM2 Function	I/O	Description	Comment
EPHY_RST_N	119	USIM2_RST	DO	(U)SIM2 card reset	
EPHY_INT_N	120	USIM2_PRESENCE	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	USIM2_CLK	DO	(U)SIM2 card clock	
SGMII_MCLK	122	USIM2_DATA	DIO	(U)SIM2 card data	
USIM2_VDD	128	USIM2_VDD	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.

The module supports hot-plugging of (U)SIM cards through the USIM_PRESENCE pin, with options for low-level and high-level detection. This feature is disabled by default but can be enabled using the **AT+QSIMDET** command. See ***document 3*** for more details about the command.

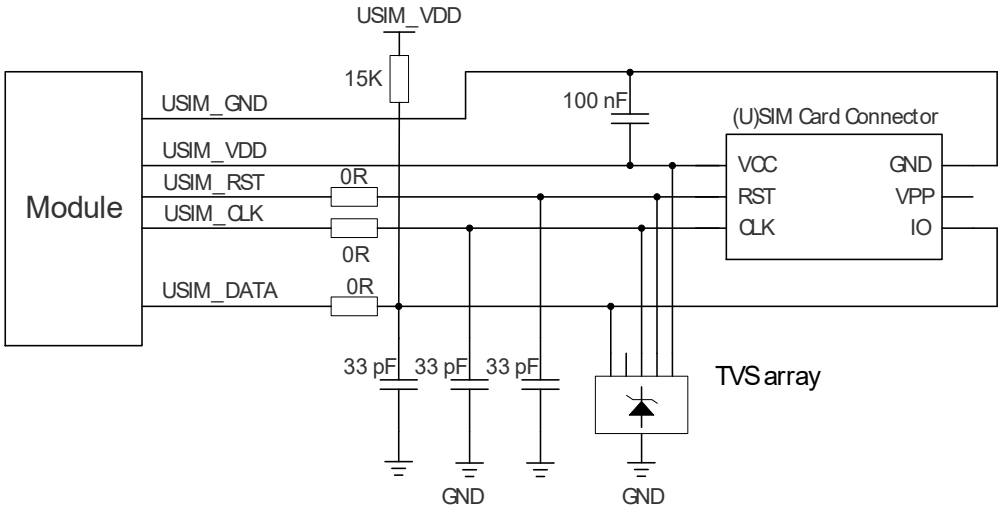
The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector



If (U)SIM card detection function is not needed, keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector



To improve the reliability and performance of the (U)SIM card in your applications, follow these guidelines when designing the (U)SIM circuit:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, add a TVS array with parasitic capacitance not exceeding 15 pF. Include 0 Ω resistors in series between the module and the (U)SIM card for easier debugging. Use 33 pF capacitors to filter RF interference. Ensure the (U)SIM circuit is located close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.12. USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification, supporting both high-speed (480 Mbps) and full-speed (12 Mbps) modes. This interface operates only as a slave device.

The interface can be used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade.

The following table shows the pin definition of USB interface.

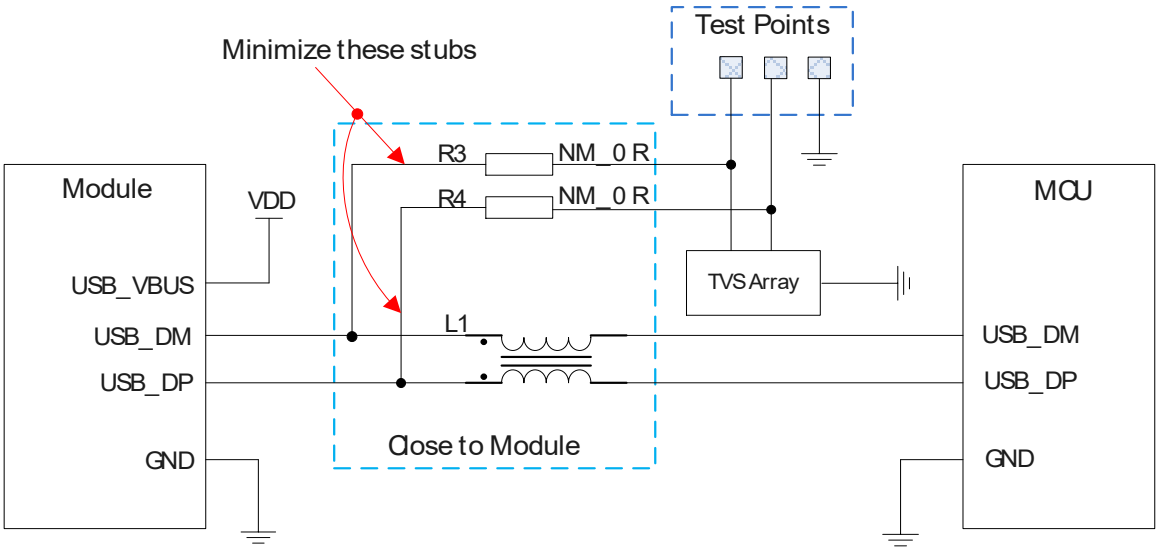
Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved. If unused, keep them open.
USB_DM	70	AIO	USB differential data (-)	
USB_VBUS	71	AI	USB connection detection	A test point must be reserved. If unused, keep it open.

For more details about the USB 2.0 specification, visit http://www.usb.org/home.

The test points are recommended to be reserved for firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

Figure 18: Reference Circuit of USB Interface



A common mode choke L1 is recommended to be added in series between the module and MCU to suppress EMI. Meanwhile, 0 Ω resistors (R3 and R4) should be added in series between the module and the test points to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R3 and R4 components must be placed close to the module, and these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.
To ensure compliance with the USB 2.0 specification when designing the USB interface, follow these guidelines:

- Route the USB signal traces as differential pairs surrounded by ground. The impedance of the USB differential traces should be 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with

ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

3.13. UART Interfaces

The module provides two UART interfaces: the main UART and the debug UART. The following shows their features.

- Main UART interface supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps, and 921600 bps. It also supports RTS and CTS hardware flow control, and can be used for both data transmission and AT command communication.
- Debug UART interface supports 115200 bps baud rate and is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 13: Pin Definition of Main UART Interface

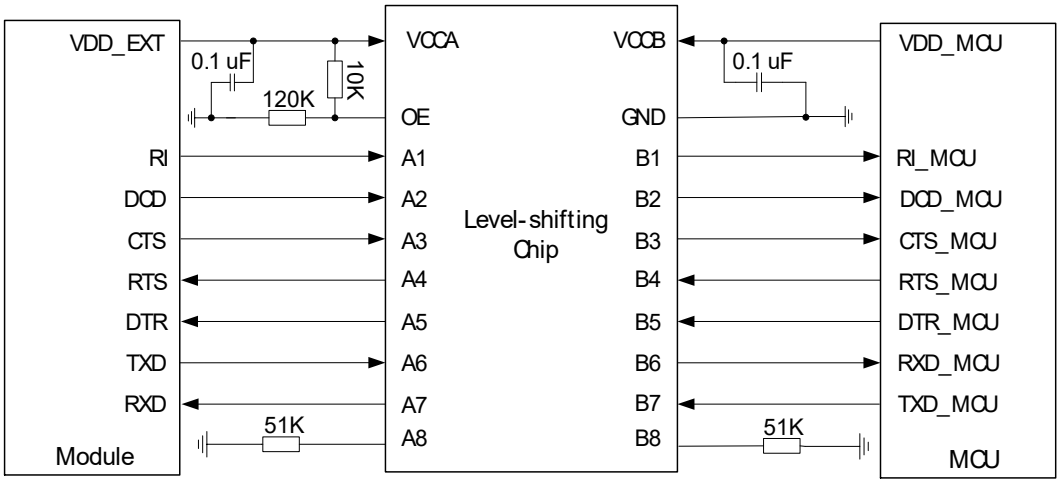
Pin Name	Pin No.	I/O	Description	Comment
RI	62	DO	Main UART ring indication	1.8 V power domain. If unused, keep them open.
DCD	63	DO	Main UART data carrier detect	
CTS	64	DO	Clear to send signal from the module	1.8 V power domain. Connect to MCU's CTS. If unused, keep it open.
RTS	65	DI	Request to send signal to the module	1.8 V power domain. Connect to MCU's RTS. If unused, keep it open.
DTR	66	DI	Main UART data terminal ready; Sleep mode control	1.8 V power domain Pulled up by default. When remains at low level, it can wake up the module. If unused, keep it open.
TXD	67	DO	Main UART transmit	1.8 V power domain. If unused, keep them open.
RXD	68	DI	Main UART receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	1.8 V power domain. Test points must be reserved. If unused, keep them open.
DBG_RXD	11	DI	Debug UART receive	

The module provides 1.8 V UART interface. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. An IC solution TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

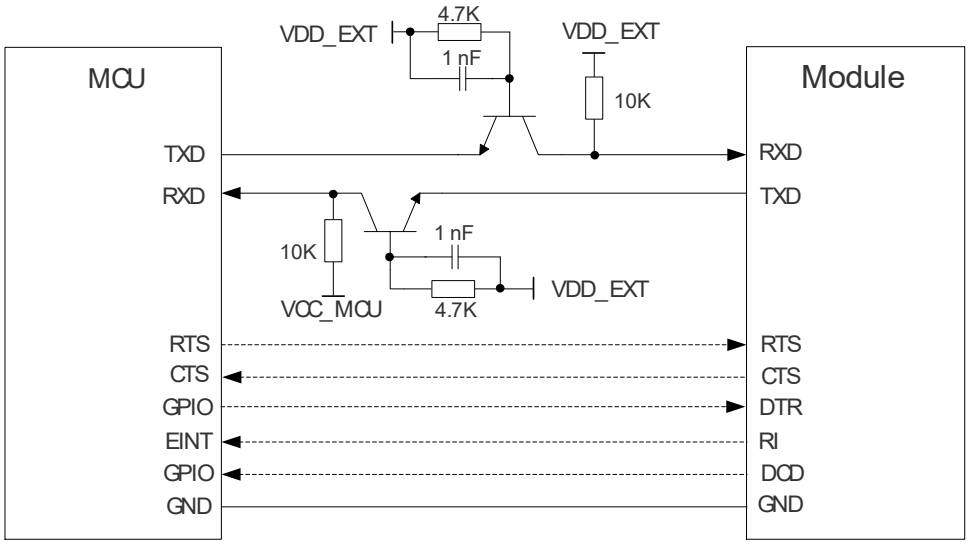
Figure 19: Reference Design of UART with Level-shifting Chip



Visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

Figure 20: Reference Circuit with Transistor Circuit



NOTE

1. Transistor circuit solution above is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

3.14. PCM and I2C Interfaces

The module provides one I2C interface and one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes:

- Short frame synchronization: The module works as both the master and slave devices.
- Long frame synchronization: The module only works as the master device.

In short frame sync mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In long frame sync mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC.

The module supports a 16-bit linear data format. The following figures show the short frame sync mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the long frame sync mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

Figure 21: Short Frame Sync Mode Timing

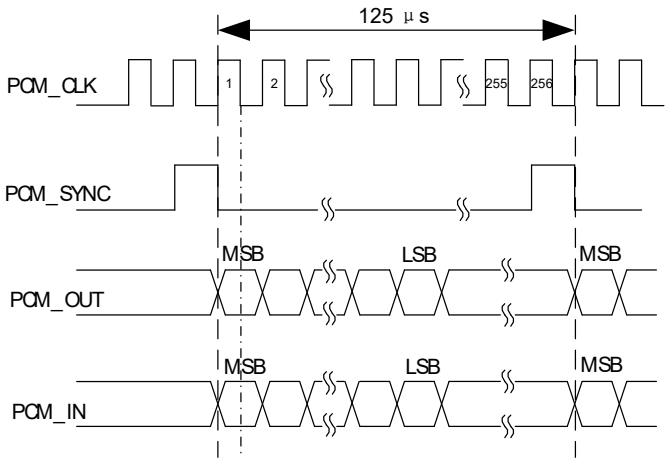
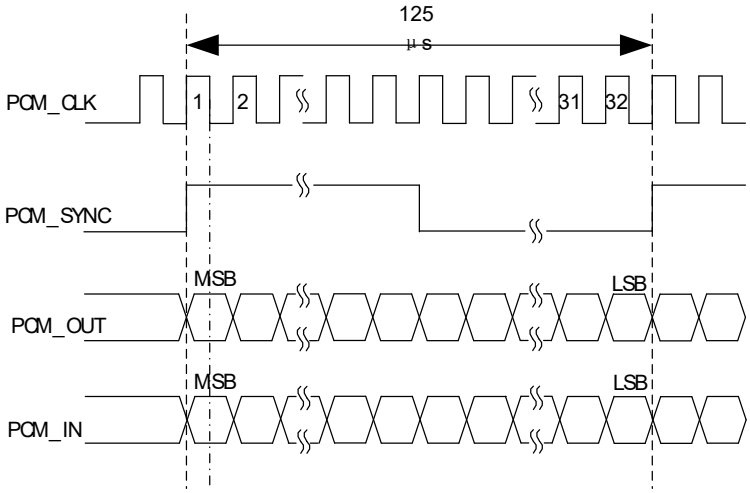


Figure 22: Long Frame Sync Mode Timing



The clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document 3*** for more details about **AT+QDAI**.

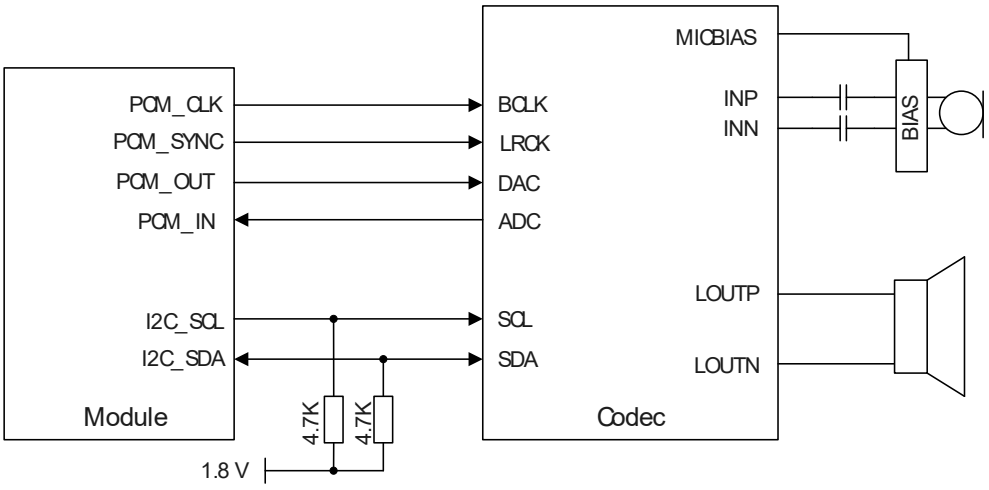
The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 15: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8 V power domain If unused, keep them open.
PCM_OUT	25	DO	PCM data output	
PCM_SYNC	26	DIO	PCM data frame sync	1.8 V power domain. Functions as an output when the module is in master mode and as an input when in slave mode. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock	
I2C_SCL	41	OD	I2C serial clock (for external codec)	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data (for external codec)	

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

Figure 23: Reference Circuit of PCM and I2C Application with Audio Codec



NOTE

1. Reserve RC circuits (R = 22 Ω, C = 22 pF) to the PCM traces, especially PCM_CLK, close to codec.
2. The module only works as a master device pertaining to I2C interface.

3.15. SD Card Interface

The SD card interface supports SD 3.0 protocol. The following table shows the pin definition of SD card interface.

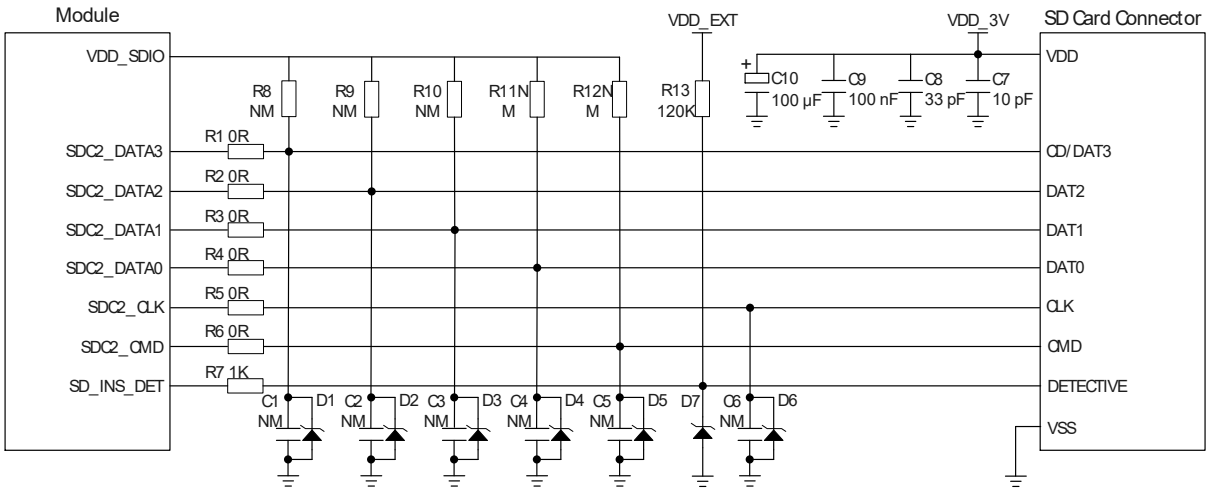
Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment

SDC2_DATA3	28	DIO	SDIO data bit 3	The SDIO signal output voltage can be adjusted to match the SD card's supported signal voltage. Refer to the SD 3.0 protocol for details. If unused, keep them open.
SDC2_DATA2	29	DIO	SDIO data bit 2	
SDC2_DATA1	30	DIO	SDIO data bit 1	
SDC2_DATA0	31	DIO	SDIO data bit 0	
SDC2_CLK	32	DO	SDIO clock	
SDC2_CMD	33	DIO	SDIO command	
VDD_SDIO	34	PO	SD card SDIO pull-up power	1.8/2.85 V configurable. Cannot be used for SD card power supply. If unused, keep it open.
SD_INS_DET	23	DI	SD card hot-plug detect	1.8 V power domain. Keep it open when SD card is not used. Otherwise, it must be connected.

The following figure shows a reference design of SD card.

Figure 24: Reference Circuit of SD Card Interface



In SD card interface design, to ensure good communication performance with SD card, the following design principles should be complied with:

- Keep SD_INS_DET open when SD card is not used. Otherwise, it must be connected.
- The SD card power supply (VDD_3V) should have a voltage range of 2.7–3.6 V and be able to provide sufficient current (up to 0.8 A). Since the maximum output current of VDD_SDIO is 50 mA

(suitable only for SDIO pull-up resistors), an external power supply is required for the SD card.

- To avoid jitter of bus, resistors R8–R12 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. VDD_SDIO should be used as the pull-up power.
- To adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series and reserve capacitors C1–C6 (not mounted by default) between the module and the SD card. All resistors and capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS array on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω ±10 %.
- Make sure the adjacent trace spacing is more than twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SDC2_CLK and SDC2_DATA[0:3]/ SDC2_CMD less than 1 mm and the total routing length less than 50 mm. The total trace length inside the module is 27 mm, so the exterior total trace length should be less than 23 mm.

3.16. WLAN and Bluetooth Application Interfaces

The module supports an SDIO 3.0 interface for WLAN function, and UART and PCM interfaces for Bluetooth function. The following table shows the pin definition of WLAN and Bluetooth application interfaces.

Table 17: Pin Definition of WLAN and Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN and Bluetooth Application Interfaces				
SDC1_DATA3	129	DIO	WLAN SDIO data bit 3	1.8 V power domain. If unused, keep them open.
SDC1_DATA2	130	DIO	WLAN SDIO data bit 2	
SDC1_DATA1	131	DIO	WLAN SDIO data bit 1	
SDC1_DATA0	132	DIO	WLAN SDIO data bit 0	
SDC1_CMD	134	DIO	WLAN SDIO command	
SDC1_CLK	133	DO	WLAN SDIO clock	
WLAN_EN	136	DO	WLAN function enable	1.8 V power domain. Active high. Cannot be pulled up before startup. If unused, keep it open.
Coexistence and Control Interfaces				
PM_ENABLE	127	DO	WLAN power supply enable	1.8 V power domain. Active high. If unused, keep it open.
WAKE_ON_ WIRELESS	135	DI	WLAN wake up the module	1.8 V power domain. Active low. If unused, keep it open.
COEX_UART_RX	137	DI	LTE & WLAN/Bluetooth coexistence receive	1.8 V power domain. Cannot be pulled up before startup.

COEX_UART_TX	138	DO	LTE & WLAN/Bluetooth coexistence transmit	If unused, keep it open.
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
Bluetooth Application Interface				
BT_RXD	39	DI	Bluetooth UART receive	1.8 V power domain. If unused, keep them open.
BT_TXD	38	DO	Bluetooth UART transmit	
BT_RTS	37	DI	Request to send signal to the module	1.8 V power domain. If unused, keep it open.
BT_CTS	40	DO	Clear to send signal from the module	1.8 V power domain. Cannot be pulled up before startup. If unused, keep it open.
BT_EN	139	DO	Bluetooth function enable	1.8 V power domain. Active high If unused, keep it open.
PCM_IN	24	DI	PCM data input	1.8 V power domain. If unused, keep it open.
PCM_OUT	25	DO	PCM data output	
PCM_SYNC	26	DO	PCM data frame sync	1.8 V power domain. Can only be used as output signals for the Bluetooth function. If unused, keep them open.
PCM_CLK	27	DO	PCM clock	

3.16.1. WLAN Application Interfaces

The module provides an SDIO 3.0 interface and a control interface for WLAN applications. The SDIO interface supports SDR mode, with a maximum frequency of up to 50 MHz.

As SDIO signals are high-speed, to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep matching length between SDC1_CLK and SDC1_DATA[0:3]/SDC1_CMD less than 1 mm and total routing length less than 50 mm.
- Keep termination resistors within 15–24 Ω on SDC1_CLK signal traces near the module and keep the routing distance from module's SDC1_CLK pin to termination resistors less than 5 mm.
- Make sure the adjacent trace spacing is more than twice the trace width and bus capacitance is less than 15 pF.

3.16.2. Bluetooth Application Interfaces

The module supports a dedicated UART interface and a PCM interface for Bluetooth application. Bluetooth UART interface supports high-speed mode up to 3 Mbps. It also supports RTS and CTS hardware flow control.

As Bluetooth UART interface signals are high-speed, comply with the following principles to ensure the Bluetooth UART interface works normally:

- The module provides a 1.8 V Bluetooth UART interface. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. Make sure the voltage-level translator supports data transmission with high rate.
- Make sure the communication cable supports data transmission with high rate.

NOTE

The module's Bluetooth functionality depends on the hardware interface and software version. For more details, contact NetPrisma Technical Support.

3.17. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

- **AT+QADC=0** can be used to read the voltage value on ADC0 pin.
- **AT+QADC=1** can be used to read the voltage value on ADC1 pin.

For more details about these AT commands, see ***document 3***.

To improve the accuracy of ADC voltage values, the trace of ADC should be surrounded by ground.

Table 18: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description	Comment
ADC0	45	General-purpose ADC interface	If unused, keep them open.
ADC1	44	General-purpose ADC interface	

The following table describes the characteristic of ADC interfaces.

Table 19: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0.3	-	VBAT_BB	V
ADC1 Input Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTE

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.18. SGMII Interface

The module includes an integrated Ethernet MAC with four SGMII data signals, two management signals and two control signals. The key features of the SGMII interface are shown below:

- IEEE802.3 compliant
- Support 10/100/1000 Mbps Ethernet work mode
- Support maximum 150 Mbps (DL)/50 Mbps (UL) for 4G network
- Support VLAN tagging

- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY such as AR8033, or to an external switch
- Management signals support 1.8 and 2.85 V dual voltage

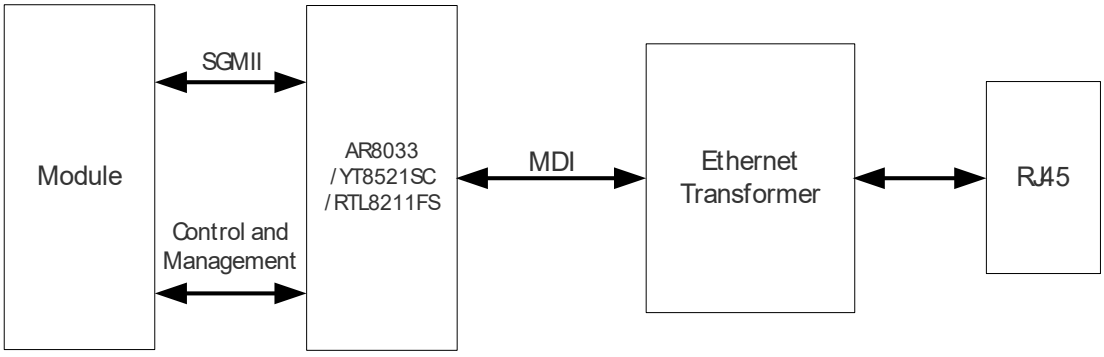
The following table shows the pin definition of SGMII interface.

Table 20: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
SGMII Control and Management Interfaces				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8/2.85 V power domain. If unused, keep it open.
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8 V power domain. If unused, keep it open.
SGMII_MDATA	121	DIO	SGMII management data	1.8/2.85 V power domain. If unused, keep them open.
SGMII_MCLK	122	DO	SGMII management data clock	
USIM2_VDD	128	PO	SGMII_MDATA pull-up power supply	Configurable power supply. 1.8/2.85 V power domain. If unused, keep it open.
SGMII Data Interface				
SGMII_TX_M	123	AO	SGMII transmit (-)	Connect this pin to a 0.1 μF capacitor near the PHY. If unused, keep them open.
SGMII_TX_P	124	AO	SGMII transmit (+)	
SGMII_RX_P	125	AI	SGMII receive (+)	Connect this pin to a 0.1 μF capacitor near the module. If unused, keep them open.
SGMII_RX_M	126	AI	SGMII receive (-)	

The following figure shows the simplified block diagram for Ethernet application.

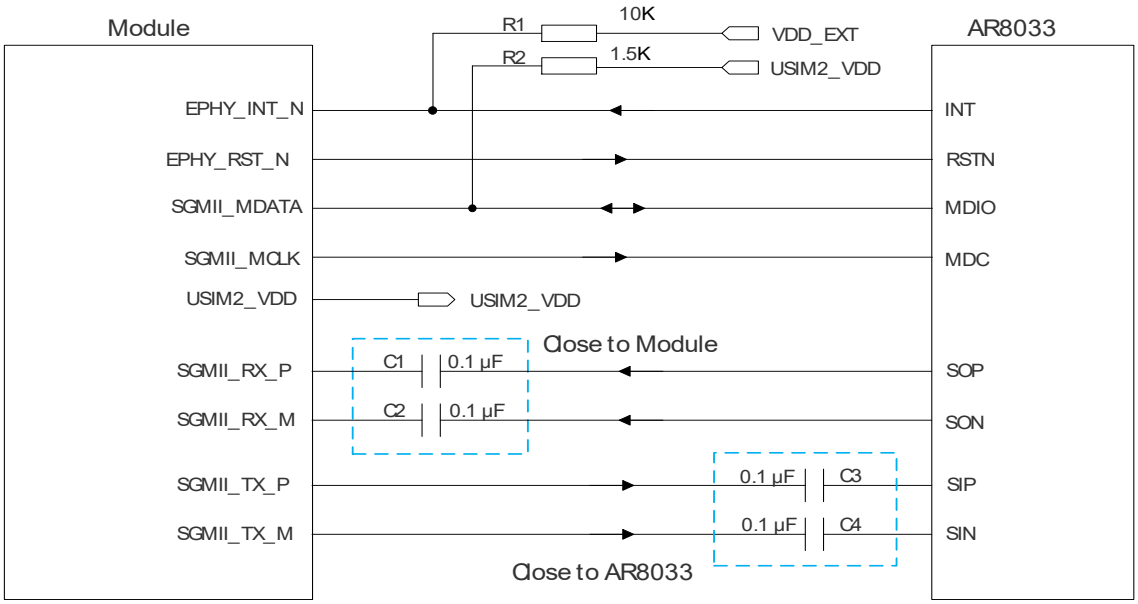
Figure 25: Simplified Block Diagram for Ethernet Application



For more information about Ethernet PHY design of YT8521SC or RTL8211FS, see ***document 6***.

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

Figure 26: Reference Circuit of SGMII Interface with PHY AR8033 Application



To enhance the reliability and availability in your applications, follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- Keep the maximum trace length less than 25.4 cm and keep the length difference on the differential pairs less than 0.5 mm.
- The differential impedance of SGMII data trace is 100 Ω ±10 %, and ensure the integrity of the reference ground.
- Make sure the trace spacing between SGMII_TX_P/_M and SGMII_RX_P/_M is at least 3 times of the trace width, and the same to the adjacent signal traces.

3.19. Indication Signals

3.19.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 21: Pin Definition of Network Indication

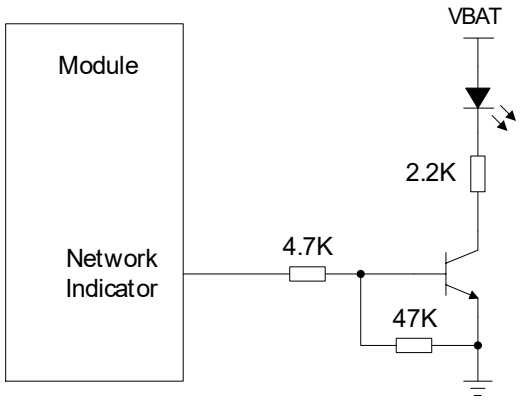
Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's network registration mode	1.8 V power domain Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	1.8 V power domain If unused, keep it open.

Table 22: Working State of Network Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on 4G network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing

A reference circuit is shown in the following figure.

Figure 27: Reference Circuit of the Network Indicator



3.19.2. STATUS

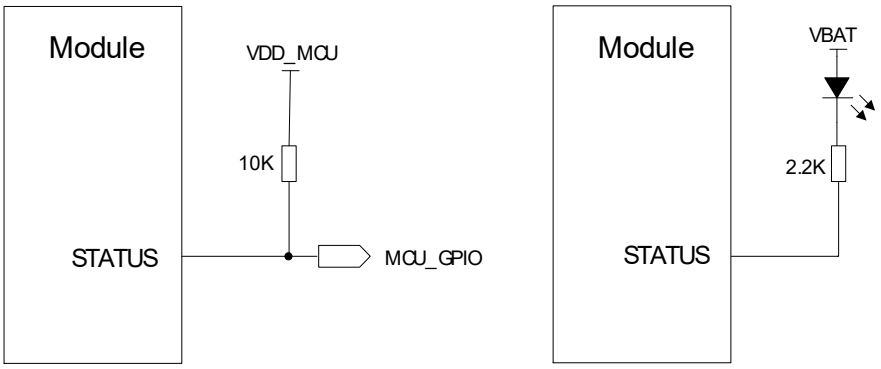
The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to the GPIO of the MCU through a pull-up resistor, or designed according to the LED indicator circuit shown in the figure below. When the module is turned on normally, the STATUS will output low level. Otherwise, the STATUS will present high-impedance state.

Table 23: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	The driving current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

Figure 28: Reference Circuits of STATUS



NOTE

The STATUS pin cannot be used as the turn-off status indication of the module when VBAT power supply is removed.

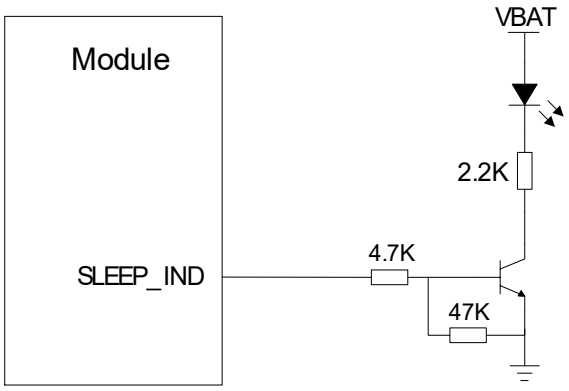
3.19.3. SLEEP_IND

SLEEP_IND is used to indicate the module's sleep mode. When the module enters sleep mode, SLEEP_IND outputs high level by default.

Table 24: Pin Definition of SLEEP_IND

Pin Name	Pin No.	I/O	Description	Comment
SLEEP_IND	3	DO	Indicate the module's sleep mode	1.8 V power domain. If unused, keep it open.

Figure 29: Reference Design of SLEEP_IND



3.19.4. RI

AT+QCFG="risignaltype","physical" can be used to configure RI behaviors. No matter on which port (main UART, USB AT port or USB modem port) a URC is presented, the URC will trigger the behaviors of

RI pin. See ***document 4*** for details.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. See ***document 3*** for details.

The default behaviors of the RI are shown as below and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document 3*** for details.

Table 25: Behaviors of RI

Status	RI Level Status
Idle	RI keeps at high level
When a new URC information returns	RI outputs 120 ms low pulse

3.20. USB_BOOT Interface

The module provides a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 26: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module to enter download mode	1.8 V power domain. Cannot be pulled up before startup. Active high. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

Figure 30: Reference Circuit of USB_BOOT Interface

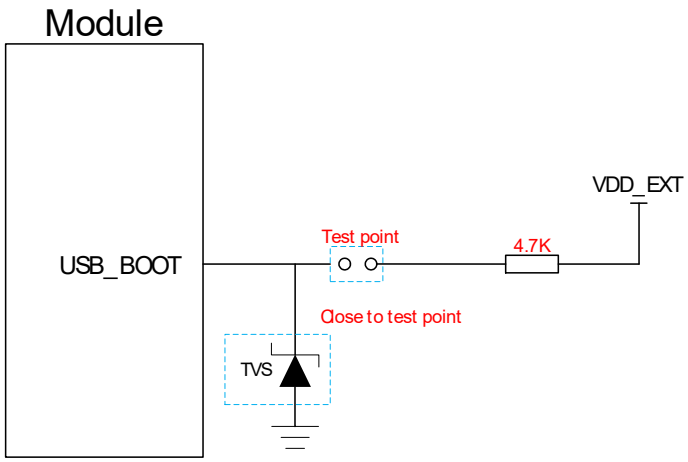
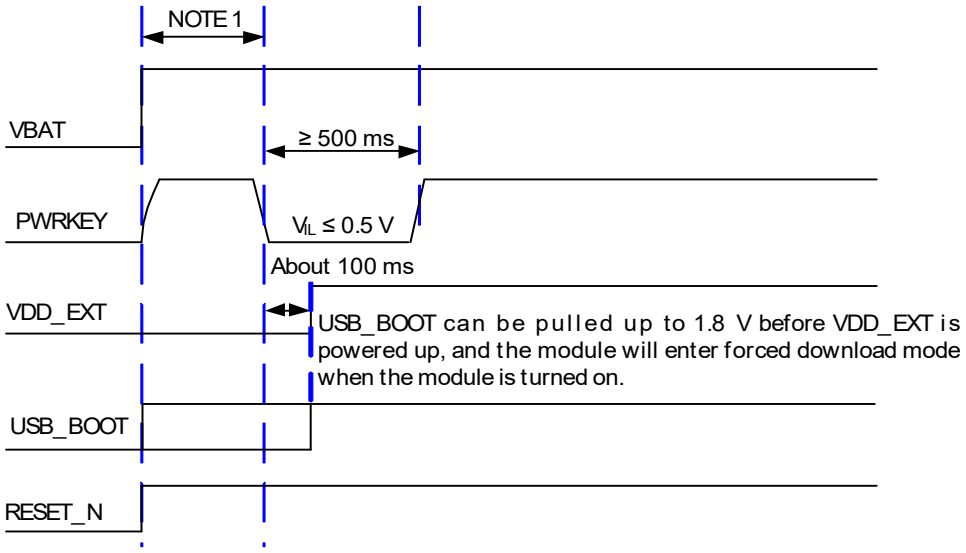


Figure 34: Timing for Entering Forced Download Mode



NOTE

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to wait at least 30 ms after powering up VBAT before pulling down the PWRKEY pin.
2. Follow the above timing when using MCU control the module to enter the forced download mode. Do not pull up USB_BOOT to 1.8 V before powering up VBAT.
3. If you need to manually force the module to enter forced download mode, directly connect the test points shown in ***Figure 30***.

4 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module includes a main antenna interface, a diversity antenna interface (designed to minimize signal loss caused by high-speed movement and multipath effects), and a GNSS antenna interface. The impedance of all antenna ports is 50 Ω.

4.1. Celluar Network

4.1.1. Antenna Interfaces and Frequency Bands

The pin definition of main antenna and diversity antenna interfaces is shown below.

Table 27: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DIV	35	AI	Diversity antenna interface	50 Ω characteristic impedance. If unused, keep it open.

4.1.2. Operating Frequency

Table 28: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B14	788–798	758–768	MHZ
LTE-FDD B66	1710–1780	2110–2180	MHz
LTE-FDD B71	663–698	617–652	MHz

4.1.3. Tx Power

The following table shows the Tx power.

Table 29: Tx Power

Frequency Band	Max. Tx Power	Min. Tx Power
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE bands	23 dBm ±2 dB	< -39 dBm

4.1.4. Receiver Sensitivity

The following tables show the conducted receiver sensitivity.

Table 30: Conducted Receiver Sensitivity

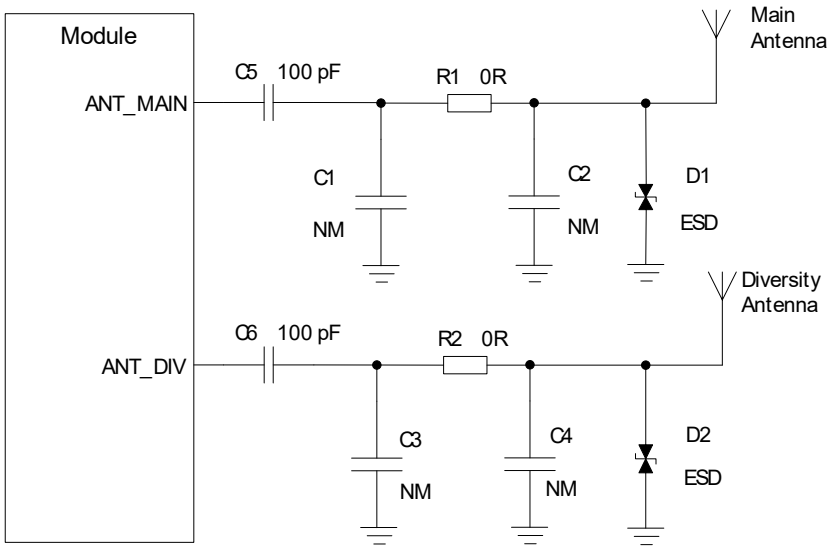
Frequency Band	Receiver Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [4]	
WCDMA B2	-109.5 dBm	-110 dBm	-110.4 dBm	-104.7 dBm
WCDMA B4	-109.6 dBm	-110 dBm	-110.6 dBm	-106.7 dBm
WCDMA B5	-110 dBm	-110 dBm	-110.7 dBm	-104.7 dBm
LTE-FDD B2 (10 MHz)	-98.0 dBm	-98.5 dBm	-101.0 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-97.5 dBm	-98.2 dBm	-100.2 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-98.5 dBm	-99.5 dBm	-101.5 dBm	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.0 dBm	-99.5 dBm	-101.8 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98.5 dBm	-99.0 dBm	-101.5 dBm	-93.3 dBm
LTE-FDD B14 (10 MHz)	-98.4 dBm	-99.0 dBm	-101.2 dBm	-93.3 dBm
LTE-FDD B66 (10 MHz)	-97.5 dBm	-98.2 dBm	-100.2 dBm	-95.8 dBm
LTE-FDD B71 (10 MHz)	-98.6 dBm	-99.5 dBm	-101.5 dBm	-93.5 dBm

4.1.5. Reference Design

A reference design of ANT_MAIN and ANT_DIV antennas is shown as below. A dual L-type circuit should be reserved for better RF performance. The capacitors C1–C4 are not mounted by default.

Figure 31: Reference Circuit of RF Antenna Interfaces

[4] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve Rx performance.



NOTE

1. Keep a proper distance between the main antenna and the diversity antenna to improve the receiver sensitivity.
2. Rx-diversity function is enabled by default. **AT+QCFG="divctl",0** can be used to disable Rx-diversity. See ***document 4*** for details.
3. Place the dual L-type components (R1/C1/C2, R2/C3/C4, C5/C6) as close to the antenna as possible.
4. Notes on C5 and C6:
   1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C5 and C6.
      b) If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.
5. It is recommended to reserve an ESD protection components (D1 and D2) and the junction capacitance should not exceed 0.05 pF.

4.2. GNSS (Optional)

4.2.1. Antenna Interfaces and Frequency Bands

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo, and QZSS.

It supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, see ***document 1***.

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 31: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50 Ω characteristic impedance. If unused, keep it open.

Table 32: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

4.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 33: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	35	s
		AGNSS start	10	s
	Warm start @ open sky	Autonomous	26	s
		AGNSS start	2.2	s
	Hot start @ open sky	Autonomous	2.5	s
		AGNSS start	1.8	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock

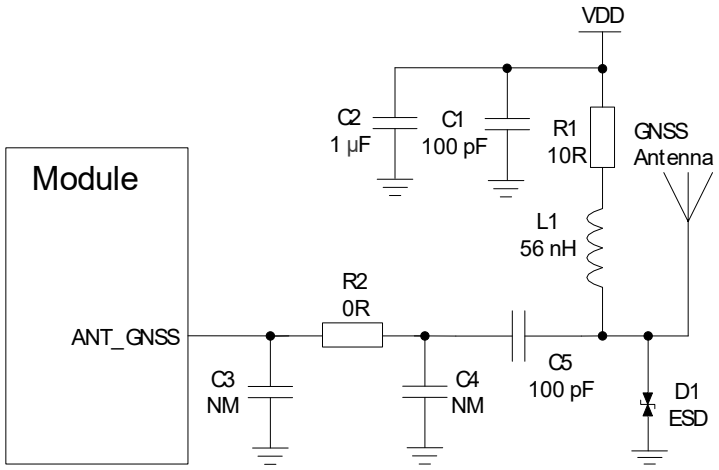
within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.2.3. Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. It is generally recommended to use a passive antenna for the module. However, if your application requires an active antenna, it is advised to include a π-type attenuation circuit and ensure the power system design uses a high-performance LDO.

A reference design of GNSS antenna is shown as below. Below is a reference design for the GNSS antenna.

Figure 32: Reference Circuit of GNSS Antenna



NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, you will not need the VDD circuit.
3. It is recommended to reserve an ESD protection component D1 and the junction capacitance should not exceed 0.05 pF.

4.2.4. Layout Guidelines

The following layout guidelines should be taken into account in your designs.

- Maximize the distance among GNSS antenna, main antenna, and diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

4.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant,

the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 33: Microstrip Design on a 2-layer PCB

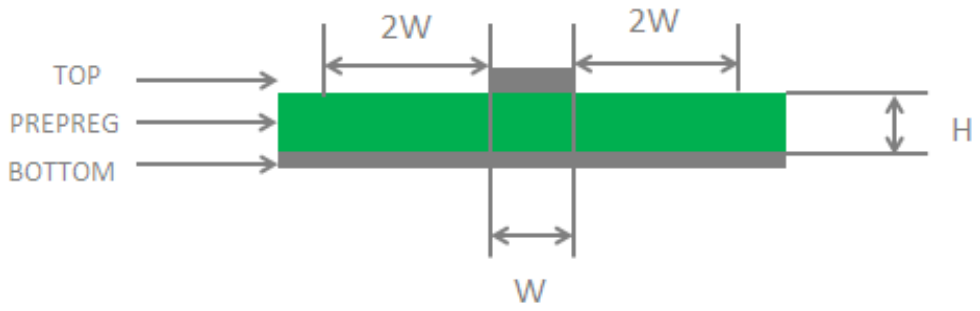


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

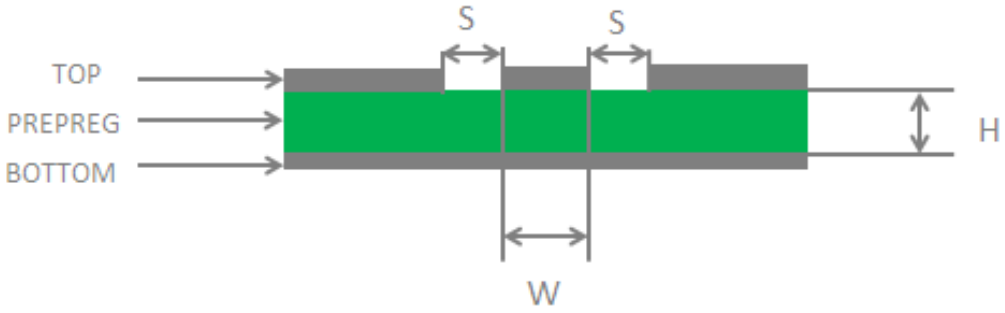


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

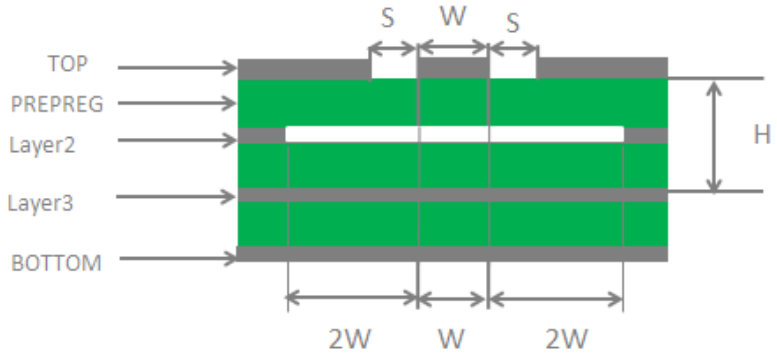
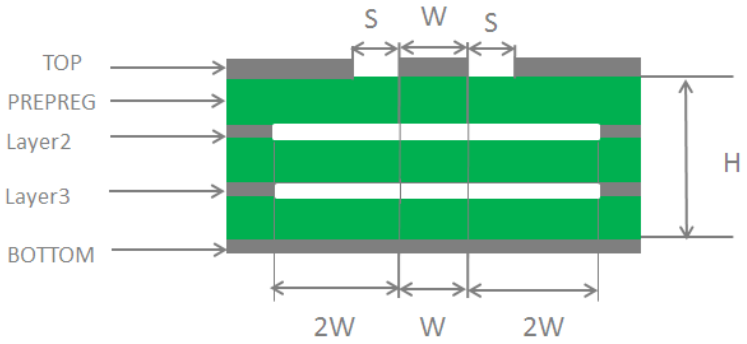


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document 7***.

4.4. Antenna Design Requirements

The following table shows the requirements on main antenna, diversity antenna and GNSS antenna.

Table 34: Antenna Design Requirements

Type	Requirements
GNSS (Optional)	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: Passive antenna gain: > 0 dBi
	For active antenna usage: ● Active antenna noise figure: < 1.5 dB ● Active antenna embedded LNA gain: < 17 dB
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max. input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: - **< 1 dB:** LB (<1 GHz) - **< 1.5 dB:** MB (1–2.3 GHz) - **< 2 dB:** HB (> 2.3 GHz)

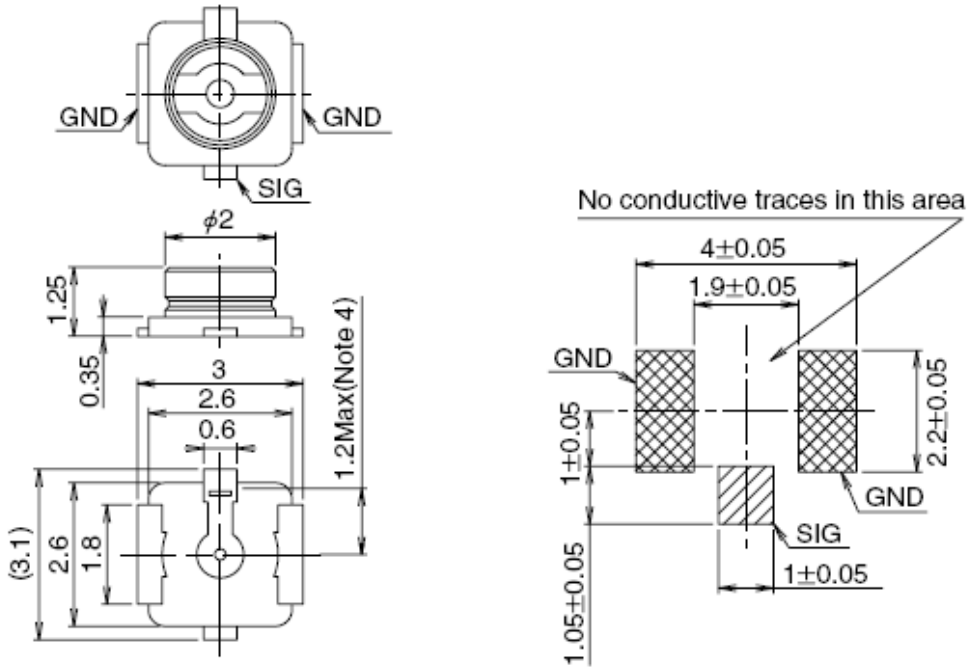
NOTE

It is recommended to use a passive antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

4.5. RF Connector Recommendation

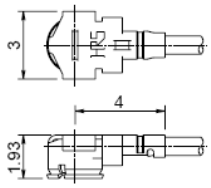
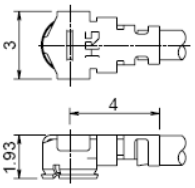
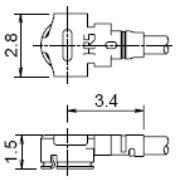
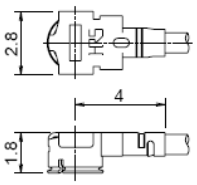
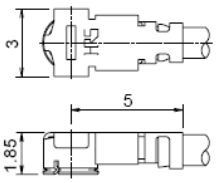
If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

Figure 37: Dimensions of the Receptacle (Unit: mm)



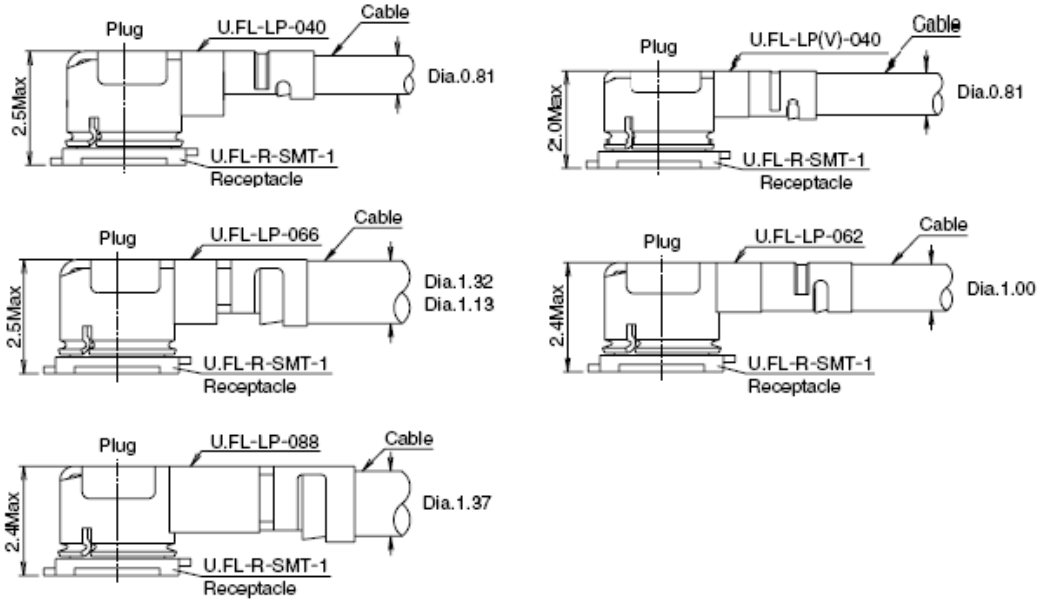
U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Figure 38: Specifications of Mated Plugs

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated connectors.

Figure 39: Space Factor of Mated Connectors (Unit: mm)



For more details, visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.3	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

5.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	At maximum power control level.	-	-	400	mV
I_{VBAT}	Peak power consumption	At maximum power control level.	-	-	1.5	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

5.3. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 37: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit

Operating Temperature Range [5]	-35	+25	+75	ºC
Extended Temperature Range [6]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

5.4. Power Consumption

The power consumption is shown below.

Table 38: Power Consumption

Description	Condition	Typ.	Unit
OFF State	Power down	8	μA
Sleep State	**AT+CFUN=0** (USB disconnected)	0.83	mA
	WCDMA PF = 64 (USB disconnected)	1.55	mA
	WCDMA PF = 128 (USB disconnected)	1.24	mA
	WCDMA PF = 256 (USB disconnected)	1.07	mA
	WCDMA PF = 512 (USB disconnected)	1.00	mA
	LTE-FDD PF = 32 (USB disconnected)	2.97	mA
	LTE-FDD PF = 64 (USB disconnected)	1.93	mA
	LTE-FDD PF = 128 (USB disconnected)	1.43	mA
	LTE-FDD PF = 256 (USB disconnected)	1.17	mA
Idle State	WCDMA PF = 64 (USB disconnected)	14.9	mA
	WCDMA PF = 64 (USB connected)	34.2	mA
	LTE-FDD PF = 64 (USB disconnected)	15.2	mA
	LTE-FDD PF = 64 (USB connected)	34.8	mA
WCDMA data transmission (GNSS OFF)	WCDMA B2 HSDPA @ 22.1 dBm	548.0	mA
	WCDMA B2 HSUPA @ 22.28 dBm	545.0	mA

[5] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[6] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

	WCDMA B4 HSDPA @ 22.2 dBm	580.0	mA
	WCDMA B4 HSUPA @ 22.2 dBm	596.0	mA
	WCDMA B5 HSDPA @ 22.1 dBm	498.0	mA
	WCDMA B5 HSUPA @ 22.0 dBm	500.0	mA
LTE data transmission (GNSS OFF)	LTE-FDD B2 @ 23.36 dBm	621.0	mA
	LTE-FDD B4 @ 22.7 dBm	702.0	mA
	LTE-FDD B5 @ 22.7 dBm	564.0	mA
	LTE-FDD B12 @ 22.66 dBm	648.0	mA
	LTE-FDD B13 @ 22.79 dBm	617.0	mA
	LTE-FDD B14 @ 22.72 dBm	622.0	mA
	LTE-FDD B66 @ 22.86 dBm	698.0	mA
	LTE-FDD B71 @ 22.73 dBm	628.0	mA

5.4.1. GNSS Power Consumption

Table 39: GNSS Power Consumption

Description	Condition	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Passive Antenna	54.0	mA
	Lost state @ Passive Antenna	53.9	mA
Tracking (**AT+CFUN=0**)	Instrument Environment	30.5	mA
	Open Sky @ Passive Antenna	33.2	mA
	Open Sky @ Active Antenna	40.8	mA

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 40: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit

VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

5.6. Thermal Dissipation

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high-power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and you can choose one or both of them according to their application structure.

Figure 40: Referenced Heatsink Design (Heatsink at the Top of the Module)

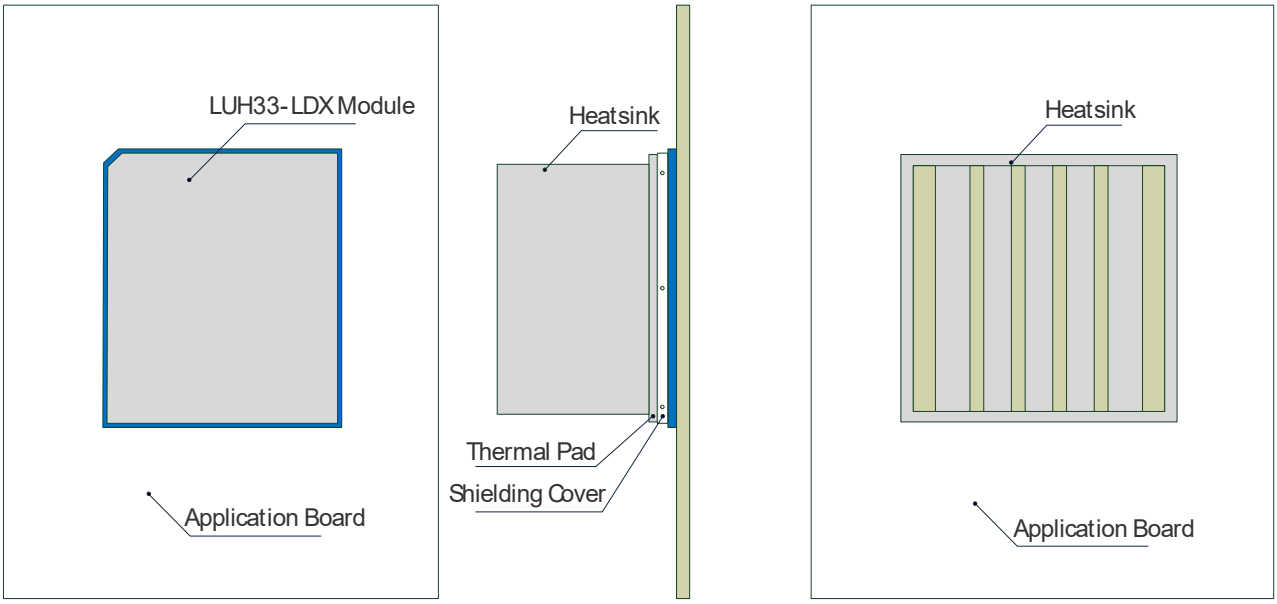
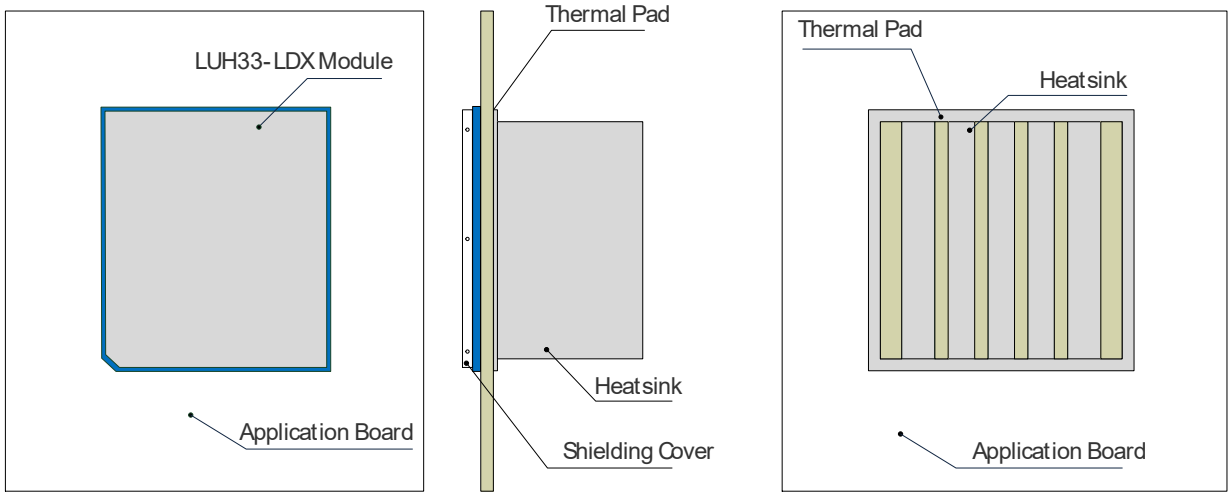


Figure 41: Referenced Heatsink Design (Heatsink at the Backside of the PCB)



NOTE

The module offers the best performance when the internal BB chip stays below 105 °C. When the maximum temperature of the BB chip reaches or exceeds 105 °C, the module works normal but provides reduced performance (such as RF output power and data rate). When the maximum BB chip temperature reaches or exceeds 115 °C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 115 °C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105 °C. Customers can execute **AT+QTEMP** and get the maximum BB chip temperature from the first returned value. For details of the command, see ***document 8***.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

Figure 42: Module Top and Side Dimensions

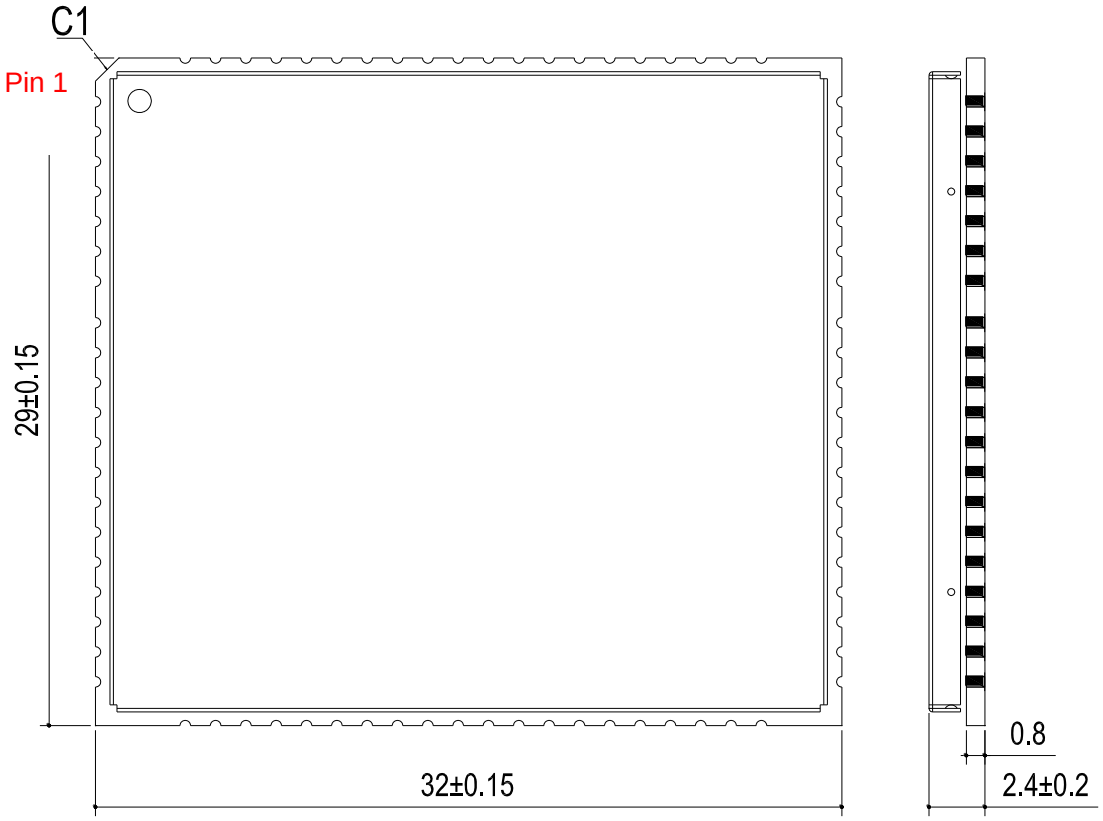
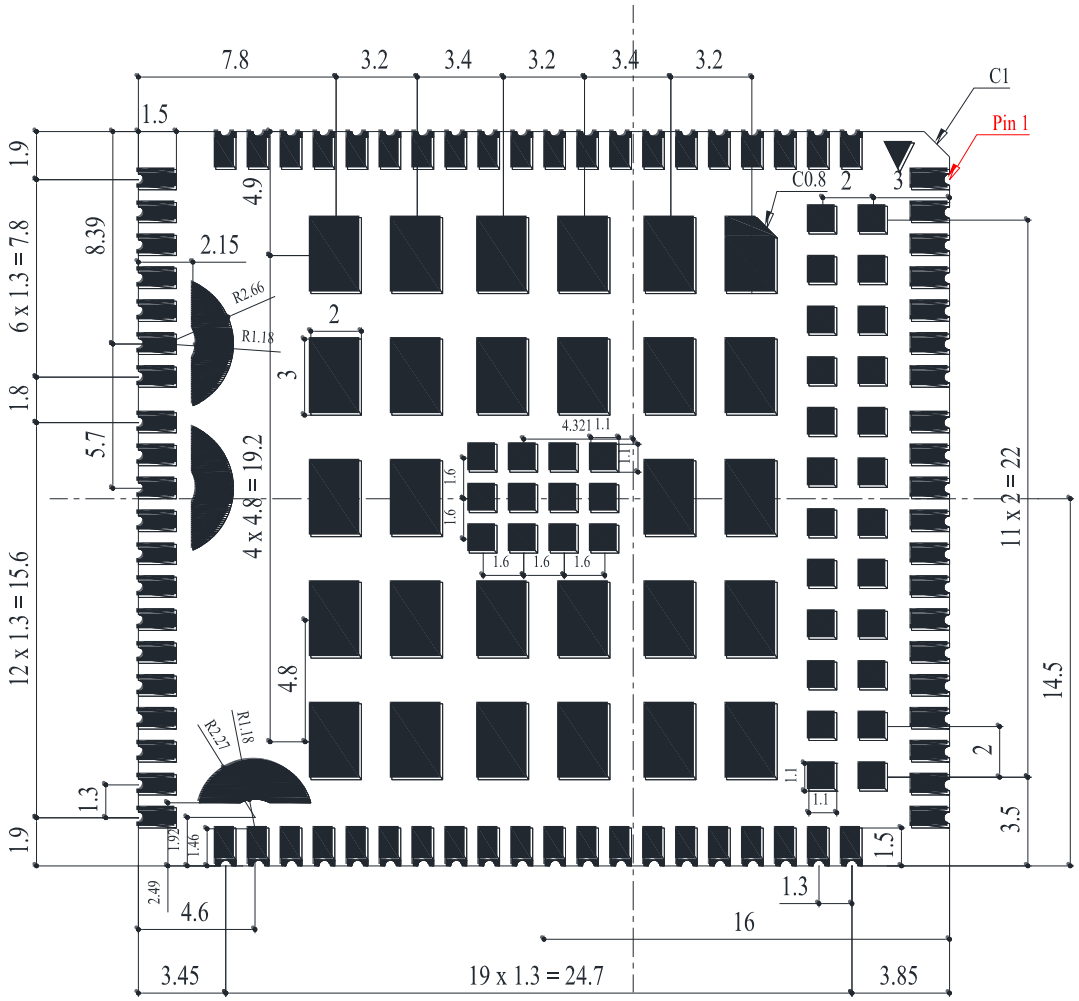


Figure 43: Bottom Dimensions (Bottom View)

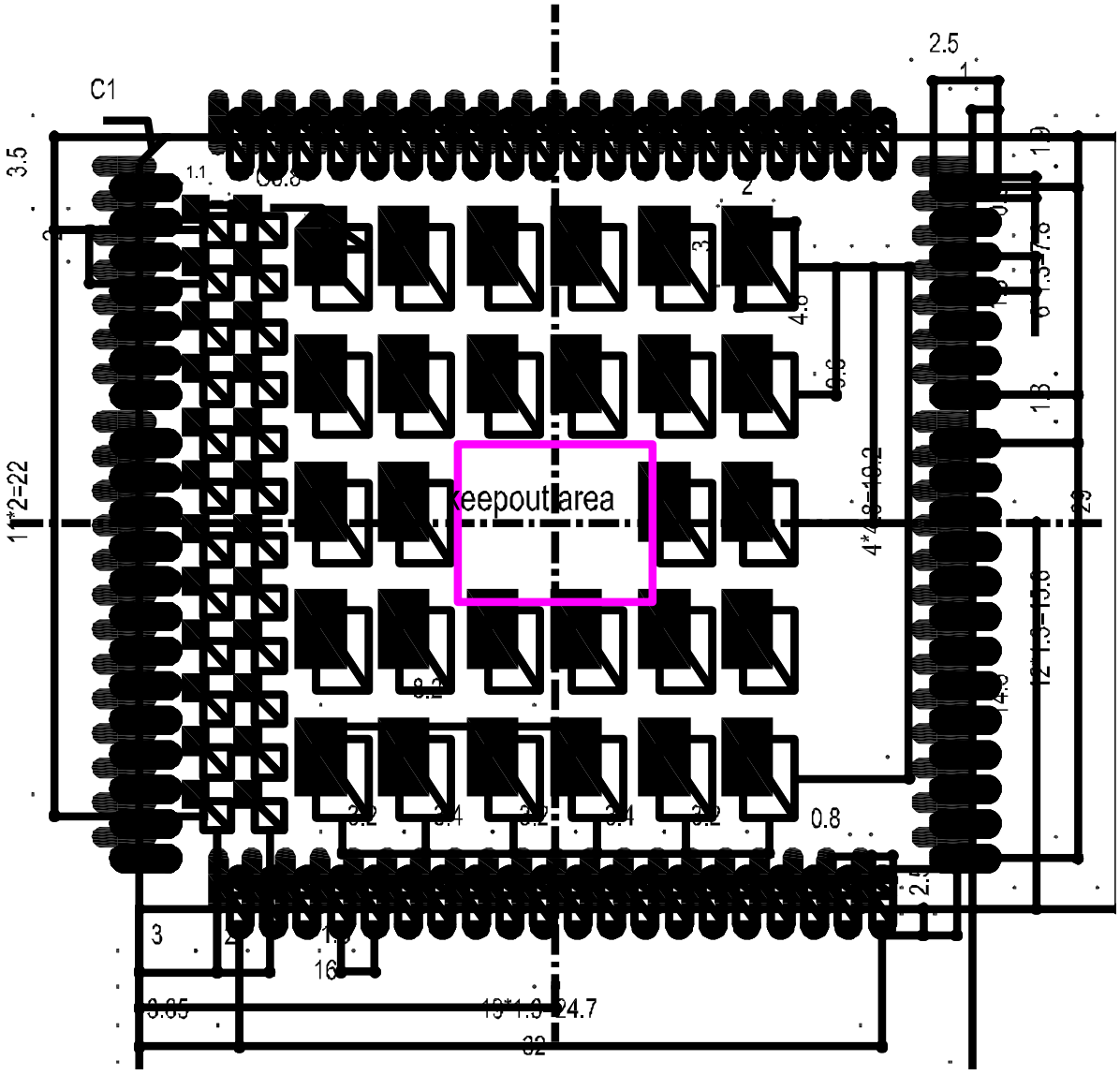


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

6.2. Recommended Footprint

Figure 44: Recommended Footprint

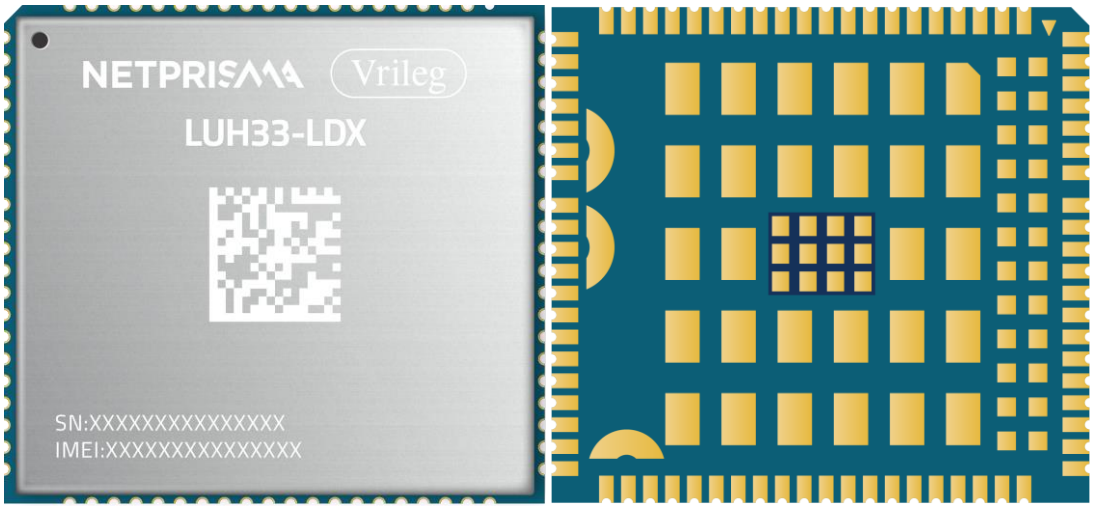


NOTE

1. The keepout area (pins 73–84) should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

Figure 45: Top and Bottom Views of the Module



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

7 Storage, Manufacturing & Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.20 mm. For more details, see ***document 9***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 46: Reflow Soldering Thermal Profile

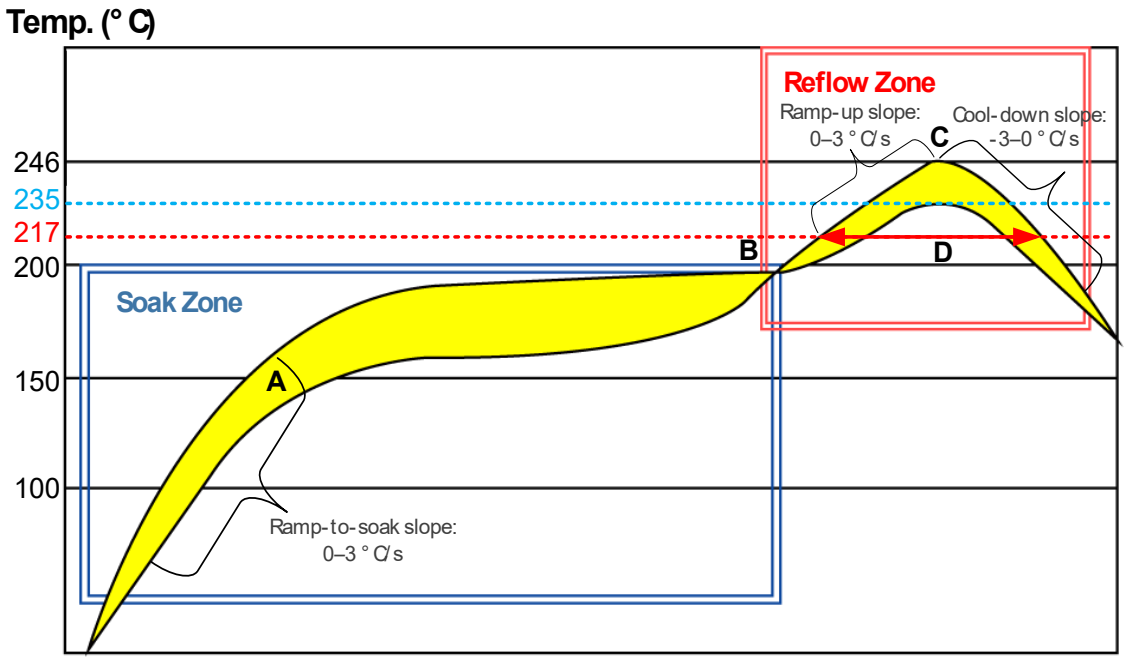


Table 41: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max. Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
6. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document 10***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 47: Carrier Tape Dimension Drawing (Unit: mm)

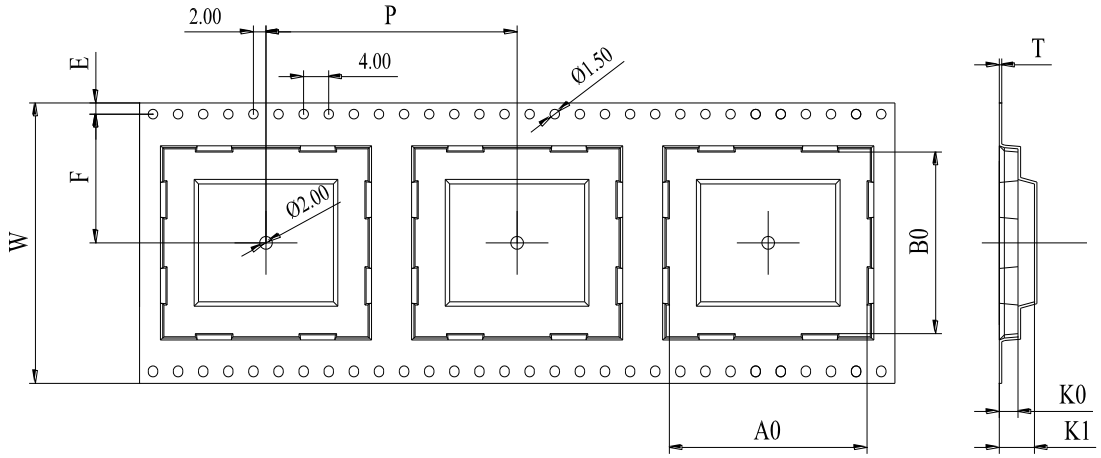


Table 42: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3	3.8	20.2	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 48: Plastic Reel Dimension Drawing

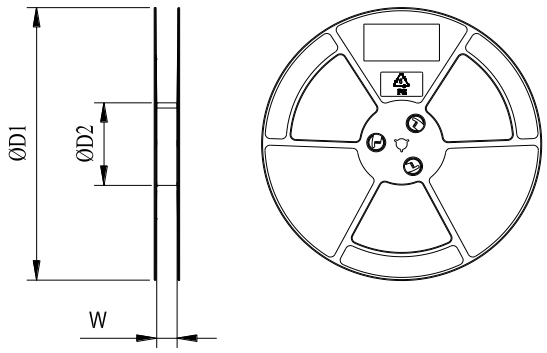
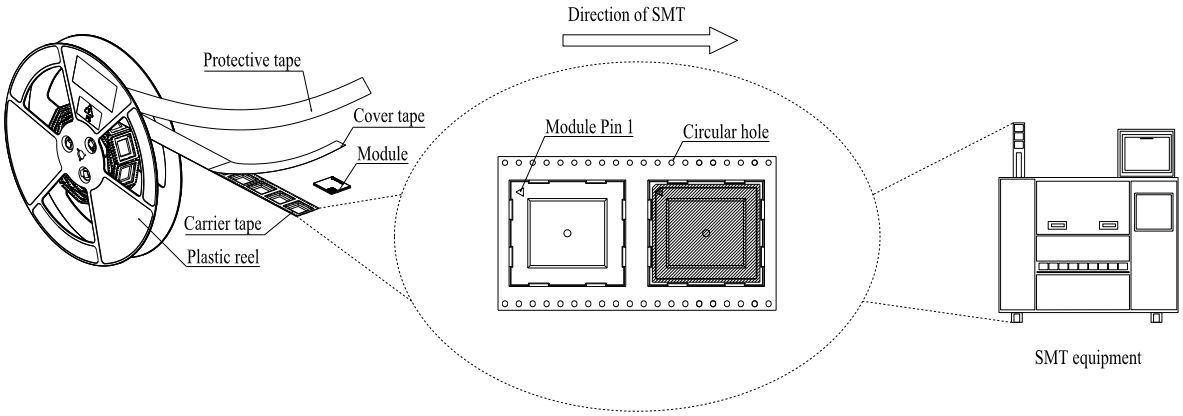


Table 43: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

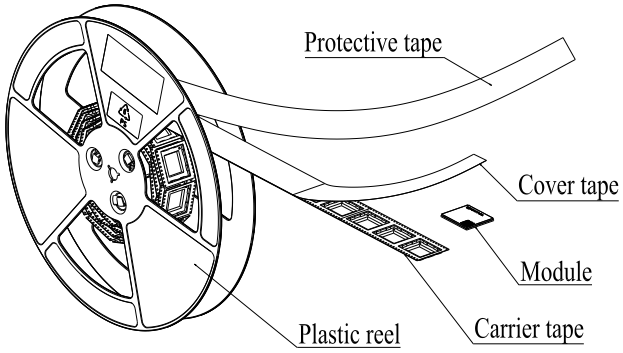
7.3.3. Mounting Direction

Figure 49: Mounting Direction



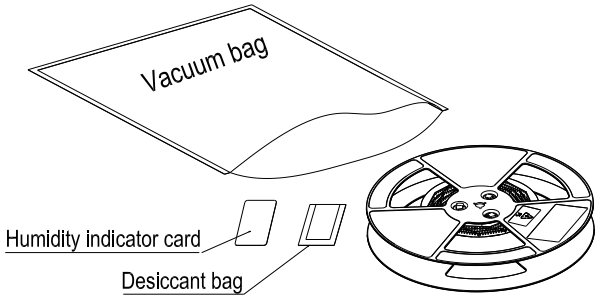
7.3.4. Packaging Process

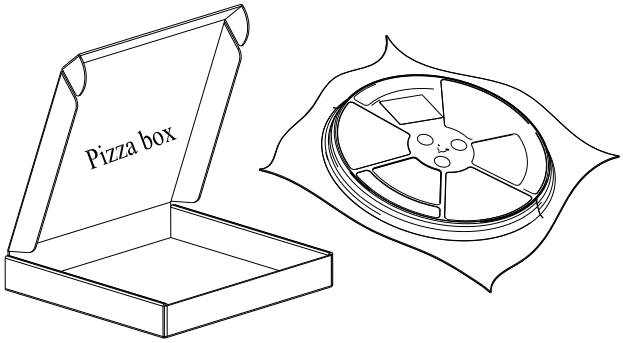
Figure 54: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can load 250 modules.

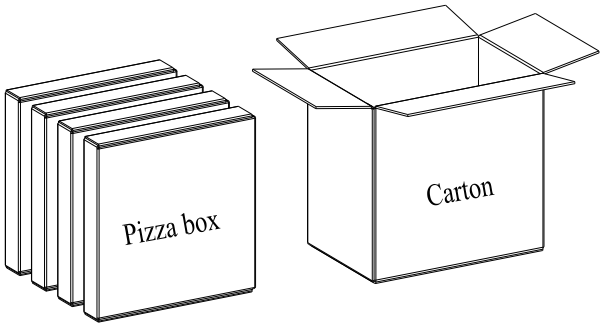
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.



8 Appendix

8.1. References

Table 44: Related Documents

Document Name
1. NetPrisma-LUH33-LDX-GNSS-Application-Note
2. NetPrisma-UMTS&LTE-EVB-User-Guide
3. NetPrisma-LUH33-LDX-AT-Commands-Manual
4. NetPrisma-LUH33-LDX-QCFG-AT-Commands-Manual
5. NetPrisma-LUH33-LDX-Low-Power-Mode-Application-Note
6. NetPrisma-LUH33-LDX-Reference-Design
7. NetPrisma-RF-Layout-Application-Note
8. NetPrisma-LUH33-LDX-Software-Thermal-Management-Guide
9. NetPrisma-Module-Stencil-Design-Requirements
10. NetPrisma-Module-SMT-Application-Note

Table 45: List of Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
AGNSS	Assisted GNSS (Global Navigation Satellite System)
AMR	Adaptive Multi-rate
APT	Average Power Tracking
BDS	BeiDou Navigation Satellite System
bps	bits per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme

CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DC-HSPA+	Dual-carrier High Speed Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FDD	Frequency Division Duplex
FILE	File Protocol
FR	Full Rate
FTPS	FTP over SSL
FTP	File Transfer Protocol
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Russian Global Navigation Satellite System
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output

Inom	Nominal Current
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LTE	Long Term Evolution
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
MCU	Microcontroller Unit
MDIO	Management Data Input/Output
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Chip
MMS	Multimedia Messaging Service
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MS	Mobile Station (GSM engine)
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
NAND	Non-volatile Memory Device
NITZ	Network Identity and Time Zone / Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PA	Power Amplifier
PAM	Power Amplifier Module
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation

PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PTP	Precision Time Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
Rx	Receive
SAW	Surface Acoustic Wave
SDR	Single Data Rate
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identity Module
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter

UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VLAN	Virtual Local Area Network
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

FCC Statement

FCC ID: 2BEY3LUH33LDXA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NetPrisma that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: 2BEY3LUH33LDXA”
“Contains IC: 32052-LUH33LDXA “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Antenna Type	Max Gain	
External Antenna	LTE Band 2: 1.59dBi LTE Band 4: 2.0dBi LTE Band 5: 2.13dBi LTE Band 12: 3.26dBi LTE Band 13: 4.45dBi LTE Band 14: 3.63dBi LTE Band 66: 2.0dBi LTE Band 71: 1.22dBi	WCDMA Band 2: 1.59dBi WCDMA Band 4: 2.0dBi WCDMA Band 5: 2.13dBi

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27 and part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC Statement

IC: 32052-LUH33LDXA

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 32052-LUH33LDXA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 32052-LUH33LDXA ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Document History

Revision	Date	Changes
A	2025-02-11	The first revision.

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