LUH32-WWD&LUH33-WWD

Hardware Design

Rev.0.1 – Draft – 2025-01-22

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Contents

Table Index

Figure Index

1 Introduction

This document defines LUH32-WWD&LUH33-WWD, and describes its air interfaces and hardware interfaces which are connected with your applications.

With this document, you can quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1 Text Conventions

Table 1: Text Conventions

dev	Unless stated otherwise, the presence of the mark "dev" following a function, feature, interface, pin name, command, argument, etc., signifies that it is still in the development phase and not yet supported. Additionally, when "dev" appears after a model, it indicates that the model sample is currently unavailable.
NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

2.1 Frequency Bands and Functions

LUH32-WWD&LUH33-WWD is LTE/WCDMA/GSM wireless communication modules with receive diversity. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. It also provides GNSS and voice functionality for your specific applications. The following table shows the supported frequency bands, GNSS and digital audio functions of LUH32-WWD&LUH33-WWD .

Table 2: Frequency Bands and Functions

Mode/Function	LUH32-WWD&LUH33-WWD
GSM	GSM850/EGSM900/DCS1800/PCS1900
WCDMA (With receive diversity)	B1/B2/B4/B5/B6/B8/B19
LTE-FDD (With receive diversity)	B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/B19/B20/B25/B26/B28/B66
LTE-TDD (With receive diversity)	B34/B38/B39/B40/B41
GNSS (Optional)	GPS, GLONASS, BDS, Galileo, QZSS
Digital Audio (PCM)	Supported
VoLTE (Voice over LTE)	Optional

LUH32-WWD&LUH33-WWD is an SMD type module which can be embedded into applications through its 144 LGA pins. With a compact profile of 29.0 mm × 32.0 mm × 2.4 mm, it can meet most requirements for M2M and IoT applications.
Note: B40 is not used for FCC and IC areas.

2.2 Key Features

The following table describes the detailed features of LUH32-WWD&LUH33-WWD.

Table 3: Key Features of LUH32-WWD&LUH33-WWD

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for GSM850 ● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800

	● Class 1 (30 dBm ±2 dB) for PCS1900 ● Class E2 (27 dBm ±3 dB) for GSM850 8-PSK ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class E2 (26 dBm ±3 dB) for PCS1900 8-PSK ● Class 3 (23 dBm ±2 dB) for WCDMA bands ● Class 3 (23 dBm ±2 dB) for LTE bands
LTE Features	● Supported non-CA category: **LUH32-WWD:** Support up to UL/DL Cat 1 **LUH33-WWD::** Support up to UL/DL Cat 4 ● Support 1.4/3/5/10/15/20 MHz RF bandwidth ● Supported modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK and 16QAM ● Support MIMO in DL direction (only for LUH33-WWD) ● Maximum transmission rates: **LUH32-WWD:** – LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL) – LTE-TDD: Max. 8.96 Mbps (DL), Max. 3.1 Mbps (UL) **LUH33-WWD:** – LTE-FDD: Max. 150 Mbps (DL), Max. 50 Mbps (UL) – LTE-TDD: Max. 130 Mbps (DL), Max. 30 Mbps (UL)
UMTS Features	● Support 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supported modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL), Max. 384 kbps (UL)
GSM Features	● **GPRS:** – Support GPRS multi-slot class 33 (33 by default) – Coding scheme: CS 1–4 – Max. 107 kbps (DL), Max. 85.6 kbps (UL) ● **EDGE:** – Support EDGE multi-slot class 33 (33 by default) – Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) – Downlink coding schemes: MCS 1–9 – Uplink coding schemes: MCS 1–9 – Max. 296 kbps (DL), Max. 236.8 kbps (UL)
Internet Protocol Features	● Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/NITZ/SMTP/ MQTT/CMUX/HTTPS/FTPS/SMTPS/SSL/MMS/FILE protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Support (U)SIM card: 1.8 V and 3.0 V
Audio Features	● Support one digital audio interface: PCM interface ● GSM: HR/FR/EFR/AMR/AMR-WB ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
USB Interface	● Compliant with USB 2.0 specification (slave only); the data transmission rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB ● Support USB serial drivers: Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x, etc.
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission

	● Baud rates reach up to 921600 bps, 115200 bps by default ● Support RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● Baud rate: 115200 bps by default
PCM Interface	● Used for audio function with external codec ● Support 16-bit linear data format ● Support long frame synchronization and short frame synchronization ● Support master and slave modes in short frame synchronization, and only support master mode in long frame synchronization
SD Card Interface	Support SD 3.0 protocol
SGMII Interface dev	● Support 10/100/1000 Mbps Ethernet work mode ● Support maximum 150 Mbps (DL)/50 Mbps (UL) for 4G network
WLAN and Bluetooth Application Interfaces dev	● WLAN application interface: SDIO 3.0 ● Bluetooth application interface: UART and PCM
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features (Optional)	● Protocol: NMEA 0183 ● Data update rate: 1 Hz by default ● Support AGNSS. For more details, see ***document 6***
AT Commands	● Compliant with *3GPP TS 27.007, 3GPP TS 27.005* ● Compliant with NetPrisma enhanced AT commands
Network Indication	Two pins NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Rx-diversity antenna interface (ANT_DIV) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Size: (29.0 ±0.2) mm × (32.0 ±0.2) mm × (2.4 ±0.2) mm ● Package: LGA ● Weight: approx. 4.9 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [1] ● Extended temperature range: -40 °C to +85 °C [2] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

NOTE

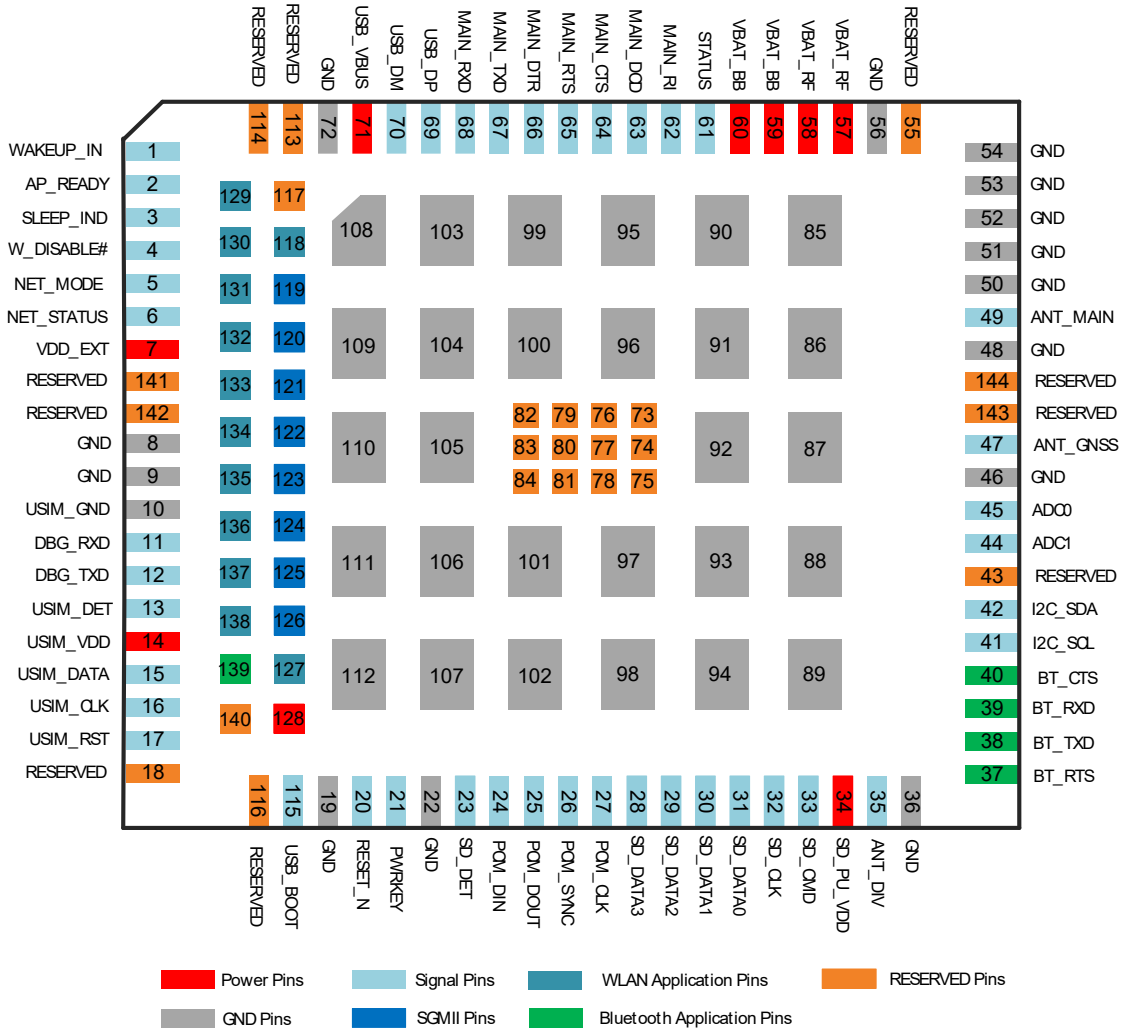
Limited by the flash size of the module, LUH32-WWD&LUH33-WWD does not support SGMII function currently. If needed, please contact NetPrisma Technical Support.

2.3 Pin Assignment

The following figure shows the pin assignment of the module.

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Figure 1: Pin Assignment (Top View)



NOTE

1. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact NetPrisma Technical Support.
2. USB_BOOT and BOOT_CONFIG property pins (WAKEUP_IN, NET_MODE, WLAN_EN [dev], COEX_RXD [dev], COEX_TXD [dev] and BT_CTS [dev]) cannot be pulled up before startup.
3. USB_BOOT and COEX_RXD are connected inside the module and share the same network.
4. Pins 24–27 can be used not only for audio function of the PCM interface, but also for Bluetooth function [dev].
5. Keep all RESERVED pins and unused pins unconnected.
6. GND pins 85–112 should be connected to ground in the design. RESERVED pins 73–84 should not be designed in schematic and PCB decal, and these pins should be served as a keepout area.
7. Pins 119–122 and 128 can be multiplexed into USIM2 interface via **AT+QDSIM=1**. For more details about the AT command, contact NetPrisma Technical Support. For more details about the pin multiplexed function of (U)SIM2 interface, see ***Table 11***.

2.4 Pin Description

The following tables show the pin definition of the module.

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	59, 60	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A. A test point is recommended to be reserved.
VBAT_RF	57, 58	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 1.8 A in a burst transmission. A test point is recommended to be reserved.
VDD_EXT	7	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	21	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the chipset.

					A test point is recommended to be reserved.
RESET_N	20	DI	Reset the module	Vnom = 1.8 V V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	A test point is recommended to be reserved.

Indication Signals

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	61	OD	Indicate the module's operation status	VDD_EXT	The driving current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.
NET_MODE	5	DO	Indicate the module's registered network status		Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status		If unused, keep them open.
SLEEP_IND	3	DO	Indicate the module's sleep status		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	71	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	69	AIO	USB 2.0 differential data (+)		USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)		

(U)SIM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	10	-	Specified ground for (U)SIM		
USIM_DET	13	DI	(U)SIM card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM_VDD	14	PO	(U)SIM card power supply	$I_O$max = 50 mA **Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	USIM_VDD	
USIM_CLK	16	DO	(U)SIM card clock		

USIM_RST	17	DO	(U)SIM card reset		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RI	62	DO	Main UART ring indication	VDD_EXT	If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect		
MAIN_CTS	64	DO	Clear to send signal from the module		If unused, keep it open. Connect to MCU's CTS.
MAIN_RTS	65	DI	Request to send signal to the module		If unused, keep it open. Connect to MCU's RTS.
MAIN_DTR	66	DI	Main UART data terminal ready		Pulled up by default. MAIN_DTR at low level can wake up the module. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit		If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	12	DO	Debug UART transmit	VDD_EXT	Test points must be reserved.
DBG_RXD	11	DI	Debug UART receive		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	45	AI	General-purpose analog to digital converter	Input voltage range: 0.3 V to VBAT_BB	If unused, keep them open.
ADC1	44	AI	General-purpose analog to digital converter		
PCM Interface [3]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_DIN	24	DI	PCM data input	VDD_EXT	If unused, keep them open.
PCM_DOUT	25	DO	PCM data output		
PCM_SYNC	26	DIO	PCM data frame sync		Master mode: output. Slave mode: input.

[3] Pins 24–27 can be used not only for audio function of the PCM interface, but also for Bluetooth function [dev].

PCM_CLK	27	DIO	PCM clock		If unused, keep them open.

I2C Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SCL	41	OD	I2C serial clock (for external codec)	VDD_EXT	Externally pulled up to 1.8 V. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data (for external codec)		

SD Card Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SD_DATA0	31	DIO	SDIO data bit 0	SD_PU_VDD	SDIO signal level can be selected according to the signal level supported by SD card. See SD 3.0 protocol for more details. If unused, keep them open.
SD_DATA1	30	DIO	SDIO data bit 1		
SD_DATA2	29	DIO	SDIO data bit 2		
SD_DATA3	28	DIO	SDIO data bit 3		
SD_CLK	32	DO	SD card clock		
SD_CMD	33	DIO	SD card command		
SD_DET	23	DI	SD card hot-plug detect	VDD_EXT	Keep it open if SD card is unused, and it must be connected if SD card is used.
SD_PU_VDD	34	PO	1.8/2.85 V output power for SD card pull-up circuits	$I_O$max = 50 mA **Low-voltage:** Vnom = 1.8 V **High-voltage:** Vnom = 2.85 V	Cannot be used for SD card power. If unused, keep it open.

WLAN & Bluetooth Application Interfaces dev

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SDC_DATA0	132	DIO	WLAN SDIO data bit 0	VDD_EXT	If unused, keep them open.
SDC_DATA1	131	DIO	WLAN SDIO data bit 1		
SDC_DATA2	130	DIO	WLAN SDIO data bit 2		
SDC_DATA3	129	DIO	WLAN SDIO data bit 3		
SDC_CLK	133	DO	WLAN SDIO clock		
SDC_CMD	134	DIO	WLAN SDIO command		
WLAN_PWR_EN	127	DO	WLAN power supply enable control		Active high. Cannot be pulled up before startup. If unused, keep it open.

WAKE_ON_WIRELESS	135	DI	WLAN/Bluetooth wakeup signal to the module		Active low. If unused, keep it open.
WLAN_EN	136	DO	WLAN function enable control		Active high. Cannot be pulled up before startup. If unused, keep it open.
COEX_RXD	137	DI	LTE & WLAN/ Bluetooth coexistence receive		Cannot be pulled up before startup. If unused, keep them open.
COEX_TXD	138	DO	LTE & WLAN/ Bluetooth coexistence transmit		
WLAN_SLP_CLK	118	DO	WLAN sleep clock		If unused, keep it open.
BT_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
BT_TXD	38	DO	Bluetooth UART transmit		If unused, keep them open.
BT_RXD	39	DI	Bluetooth UART receive		
BT_CTS	40	DO	Clear to send signal from the module		Connect to MCU's CTS. Cannot be pulled up before startup. If unused, keep it open.
BT_EN	139	DO	Bluetooth enable control		If unused, keep it open.

SGMII Interface [dev]

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SGMII_RST_N	119 [4]	DO	Ethernet PHY reset	SGMII_MDIO_VDD	If unused, keep it open.
SGMII_INT_N	120 [4]	DI	Ethernet PHY interrupt	VDD_EXT	If unused, keep it open.
SGMII_MDIO	121 [4]	DIO	SGMII management data	SGMII_MDIO_VDD	Externally pulled up to SGMII_MDIO_VDD, and the pull-up resistor is 1.5 kΩ. If unused, keep it open.
SGMII_MDC	122 [4]	DO	SGMII management data clock		If unused, keep it open.
SGMII_TX_M	123	AO	SGMII transmit (-)		Add a 0.1 μF capacitor close to the PHY chip. If unused, keep it open.
SGMII_TX_P	124	AO	SGMII transmit (+)		
SGMII_RX_P	125	AI	SGMII receive (+)		Add a 0.1 μF capacitor close to the module. If unused, keep them
SGMII_RX_M	126	AI	SGMII receive (-)		

[4] Pins 119–122 and 128 can be multiplexed into USIM2 interface via **AT+QDSIM=1**. For more details about the AT command, contact NetPrisma Technical Support. For more details about the pin multiplexed function of (U)SIM2 interface, see ***Table 11***.

					open.
SGMII_MDIO_VDD	128 [4]	PO	SGMII_MDIO pull up power supply	$I_O$max = 50 mA **Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V	Configurable power source. If unused, keep it open.

Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_DIV	35	AI	Diversity antenna interface		50 Ω characteristic impedance. If unused, keep it open.
ANT_MAIN	49	AIO	Main antenna interface		50 Ω characteristic impedance.
ANT_GNSS	47	AI	GNSS antenna interface		50 Ω characteristic impedance. If unused, keep it open.

Other Interface Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WAKEUP_IN	1	DI	External wakeup signal to the module	VDD_EXT	Cannot be pulled up before startup. WAKEUP_IN at low level can wake up the module. If unused, keep it open.
W_DISABLE#	4	DI	Airplane mode control		Pulled up by default. If unused, keep it open.
AP_READY	2	DI	Application processor ready		If unused, keep it open.
USB_BOOT	115	DI	Force the module into download mode		Cannot be pulled up before startup. A test point is recommended to be reserved.

RESERVED Pins

Pin Name	Pin No.	Comment
RESERVED	18, 43, 55, 73–84, 113, 114, 116, 117, 140–144	Keep them unconnected.

2.5 EVB Kit

NetPrisma supplies an evaluation board (UMTS & LTE EVB) with accessories to develop and test the module. For more details, see ***document 1***.

3 Operating Characteristics

3.1 Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate.
Airplane Mode	**AT+CFUN=4** or W DISABLE# pin can set the module to enter airplane mode. In this case, RF function will be invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Sleep Mode	The power consumption of the module will be reduced to an ultra-low level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	The power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

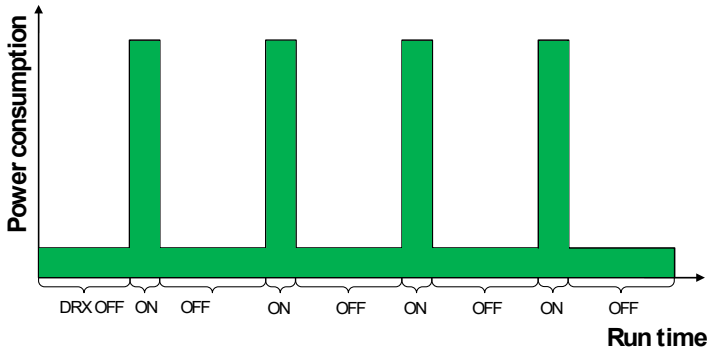
NOTE

See ***document 2*** for details of **AT+CFUN**.

3.2 Sleep Mode

In sleep mode, the module reduces power consumption to an ultra-low level.

Figure 2: Module Power Consumption in Sleep Mode



NOTE

DRX cycle values are transmitted over the wireless network.

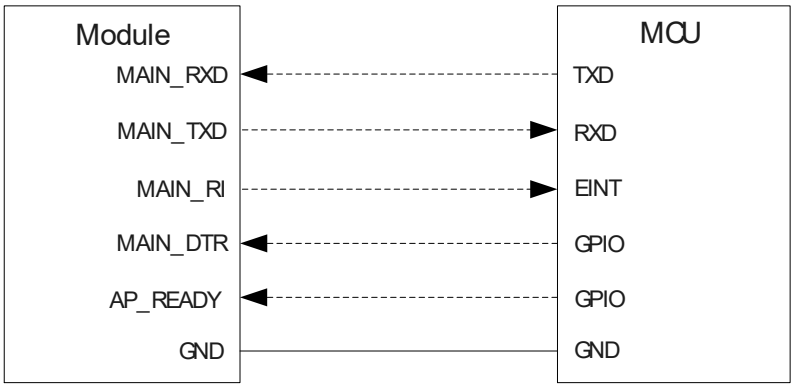
3.2.1 UART Application Scenario

If the MCU communicates with module via UART interfaces, the following preconditions can make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode. For details of the command, see ***document 2***.
- Drive MAIN_DTR to high level.
- Make sure that USB_VBUS is kept low or unconnected.

The following figure shows the connection between the module and the MCU.

Figure 3: Sleep Mode Application via UART



- Driving MAIN_DTR to low level will wake up the module.
- When the module has a URC to report, MAIN_RI will wake up the MCU. See ***Chapter 4.9.4*** for details about MAIN_RI behaviors.
- AP_READY will detect the sleep state of the MCU (It can be configured to high-level or low-level detection). See ***document 3*** for details about **AT+QCFG="apready"**.

NOTE

Pay attention to the level match shown in dotted line between the module and the MCU.

3.2.2 USB Application Scenario

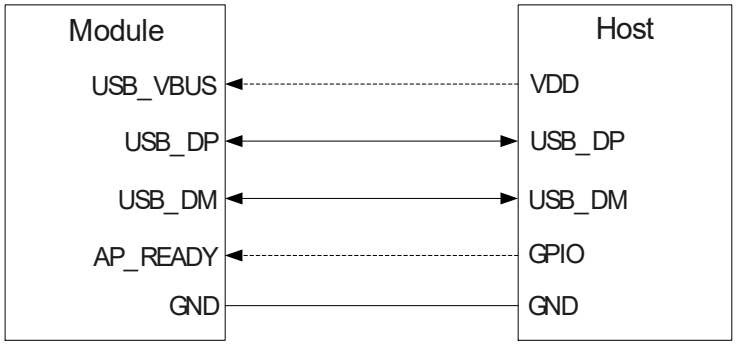
3.2.2.1 USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to set the module to sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

Figure 4: Sleep Mode Application with USB Remote Wakeup



- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, it will send remote wakeup signals via USB bus to wake up the host.

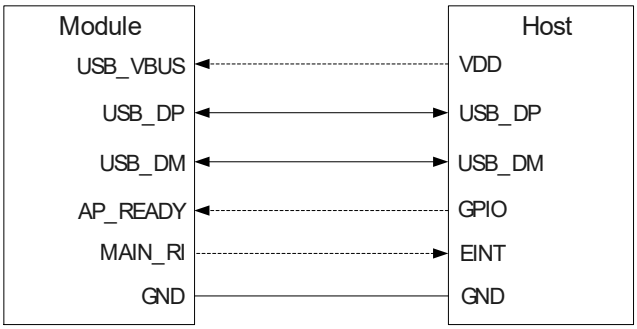
3.2.2.2 USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend and Resume, but does not support remote wakeup function, MAIN_RI signal is needed to wake up the host.
There are three preconditions to set the module to sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters Suspend state.

The following figure shows the connection between the module and the host.

Figure 5: Sleep Mode Application with MAIN_RI



- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the host.

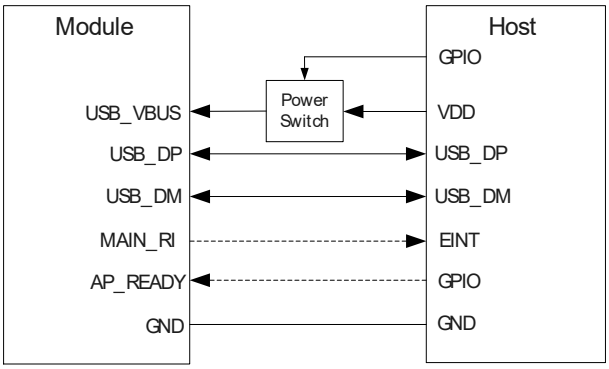
3.2.2.3 USB Application without USB Suspend Function

If the host does not support USB Suspend function, USB_VBUS should be disconnected with an external control circuit to set the module to sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

Figure 6: Sleep Mode Application without Suspend Function



Restore the power supply of USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in dotted line between the module and the host. For more details about the power management application of the module, see ***document 4***.

3.2.3 Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will make the module enter airplane mode.

Software:

AT+CFUN provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4. For more details about **AT+CFUN**, see ***document 2***.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

NOTE

1. The W_DISABLE# control function is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**. For more details, see ***document 3***.
2. The execution of **AT+CFUN** will not affect GNSS function.

3.3 Power Supply

3.3.1 Power Supply Pins

The module provides four VBAT pins for the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's BB part

The following table shows the details of VBAT pins and ground pins.

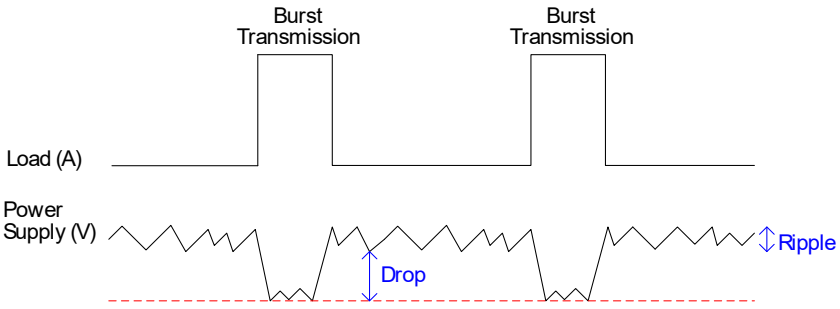
Table 7: Pin Definition of VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	59, 60	Power supply for module's BB part	3.3	3.8	4.3	V
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50–54, 56, 72, 85–112					

3.3.2 Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure that the input voltage will never drop below 3.3 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

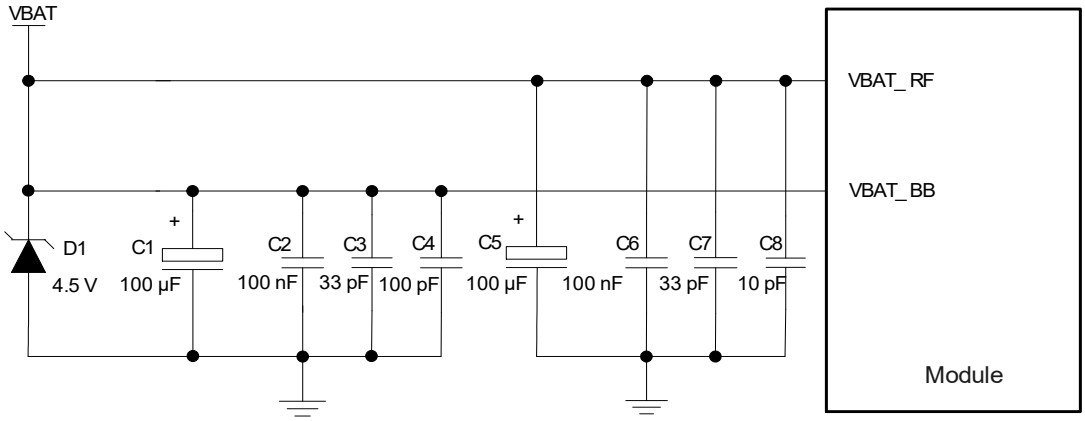
Figure 7: Power Supply Limits during Burst Transmission



To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω) should be used for VBAT_BB and VBAT_RF respectively, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use six ceramic capacitors (100 nF, 33 pF, 100 pF for VBAT_BB, and 100 nF, 33 pF, 10 pF for VBAT_RF) for composing the MLCC array, and place these capacitors close to VBAT_BB and VBAT_RF. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be at least 1 mm, and the width of VBAT_RF trace should be at least 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS diode with suggested low reverse stand-off voltage V_{RWM} 4.5 V, low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows the star structure of the power supply.

Figure 8: Star Structure of the Power Supply

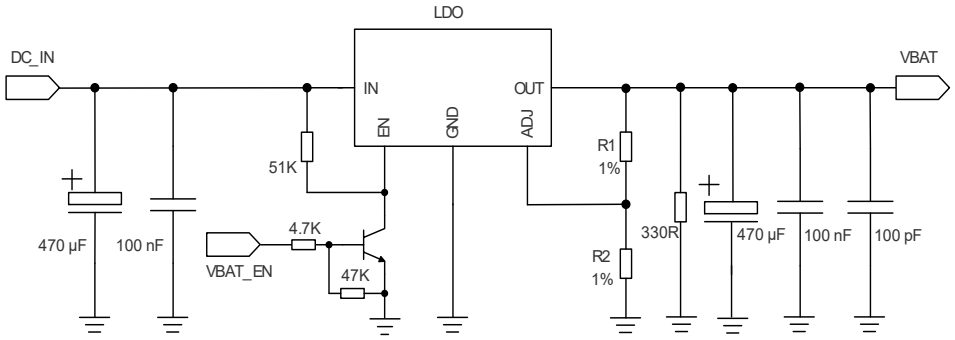


3.3.3 Reference Design for Power Supply

Power design for the module is very important. The power supply should be able to provide sufficient current up to 2 A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5.0 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

Figure 9: Reference Circuit of Power Supply



NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.3.4 Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document 2***.

3.4 Turn On

3.4.1 Turn On with PWRKEY

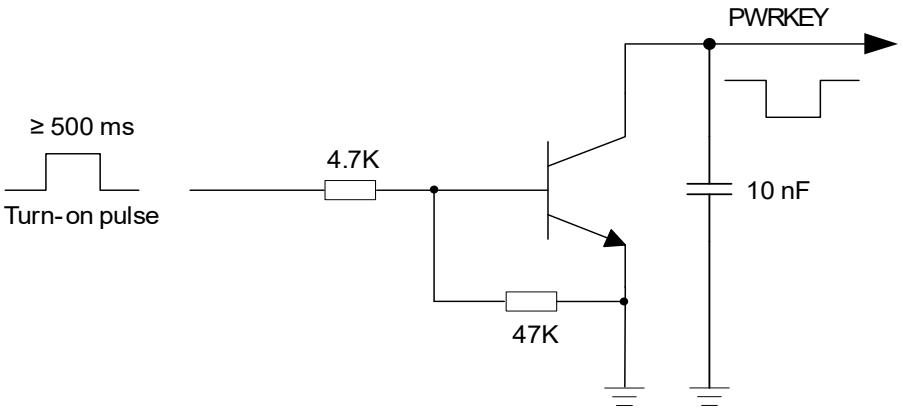
The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the chipset. A test point is recommended to be reserved.

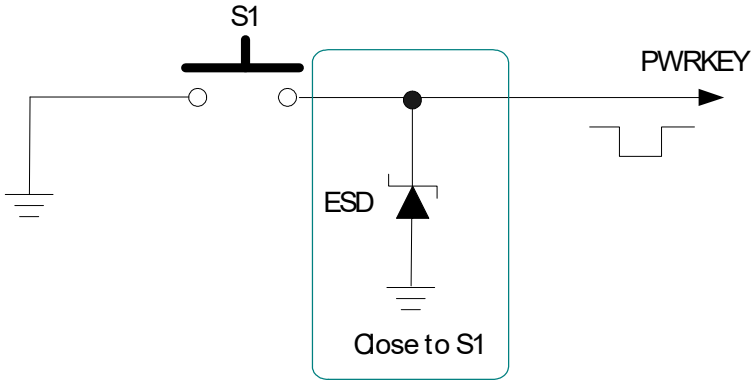
When the module is in turn-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY, and release it after the STATUS pin (requiring an external pull-up resistor) outputs a low level. The STATUS pin is used as an indicator to show that the module has been turned on normally. A simple reference circuit is illustrated in the following figure.

Figure 10: Turn On the Module by Using Driving Circuit



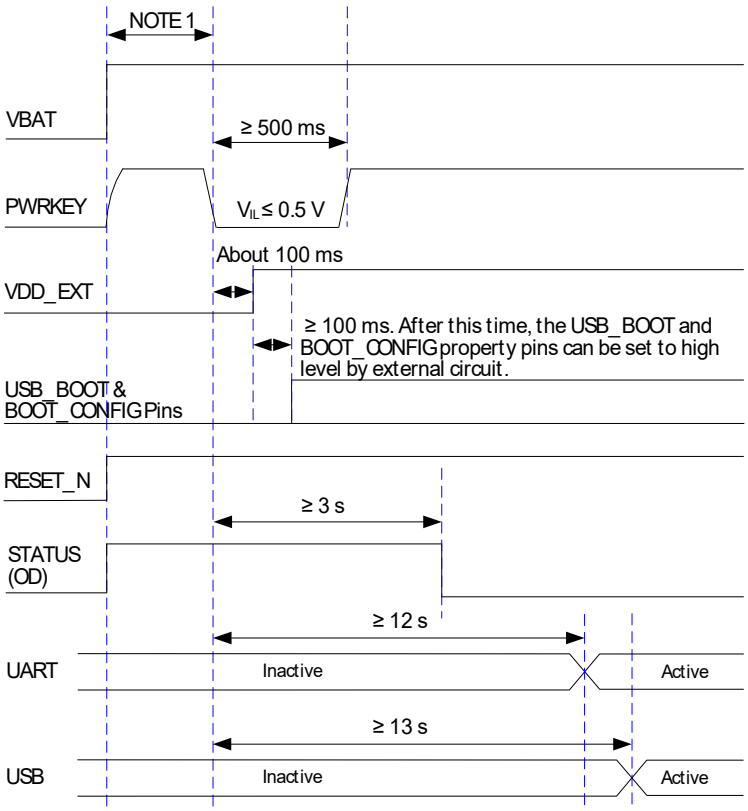
The other way to control the PWRKEY is to use a button. When pressing the button, electrostatic strike may generate from finger. Therefore, an ESD component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

Figure 11: Turn On the Module by Using a Button



The turn-on timing is illustrated in the following figure.

Figure 12: Turn-on Timing



NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor if the module needs to be turned on automatically and turnoff is not needed.
3. USB_BOOT and BOOT_CONFIG property pins (WAKEUP_IN, NET_MODE, WLAN_EN [dev], COEX_RXD [dev], COEX_TXD [dev] and BT_CTS [dev]) cannot be pulled up before startup.
4. Ensure that there is no large capacitance on the PWRKEY pin.

3.5 Turn Off

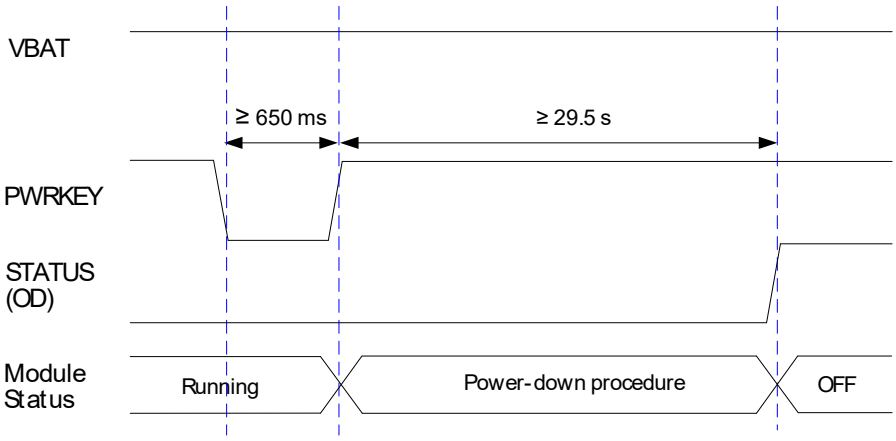
The following procedures can be used to turn off the module normally:

- Use the PWRKEY pin.
- Use **AT+QPOWD** command. For details of the command, see ***document 2***.

3.5.1 Turn Off with PWRKEY

Driving PWRKEY low for at least 650 ms, the module will execute power-down procedure after the PWRKEY is released. The turn-off timing is illustrated in the following figure.

Figure 13: Turn-off Timing



3.5.2 Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on again after successfully turn-off.

3.6 Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N low for 150–460 ms.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	A test point is recommended to be reserved.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

Figure 14: Reference Circuit of RESET_N by Using Driving Circuit

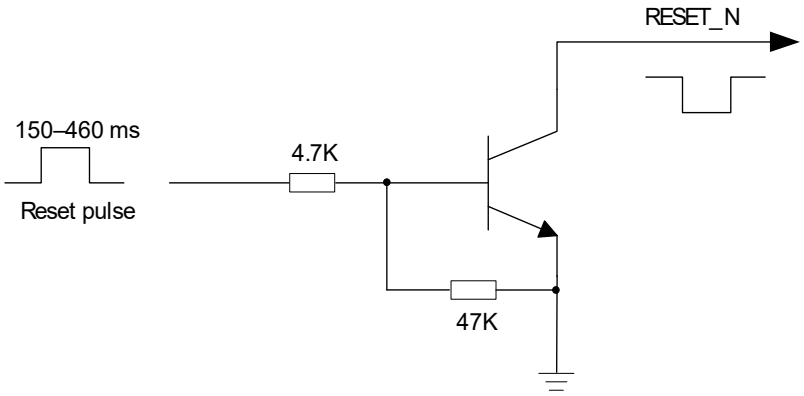
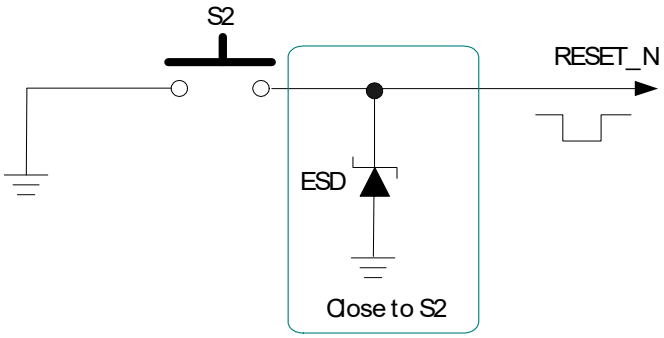
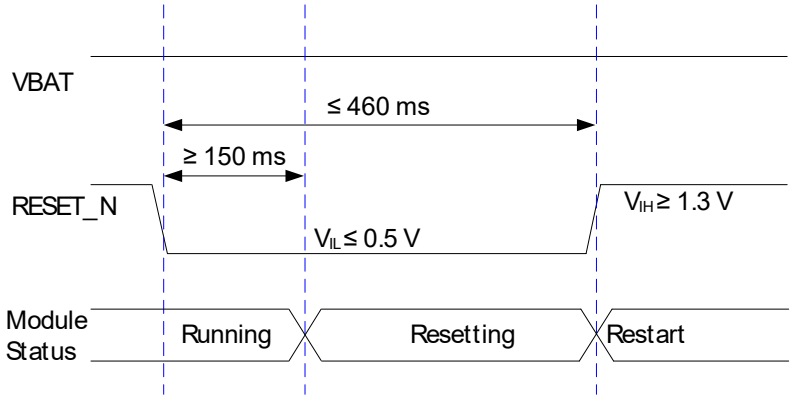


Figure 15: Reference Circuit of RESET_N by Using a Button



The reset timing is illustrated in the following figure.

Figure 16: Reset Timing



NOTE

1. Use RESET_N only when failed to turn off the module by **AT+QPOWD** and PWRKEY pin.
2. Ensure that there is no large capacitance on RESET_N pin.

4 Application Interfaces

4.1 (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	(U)SIM card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM_DATA	15	DIO	(U)SIM card data	
USIM_CLK	16	DO	(U)SIM card clock	
USIM_RST	17	DO	(U)SIM card reset	
USIM_DET	13	DI	(U)SIM card hot-plug detect	If unused, keep it open.
USIM_GND	10	-	Specified ground for (U)SIM	

Table 11: Pin Multiplexed Function of (U)SIM2 Interface

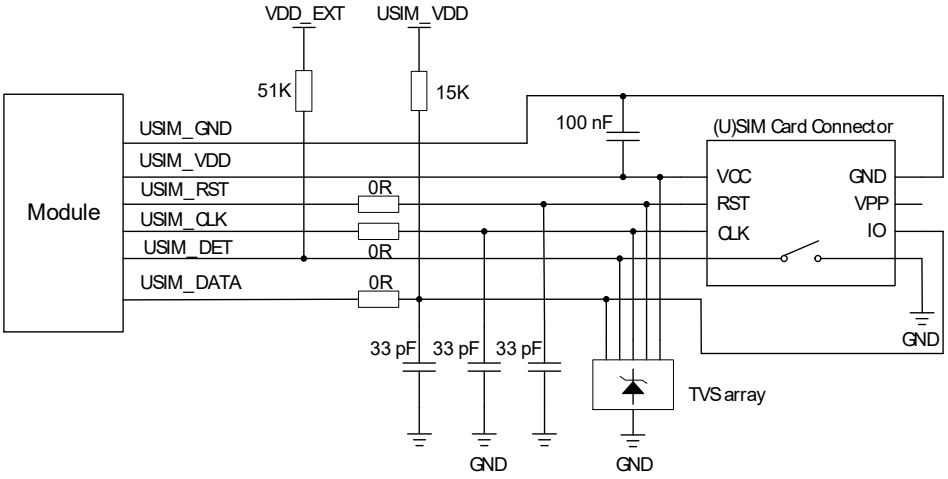
Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
SGMII_RST_N	119	USIM2_RST	DO	(U)SIM2 card reset	
SGMII_INT_N	120	USIM2_DET	DI	(U)SIM2 card hot-plug detect	If unused, keep it open.
SGMII_MDIO	121	USIM2_CLK	DO	(U)SIM2 card clock	
SGMII_MDC	122	USIM2_DATA	DIO	(U)SIM2 card data	
SGMII_MDIO_VDD	128	USIM2_VDD	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.

Pins 119–122 and 128 can be multiplexed into USIM2 interface via **AT+QDSIM=1**. For more details about the AT command, contact NetPrisma Technical Support.

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both high-level and low-level detection are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document 2*** for more details.

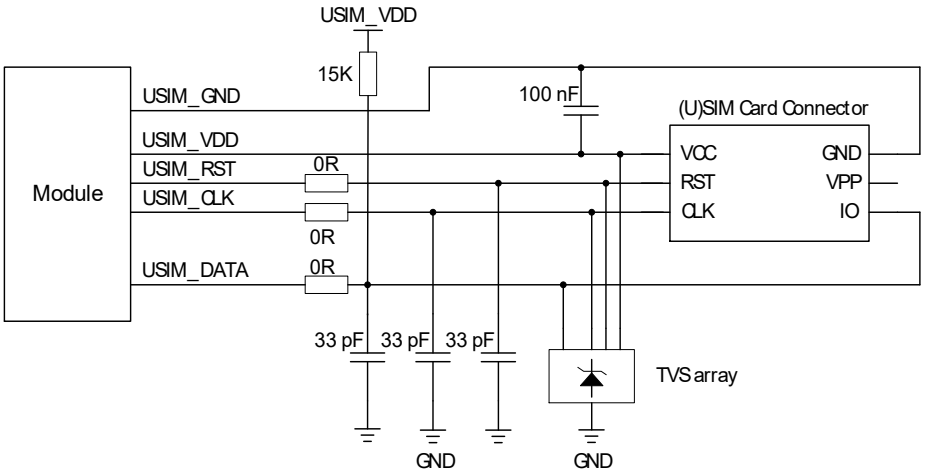
The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector



If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector



To enhance the reliability and availability of the (U)SIM card in your applications, follow the criteria below in (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signal traces away from RF and power supply traces.
- Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1 μF, and place it as close to (U)SIM card connector as possible. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering out RF interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

4.2 USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB

interface can only serve as the slave device.

USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

The following table shows the pin definition of USB interface.

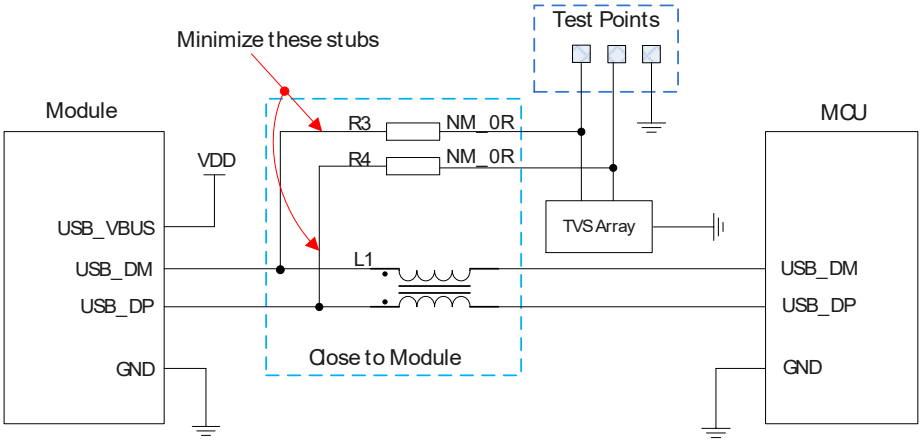
Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	AIO	USB 2.0 differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	70	AIO	USB 2.0 differential data (-)	
USB_VBUS	71	AI	USB connection detect	A test point must be reserved.

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Test points of the USB interface must be reserved, which can be used for software debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

Figure 19: Reference Circuit of USB Interface



A common-mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the integrity of USB data trace signal, L1, R3 and R4 must be placed close to the module, and these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection components to the USB connector as close as possible.

4.3 UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It also supports RTS and CTS hardware flow control, and can be used for data transmission and AT command communication.
- The debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the UART interfaces.

Table 13: Pin Definition of Main UART Interface

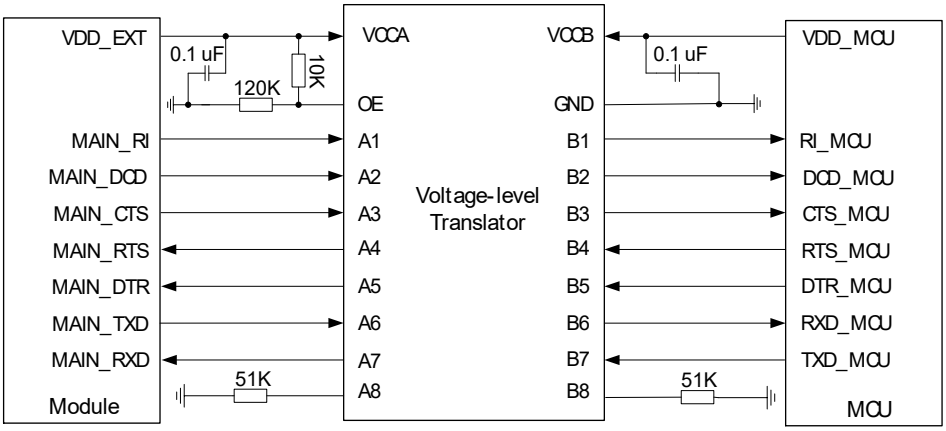
Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	62	DO	Main UART ring indication	If unused, keep them open.
MAIN_DCD	63	DO	Main UART data carrier detect	
MAIN_CTS	64	DO	Clear to send signal from the module	If unused, keep it open. Connect to MCU's CTS.
MAIN_RTS	65	DI	Request to send signal to the module	If unused, keep it open. Connect to MCU's RTS.
MAIN_DTR	66	DI	Main UART data terminal ready	Pulled up by default. MAIN_DTR at low level can wake up the module. If unused, keep it open.
MAIN_TXD	67	DO	Main UART transmit	If unused, keep them open.
MAIN_RXD	68	DI	Main UART receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	12	DO	Debug UART transmit	Test points must be reserved.
DBG_RXD	11	DI	Debug UART receive	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. An IC solution TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

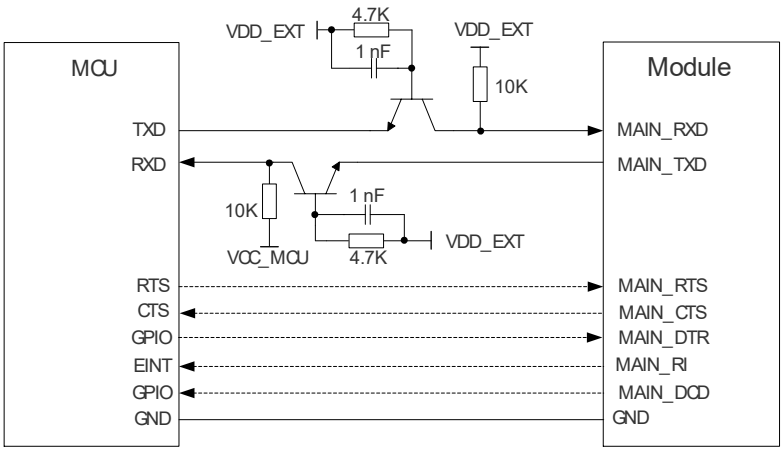
Figure 20: Reference Design of UART with a Voltage-level Translator



Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

Figure 21: Reference Circuit of UART with Transistor Circuit



NOTE

1. Transistor circuit above is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.4 PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design and one I2C interface. PCM interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK and an 8 kHz, 50 % duty cycle PCM_SYNC.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

Figure 22: Primary Mode Timing

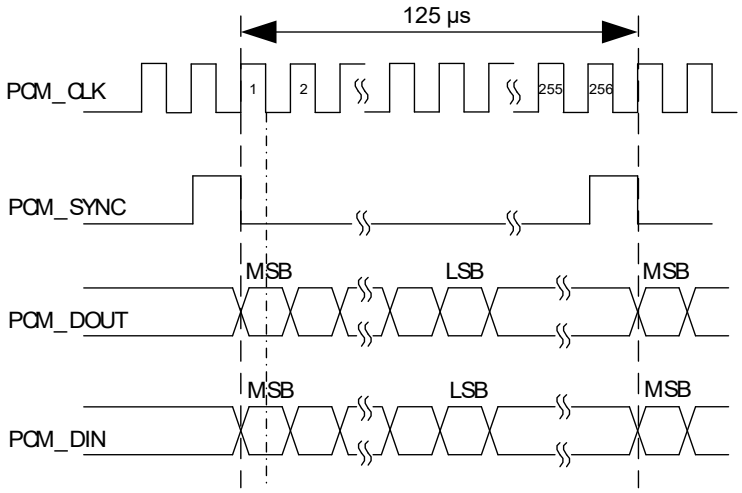
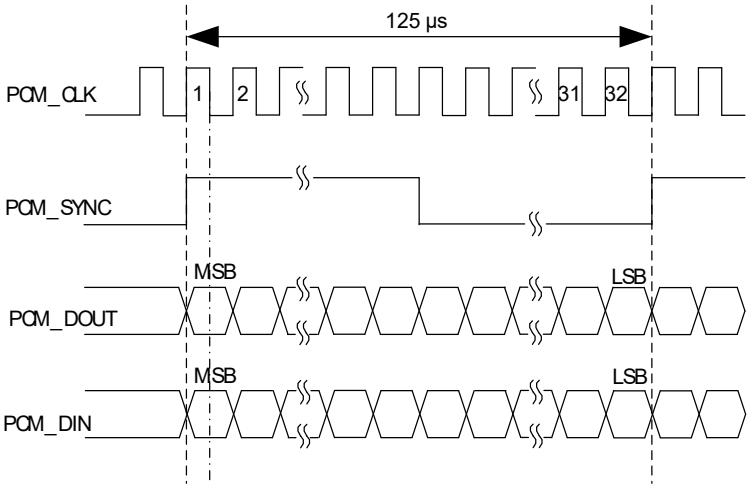


Figure 23: Auxiliary Mode Timing



The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 15: Pin Definition of PCM and I2C Interfaces

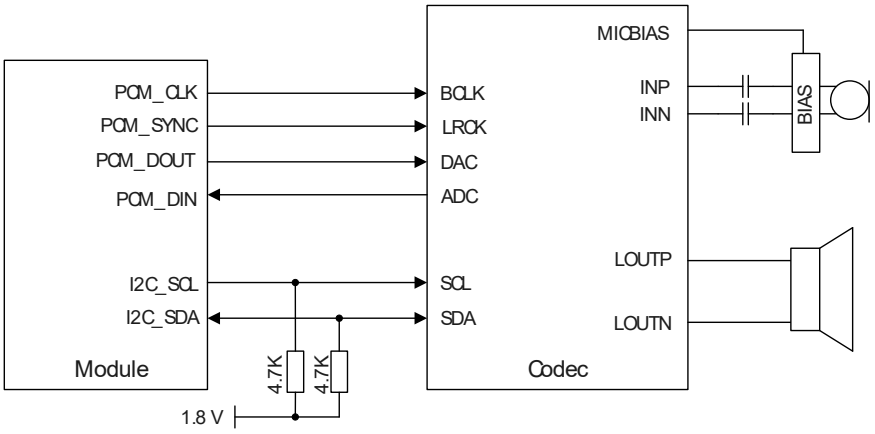
Pin Name	Pin No.	I/O	Description	Comment

PCM_DIN	24	DI	PCM data input	If unused, keep them open.
PCM_DOUT	25	DO	PCM data output	
PCM_SYNC	26	DIO	PCM data frame sync	Master mode: output. Slave mode: input. If unused, keep them open.
PCM_CLK	27	DIO	PCM clock	
I2C_SCL	41	OD	I2C serial clock (for external codec)	Externally pulled up to 1.8 V. If unused, keep them open.
I2C_SDA	42	OD	I2C serial data (for external codec)	

Clock and mode can be configured by AT command, and the default configuration is the master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document 2*** for more details about **AT+QDAI**.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

Figure 24: Reference Circuit of PCM and I2C Application with Audio Codec



NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit close to codec on the PCM traces, especially for PCM_CLK.
2. The module works as a master device pertaining to I2C interface.

4.5 SD Card Interface

The module supports an SDIO 3.0 interface for SD card. The following table shows the pin definition of SD card interface.

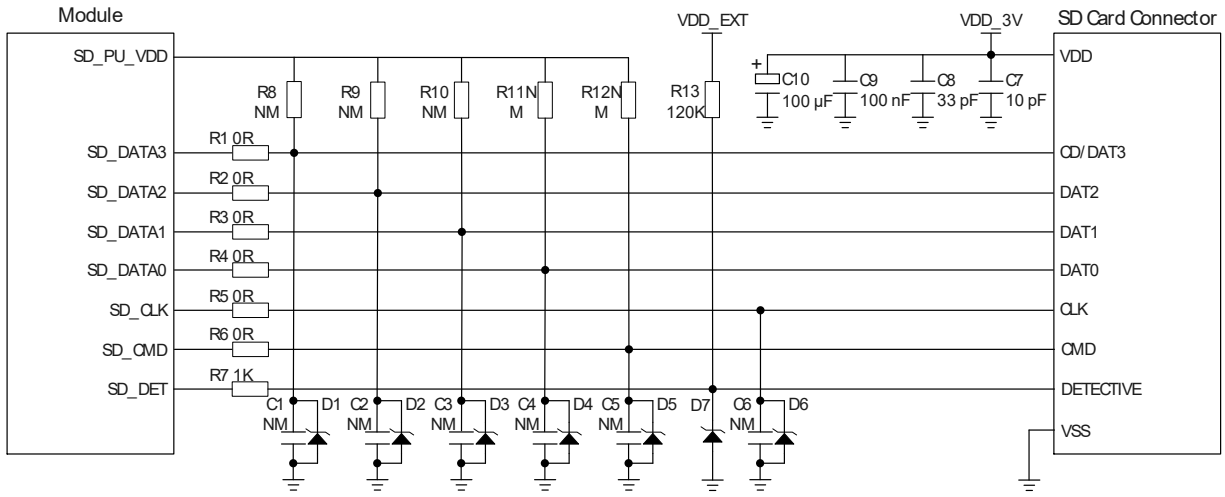
Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment

SD_DATA0	31	DIO	SDIO data bit 0	SDIO signal level can be selected according to the signal level supported SD card. See SD 3.0 protocol for more details. If unused, keep them open.
SD_DATA1	30	DIO	SDIO data bit 1	
SD_DATA2	29	DIO	SDIO data bit 2	
SD_DATA3	28	DIO	SDIO data bit 3	
SD_CLK	32	DO	SD card clock	
SD_CMD	33	DIO	SD card command	
SD_PU_VDD	34	PO	1.8/2.85 V output power for SD card pull-up circuits	Cannot be used for SD card power. If unused, keep it open.
SD_DET	23	DI	SD card insertion detect	Keep it open if SD card is unused, and it must be connected if SD card is used.

The following figure shows a reference design of SD card.

Figure 25: Reference Circuit of SD Card Interface



In SD card interface design, to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_DET must be connected if SD card is used, and keep SD _DET open if SD card is unused.
- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SD_PU_VDD is 50 mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R8–R12 are needed to pull up SDIO to SD_PU_VDD. Value of these resistors is among 10–100 kΩ and the recommended value is 100 kΩ. SD_PU_VDD should be used as the pull-up power.
- To adjust signal quality, it is recommended to add 0 Ω resistors R1–R6 in series between the module and the SD card. The bypass capacitors C1–C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- To offer good ESD protection, it is recommended to add a ESD on SD card pins near the SD card connector with junction capacitance less than 15 pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50 Ω (±10 %).
- Make sure the adjacent trace spacing is twice of the trace width and the load capacitance of SDIO bus should be less than 15 pF.
- It is recommended to keep the trace length difference between SD_CLK and SD_DATA[0:3]/ SD_CMD less than 1mm and the total routing length less than 50 mm. The total trace length inside

the module is 27 mm, so the exterior total trace length should be less than 23 mm.

4.6 WLAN and Bluetooth Application Interfaces [dev]

The module supports a SDIO 3.0 interface for WLAN function, and UART and PCM interfaces for Bluetooth function. The following table shows the pin definition of WLAN and Bluetooth application interfaces.

Table 17: Pin Definition of WLAN & Bluetooth Application Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN Application Interfaces				
SDC_DATA0	132	DIO	WLAN SDIO data bit 0	If unused, keep them open.
SDC_DATA1	131	DIO	WLAN SDIO data bit 1	
SDC_DATA2	130	DIO	WLAN SDIO data bit 2	
SDC_DATA3	129	DIO	WLAN SDIO data bit 3	
SDC_CLK	133	DO	WLAN SDIO clock	
SDC_CMD	134	DIO	WLAN SDIO command	
WLAN_EN	136	DO	WLAN function enable control	Active high. Cannot be pulled up before startup. If unused, keep it open.
Coexistence and Control Interfaces				
WLAN_PWR_EN	127	DO	WLAN power supply enable control	Active high. Cannot be pulled up before startup. If unused, keep it open.
WAKE_ON_WIRELESS	135	DI	WLAN/Bluetooth wakeup signal to the module	Active low. If unused, keep it open.
COEX_RXD	137	DI	LTE & WLAN/Bluetooth coexistence receive	Cannot be pulled up before startup. If unused, keep them open.
COEX_TXD	138	DO	LTE & WLAN/Bluetooth coexistence transmit	
WLAN_SLP_CLK	118	DO	WLAN sleep clock	If unused, keep it open.
Bluetooth Application Interfaces				
BT_RTS	37	DI	Request to send signal to the module	Connect to MCU's RTS. If unused, keep it open.
BT_TXD	38	DO	Bluetooth UART transmit	If unused, keep them open.
BT_RXD	39	DI	Bluetooth UART receive	
BT_CTS	40	DO	Clear to send signal from the module	Connect to MCU's CTS. Cannot be pulled up before startup. If unused, keep it open.
BT_EN	139	DO	Bluetooth enable control	If unused, keep it open.

PCM_DIN [5]	24	DI	PCM data input	If unused, keep them open.
PCM_DOUT [5]	25	DO	PCM data output	
PCM_SYNC [5]	26	DIO	PCM data frame sync	Master mode: output. Slave mode: input. If unused, keep them open.
PCM_CLK [5]	27	DIO	PCM clock	

4.6.1 WLAN Application Interface

The module provides a SDIO 3.0 interface and control interface for WLAN design. SDIO interface supports SDR mode, and the maximum frequency is up to 50 MHz.

As SDIO signals are very high-speed, to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signals far away from other sensitive circuits or signals such as RF circuits and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep matching length between SDC_CLK and SDC_DATA[0:3]/SDC_CMD less than 1 mm and total routing length less than 50 mm.
- Keep termination resistors within 15–24 Ω on clock traces near the module and keep the route distance from the module clock pins to termination resistors less than 5 mm.
- Make sure the adjacent trace spacing is twice the trace width and bus capacitance is less than 15 pF.

4.6.2 Bluetooth Application Interface

The module supports a dedicated UART interface and a PCM interface for Bluetooth application. Further information about Bluetooth interface will be added in the future version of this document.

4.7 ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces.

- **AT+QADC=0** can be used to read the voltage value on ADC0 pin.
- **AT+QADC=1** can be used to read the voltage value on ADC1 pin.

For more details about these AT commands, see ***document 2***. To improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 18: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	45	AI	General-purpose analog to digital converter	If unused, keep them open.
ADC1	44	AI	General-purpose analog to digital converter	

Table 19: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0.3	-	VBAT_BB	V

[5] Pins 24–27 can be used not only for audio function of the PCM interface, but also for Bluetooth function [dev].

ADC1 Input Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	15	-	bits

NOTE

1. ADC input voltage must not exceed that of VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT power supply is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

4.8 SGMII Interface dev

The module includes an integrated Ethernet MAC with four SGMII data signals, two management signals and two control signals. The key features of the SGMII interface are shown below:

- Compliant with IEEE802.3
- Support 10/100/1000 Mbps Ethernet work mode
- Support maximum 150 Mbps (DL)/50 Mbps (UL) for 4G network
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces supporting dual voltage 1.8/2.85 V

The following table shows the pin definition of SGMII interface.

Table 20: Pin Definition of SGMII Interface

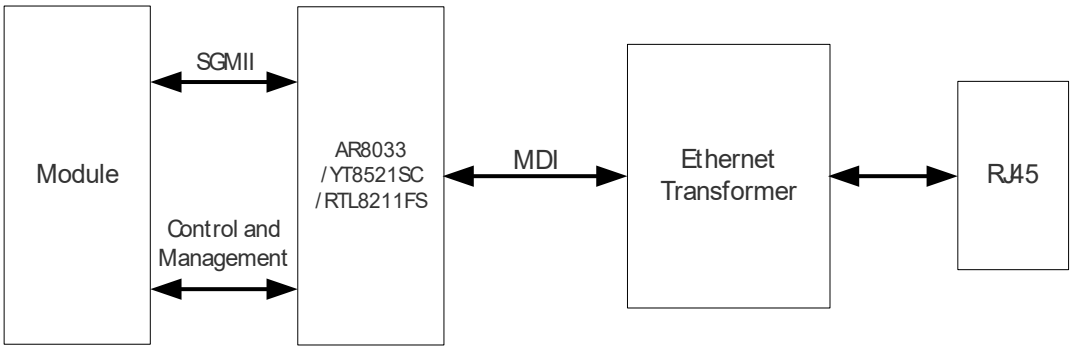
Pin Name	Pin No.	I/O	Description	Comment
Control and Management Signals				
SGMII_RST_N	119 [6]	DO	Ethernet PHY reset	If unused, keep it open.
SGMII_INT_N	120 [6]	DI	Ethernet PHY interrupt	If unused, keep it open.
SGMII_MDIO	121 [6]	DIO	SGMII management data	Externally pulled up to SGMII_MDIO_VDD, and the pull-up resistor is 1.5 kΩ. If unused, keep it open.
SGMII_MDC	122 [6]	DO	SGMII management data clock	If unused, keep it open.
SGMII_MDIO_VDD	128 [6]	PO	SGMII_MDIO pull up power supply	Configurable power source. If unused, keep it open.
SGMII Data Signals				
SGMII_TX_M	123	AO	SGMII transmit (-)	Add a 0.1 μF capacitor close to the PHY chip. If unused, keep them open.
SGMII_TX_P	124	AO	SGMII transmit (+)	
SGMII_RX_P	125	AI	SGMII receive (+)	Add a 0.1 μF capacitor close to the module. If unused, keep them open.

[6] Pins 119–122 and 128 can be multiplexed into USIM2 interface via **AT+QDSIM=1**. For more details about the AT command, contact NetPrisma Technical Support. For more details about the pin multiplexed function of (U)SIM2 interface, see ***Table 11***.

SGMII_RX_M	126	AI	SGMII receive (-)

The following figure shows the simplified block diagram for Ethernet application.

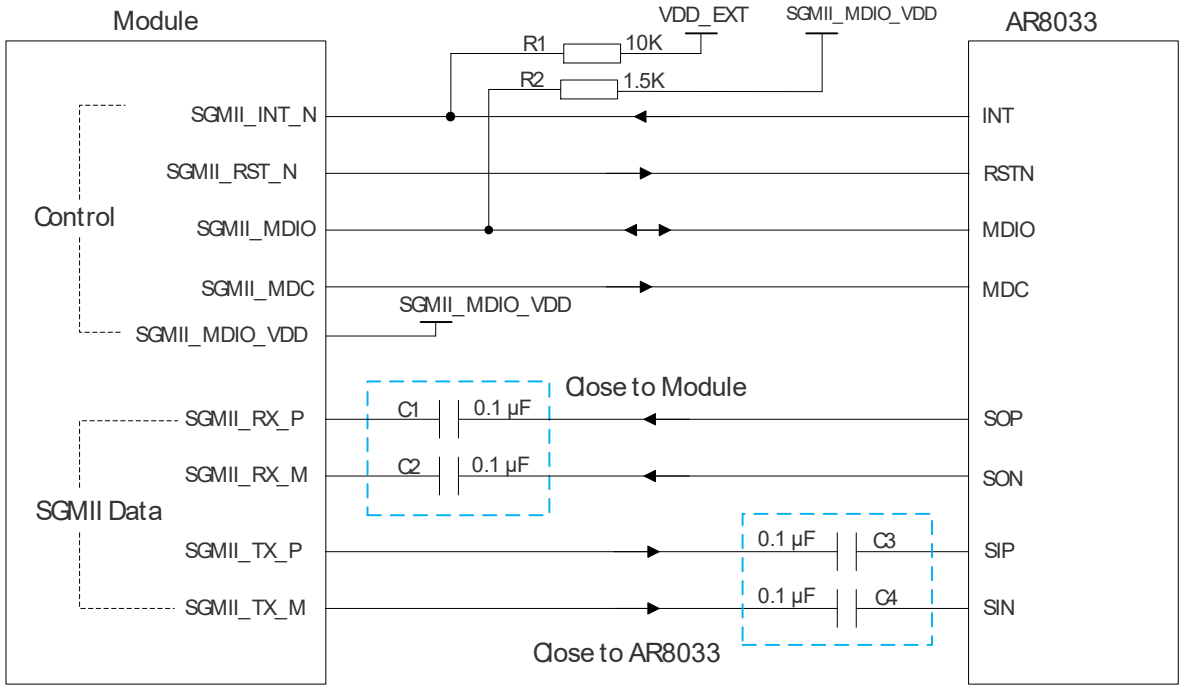
Figure 26: Simplified Block Diagram for Ethernet Application



For more information about Ethernet PHY design of YT8521SC or RTL8211FS, see ***document 5***.

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

Figure 27: Reference Circuit of SGMII Interface with PHY AR8033 Application



To enhance the reliability and availability in your applications, follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits or signals such as RF circuits, analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- Keep the maximum trace length less than 25.4 cm and keep the length difference on the differential pairs less than 0.5 mm.
- Keep the differential impedance of SGMII data traces within 100 Ω ±10 % and ensure the integrity of the reference ground.
- Make sure the trace spacing between SGMII_TX_P/M and SGMII_RX_P/M is at least 3 times the trace width, and the same to the adjacent signal traces.

NOTE

Limited by the flash size of the module, LUH32-WWD&LUH33-WWD does not support SGMII function currently. If needed, please contact NetPrisma Technical Support.

4.9 Indication Signals

4.9.1 Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 21: Pin Definition of Network Indication

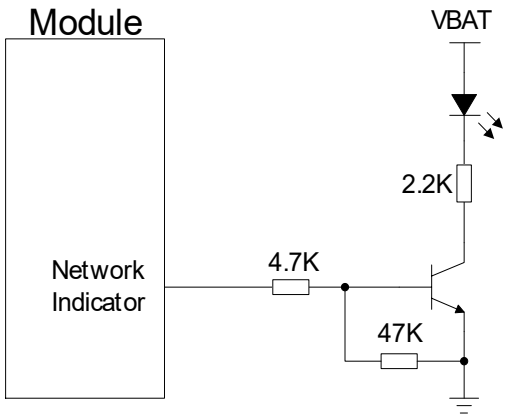
Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module's registered network status	Cannot be pulled up before startup. If unused, keep it open.
NET_STATUS	6	DO	Indicate the module's network activity status	If unused, keep it open.

Table 22: Working State of Network Indication

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on 4G network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

Figure 28: Reference Circuit of the Network Indication



4.9.2 STATUS

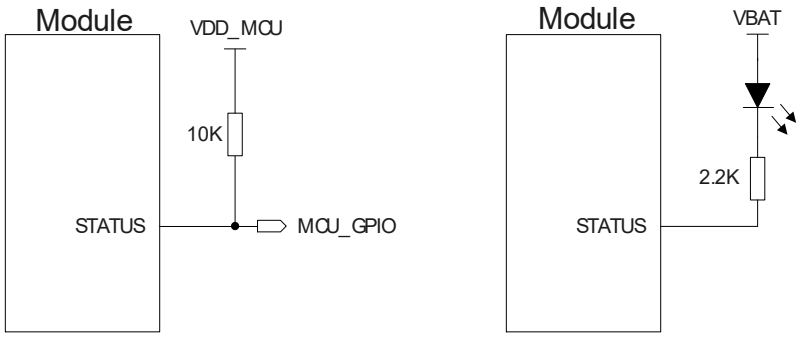
The STATUS pin is an open drain output signal used to indicate the module's operation status. This pin can be connected to the GPIO of the MCU through a pull-up resistor, or designed according to the LED indicator circuit shown in the figure below. When the module is turned on normally, the STATUS will output low level. Otherwise, the STATUS will output high-impedance state.

Table 23: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	The driving current should be less than 0.9 mA. An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and you can choose the applicable one according to your demands.

Figure 29: Reference Circuits of STATUS



NOTE

The STATUS pin cannot be used as the turn-off status indication of the module when VBAT power supply is removed.

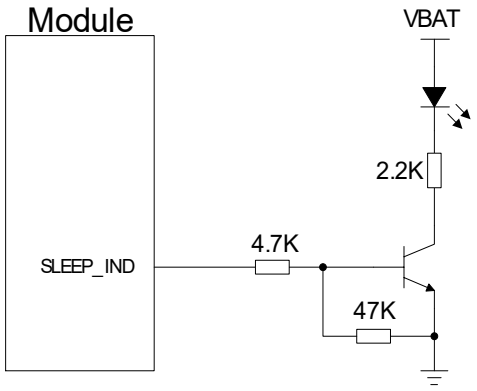
4.9.3 SLEEP_IND

SLEEP_IND is used to indicate the module's sleep status. When the module enters sleep mode, SLEEP_IND outputs a high level.

Table 24: Pin Definition of SLEEP_IND

Pin Name	Pin No.	I/O	Description	Comment
SLEEP_IND	3	DO	Indicate the module's sleep status	If unused, keep it open.

Figure 30: Reference Circuit of SLEEP_IND



4.9.4 MAIN_RI

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behaviors. No matter on which port (main UART, USB AT port or USB modem port) a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

The default behaviors of the MAIN_RI are shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**. See ***document 3*** for details.

Table 25: Behaviors of MAIN_RI

Module Status	MAIN_RI Level Status
Idle	High
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. See ***document 2*** for details.

4.10 USB_BOOT

The module provides a USB_BOOT pin. Pull up USB_BOOT to 1.8 V before VDD_EXT is powered up, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 26: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module into download mode	Cannot be pulled up before startup. A test point is recommended to be reserved.

The following figures show the reference circuit of USB_BOOT interface and timing of entering forced download mode.

Figure 31: Reference Circuit of USB_BOOT Interface

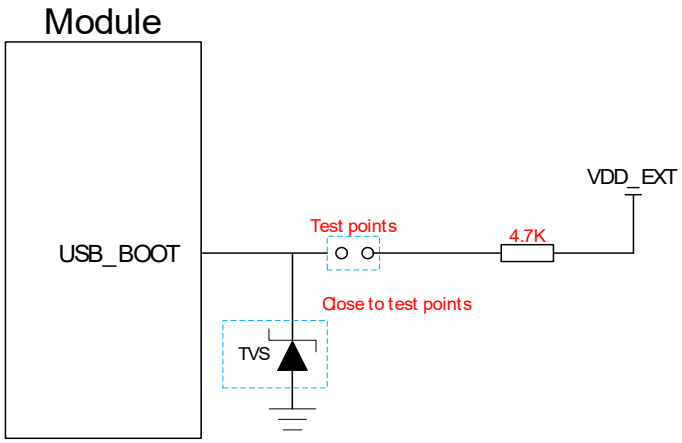
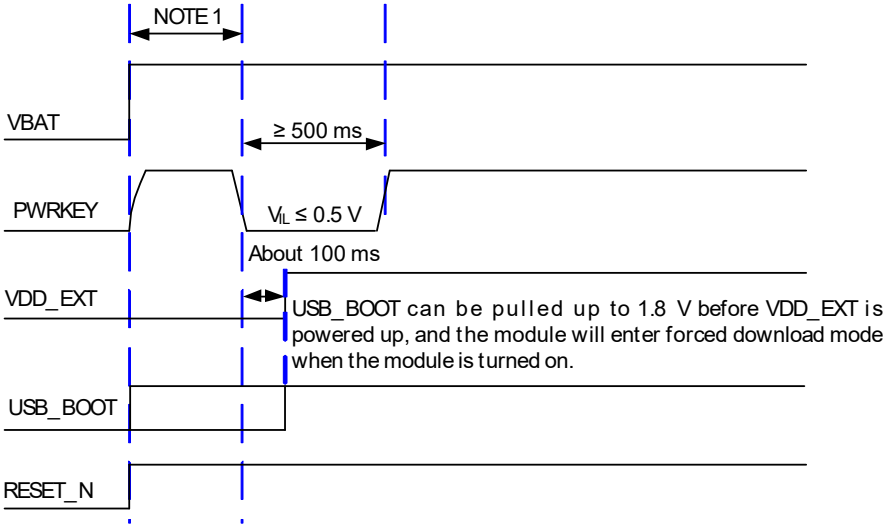


Figure 32: Timing of Entering Forced Download Mode



NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. Follow the above timing when using MCU to control the module to enter the forced download mode. Do not pull up USB_BOOT to 1.8 V before powering up VBAT.
3. If you need to manually force the module to enter download mode, directly connect the test points shown in ***Figure 31***.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1 Cellular Network

5.1.1 Antenna Interface & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

Table 27: Pin Definition of Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT_DIV	35	AI	Diversity antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 28: Frequency Bands

3GPP Band	Transmit	Receive	Unit
GSM850	824–849	869–894	MHz
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
PCS1900	1850–1910	1930–1990	MHz
WCDMA B1	1920–1980	2110–2170	MHz
WCDMA B2	1850–1910	1930–1990	MHz
WCDMA B4	1710–1755	2110–2155	MHz
WCDMA B5	824–849	869–894	MHz
WCDMA B6	830–840	875–885	MHz
WCDMA B8	880–915	925–960	MHz
WCDMA B19	830–845	875–890	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B2	1850–1910	1930–1990	MHz

LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B4	1710–1755	2110–2155	MHz
LTE-FDD B5	824–849	869–894	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B12	699–716	729–746	MHz
LTE-FDD B13	777–787	746–756	MHz
LTE-FDD B18	815–830	860–875	MHz
LTE-FDD B19	830–845	875–890	MHz
LTE-FDD B20	832–862	791–821	MHz
LTE-FDD B25	1850–1915	1930–1995	MHz
LTE-FDD B26	814–849	859–894	MHz
LTE-FDD B28	703–748	758–803	MHz
LTE-TDD B34	2010–2025	2010–2025	MHz
LTE-TDD B38	2570–2620	2570–2620	MHz
LTE-TDD B39	1880–1920	1880–1920	MHz
LTE-TDD B40	2300–2400	2300–2400	MHz
LTE-TDD B41	2496–2690	2496–2690	MHz
LTE-FDD B66	1710–1780	2110–2180	MHz

NOTE

B41 only supports 194 MHz (2496–2690 MHz).

5.1.2 Tx Power

The following table shows the RF output power of the module.

Table 29: Tx Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
GSM850/EGSM900	33 dBm ±2 dB	5 dBm ±5 dB

DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
GSM850/EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800/PCS1900 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE bands	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16.***

5.1.3 Rx Sensitivity

The following tables show the conducted RF receiver sensitivity of the module.

5.1.3.1 LUH32-WWD Conducted RF Receiver Sensitivity

Table 30: LUH32-WWD Conducted RF Receiver Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP Requirement（SIMO）
	Primary	Diversity	SIMO [7]	
GSM850	-107 dBm	-	-	-102 dBm
EGSM900	-108 dBm	-	-	-102 dBm
DCS1800	-108 dBm	-	-	-102 dBm
PCS1900	-107.6 dBm	-	-	-102 dBm
WCDMA B1	-108.9 dBm	-109.2 dBm	-	-106.7 dBm
WCDMA B2	-110.4 dBm	-111.1 dBm	-	-104.7 dBm
WCDMA B4	-108.4 dBm	-109.1 dBm	-	-104.7 dBm
WCDMA B5	-109.7 dBm	-111.4 dBm	-	-104.7 dBm
WCDMA B6	-109.8 dBm	-111.7 dBm	-	-106.7 dBm
WCDMA B8	-109.5 dBm	-111.4 dBm	-	-103.7 dBm
WCDMA B19	-109.7 dBm	-111.7 dBm	-	-106.7 dBm

[7] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve Rx performance.

LTE-FDD B1 (10 MHz)	-97.4 dBm	-97.4 dBm	-100.5 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-98.3 dBm	-99.1 dBm	-101.7 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-97.8 dBm	-98.8 dBm	-101.3 dBm	-93.3 dBm
LTE-FDD B4 (10 MHz)	-96.6 dBm	-97.4 dBm	-100.1 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-97.5 dBm	-99.4 dBm	-101.7 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.0 dBm	-97.6 dBm	-100.1 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.1 dBm	-99.4 dBm	-102.1 dBm	-93.3 dBm
LTE-FDD B12 (10 MHz)	-98.3 dBm	-98.9 dBm	-101.7 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-97.9 dBm	-99.1 dBm	-101.8 dBm	-93.3 dBm
LTE-FDD B18 (10 MHz)	-97.6 dBm	-99.6 dBm	-101.9 dBm	-96.37 dBm
LTE-FDD B19 (10 MHz)	-97.6 dBm	-99.5 dBm	-101.7 dBm	-96.3 dBm
LTE-FDD B20 (10 MHz)	-97.3 dBm	-99.1 dBm	-101.4 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-98.2 dBm	-98.9 dBm	-101.6 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-97.4 dBm	-99.4 dBm	-101.6 dBm	-93.86 dBm
LTE-FDD B28 (10 MHz)	-97.9 dBm	-99.9 dBm	-101.7 dBm	-94.8 dBm
LTE-TDD B34 (10 MHz)	-97.0 dBm	-97.2 dBm	-100.4 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97.3 dBm	-97.1 dBm	-101.2 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-97.3 dBm	-99.4 dBm	-100.2 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.2 dBm	-97.3 dBm	-101.6 dBm	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.8 dBm	-96.2 dBm	-100.1 dBm	-94.3 dBm
LTE-FDD B66 (10 MHz)	-96.6 dBm	-97.4 dBm	-99.5 dBm	-96.5 dBm

5.1.3.2 LUH33-WWD Conducted RF Receiver Sensitivity

Table 31: LUH33-WWD Conducted RF Receiver Sensitivity

Frequency Band	Receiver Sensitivity (Typ.)			3GPP Requirement（SIMO）
	Primary	Diversity	SIMO [7]	
GSM850	-107 dBm	-	-	-102 dBm
EGSM900	-108 dBm	-	-	-102 dBm

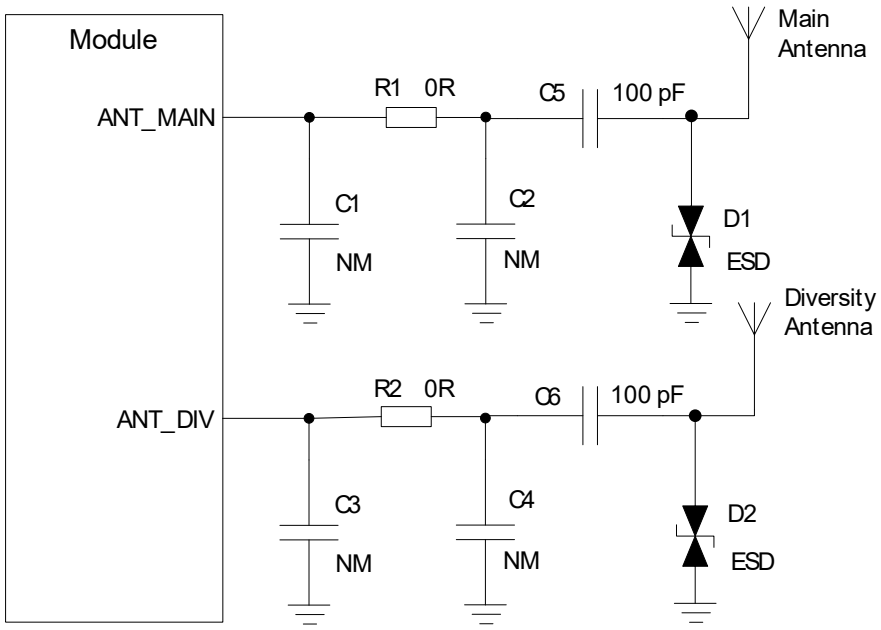
DCS1800	-108 dBm	-	-	-102 dBm
PCS1900	-107.6 dBm	-	-	-102 dBm
WCDMA B1	-108.9 dBm	-109.2 dBm	-	-106.7 dBm
WCDMA B2	-110.4 dBm	-111.1 dBm	-	-104.7 dBm
WCDMA B4	-108.4 dBm	-109.1 dBm	-	-104.7 dBm
WCDMA B5	-109.7 dBm	-111.4 dBm	-	-104.7 dBm
WCDMA B6	-109.8 dBm	-111.7 dBm	-	-106.7 dBm
WCDMA B8	-109.5 dBm	-111.4 dBm	-	-103.7 dBm
WCDMA B19	-109.7 dBm	-111.7 dBm	-	-106.7 dBm
LTE-FDD B1 (10 MHz)	-97.1 dBm	-97.4 dBm	-100.5 dBm	-96.3 dBm
LTE-FDD B2 (10 MHz)	-97.2 dBm	-99.1 dBm	-100.7 dBm	-94.3 dBm
LTE-FDD B3 (10 MHz)	-97.4 dBm	-98.8 dBm	-101.3 dBm	--93.3 dBm
LTE-FDD B4 (10 MHz)	-96.5 dBm	-97.4 dBm	-100.1 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-97.0 dBm	-99.4 dBm	-101.7 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.5 dBm	-97.6 dBm	-99.4 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-97.6 dBm	-99.4 dBm	-101.6 dBm	-93.3 dBm
LTE-FDD B12 (10 MHz)	-98.3 dBm	-98.9 dBm	-101.7 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-97.3 dBm	-99.1 dBm	-101.6 dBm	-93.3 dBm
LTE-FDD B18 (10 MHz)	-97.6 dBm	-99.6 dBm	-101.7 dBm	-96.37 dBm
LTE-FDD B19 (10 MHz)	-97.6 dBm	-99.5 dBm	-101.7 dBm	-96.3 dBm
LTE-FDD B20 (10 MHz)	-97.3 dBm	-99.1 dBm	-101.4 dBm	-93.3 dBm
LTE-FDD B25 (10 MHz)	-98.4 dBm	-98.9 dBm	-101.6 dBm	-92.8 dBm
LTE-FDD B26 (10 MHz)	-97.2 dBm	-99.4 dBm	-101.6 dBm	-93.86 dBm
LTE-FDD B28 (10 MHz)	-97.9 dBm	-99.9 dBm	-101.7 dBm	-94.8 dBm
LTE-TDD B34 (10 MHz)	-97.3 dBm	-97.2 dBm	-101.4 dBm	-96.3 dBm
LTE-TDD B38 (10 MHz)	-97.3 dBm	-97.1 dBm	-100.2 dBm	-96.3 dBm
LTE-TDD B39 (10 MHz)	-97.5 dBm	-99.4 dBm	-101.8 dBm	-96.3 dBm
LTE-TDD B40 (10 MHz)	-97.3 dBm	-97.3 dBm	-100.6 dBm	-96.3 dBm

LTE-TDD B41 (10 MHz)	-97.5 dBm	-96.2 dBm	-99.5 dBm	-94.3 dBm
LTE-FDD B66 (10 MHz)	-96.6 dBm	-97.4 dBm	-100.5 dBm	-96.5 dBm

5.1.4 Reference Design

A reference design of ANT_MAIN and ANT_DIV antennas is shown as below. A dual L-type circuit should be reserved for better RF performance. The capacitors C1–C4 are not mounted by default.

Figure 33: Reference Circuit of RF Antenna Interface



NOTE

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiver sensitivity.
2. ANT_DIV function is enabled by default. Use **AT+QCFG="divctl", 0** can disable this function, see ***document 3*** for details.
3. Place the dual L-type components (R1/C1/C2, R2/C3/C4 and C5/C6) as close to the antenna as possible.
4. Notes on C5 and C6:
   1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      ① Do not reserve C5 and C6.
      ② If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.
5. It is recommended to reserve ESD protection components (D1 and D2) for the antenna interfaces and the junction capacitance should not exceed 0.05 pF.

5.2 GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS. The module supports standard NMEA 0183 protocol, and outputs

NMEA sentences at 1 Hz data update rate via USB interface by default.

The GNSS engine of the module is turned off by default. It can be turned on by the AT command. For more details about GNSS engine technology and configurations, see ***document 6***.

5.2.1 Antenna Interface & Frequency Bands

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 33: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42	MHz

5.2.2 GNSS Performance

The following table shows the GNSS performance of the module.

Table 34: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	35	s
		AGNSS start	18	s
	Warm start @ open sky	Autonomous	26	s
		AGNSS start	2.2	s
	Hot start @ open sky	Autonomous	2.5	s
		AGNSS start	1.8	s

Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

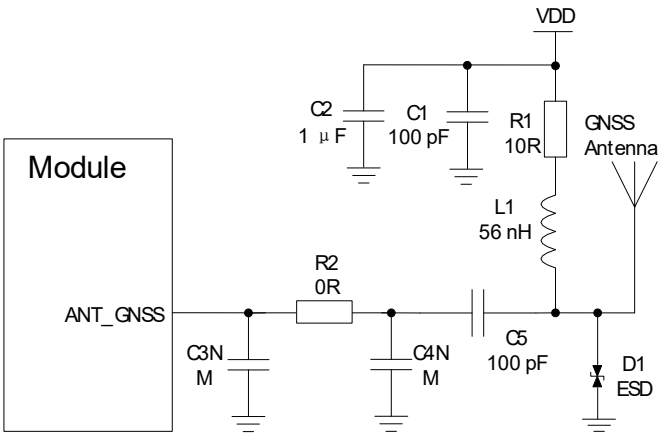
1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3 Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design.

A reference design of GNSS antenna is shown as below.

Figure 34: Reference Circuit of GNSS Antenna



NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, you will not need the VDD circuit.
3. It is recommended to reserve an ESD protection component D1 and the junction capacitance should not exceed 0.05 pF.

The following layout guidelines should be taken into account in your design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

5.3 RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant,

the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 35: Microstrip Design on a 2-layer PCB

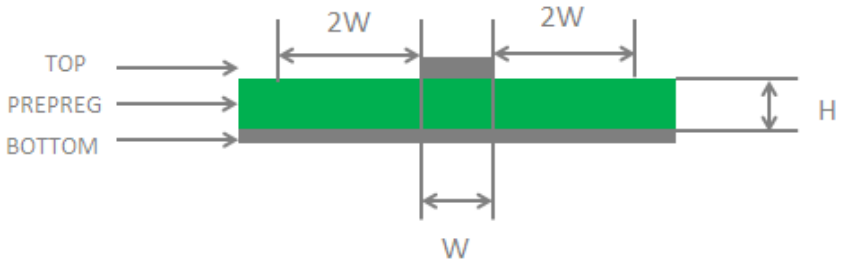


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

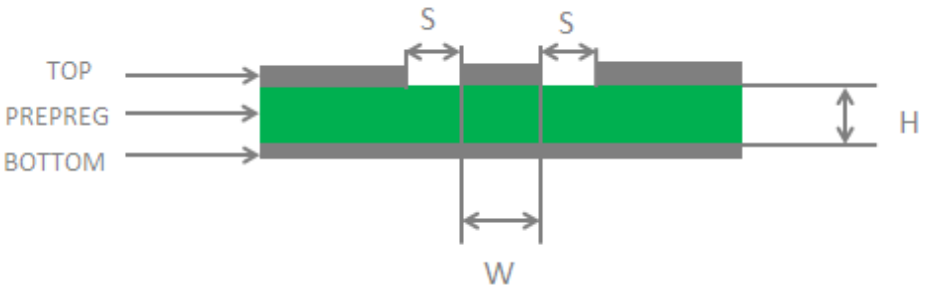


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

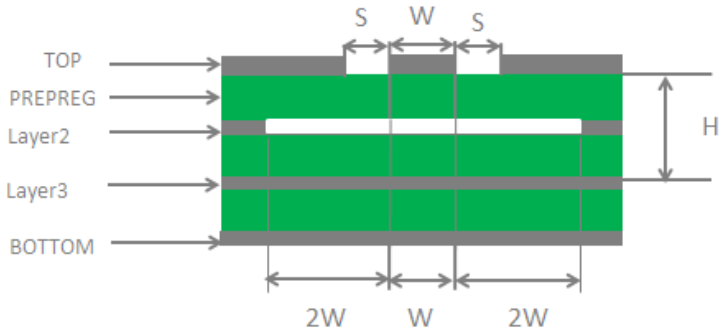
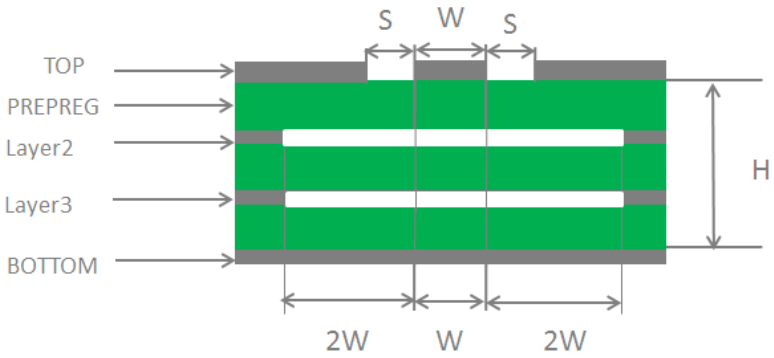


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document 7***.

5.4 Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 35: Antenna Requirements

Type	Requirements
GNSS (Optional)	● Frequency range: 1559–1609 MHz (L1) ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: ● Passive antenna gain: > 0 dBi
	For active antenna usage: ● Active antenna noise figure: < 1.5 dB ● Active antenna embedded LNA gain: < 17 dB
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max. input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

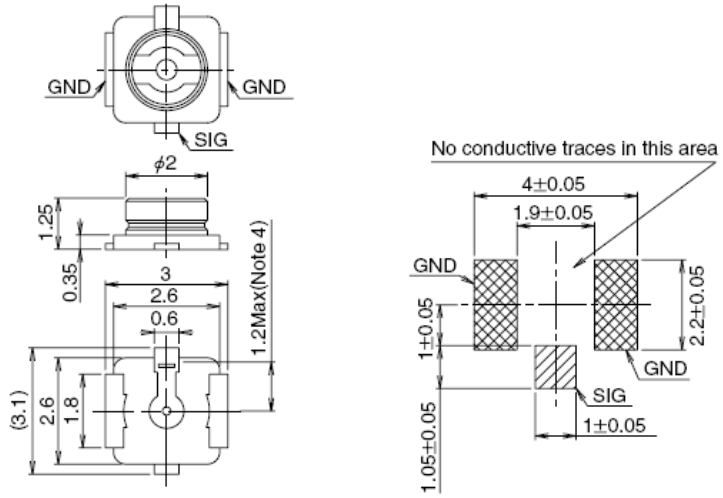
NOTE

It is recommended to use a passive GNSS antenna when LTE B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.5 RF Connector Recommendation

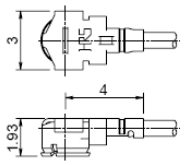
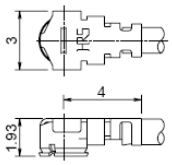
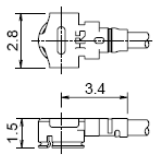
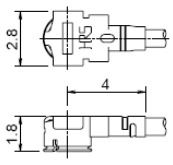
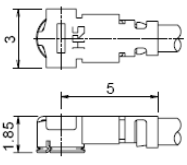
If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

Figure 39: Dimensions of the Receptacle (Unit: mm)



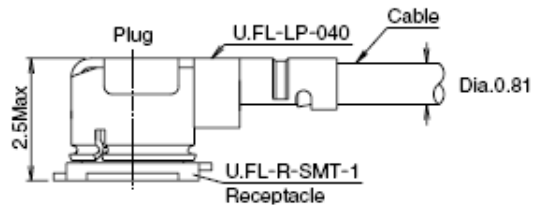
U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

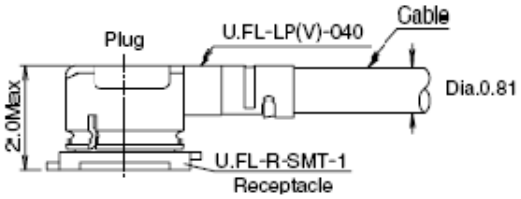
Figure 40: Specifications of Mated Plugs

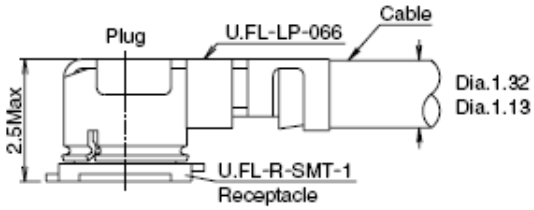
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

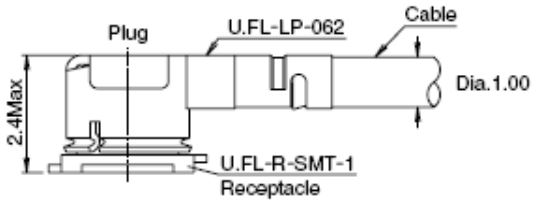
The following figure describes the space factor of mated connectors.

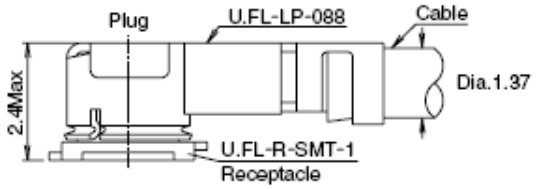
Figure 41: Space Factor of Mated Connectors (Unit: mm)











For more details, visit http://www.hirose.com

6 Electrical Characteristics and Reliability

6.1 Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 36: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Input Voltage at ADCs	0	VBAT_BB	V

6.2 Power Supply Ratings

Table 37: Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drops during burst transmission	At maximum power control level	-	-	400	mV
I_{VBAT}	Peak power consumption	At maximum power control level	-	1.8	2.0	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

6.3 Power Consumption

6.3.1 LUH32-WWD Power Consumption

Table 38: LUH32-WWD Power Consumption

Description	Condition	Typ.	Unit

Power-off	Power down	12	μA
	AT+CFUN=0 (USB disconnected)	1.26	mA
	AT+CFUN=0 (USB Suspend)	1.50	mA
	AT+CFUN=4 (USB disconnected)	1.33	mA
	AT+CFUN=4 (USB Suspend)	1.60	mA
	GSM850 @ DRX = 2 (USB disconnected)	2.38	mA
	GSM850 @ DRX = 5 (USB disconnected)	1.79	mA
	GSM850 @ DRX = 5 (USB Suspend)	2.03	mA
	GSM850 @ DRX = 9 (USB disconnected)	1.64	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.41	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.82	mA
	DCS1800 @ DRX = 5 (USB Suspend)	2.08	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.67	mA
	WCDMA @ PF = 64 (USB disconnected)	2.20	mA
Sleep state	WCDMA @ PF = 64 (USB Suspend)	2.47	mA
	WCDMA @ PF = 128 (USB disconnected)	1.89	mA
	WCDMA @ PF = 256 (USB disconnected)	1.67	mA
	WCDMA @ PF = 512 (USB disconnected)	1.64	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.81	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.69	mA
	LTE-FDD @ PF = 64 (USB Suspend)	2.91	mA
	LTE-FDD @ PF = 128 (USB disconnected)	2.08	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.81	mA
	LTE-TDD @ PF = 32 (USB disconnected)	4.10	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.74	mA
	LTE-TDD @ PF = 64 (USB Suspend)	3.00	mA
	LTE-TDD @ PF = 128 (USB disconnected)	2.07	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.79	mA

Idle state	EGSM900 @ DRX = 5 (USB disconnected)	15.41	mA
	EGSM900 @ DRX = 5 (USB connected)	25.24	mA
	WCDMA @ PF = 64 (USB disconnected)	15.29	mA
	WCDMA @ PF = 64 (USB connected)	25.30	mA
	LTE-FDD @ PF = 64 (USB disconnected)	15.76	mA
	LTE-FDD @ PF = 64 (USB connected)	25.84	mA
	LTE-TDD @ PF = 64 (USB disconnected)	15.74	mA
	LTE-TDD @ PF = 64 (USB connected)	25.75	mA
GPRS data transmission (GNSS OFF)	GSM850 4DL/1UL @ 31.97 dBm	250	mA
	GSM850 3DL/2UL @ 30.08 dBm	370	mA
	GSM850 2DL/3UL @ 29.01 dBm	470	mA
	GSM850 1DL/4UL @ 27.50 dBm	530	mA
	EGSM900 4DL/1UL @ 32 dBm	260	mA
	EGSM900 3DL/2UL @ 30.7dBm	400	mA
	EGSM900 2DL/3UL @ 29.2 dBm	490	mA
	EGSM900 1DL/4UL @ 28.1 dBm	580	mA
	DCS1800 4DL/1UL @ 28.69 dBm	180	mA
	DCS1800 3DL/2UL @ 28.25 dBm	280	mA
	DCS1800 2DL/3UL @ 26.18 dBm	350	mA
	DCS1800 1DL/4UL @ 25.51 dBm	410	mA
	PCS1900 4DL/1UL @ 29.11 dBm	170	mA
	PCS1900 3DL/2UL @ 28.10 dBm	270	mA
	PCS1900 2DL/3UL @ 26.26 dBm	350	mA
	PCS1900 1DL/4UL @ 25.17 dBm	400	mA
EDGE data transmission (GNSS OFF)	GSM850 4DL/1UL @ 25.22 dBm	190	mA
	GSM850 3DL/2UL @ 24.69 dBm	300	mA
	GSM850 2DL/3UL @ 22.89 dBm	405	mA
	GSM850 1DL/4UL @ 21.71 dBm	560	mA

	EGSM900 4DL/1UL @ 26.11 dBm	190	mA
	EGSM900 3DL/2UL @ 24.93 dBm	320	mA
	EGSM900 2DL/3UL @ 23.24 dBm	450	mA
	EGSM900 1DL/4UL @ 22.07 dBm	560	mA
	DCS1800 4DL/1UL @ 25.19 dBm	160	mA
	DCS1800 3DL/2UL @ 24.61 dBm	270	mA
	DCS1800 2DL/3UL @ 23.48 dBm	380	mA
	DCS1800 1DL/4UL @ 22.25 dBm	480	mA
	PCS1900 4DL/1UL @ 25.04 dBm	160	mA
	PCS1900 3DL/2UL @ 24.76 dBm	270	mA
	PCS1900 2DL/3UL @ 23.42 dBm	380	mA
	PCS1900 1DL/4UL @ 22.83 dBm	460	mA
WCDMA data transmission (GNSS OFF)	WCDMA B1 HSDPA @ 22.6 dBm	630	mA
	WCDMA B1 HSUPA @ 22.4 dBm	630	mA
	WCDMA B2 HSDPA @ 22.73 dBm	650	mA
	WCDMA B2 HSUPA @ 22.89 dBm	630	mA
	WCDMA B4 HSDPA @ 22.72 dBm	650	mA
	WCDMA B4 HSUPA @ 22.24 dBm	660	mA
	WCDMA B5 HSDPA @ 22.48 dBm	640	mA
	WCDMA B5 HSUPA @ 22 dBm	620	mA
	WCDMA B6 HSDPA @ 22.38 dBm	620	mA
	WCDMA B6 HSUPA @ 22.14 dBm	620	mA
	WCDMA B8 HSDPA @ 22.45 dBm	640	mA
	WCDMA B8 HSUPA @ 22.16 dBm	640	mA
	WCDMA B19 HSDPA @ 22.6 dBm	670	mA
	WCDMA B19 HSUPA @ 22.03 dBm	600	mA
LTE data transmission (GNSS OFF)	LTE-FDD B1 @ 23.41 dBm	770	mA
	LTE-FDD B2 @ 23.54 dBm	770	mA

	LTE-FDD B3 @ 22.94 dBm	730	mA
	LTE-FDD B4 @ 23.14 dBm	780	mA
	LTE-FDD B5 @ 23.04 dBm	720	mA
	LTE-FDD B7 @ 22.77 dBm	830	mA
	LTE-FDD B8 @ 23.3 dBm	720	mA
	LTE-FDD B12 @ 23.15 dBm	680	mA
	LTE-FDD B13 @ 22.91 dBm	710	mA
	LTE-FDD B18 @ 23.06 dBm	790	mA
	LTE-FDD B19 @ 22.88 dBm	770	mA
	LTE-FDD B20 @ 22.92 dBm	770	mA
	LTE-FDD B25 @ 22.87 dBm	740	mA
	LTE-FDD B26 @ 22.88 dBm	780	mA
	LTE-FDD B28 @ 23.33 dBm	790	mA
	LTE-TDD B34 @ 23.54 dBm	360	mA
	LTE-TDD B38 @ 22.51 dBm	370	mA
	LTE-TDD B39 @ 22.74 dBm	340	mA
	LTE-TDD B40 @ 22.63 dBm	380	mA
	LTE-TDD B41 @ 22.55 dBm	380	mA
	LTE-FDD B66 @ 23.43 dBm	750	mA
GSM voice call	GSM850 PCL = 5 @ 32.21 dBm	290	mA
	GSM850 PCL = 12 @ 18.53 dBm	150	mA
	GSM850 PCL = 19 @ 2.90 dBm	90	mA
	EGSM900 PCL = 5 @ 32.22 dBm	270	mA
	EGSM900 PCL = 12 @ 19.11 dBm	140	mA
	EGSM900 PCL = 19 @ 3.09 dBm	90	mA
	DCS1800 PCL = 0 @ 28.71 dBm	180	mA
	DCS1800 PCL = 7 @ 15.73 dBm	140	mA
	DCS1800 PCL = 15 @ -1.51 dBm	80	mA

	PCS1900 PCL = 0 @ 29.31 dBm	170	mA
	PCS1900 PCL = 7 @ 15.71 dBm	140	mA
	PCS1900 PCL = 15 @ -0.75 dBm	78	mA
WCDMA voice call	WCDMA B1 @ 23.55 dBm	670	mA
	WCDMA B2 @ 23.76 dBm	700	mA
	WCDMA B4 @ 23.77 dBm	640	mA
	WCDMA B5 @ 23.25 dBm	680	mA
	WCDMA B6 @ 23.15 dBm	670	mA
	WCDMA B8 @ 23.6 dBm	650	mA
	WCDMA B19 @ 23.17 dBm	660	mA

6.3.2 LUH33-WWD Power Consumption

Table 39: LUH33-WWD Power Consumption

Description	Condition	Typ.	Unit
Power-off	Power down	7	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.27	mA
	AT+CFUN=0 (USB Suspended)	1.51	mA
	AT+CFUN=4 (USB disconnected)	1.31	mA
	AT+CFUN=4 (USB Suspended)	1.54	mA
	GSM850 @ DRX = 2 (USB disconnected)	2.32	mA
	GSM850 @ DRX = 5 (USB disconnected)	1.75	mA
	GSM850 @ DRX = 5 (USB Suspended)	1.98	mA
	GSM850 @ DRX = 9 (USB disconnected)	1.56	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.32	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.76	mA
	DCS1800 @ DRX = 5 (USB Suspended)	1.98	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.55	mA
	WCDMA @ PF = 64 (USB disconnected)	2.18	mA

	WCDMA @ PF = 64 (USB Suspended)	2.41	mA
	WCDMA @ PF = 128 (USB disconnected)	1.82	mA
	WCDMA @ PF = 256 (USB disconnected)	1.63	mA
	WCDMA @ PF = 512 (USB disconnected)	1.54	mA
	LTE-FDD @ PF = 32 (USB disconnected)	3.74	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.56	mA
	LTE-FDD @ PF = 64 (USB Suspended)	2.84	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.97	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.67	mA
	LTE-TDD @ PF = 32 (USB disconnected)	4.01	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.64	mA
	LTE-TDD @ PF = 64 (USB Suspended)	2.92	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.95	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.60	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	15.66	mA
	EGSM900 @ DRX = 5 (USB connected)	25.30	mA
	WCDMA @ PF = 64 (USB disconnected)	15.91	mA
	WCDMA @ PF = 64 (USB connected)	25.53	mA
	LTE-FDD @ PF = 64 (USB disconnected)	16.36	mA
	LTE-FDD @ PF = 64 (USB connected)	26.01	mA
	LTE-TDD @ PF = 64 (USB disconnected)	16.42	mA
	LTE-TDD @ PF = 64 (USB connected)	26.20	mA
GPRS data transmission (GNSS OFF)	GSM850 4DL/1UL @ 31.97 dBm	250	mA
	GSM850 3DL/2UL @ 30.08 dBm	370	mA
	GSM850 2DL/3UL @ 29.01 dBm	470	mA
	GSM850 1DL/4UL @ 27.50 dBm	530	mA
	EGSM900 4DL/1UL @ 32 dBm	260	mA
	EGSM900 3DL/2UL @ 30.7dBm	400	mA

	EGSM900 2DL/3UL @ 29.2 dBm	490	mA
	EGSM900 1DL/4UL @ 28.1 dBm	580	mA
	DCS1800 4DL/1UL @ 28.69 dBm	180	mA
	DCS1800 3DL/2UL @ 28.25 dBm	280	mA
	DCS1800 2DL/3UL @ 26.18 dBm	350	mA
	DCS1800 1DL/4UL @ 25.51 dBm	410	mA
	PCS1900 4DL/1UL @ 29.11 dBm	170	mA
	PCS1900 3DL/2UL @ 28.10 dBm	270	mA
	PCS1900 2DL/3UL @ 26.26 dBm	350	mA
	PCS1900 1DL/4UL @ 25.17 dBm	400	mA
EDGE data transmission (GNSS OFF)	GSM850 4DL/1UL @ 25.22 dBm	190	mA
	GSM850 3DL/2UL @ 24.69 dBm	300	mA
	GSM850 2DL/3UL @ 22.89 dBm	405	mA
	GSM850 1DL/4UL @ 21.71 dBm	560	mA
	EGSM900 4DL/1UL @ 26.11 dBm	190	mA
	EGSM900 3DL/2UL @ 24.93 dBm	320	mA
	EGSM900 2DL/3UL @ 23.24 dBm	450	mA
	EGSM900 1DL/4UL @ 22.07 dBm	560	mA
	DCS1800 4DL/1UL @ 25.19 dBm	160	mA
	DCS1800 3DL/2UL @ 24.61 dBm	270	mA
	DCS1800 2DL/3UL @ 23.48 dBm	380	mA
	DCS1800 1DL/4UL @ 22.25 dBm	480	mA
	PCS1900 4DL/1UL @ 25.04 dBm	160	mA
	PCS1900 3DL/2UL @ 24.76 dBm	270	mA
	PCS1900 2DL/3UL @ 23.42 dBm	380	mA
	PCS1900 1DL/4UL @ 22.83 dBm	460	mA
WCDMA data transmission (GNSS OFF)	WCDMA B1 HSDPA @ 22.6 dBm	630	mA
	WCDMA B1 HSUPA @ 22.4 dBm	630	mA

	WCDMA B2 HSDPA @ 22.73 dBm	650	mA
	WCDMA B2 HSUPA @ 22.89 dBm	630	mA
	WCDMA B4 HSDPA @ 22.72 dBm	650	mA
	WCDMA B4 HSUPA @ 22.24 dBm	660	mA
	WCDMA B5 HSDPA @ 22.48 dBm	640	mA
	WCDMA B5 HSUPA @ 22 dBm	620	mA
	WCDMA B6 HSDPA @ 22.38 dBm	620	mA
	WCDMA B6 HSUPA @ 22.14 dBm	620	mA
	WCDMA B8 HSDPA @ 22.45 dBm	640	mA
	WCDMA B8 HSUPA @ 22.16 dBm	640	mA
	WCDMA B19 HSDPA @ 22.6 dBm	670	mA
	WCDMA B19 HSUPA @ 22.03 dBm	600	mA
LTE data transmission (GNSS OFF)	LTE-FDD B1 @ 23.41 dBm	770	mA
	LTE-FDD B2 @ 23.54 dBm	770	mA
	LTE-FDD B3 @ 22.94 dBm	730	mA
	LTE-FDD B4 @ 23.14 dBm	780	mA
	LTE-FDD B5 @ 23.04 dBm	720	mA
	LTE-FDD B7 @ 22.77 dBm	830	mA
	LTE-FDD B8 @ 23.3 dBm	720	mA
	LTE-FDD B12 @ 23.15 dBm	680	mA
	LTE-FDD B13 @ 22.91 dBm	710	mA
	LTE-FDD B18 @ 23.06 dBm	790	mA
	LTE-FDD B19 @ 22.88 dBm	770	mA
	LTE-FDD B20 @ 22.92 dBm	770	mA
	LTE-FDD B25 @ 22.87 dBm	740	mA
	LTE-FDD B26 @ 22.88 dBm	780	mA
	LTE-FDD B28 @ 23.33 dBm	790	mA
	LTE-TDD B34 @ 23.54 dBm	360	mA

	LTE-TDD B38 @ 22.51 dBm	370	mA
	LTE-TDD B39 @ 22.74 dBm	340	mA
	LTE-TDD B40 @ 22.63 dBm	380	mA
	LTE-TDD B41 @ 22.55 dBm	380	mA
	LTE-FDD B66 @ 23.43 dBm	750	mA
GSM voice call	GSM850 PCL = 5 @ 32.21 dBm	290	mA
	GSM850 PCL = 12 @ 18.53 dBm	150	mA
	GSM850 PCL = 19 @ 2.90 dBm	90	mA
	EGSM900 PCL = 5 @ 32.22 dBm	270	mA
	EGSM900 PCL = 12 @ 19.11 dBm	140	mA
	EGSM900 PCL = 19 @ 3.09 dBm	90	mA
	DCS1800 PCL = 0 @ 28.71 dBm	180	mA
	DCS1800 PCL = 7 @ 15.73 dBm	140	mA
	DCS1800 PCL = 15 @ -1.51 dBm	80	mA
	PCS1900 PCL = 0 @ 29.31 dBm	170	mA
	PCS1900 PCL = 7 @ 15.71 dBm	140	mA
	PCS1900 PCL = 15 @ -0.75 dBm	78	mA
WCDMA voice call	WCDMA B1 @ 23.55 dBm	670	mA
	WCDMA B2 @ 23.76 dBm	700	mA
	WCDMA B4 @ 23.77 dBm	640	mA
	WCDMA B5 @ 23.25 dBm	680	mA
	WCDMA B6 @ 23.15 dBm	670	mA
	WCDMA B8 @ 23.6 dBm	650	mA
	WCDMA B19 @ 23.17 dBm	660	mA

6.4 Digital I/O Characteristics

Table 40: VDD_EXT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.2
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT
V_{OH}	High-level output voltage	VDD_EXT - 0.45	VDD_EXT
V_{OL}	Low-level output voltage	0	0.45

Table 41: (U)SIM Low/High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.8 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	-0.3	0.12 × USIM_VDD
V_{OH}	High-level output voltage	0.8 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.4

Table 42: SD_PU_VDD Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × SD_PU_VDD	SD_PU_VDD + 0.2
V_{IL}	Low-level input voltage	-0.3	0.32 × SD_PU_VDD
V_{OH}	High-level output voltage	0.78 × SD_PU_VDD	SD_PU_VDD
V_{OL}	Low-level output voltage	0	0.45

Table 43: SD_PU_VDD High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.63 × SD_PU_VDD	SD_PU_VDD + 0.3
V_{IL}	Low-level input voltage	-0.3	0.25 × SD_PU_VDD
V_{OH}	High-level output voltage	0.75 × SD_PU_VDD	SD_PU_VDD
V_{OL}	Low-level output voltage	0	0.12 × SD_PU_VDD

Table 44: SGMII Low/High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × SGMII_MDIO_VDD	SGMII_MDIO_VDD + 0.3
V_{IL}	Low-level input voltage	-0.3	0.2 × SGMII_MDIO_VDD
V_{OH}	High-level output voltage	0.8 × SGMII_MDIO_VDD	SGMII_MDIO_VDD
V_{OL}	Low-level output voltage	0	0.4

6.5 ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 45: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6 Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

Table 46: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [8]	-35	+25	+75	ºC
Extended Temperature Range [9]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

[8] Within the operating temperature range, the module meets 3GPP specifications.
[9] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1 Mechanical Dimensions

Figure 42: Module Top and Side Dimensions

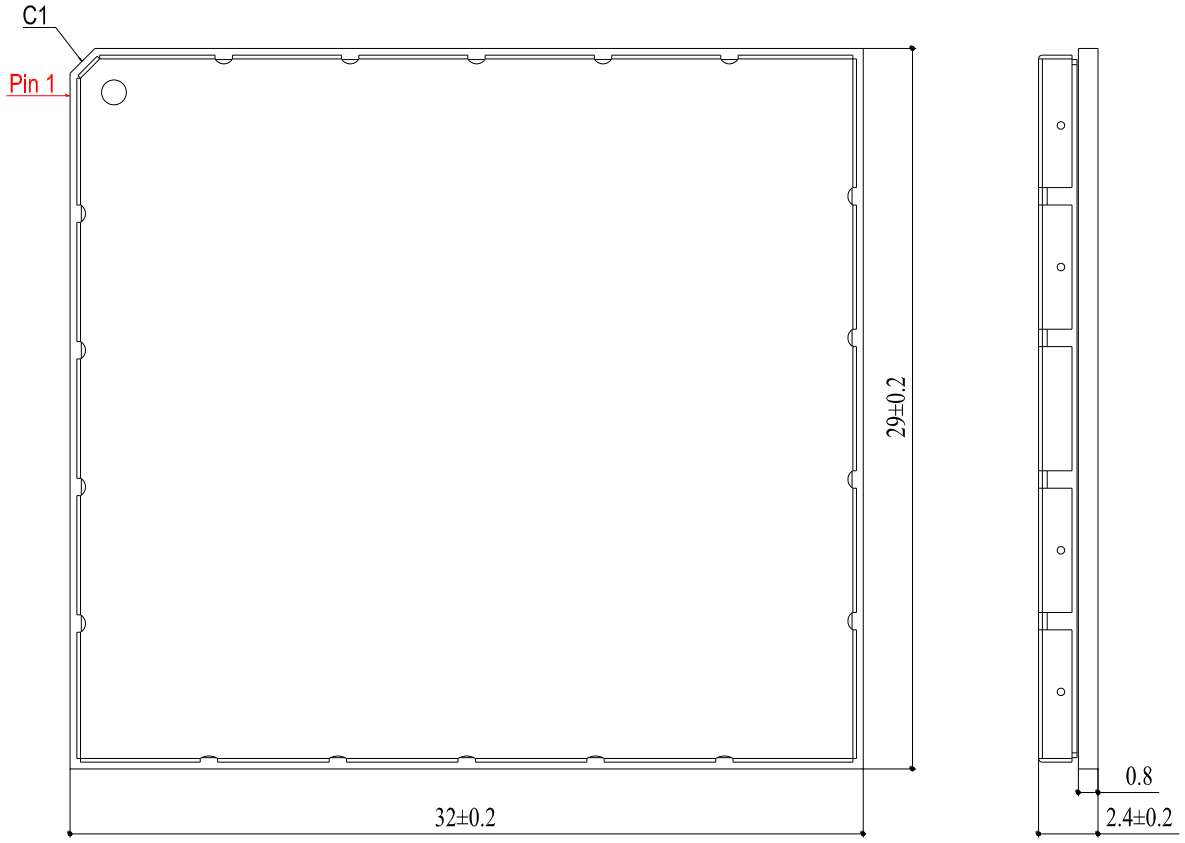
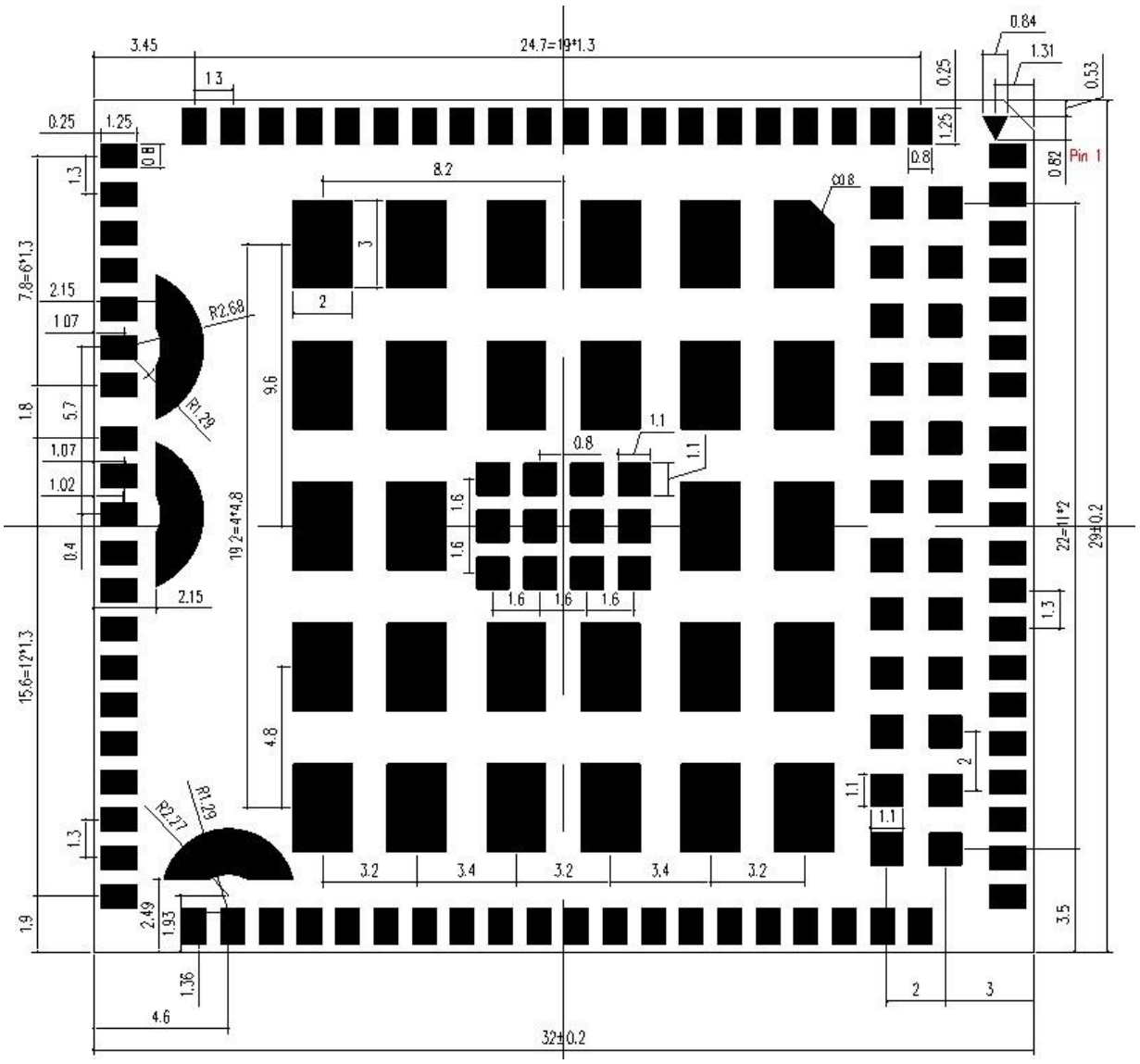


Figure 43: Bottom Dimensions (Bottom View)

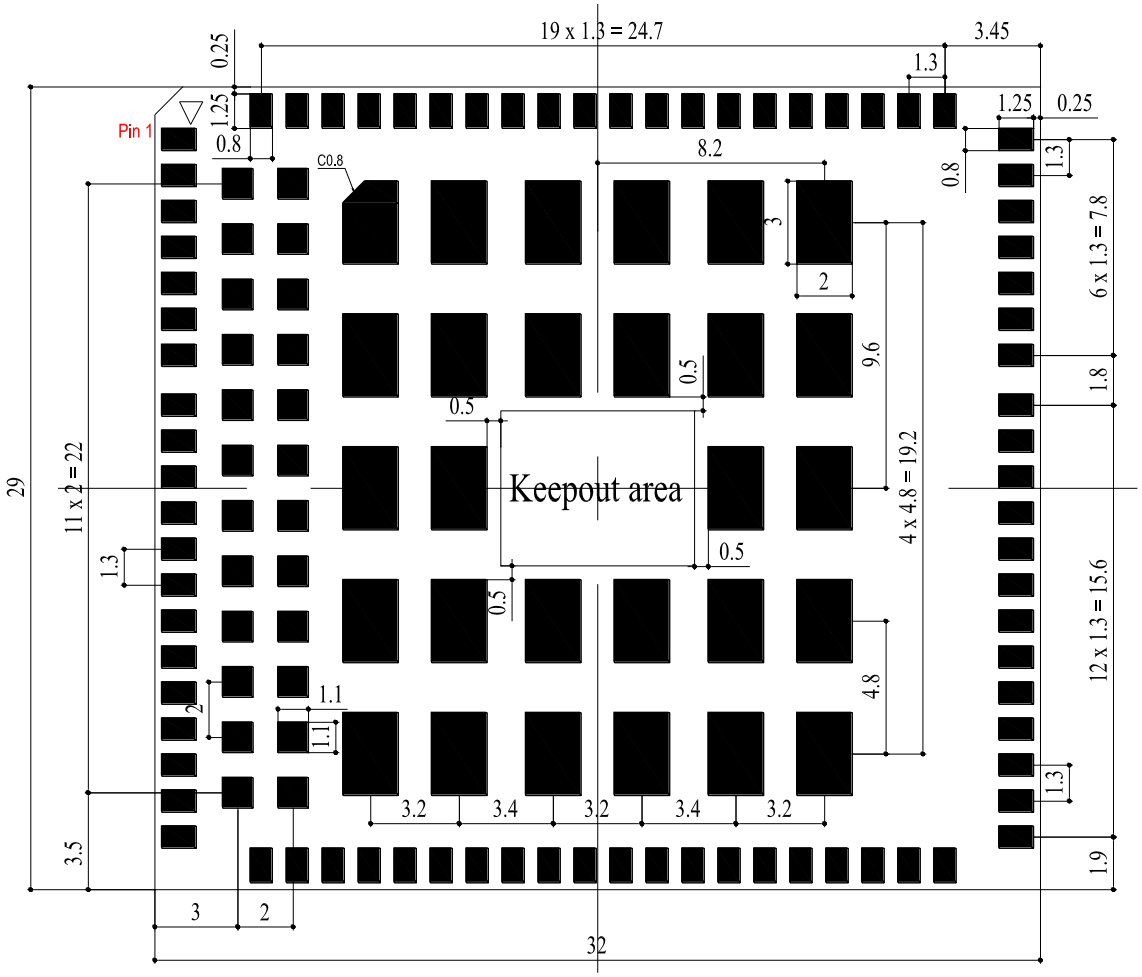


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2 Recommended Footprint

Figure 44: Recommended Footprint

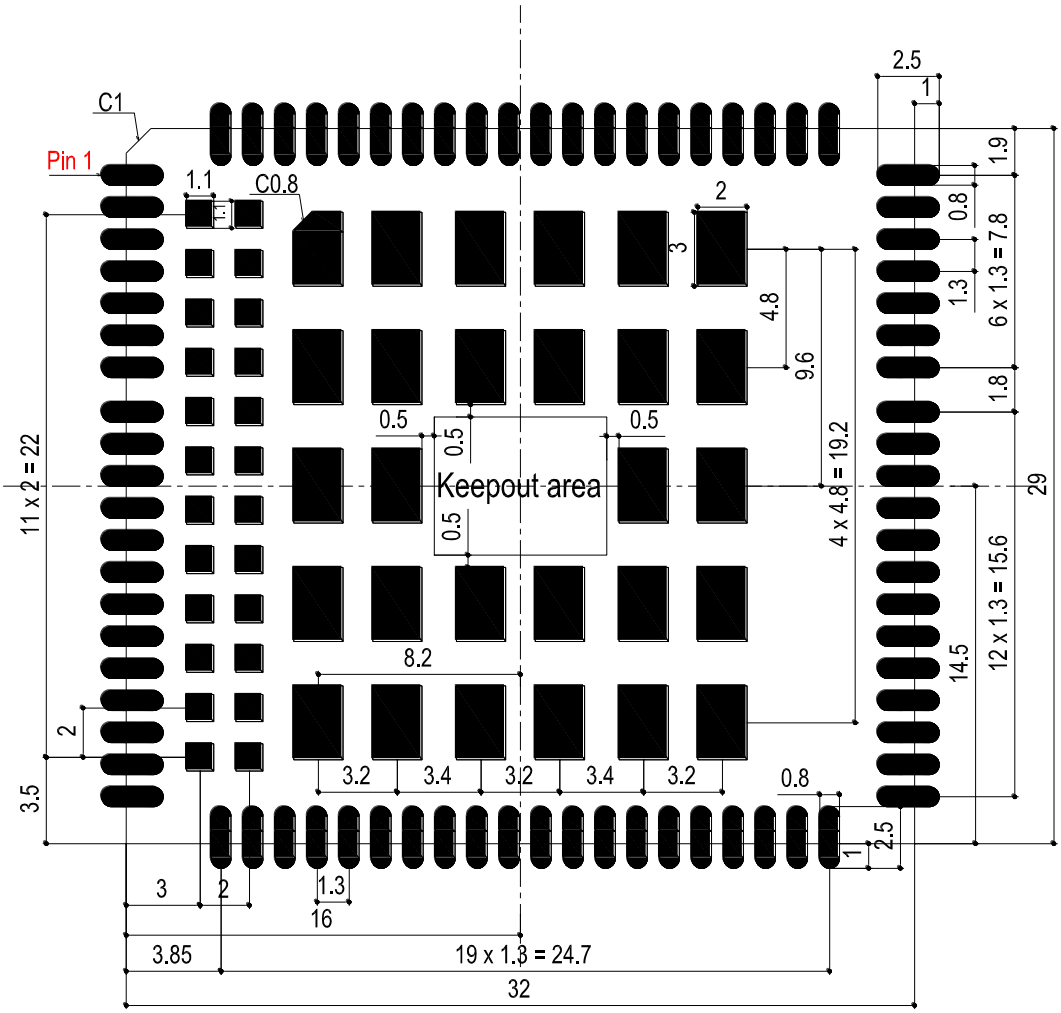


NOTE

1. The keepout area should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3 Recommended Compatible Footprint

Figure 45: Recommended Compatible Footprint

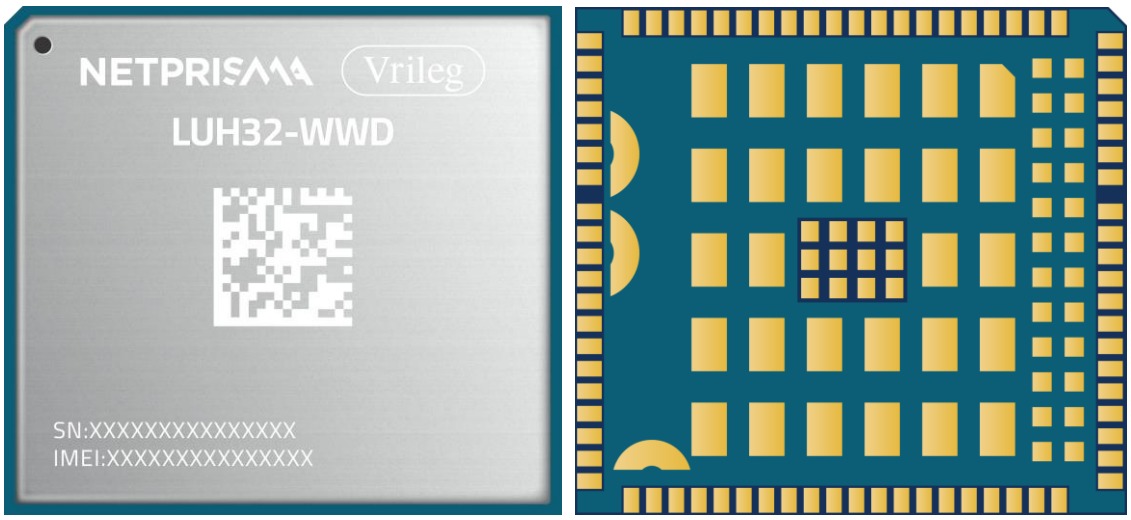


NOTE

1. The keepout area should not be designed.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.4 Top and Bottom Views

Figure 46: Top and Bottom Views of the Module



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

8 Storage, Manufacturing and Packaging

8.1 Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [10] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2 Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document 8***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB

[10] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 47: Recommended Reflow Soldering Thermal Profile

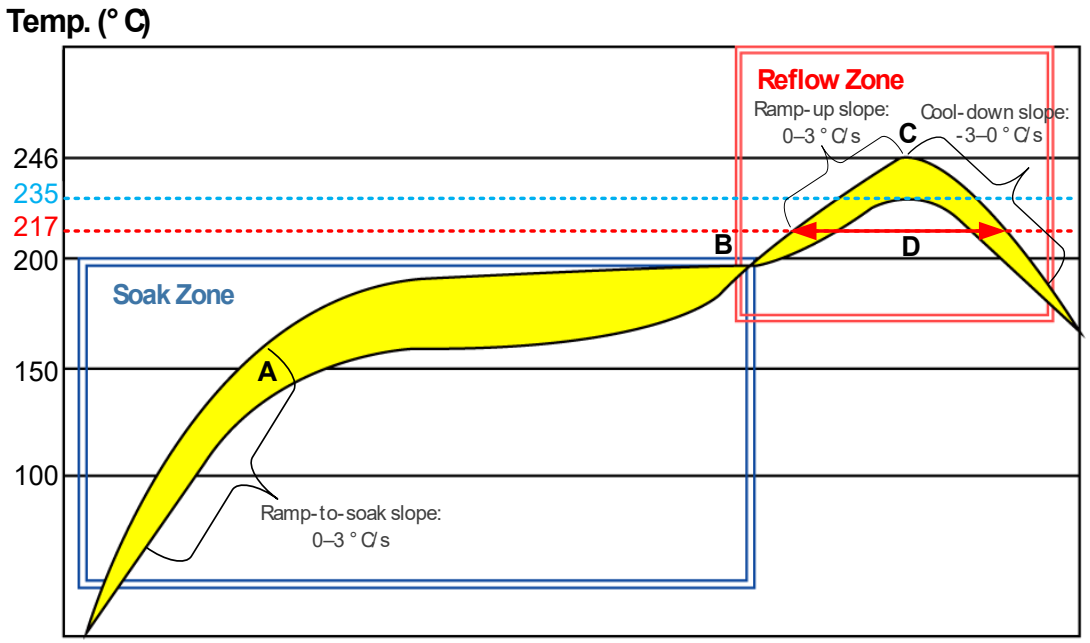


Table 47: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
6. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document 9***.

8.3 Packaging Specifications

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1 Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 48: Carrier Tape Dimension Drawing (Unit: mm)

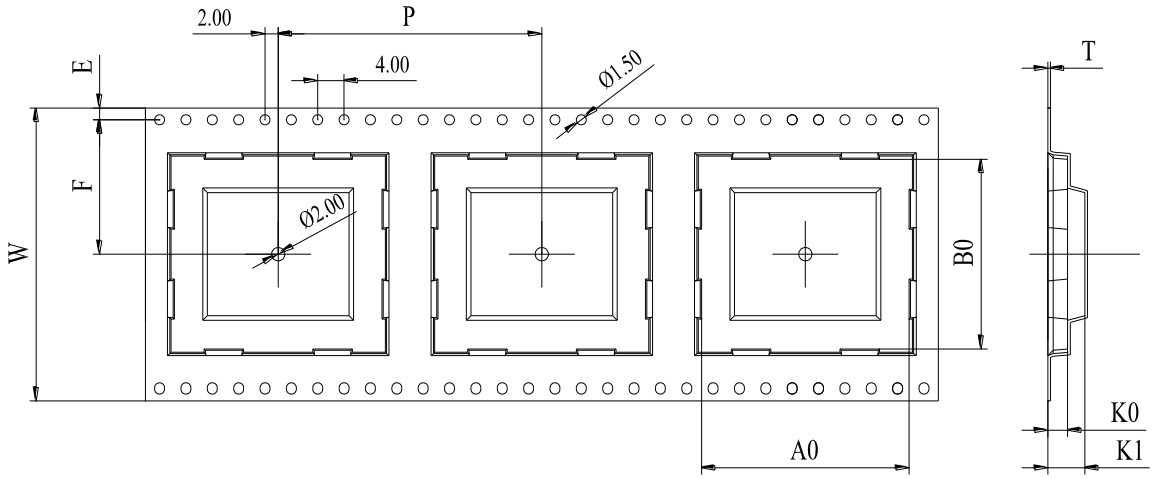


Table 48: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	44	0.35	32.5	29.5	3.0	3.8	20.2	1.75

3.6.1 Plastic Reel

Figure 49: Plastic Reel Dimension Drawing

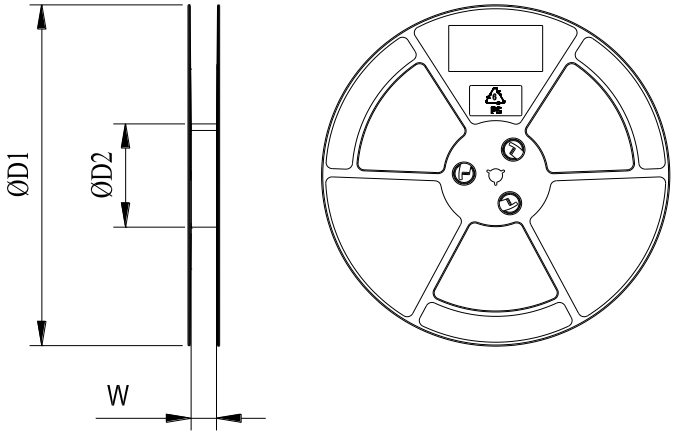
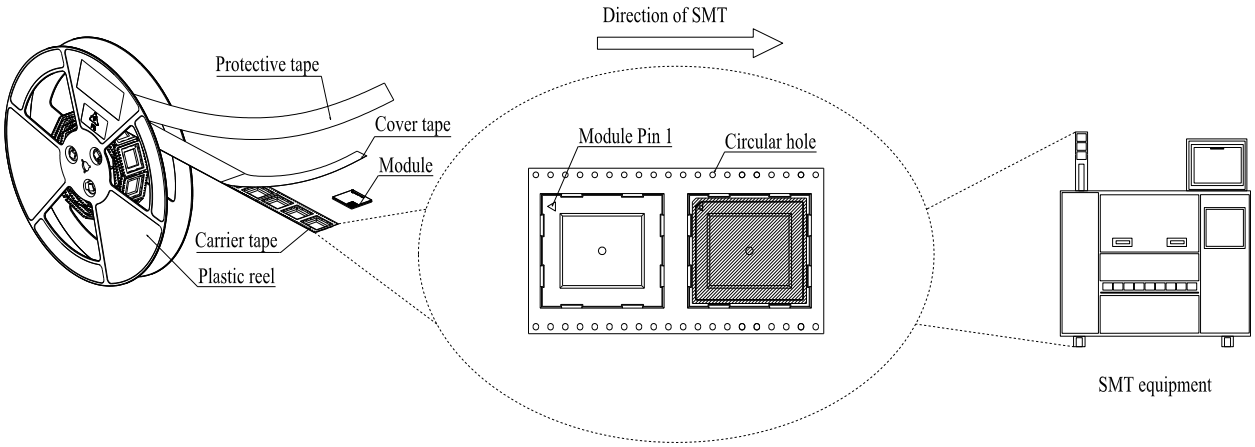


Table 49: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

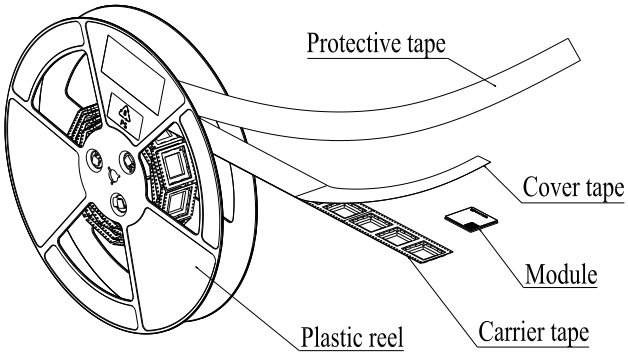
3.6.2 Mounting Direction

Figure 50: Mounting Direction



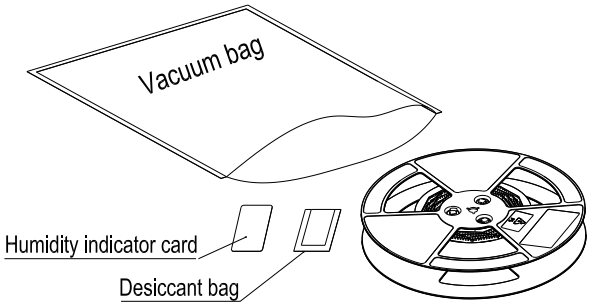
3.6.3 Packaging Process

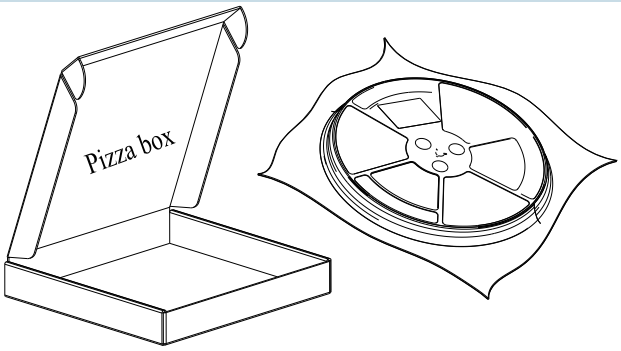
Figure 51: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can load 250 modules.

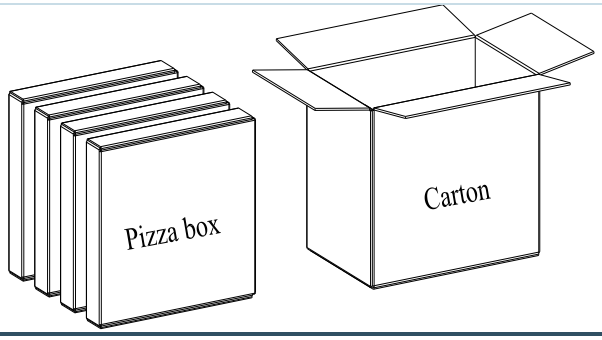
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.



9 Appendix

Table 50: Related Documents

Document Name
1. NetPrisma-UMTS&LTE-EVB-User-Guide
2. NetPrisma-LUH32-WWD&LUH33-WWD-AT-Commands-Manual
3. NetPrisma-LUH32-WWD&LUH33-WWD-QCFG-AT-Commands-Manual
4. NetPrisma-LUH32-WWD&LUH33-WWD-Low-Power-Mode-Application-Note
5. NetPrisma-LUH32-WWD&LUH33-WWD-Reference-Design
6. NetPrisma-LUH32-WWD&LUH33-WWD-GNSS-Application-Note
7. NetPrisma-RF-Layout-Application-Note
8. NetPrisma-Module-Stencil-Design-Requirements
9. NetPrisma-Module-SMT-Application-Note

Table 51: List of Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AGNSS	Assisted GNSS (Global Navigation Satellite System)
AMR	Adaptive Multi-rate
AMR-WB	Adaptive Multi-Rate Wideband
bps	Bits Per Second
BDS	BeiDou Navigation Satellite System
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
CS	Coding Scheme
CTS	Clear to Send
DC-HSPA+	Dual-carrier High Speed Packet Access

DCS	Digital Communication System
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure

IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long Term Evolution
MAC	Medium Access Control
M2M	Machine to Machine
MCS	Modulation and Coding Scheme
MIMO	Multiple Input Multiple Output
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MS	Mobile Station
MSL	Moisture Sensitivity Level
MT	Mobile Termination
NAND	NON-AND
NITZ	Network Identity and Time Zone / Network Informed Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PING	Packet Internet Groper
POS	Point of Sale
PPP	Point-to-Point Protocol

PTP	Precision Time Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QMI	Qualcomm Message Interface
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RTS	Ready To Send
Rx	Receive
SDR	Software-Defined Radio
SGMII	Serial Gigabit Media Independent Interface
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VLAN	Virtual Local Area Network

Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High Level Voltage
V_{IL}max	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

Document History

Version	Date	Description
0.1	2025-01-22	Draft

FCC Statement

FCC ID: 2BEY3LUH32WWDA

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NetPrisma that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:
“Contains FCC ID: 2BEY3LUH32WWDA”
“Contains IC: 32052-LUH32WWDA “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Antenna Type	Max Gain	
External Antenna	LTE Band 2: 1.59dBi LTE Band 4: 2.0dBi LTE Band 5: 2.13dBi LTE Band 7: 3.0dBi LTE Band 12: 3.26dBi LTE Band 13: 4.45dBi LTE Band 25: 1.59dBi LTE Band 26: 2.53dBi LTE Band 38: 2.06dBi LTE Band 41: 3.0dBi LTE Band 66: 2.0dBi	WCDMA Band 2: 1.59dBi WCDMA Band 4: 2.0dBi WCDMA Band 5: 2.13dBi GSM850: 2.13dBi GSM1900: 1.59dBi

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27 and part 90 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC Statement

IC: 32052-LUH32WWDA

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following

two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 32052-LUH32WWDA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 32052-LUH32WWDA ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

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