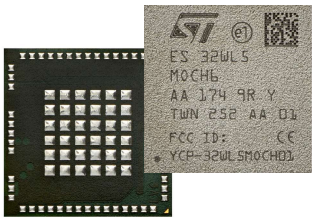
life.augmented

STM32WL5MOC

Datasheet

Multiprotocol LPWAN dual-core module 32-bit Arm® Cortex®-M4/M0+ LoRa®, (G)FSK, (G)MSK, BPSK



LGA92 (10x10 mm)
Non-contractual images

Product status
STM32WL5MOC

Features

Includes ST state-of-the-art patented technology.

Integration of STM32WL55JC:

- Dual-core Arm® Cortex®-M0 and Arm® Cortex®-M4 CPU
- ART Accelerator with a speed of up to 48 MHz
- 256-Kbyte flash memory
- 64- Kbyte SRAM with sub-GHz radio transceiver
- Embedded 32 MHz radio TCXO and 32 kHz RTC crystals
- All RF components for transmission and reception matching network, including default antenna filter
- STSAFE-A110 footprint
- Metal shield coating

Supporting:

- Frequencies from 864 MHz to 928 MHz
- Compatible with standardized or proprietary protocols such as LoRaWAN®, Sigfox™, or W- MBus (fully open wireless system-on-chip mioty).
- Compliant with radio frequency regulations such as ETSI EN 300 220, FCC CFR 47 Part 15, and Japanese ARIB STD- T-108:
  - FCC ID: YCP-32WL5MOCH01
  - IC: 8976A-32WL5MOCH01
  - If other power or modulation settings than the type documented in the FCC and ISED-Canada filings are used, a class 2 permissive change must be filed with FCC and ISED.
- Rx sensitivity: –123 dBm for 2-FSK (at 1.2 Kbit/s), –148 dBm for LoRa® (at 10.4 kHz, spreading factor 12)
- Transmitter high output power, programmable up to +22 dBm
- Transmitter low output power, programmable up to +15 dBm
- 37 GPIOs

Hardware configurations (2-layer PCB compatible)

- Transmitter high-output power programmable up to 22 dBm
- Transmitter low-output power programmable up to 15 dBm
- Transmitter high- or low-output power capable with external switch control

Ultra-low-power platform

- 1.8 V to 3.6 V V_{DD} voltage range
- -40°C to 85°C temperature range
- Embedded SMPS

10x10 small form factor

All packages are ECOPACK2 compliant.

1 Introduction

This document provides information on STM32WL5MOC modules, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

For further details on the STM32WL55 module, refer to the dedicated product datasheet (DS13293) and reference manual (RM0453).

This document should be read with the multiprotocol LPWAN dual core 32-bit Arm®Cortex®-M4/M0+ LoRa®, (G)FSK, (G)MSK, BPSK, up to 256KB flash, 64KB SRAM datasheet (DS13293) and the STM32WL5x advanced Arm®-based 32-bit MCUs with sub-GHz radio solution reference manual (RM0453). Both documents are available from the STMicroelectronics website *http://www.st.com*.

For information on the Arm® Cortex®-M4 and Arm® Cortex®-M0+ cores, refer respectively to the Cortex®-M4 technical reference manual and to the Cortex®-M0+ technical reference manual, available from the www.arm.com website.

For information on LoRa® modulation, refer to the Semtech website. (https://www.semtech.com/technology/lora).

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

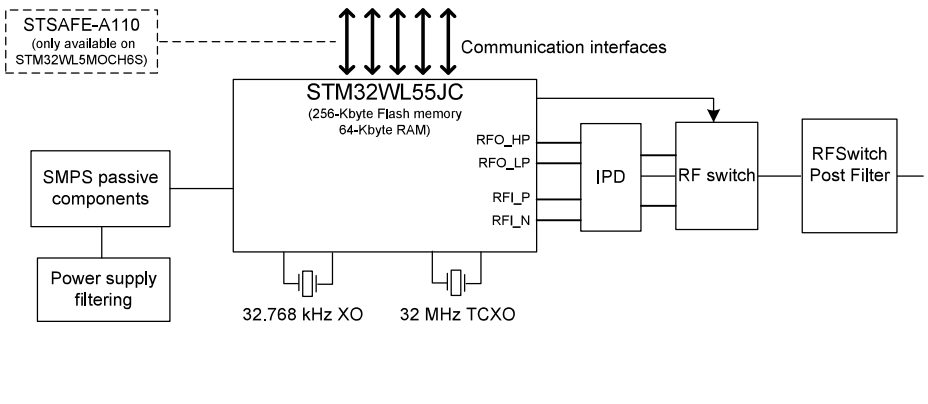
The STM32WL5MOC long-range wireless and ultralow-power certified module embeds a powerful and ultralow-power LPWAN-compliant radio solution, enabling the following modulations: LoRa®, (G)FSK, (G)MSK, and BPSK. The STM32WL5MOC does not require any RF expertise. It is the best way to speed up any development, and to reduce associated costs. This module is completely protocol stack royalty-free.

Table 1. STM32WL5MOC features and peripheral counts

Feature		STM32WL5MOC
CPU		Arm®Cortex®-M4 and Cortex®-M0
Maximum CPU frequency (MHz)		48
Flash memory density (Kbytes)		256
SRAM density (Kbytes)	SRAM1	32
	SRAM2	32
Radio	LoRa	yes
	(G)FSK	
	(G)MSK	
	BPSK	
Radio PA	Low output power (up to 15 dBm)	yes
	High output power (up to 22 dBm)	
Timer	General purpose	4
	Low power	3
	SysTick	1
Communication interface	SPI/I2S	2 (1 supporting I2S)
	I2C	3
	USART	2
	LPUART	1
Watchdog	Independent	1
	Window	1
RTC (with wake-up counter)		1
DMA (7 channels)		2
Mailbox and semaphores		1
Security	AES 256 bits	1
	RNG	1
	PKA	1
	PCROP, RDP, WRP	1
	CRC	1
	64-bit UID compliant with IEEE 802-2001 standard	1
	96-bit die ID	1
	Storage and management of secure keys	1
	Secure sub-GHz MAC layer	1

Feature		STM32WL5MOC
Security	Secure firmware update	1
	Secure firmware install	1
Tamper pins		3
Wake-up pins		3
GPIOs		37 (35 on STM32WL5MOCH6S)
ADC (number of channels, ext + int)		1 (12+4)
DAC (number of channels)		1 (1)
Internal VREFBUF		Yes
Analog comparator		2
Operating voltage		1.8 to 3.6 V
Ambient operating temperature		–40 to +85 °C
Package		LGA92 (10x10 mm)
STSAFE-A110		Available on STM32WL5MOCH6S part numbers. Not available on STM32WL5MOCH6 part numbers.

Figure 1. STM32WL5MOC block diagram



3 Functional overview

The module is an SIP LGA92 package (system in package land grid array) that integrates the STM32WL55JC microcontroller (MCU).

The STM32WL5MOC includes the following components:

- LSE 32 kHz XO (crystal oscillator).
- HSE 32 MHz TCXO (temperature compensated crystal oscillator).
- An IPD (integrated passive device), integrating matching network for transmission output to matching network.
- Passive components for SMPS.
- An antenna matching.
- STSAFE-A110 footprint.

Note: For more information on the STSAFE option, contact the local STMicroelectronics sales office.

3.1 Power supply

Power supply requirements are identical to a regular STM32WL55 MCU. Refer to the product datasheet (DS13293).

Filtering capacitors on power-supply pins and components for the SMPS are already integrated into the module.

3.2 SMPS

The SMPS passive components are fitted in the module (see the reference manual and application notes for recommendations on how to use the SMPS).

3.3 Clocks

As the module integrates a 32.768 kHz crystal for LSE, and a 32 MHz crystal for HSE, it is not possible to use any clock in bypass mode.

- The LSE must be used in high-driving capability: RCC_BDCR_LSEDRV[1:0] = 11 (see the reference manual for more details).
- The HSE does not need any tuning or calibration as a TCXO is used.
- LSCO and MCO outputs are available.

3.4 RF antenna impact

The module can be connected to different antenna types. However, depending on the impedance seen by the module, the RF performance (Tx or Rx) may be impacted.

This section details the limitations obtained by load pull and source pull measurements on the MB1779 (CEB) board.

3.4.1 Impact of the antenna choice on the Tx performances

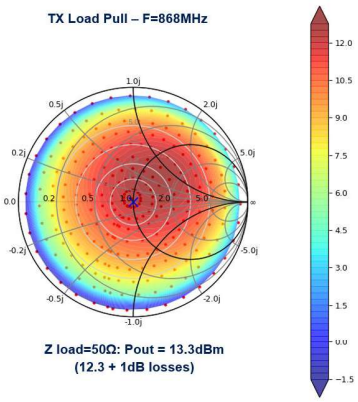
Load pull setup

Figure 2. Load pull setup

Note: Loss coming from both the tuner and the cable is estimated at 1dB.

Limitations obtained in Low power mode at 868 MHz

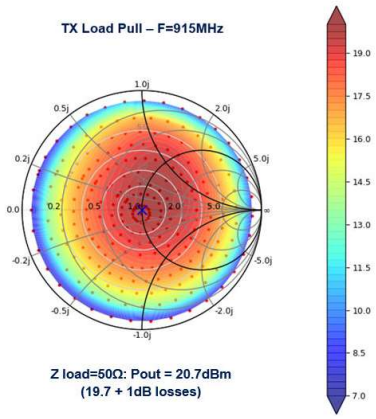
Figure 3. Limitations in Low power mode at 868 MHz



- To keep an output power > 13 dBm, the TOS presented to the module should be ≤2.
- The maximum output power (13.7 dBm) is obtained for Z load = 62 + j×30.

Limitations obtained in High power mode at 915 MHz:

Figure 4. Limitations in High power mode at 915 MHz



- To keep an output power > 20 dBm, the TOS presented to the module should be ≤2.
- Max output power 21 dBm is obtained for Z load = 63 + j×22.

3.4.2 Impact of the antenna choice on the Rx performances

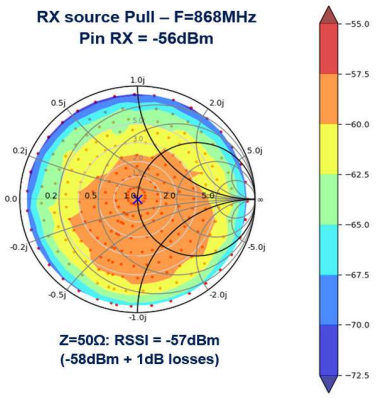
Source pull setup

Figure 5. Source pull setup

Note: Loss coming from both the tuner and the cable is estimated at 1 dB.

Limitations obtained at 868 MHz

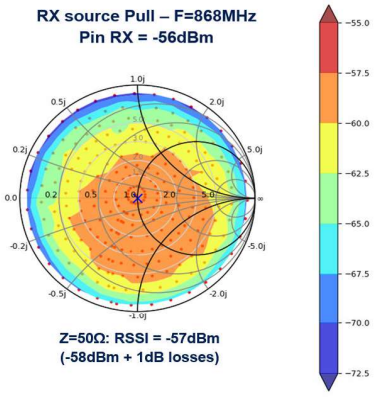
Figure 6. Limitations obtained at 868 MHz



- To keep a correct RSSI, the TOS presented to the module should be ≤2.

Limitations obtained at 915 MHz

Figure 7. Limitations obtained at 915 MHz



- To keep a correct RSSI, the TOS presented to the module should be ≤2.
- To keep good RF performances for both Tx and Rx, the TOS of the antenna should be ≤2.

3.4.3 RF path design

To ensure an efficient transmission through the air, we need to have a proper RF path design. So that an appropriate antenna type and PCB design should be considered.

To feed an antenna, transmission lines on PCBs, designed considering their characteristic impedances, are used. Then, comprehensive functional tests of the RF part are required before mass production of terminal products.

This chapter is intended to give some general guidelines when routing an RF path design.

3.4.3.1 Antenna design requirements

The antenna used on the B-WL5M-SUBG1 product is the ANT-SS900 from LPRS.

Table 2. Antenna design requirements

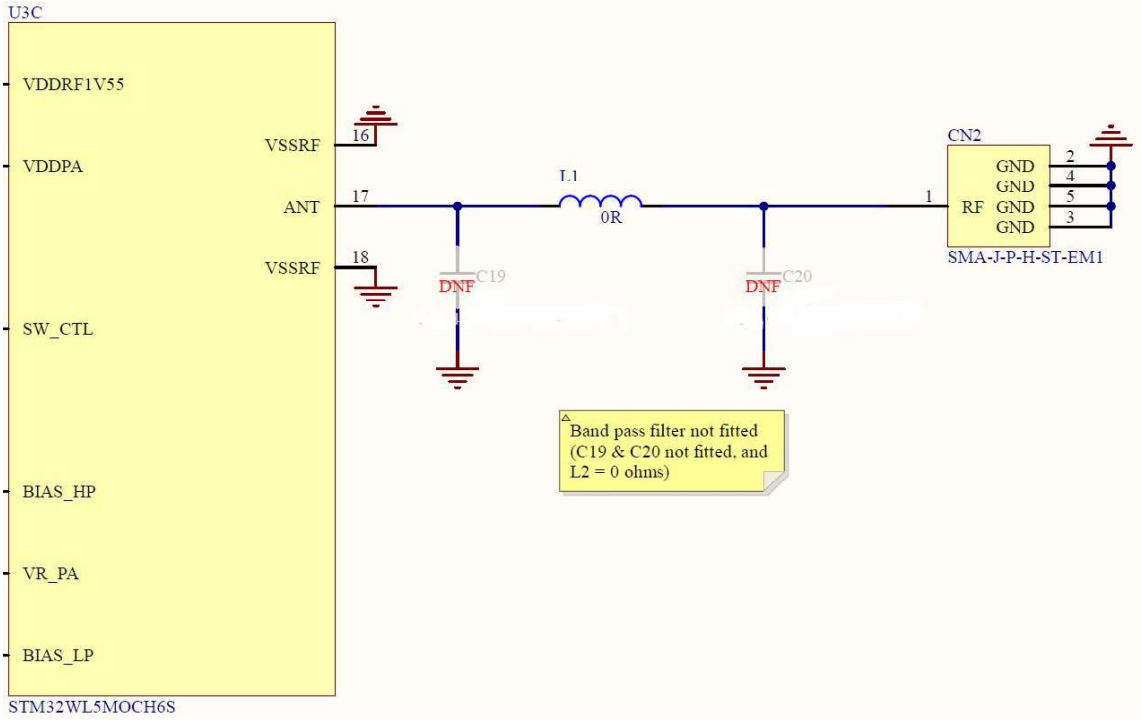
Parameter	Requirement
Frequency range	824 – 928 MHz
Nominal impedance	50 Ω
Maximum input power	50 W
Antenna gain	2dBi max

All stubby antennas with similar characteristics can be used.

3.4.3.2 *Reference schematic design*

The Reference schematic is displayed below:

Figure 8. Reference schematic design at antenna interface



It can be usefull to reserve a matching circuit (π structure) for better RF performances. The topology of the π filter (C19, L1, C20) should be placed as close as possible to the antenna connector. It is recommanded to not fit C19 and C20 and place a 0 Ω resistor at L1 position.

3.4.3.3 *RF track routing guidelines*

The characteristic impedance of the RF line between the STM32WL5MOCH and the antenna connector must be controlled to 50 Ω.

The geometry of the RF path (path width (W)), spacing between RF path and the ground (G) as well as the height (H) of the RF path to the reference ground determine its impedance. The layer of the PCB that the transmission line is routed on and the dielectric constant of the PCB materials are also used to calculate the impedance of these types of path. There are many impedance calculators with coplanar waveguide and microstrip models that are available for making these calculations.

Figure 9. **Microstrip design on a 2 PCB layer**

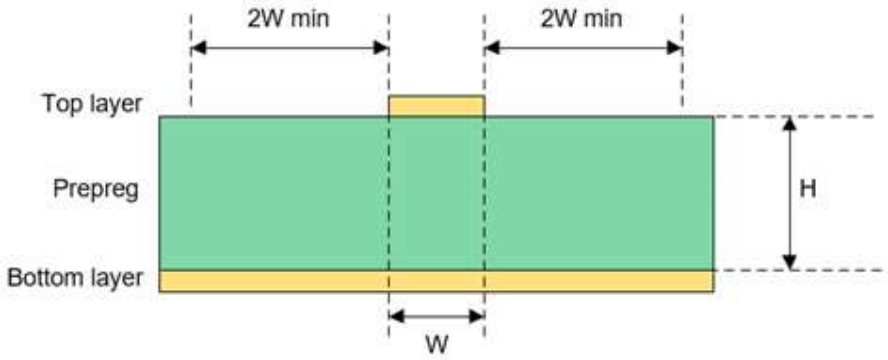
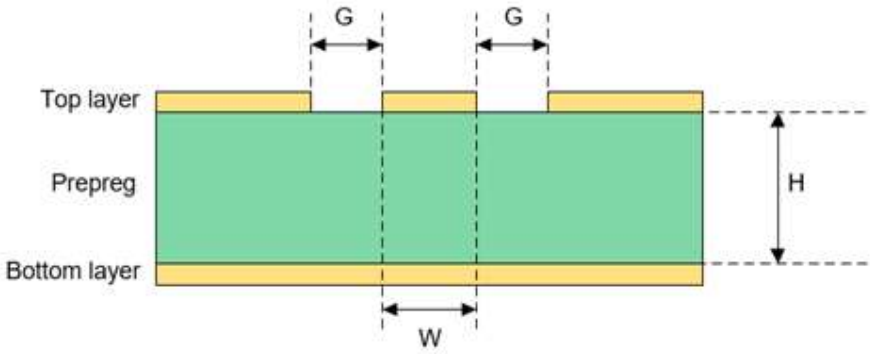


Figure 10. **Coplanar Waveguide design on a 2-PCB layer**



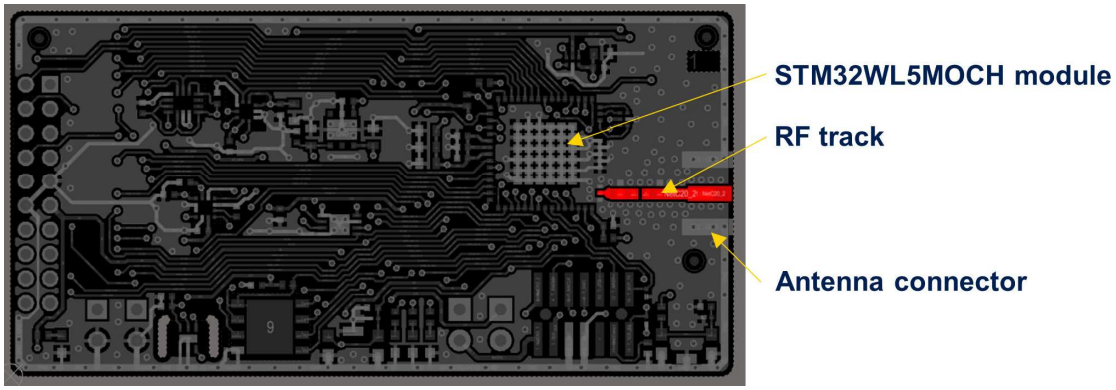
A 4-layers PCB can also be used as soon as the RF path remains controlled to 50 Ω.

Some general guidelines when routing an RF PCB are listed below:

- RF path must be short and straightforward. Make the transmission lines short and straightforward to avoid reflections, save power, and reduce high-frequency issues.
- Use an impedance simulation tool to ensure the characteristic impedance of the RF track to 50 Ω. Contact your PCB maker to verify if the values on the stack-up selected can be ensured.
- Try to maintain the characteristic impedance (50 Ω) constant. Avoid discontinuities, such as different pad sizes on transmission lines, bends, or T-junctions, or changing the RF trace width along the line.
- Minimize the distance between the STM32WL5M module RF output to the antenna connector.
- The reference ground of the RF signal should be complete. Adding some ground vias along the RF tracks can improve the RF performance.
- Keep critical signals away from RF. High-frequency signals can induce some undesired effects in critical signals such as electric and/or magnetic coupling.

Below is displayed the RF track routing of the B-WL5M-SUBG1 product.

Figure 11. **RF track routing**

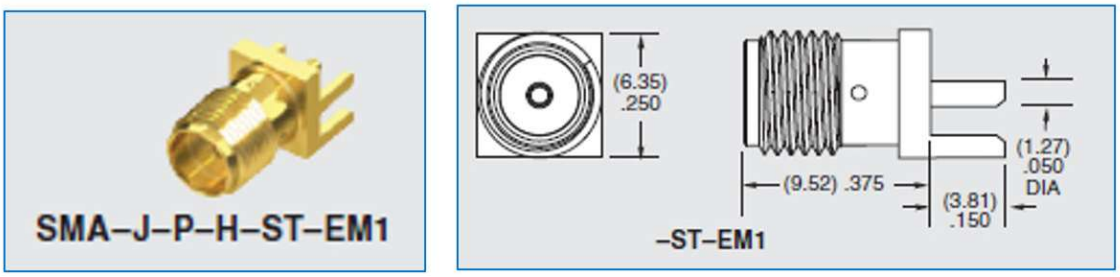


There is no specific requirement for placement as long as the above guidelines are respected.

3.4.3.4 *Antenna connector recommendations*

The SMA-J-P-H-ST-EM1 SMA connector from SAMTEC can be used.

Figure 12. **SMA-J-P-H-ST-EM1 SMA connector**



This kind of SMA connector is standard, so that an equivalent SMA connector can be used.

The antenna is stuck to the SMA connector because of FCC constraints. Indeed, it is mentioned in the FCC regulations that as soon as a product is considered general public, the FCC implies that the antenna must be stuck to the board connector with epoxy glue. Refer to the FCC documentation BASIC EQUIPMENT AUTHORIZATION GUIDANCE FOR ANTENNAS USED WITH PART 15 INTENTIONAL RADIATORS in the chapter ANTENNA REQUIREMENTS—Section 15.203. The purpose of Section 15.203 is to prevent attaching any other antennas [other than approved with the device] to a part 15 transmitter.

3.5 Hardware configurations

3.5.1 Solder bridge vs DC switch configuration

Figure 13. Solder bridge configuration

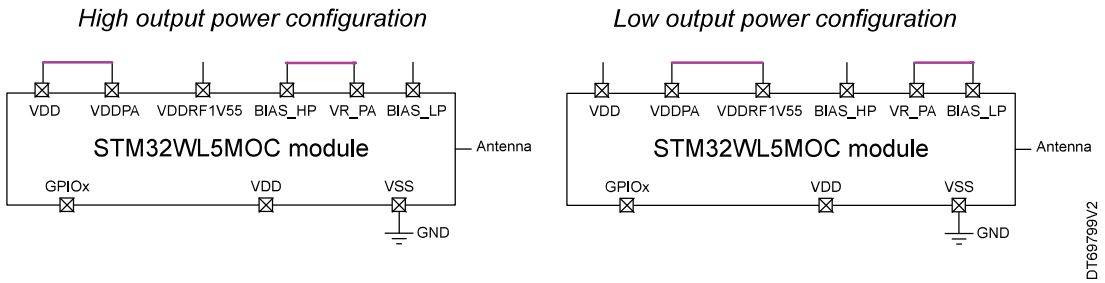
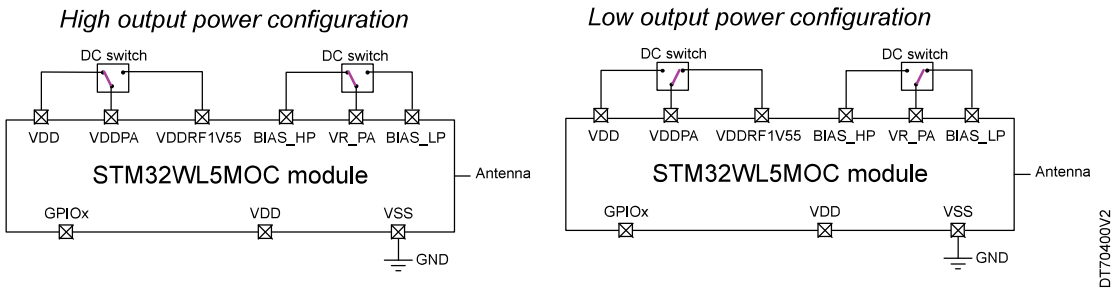


Figure 14. DC switch configuration



3.5.2 STSAFE supply

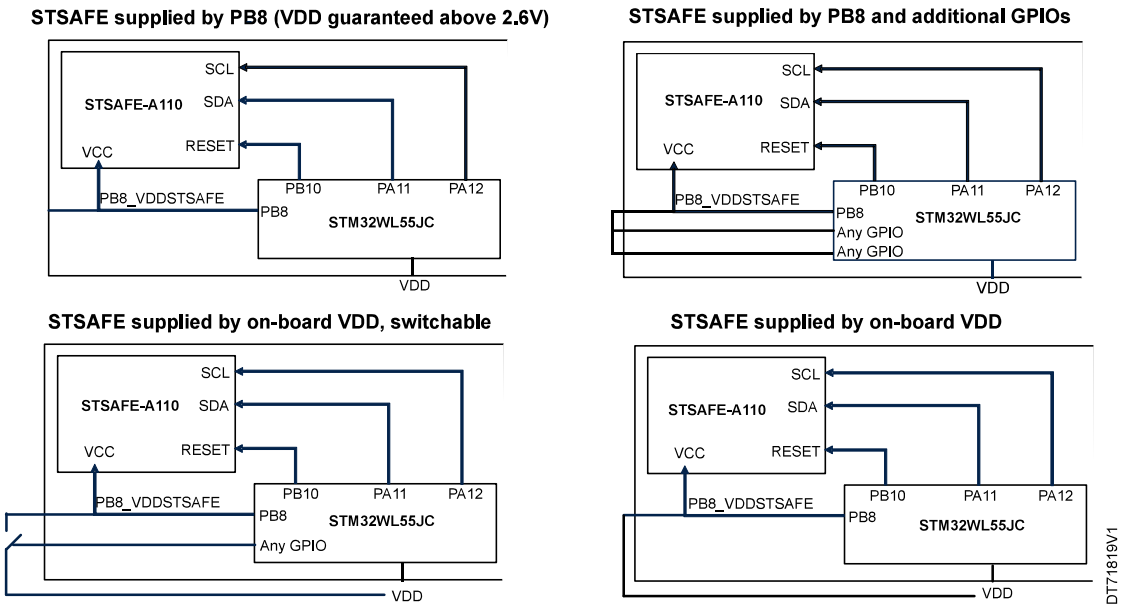
STSAFE is integrated in STM32WL5MOCH6S. To optimize power consumption, in particular in low-power mode, the GPIO PB8 controls the STSAFE supply.

When STSAFE needs to be used, GPIO PB8 must then be set up in an output configuration, and forced to '1'. STSAFE can sink up to 21 mA of power consumption. Using only PB8 as a supply limits VDD to a voltage ranging from 2.6 V to 3.6 V. See the schema “STSAFE supplied by PB8 (VDD guaranteed above 2.6 V)”.

To support the full voltage range (1.8 V to 3.6 V), different options are available:

- Connecting several GPIOs to PB8 externally, and using them as supply. See the schema “STSAFE supplied by PB8 and additional GPIOs” in Figure 15. STSAFE configurations.
- Adding an external switch-on VDD, controlled by a GPIO. See the schema “STSAFE supplied by on-board VDD, switchable” in Figure 15. STSAFE configurations.
- Connecting VDD to PB8, and configuring PB8 in Output forced to '1'. See the schema “STSAFE supplied by on-board VDD” in Figure 15. STSAFE configurations.

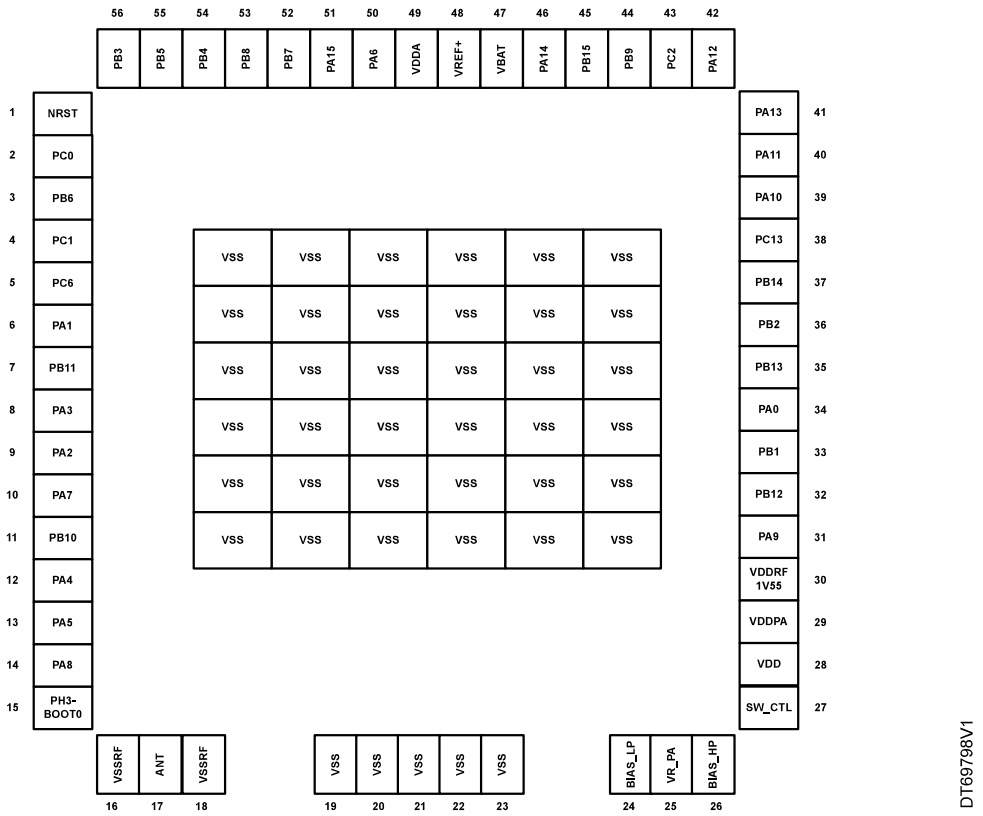
Figure 15. **STSAFE configurations**



4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 16. SIP LGA92 pinout



1. *Package top view.*

4.2 Pin description

Table 3. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/output pin
	O	Output only pin
I/O structure	FT	5 V-tolerant I/O
	RF	Radio RF pin
	Option for FT I/Os	

Name		Abbreviation	Definition
I/O structure		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 4. STM32WL5MOC pin definition

Pin number SIPLGA92	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
1	NRST	I/O	FT	-	-	-
2	PC0	I/O	FT_f	-	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT	-
3	PB6	I/O	FT_f	-	LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT	-
4	PC1	I/O	FT_f	-	LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT	-
5	PC6	I/O	FT	-	I2S2_MCK, CM4_EVENTOUT	-
6	PA1	I/O	FT_a	-	TIM2_CH2, LPTIM3_OUT, I2C1_SMBA, SPI1_SCK, USART2_RTS, LPUART1_RTS, DEBUG_PWR_REGLP2S, CM4_EVENTOUT	-
7	PB11	I/O	FT_f	-	TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT	-
8	PA3	I/O	FT_a	-	TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT	-
9	PA2	I/O	FT_a	-	LSCO, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT	LSCO
10	PA7	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_MOSIOUT, TIM17_CH1, CM4_EVENTOUT	-
11	PB10[(1)]	I/O	FT_f	-	TIM2_CH3, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT	-
12	PA4	I/O	FT	-	RTC_OUT2, LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_NSSOUT, LPTIM2_OUT, CM4_EVENTOUT	-
13	PA5	I/O	FT	-	TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_SCKOUT, LPTIM2_ETR, CM4_EVENTOUT	-
14	PA8	I-O	FT_a	-	MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT	-
15	PH3-BOOT0	I/O	FT	-	CM4_EVENTOUT	BOOT0
16	VSSRF	S	-	-	-	-
17	ANT	I/O	RF	-	-	-
18	VSSRF	S	-	-	-	-
19	VSS	S	-	-	-	-
20	VSS	S	-	-	-	-
21	VSS	S	-	-	-	-

Pin number SIPLGA92	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
22	VSS	S	-	-	-	-
23	VSS	S	-	-	-	-
24	BIAS_LP	O	RF	-	-	-
25	VR_PA	S	RF	-	-	-
26	BIAS_HP	O	RF	-	-	-
27	SW_CTL	I/O	FT	-	CM4_EVENTOUT	-
28	VDD	S	-	-	-	-
29	VDDPA	S	RF	-	-	-
30	VDDRF1V55	S	RF	-	-	-
31	PA9	I/O	FT_fa	-	TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT	-
32	PB12	I/O	FT	-	TIM1_BKIN, I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT	-
33	PB1	I/O	FT_a	-	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	COMP2_INP, ADC_IN5
34	PA0	I/O	FT_a	-	TIM2_CH1, I2C3_SMBA, I2S_CKIN, USART2_CTS, COMP1_OUT, DEBUG_PWR_REGLP1S, TIM2_ETR, CM4_EVENTOUT	PVD_IN, TAMP_IN2/ WKUP1
35	PB13	I/O	FT_fa	-	TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT	ADC_IN0
36	PB2	I/O	FT_a	-	LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSRDY, CM4_EVENTOUT	COMP1_INP, COMP2_INM, ADC_IN4
37	PB14	I/O	FT_fa	-	IM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT	ADC_IN1
38	PC13	I/O	FT	-	CM4_EVENTOUT	TAMP_IN1/ RTC_OUT1/ RTC_TS/WKUP2
39	PA10	I/O	FT_fa	-	RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/ I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INM, COMP2_INM, DAC_OUT1, ADC_IN6
40	PA11[2]	I/O	FT_fa	-	TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN7
41	PA13	I/O	FT_a	-	JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT	ADC_IN9
42	PA12[3]	I/O	FT_fa	-	TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT	ADC_IN8
43	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO, CM4_EVENTOUT	-
44	PB9	I/O	FT_f	-	TIM1_CH3N, I2C1_SDA, SPI2_NSS/I2S2_WS, IR_OUT, TIM17_CH1, CM4_EVENTOUT	-
45	PB15	I/O	FT_f	-	TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT	-
46	PA14	I/O	FT_a	-	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	ADC_IN10
47	VBAT	S	-	-	-	-

Pin number SIPLGA92	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
48	VREF+	S	-	-	-	-
49	VDDA	S	-	-	-	-
50	PA6	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_MISOOUT, TIM16_CH1, CM4_EVENTOUT	-
51	PA15	I/O	FT_fa	-	JTDI, TIM2_CH1, TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT	COMP1_INM, COMP2_INP, ADC_IN11
52	PB7	I/O	FT_f	-	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	-
53	PB8(4)	I/O	FT_f	-	TIM1_CH2N, I2C1_SCL, RF_IRQ2, TIM16_CH1, CM4_EVENTOUT	-
54	PB4	I/O	FT_fa	-	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INP, COMP2_INP, ADC_IN3
55	PB5	I/O	FT_a	-	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN, CM4_EVENTOUT	-
56	PB3	I/O	FT_a	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, DEBUG_RF_DTB1, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN2, TAMP_IN3/WKUP3
57	VSS	S	-	-	-	-
58	VSS	S	-	-	-	-
59	VSS	S	-	-	-	-
60	VSS	S	-	-	-	-
61	VSS	S	-	-	-	-
62	VSS	S	-	-	-	-
63	VSS	S	-	-	-	-
64	VSS	S	-	-	-	-
65	VSS	S	-	-	-	-
66	VSS	S	-	-	-	-
67	VSS	S	-	-	-	-
68	VSS	S	-	-	-	-
69	VSS	S	-	-	-	-
70	VSS	S	-	-	-	-
71	VSS	S	-	-	-	-
72	VSS	S	-	-	-	-
73	VSS	S	-	-	-	-
74	VSS	S	-	-	-	-
75	VSS	S	-	-	-	-
76	VSS	S	-	-	-	-
77	VSS	S	-	-	-	-
78	VSS	S	-	-	-	-

Pin number SIPLGA92	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
79	VSS	S	-	-	-	-
80	VSS	S	-	-	-	-
81	VSS	S	-	-	-	-
82	VSS	S	-	-	-	-
83	VSS	S	-	-	-	-
84	VSS	S	-	-	-	-
85	VSS	S	-	-	-	-
86	VSS	S	-	-	-	-
87	VSS	S	-	-	-	-
88	VSS	S	-	-	-	-
89	VSS	S	-	-	-	-
90	VSS	S	-	-	-	-
91	VSS	S	-	-	-	-
92	VSS	S	-	-	-	-

1. *For STM32WL5MOCH6S, this GPIO controls the STSAFE reset, which can be controlled by your own FW.*
2. *It must be used only as I2C2_SDA on STM32WL5MOCH6S.*
3. *It must be used only as I2C2_SCL on STM32WL5MOCH6S.*
4. *It must be used only as STSAFE supply on STM32WL5MOCH6S.*

4.3 Alternate functions

Table 5. Alternate function AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TM2	SPI2/ TIM1/LPTIM3	I2C1/I2C2/ I2C3	SPI1/SPI2S2	RF	USART1/ USART2
Port A	PA0	-	TIM2_CH1	-	-	I2C3_SMBA	I2S_CKIN	-	USART2_CTS
	PA1	-	TIM2_CH2	-	LPTIM3_OUT	I2C1_SMBA	SPI1_SCK	-	USART2_RTS
	PA2	LSCO	TIM2_CH3	-	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	-	-	-	I2S2_MCK	-	USART2_RX
	PA4	RTC_OUT2	LPTIM1_OUT	-	-	-	SPI1_NSS	-	USART2_CX
	PA5	-	TIM2_CH1	TIM2_ETR	SPI2_MISO	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI1_MISO	-	-
	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	SPI2_SCK/ I2S2_CK	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_NSS/ I2S2_WS	I2C1_SCL	SPI2_SCK/ I2S2_CK	-	USART1_TX
	PA10	RTC_REFIN	TIM1_CH3	-	-	I2C1_SDA	SPI2_MOSI/ I2S2_SD	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	LPTIM3_ETR	I2C2_SDA	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	LPTIM3_IN1	I2C2_SCL	SPI1_MOSI	RF_BUSY	USART1_RTS

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TM2	SPI2/ TIM1/LPTIM3	I2C1/I2C2/ I2C3	SPI1/SPI2S2	RF	USART1/ USART2
Port A	PA13	JTMS/ SWDIO	-	-	-	I2C2_SMBA	-	-	-
	PA14	JTCK/ SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	I2C1_SDA	SPI1_NSS	-	-
Port B	PB1	-	-	-	-	-	-	-	-
	PB2	-	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	RF_IRQ0	USART1_RTS
	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS
	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	RF_IRQ1	USART1_CK
	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX
	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX
	PB8	-	TIM1_CH2N	-	-	I2C1_SCL	-	RF_IRQ2	-
	PB9	-	TIM1_CH3N	-	-	I2C1_SDA	SPI2_NSS/ I2S2_WS	-	-
	PB10	-	TIM2_CH3	-	-	I2C3_SCL	SPI2_SCK/ I2S2_CK	-	-
	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	-
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS/ I2S2_WS	-	-
	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK/ I2S2_CK	-	-
	PB14	-	TIM1_CH2N	-	I2S2_MCK	I2C3_SDA	SPI2_MISO	-	-
	PB15	-	TIM1_CH3N	-	-	I2C2_SCL	SPI2_MOSI/ I2S2_SD	-	-
Port C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	-
	PC1	-	LPTIM1_OUT	-	SPI2_MOSI/ I2S2_SD	I2C3_SDA	-	-	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-
	PC6	-	-	-	-	-	I2S2_MCK	-	-
	PC13	-	-	-	-	-	-	-	-
Port H	PH3	-	-	-	-	-	-	-	-