

(JAKA RTL8822CE) User's Manual

Preliminary Version

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ENVIRONMENTAL

Operating

Operating Temperature: 0°C to +70 °C

Relative Humidity: 5-90% (non-condensing)

Storage

Temperature: -40°C to +80°C (non-operating)

Relevant Humidity: 5-95% (non-condensing)

MTBF caculation

Over 150,000hours

IMPORTANT NOTE:

This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated.

Additional testing and certification may be necessary when multiple modules are used.

20cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the IC RSS-102 radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept

any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following "Contains IC: 34212-RTL8822CE".

The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

Japan Statement

Host system must be labeled with "Contains MIC ID:211-250702“, MIC ID displayed on label

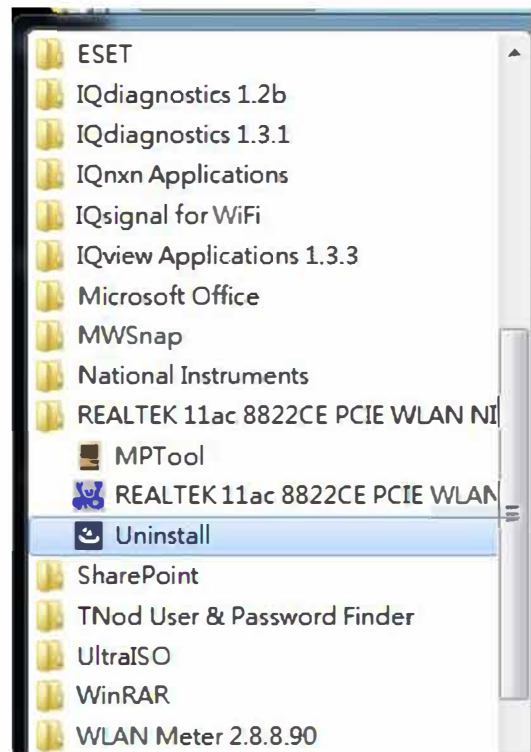
South Korea Statement

	
상 호	JAKA Robotics Co., Ltd
기자재 명칭	Wifi module
모델명	RTL8822CE
기자재 관리번호	R-C-FV3-RTL8822CE
제 조 자	JAKA Robotics Co., Ltd
제조년월	2025. 05
제 조 국 가	Made In China

Software

A. Uninstall the RTL8822CE WLAN Driver from "Start"→ "All Programs"→
"REALTEK 11ac 8822CE PCIE WLAN NIC Massproduction kit"

Please click "Uninstall" to remove RTL8822CE WLAN driver.



RTL8822CE

**SINGLE-CHIP 802.11ac/a/b/g/n 2T2R WLAN WITH
PCI EXPRESS /USB2.0 MIXED INTERFACE**

DATASHEET

1. General Description

The Realtek RTL8822CE is a highly integrated single-chip that support 2-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input , Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface controller .It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in single chip.

The RTL8822CE baseband implements Multi-user Multiple Input, Multiple Output (MU-MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8822CE provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8822CE also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8822CE builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths, and Maximum-Likelihood Detection (MLD) are implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8822CE supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8822CE MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The

RTL8822CE provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 76-pin QFN
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 2x2, Wave-2 compliant with MU-MIMO
- Complete 802.11n MIMO solution for 2.4GHz and 5GHz band
- Maximum PHY data rate up to 173.3 Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates.
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with PCI Express Base Specification Revision 2.1.
- Complies with USB2.0 FS-mode Specification for Bluetooth.
- PCIe LTR/L1.Off state supported.
- USB Selective Suspend supported.

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN.
- IEEE 802.11e QoS Enhancement (WMM).
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services.
- IEEE 802.11h DFS, TPC, Spectrum Measurement.
- IEEE 802.11k Radio Resource Measurement.
- WAPI (Wireless Authentication Privacy Infrastructure) certified.

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU).
- Low latency immediate Block Acknowledgement (BA).
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8822CE to assume multiple MAC identities when used as a wireless bridge.
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth.
- WiFi Direct supports wireless peer to peer applications

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame.
- Transmit Beamforming.
- Support S3/S4 AES/TKIP group key update.
- Support Network List Offload.

- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload.

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins.
- Two configurable LED pins.
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only.

PHY Features

- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation.
Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

3. Pin Descriptions

The following signal type codes are used in the tables:

I:Input

O:Output

T/S:Tri-State bi-directional input/output pin

O/D:Open Drain

N/A:No Bonding pin

S/T/S:Sustained Tri-State

P:Power pin

3.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	73	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode

3.2. PCI Express Transceiver Interface

2. PCI Express Transceiver Interface

Symbol	Type	Pin No	Description	Voltage
HSIN/HSIP	I	53,54	PCI Express Receive Differential Pair	
HSO/HSOP	O	50,51	PCI Express Transmit Differential Pair	
REFCLK N/RE FCLK P	I	47,48	PCI Express Differential Reference Clock Source: 100MHz $\pm$ 300ppm	
CLKREQ#	I/O/D	33	Reference Clock Request Signal. Also used by L1 PM substates. This signal is used by the RTL8822CE to request for the PCI Express reference clock.	3.3V
WAKE#	O/D	32	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks This WAKE# can be shared with BT wake up host function via sideband signals	3.3V
PERST#	I	31	PCI Express Reset Signal: active low. When the PERST# is asserted at power-on state, the RTL8822CE returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#.	3.3V

3.3. USB Transceiver Interface

Table 3. USB Transceiver Interface

Type	Pin No	Description
IO	56	High-Speed USB D+ Signal
IO	57	High-Speed USB D- Signal

3.4. RF Interface

Table 4. RF Interface

Symbol	Type	Pin No	Description
RFI WL2G S1	I	3	WLAN 2G RF input for path S1 in external LNA/FEM configuration
RFIO WL2G S1/BT	I/O O	4	(1) RF input/output of BT and path S1 WLAN 2G. (TDM for Tx) (LNA sharing for Rx) (2) Or RF output of path S1 WLAN 2G in external PA/FEM configuration
TSSI S1	I	6	TSSI input from external PA/FEM
RFI WL5G S1	I	7	WLAN 5G RF input for path S1 in external LNA/FEM configuration
RFIO WL5G S1	I/O O	9	(1) WLAN 5G RF input/output for path S1 (2) Or WLAN 5G RF output for path S1 in external PA/FEM configuration
RFI WL2G S0	I	11	WLAN 2G RF input for path S0 in external LNA/FEM configuration

RFIO_WL2G_S0	I/O O	12	(1) RF input/output of path S0 WLAN 2G (2) Or RF output of path S0 WLAN 2G in external PA/FEM configuration
TSSI_S0	I	14	TSSI input from external PA/FEM
RFIO_WL5G_S0	I/O O	17	(1) WLAN 5G RF input/output for path S0 (2) Or WLAN 5G RF output for path S0 in external PA/FEM configuration
RFI_WL5G_S0	I	18	WLAN 5G RF input for path S0 in external LNA/FEM configuration

3.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
WL_LED	O	66	WL LED Pin (Active Low), shared with GPIO8

3.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS#	I	27	Shared with GPIO9. This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN function will be Radio-off. When this function is not required, external pull high is not required.
HOST_WAKE_WL	O	29	Shared with GPIO12. The Host wakes up the WLAN controller in Remote Wakeup Mode.

3.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	22	40MHz OSC Input 40MHz crystal reference clock input
XO	O	23	40MHz Crystal reference clock output
SUS_CLK	I	67	External 32K or RTC clock input.
EESK	I	68	WLAN eFuse autoload
GPIO0	IO	69	General Purpose Input/Output Pin
GPIO1	IO	70	General Purpose Input/Output Pin
GPIO2	IO	71	General Purpose Input/Output Pin
GPIO3	IO	72	General Purpose Input/Output Pin
GPIO4	IO	73	General Purpose Input/Output Pin
GPIO5	IO	26	General Purpose Input/Output Pin
GPIO6	IO	28	General Purpose Input/Output Pin
GPIO7	IO	30	General Purpose Input/Output Pin
GPIO8	IO	66	General Purpose Input/Output Pin
GPIO9	IO	27	General Purpose Input/Output Pin
GPIO10	IO	63	General Purpose Input/Output Pin
GPIO11	IO	29	General Purpose Input/Output Pin
GPIO12	IO	61	General Purpose Input/Output Pin
GPIO13	IO	62	General Purpose Input/Output Pin

3.8. HCI Power Pins

Table 8. HCI Power Pins

Symbol	Type	Pin No	Description
LDO_V13_PHY_I	P	46	LDO 1.3V PHY Input
GND_TX	P	52	Ground for host interface
RREF	P	45	Precision Resistor for Bandgap
VD10_VDDTX	P/I	49	1.05V for analog circuits in interface

VD33_USB	P	59	3.3V for USB
VD10_USB	P	55	1.05V for USB
GND_USB	P	58	Digital GND

3.9. Digital Power Pins

Table 9. Digital Power Pins

Symbol	Type	Pin No	Description
VD33_IO	P	43	VDD3.3V for Digital IO (PERST#, WAKE#, CLKREQ#, WL_LED)
VDD_IO	P	60	VDD for GPIO[0:14], SUS_CLK, EESK
VD10D_WLBB_TOP/VD10D_WLBB_RIGHT	P	44,31	1.05V for WLAN BB digital power

3.10. REGU Power Pins

Table 10. REGU Power Pins

Symbol	Type	Pin No	Description
LX_SPS_V13_O	P	40,41	Switching Regulator 1.3V Output
VD33_SPS	P	42	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
LDO_V13_I	P	37,38	LDO 1.3V Input
LDO_V10_O	P	35,36	LDO 1.05V Output
GND_SPS	P	39	Switching Regulator Ground

3.11. RF Power Pins

Table 11. RF Power Pins

Symbol	Type	Pin No	Description
VD33_LDO_WL	P	1	VDD 3.3V for internal LDO input
VD13_TRX_S1	P	2	VDD 1.3V for S1 WLAN RF
VD33_TX2G_S1	P	5	VDD 3.3V for S1 2G WLAN PA
VD33_TX5G_S1	P	8	VDD 3.3V for S1 5G WLAN PA
VD33_PAD_S1	P	10	VDD 3.3V for S1 2/5G WLAN PAD
VD33_TX2G_S0	P	13	VDD 3.3V for S0 2G WLAN PA
VD33_PAD_S0	P	15	VDD 3.3V for S0 2/5G WLAN PAD
VD33_TX5G_S0	P	16	VDD 3.3V for S0 5G WLAN PA
VD13_TRX_S0	P	19	VDD 1.3V for S0 WLAN RF
VD13_SYN	P	20	VDD 1.3V for WLAN synthesizer
VD33_SYN	P	21	VDD 3.3V for WLAN synthesizer
VD33X	P		VDD 3.3V for Crystal
VD13_AFE	P		VDD 1.3V for WLAN AFE