# AF61Y Hardware Design

**Automotive Wi-Fi&Bluetooth Module Series**

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

| | |
|---|---|
|  | Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving. |
|  | Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft. |
|  | Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities. |
|  | Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances. |
|  | The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment. |
|  | In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders. |

# About the Document

## Revision History

| Version | Date | Author | Description |
|---|---|---|---|
| - | 2023-05-06 | Isabella LI/ Ashley HUANG/ Morris XIAO | Creation of the document |
| 1.0 | 2024-02-07 | Isabella LI/ Gwara ZHANG/ Morris XIAO | First official release |

# Contents

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# 1 Introduction

This document describes the AF61Y features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information as well.

## 1.1. Special Mark

**Table 1: Special Mark**

| Mark | Definition |
|---|---|
| * | Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable. |

# 2 Product Overview

AF61Y is an automotive Wi-Fi and Bluetooth module with low power consumption and high performance. It is compliant with IEEE 802.11a/b/g/n/ac and Bluetooth 5.2 standard protocols. The module provides a PCIe interface for Wi-Fi application and UART and PCM interfaces for Bluetooth application, and it also supports a WWAN & WLAN/Bluetooth coexistence interface. It is an SMD module with compact packaging. Related information is listed in the table below:

**Table 2: Basic Information**

| AF61Y | |
|---|---|
| Packaging type | LGA |
| Pin counts | 112 |
| Dimensions | (23.0 ±0.2) mm × (23.0 ±0.2) mm × (3.0 ±0.2) mm |
| Weight | Approx. 3.58 g |

## 2.1. Key Features

**Table 3: Key Features**

| Category | Description |
|---|---|
| Supply Voltages | **VDD_CORE:**<br>● 1.71–1.89 V<br>● Typical: 1.8 V<br>**VDD_IO:**<br>● 1.62–1.98 V<br>● Typical: 1.8 V<br>**VDD_PA:**<br>● 2.09–2.31 V<br>● Typical: 2.2 V |

| | |
|---|---|
| Operating Frequencies | **Wi-Fi:**<br>● 2.4 GHz: 2.400–2.4835 GHz<br>● 5 GHz: 5.150–5.850 GHz<br>**Bluetooth:**<br>● 2.402–2.480 GHz |
| Wi-Fi Data Rates | **2.4 GHz:**<br>● 802.11b: 1 Mbps, 2 Mbps, 5.5 Mbps, 11 Mbps<br>● 802.11g: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps<br>● 802.11n: HT20 (MCS 0–7), HT40 (MCS 0–7)<br>**5 GHz:**<br>● 802.11a: 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps<br>● 802.11n: HT20 (MCS 0–7), HT40 (MCS 0–7)<br>● 802.11ac: VHT20 (MCS 0–8), VHT40 (MCS 0–9), VHT80 (MCS 0–9) |
| Wi-Fi Transmit Power | **2.4 GHz:**<br>● 802.11b @ 11 Mbps: 17.5 dBm<br>● 802.11g @ 54 Mbps: 15 dBm<br>● 802.11n @ HT20 MCS 7: 13.5 dBm<br>● 802.11n @ HT40 MCS 7: 12 dBm<br>**5 GHz:**<br>● 802.11a @ 54 Mbps: 13 dBm<br>● 802.11n @ HT20 MCS 7: 12.5 dBm<br>● 802.11n @ HT40 MCS 7: 12 dBm<br>● 802.11ac @ VHT20 MCS 8: 11.5 dBm<br>● 802.11ac @ VHT40 MCS 9: 10 dBm<br>● 802.11ac @ VHT80 MCS 9: 9.5 dBm |
| Wi-Fi Protocol Features | The module complies with IEEE 802.11a/b/g/n/ac protocol |
| Wi-Fi Modulations | CCK, BPSK, QPSK, 16QAM, 64QAM and 256QAM |
| Wi-Fi Operating Modes | AP and STA |
| Bluetooth Protocol Features | Bluetooth 5.2 |
| Bluetooth Modulations | GFSK, 8-DPSK and π/4-DQPSK |
| Bluetooth Operating Modes | ● Bluetooth Classic (BR + EDR)<br>● Bluetooth Low Energy (BLE) |
| Wi-Fi & Bluetooth Application Interfaces | ● PCIe interface: for Wi-Fi application<br>● UART & PCM interfaces: for Bluetooth application |
| Antenna Interfaces | ● Bluetooth & Wi-Fi 0 antenna interface (ANT_WIFI0)<br>● Wi-Fi 1 antenna interface (ANT_WIFI1)<br>● Reserved dedicated Bluetooth antenna interface (ANT_BT*) |

| | |
|---|---|
| | ● 50 Ω characteristic impedance |
| Temperature Ranges | ● Normal operating temperature [1]: -40 °C to +85 °C<br>● Storage temperature: -40 °C to +90 °C |
| RoHS | All hardware components are fully compliant with EU RoHS directive |

## 2.2. Functional Diagram

The functional diagram illustrates the following major functional parts:

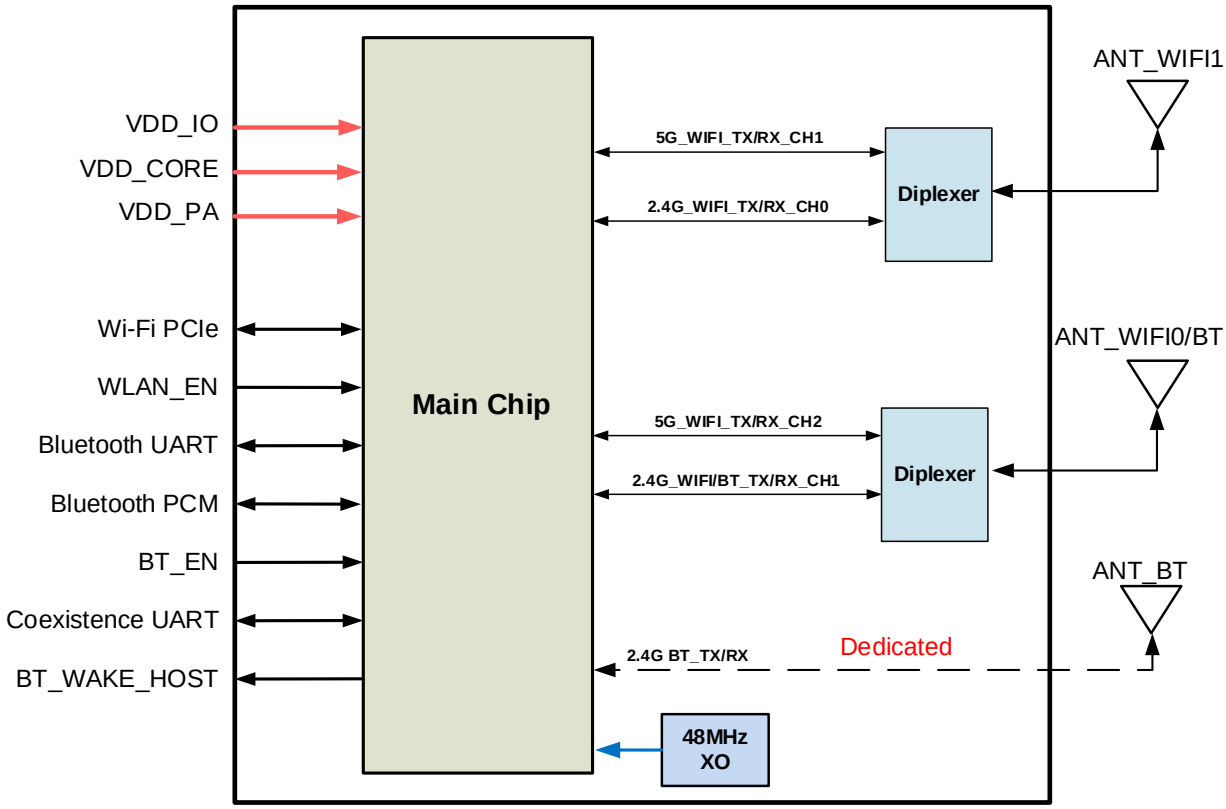



**Figure 1: Functional Diagram**

[1] Within this operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.

## 2.3. Pin Assignment

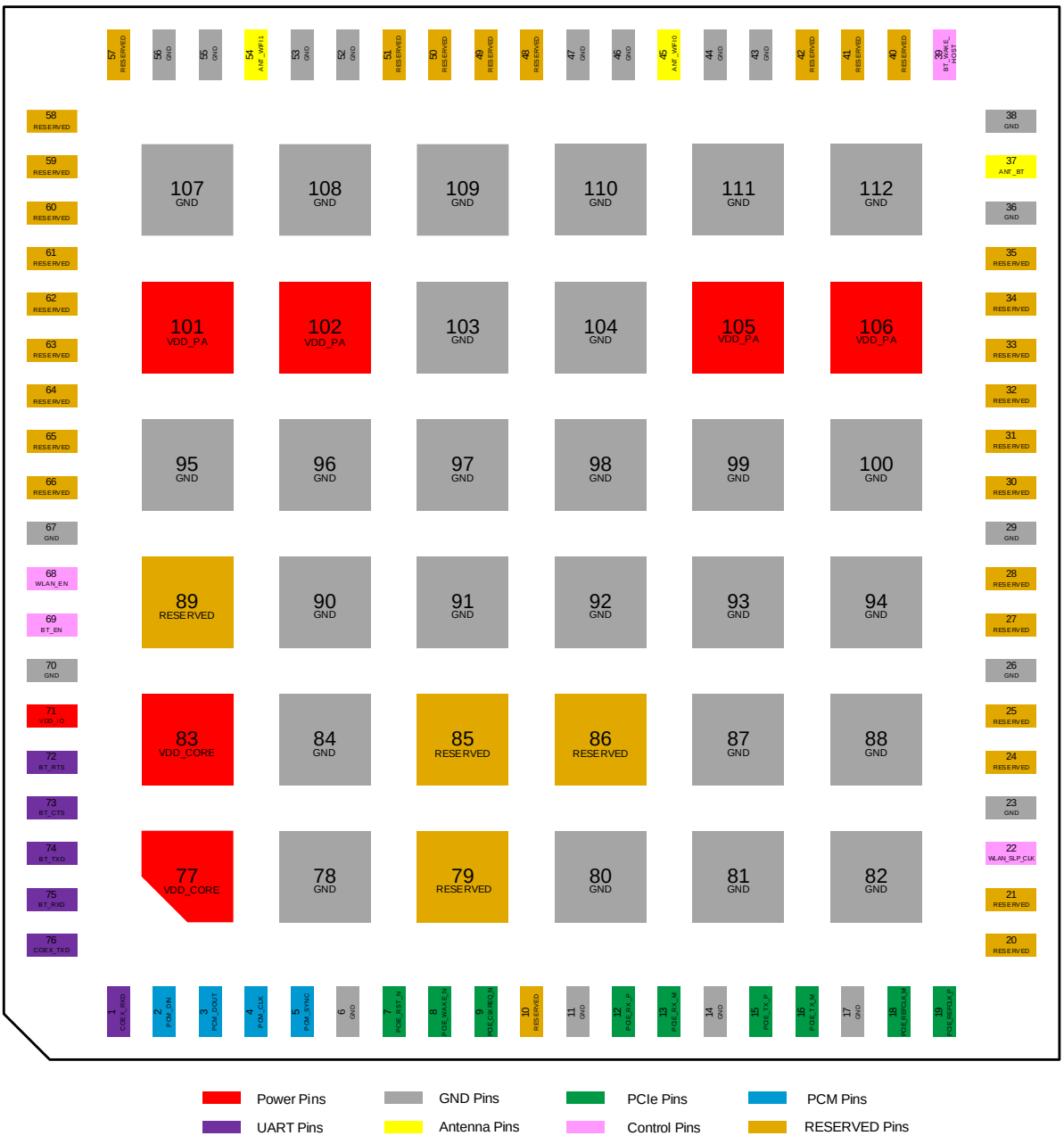



**Figure 2: Pin Assignment (Top View)**

**NOTE**

1. Keep all RESERVED and unused pins unconnected.
2. All GND pins should be connected to ground.

## 2.4. Pin Description

**Table 4: Parameter Definition**

| Parameter | Description |
|---|---|
| AI | Analog Input |
| AO | Analog Output |
| AIO | Analog Input/Output |
| DI | Digital Input |
| DO | Digital Output |
| PI | Power Input |

DC characteristics include power domain and rated current.

**Table 5: Pin Description**

| **Power Supply and GND** | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |
| VDD_CORE | 77, 83 | PI | Main power supply for the module | Vmin = 1.71 V<br>Vnom = 1.8 V<br>Vmax = 1.89 V | It must be provided with sufficient current up to 1.3 A. |
| VDD_PA | 101, 102, 105, 106 | PI | Power supply for RF | Vmin = 2.09 V<br>Vnom = 2.2 V<br>Vmax = 2.31 V | It must be provided with sufficient current up to 1.5 A. |
| VDD_IO | 71 | PI | Power supply for the module's I/O pins | Vmin = 1.62 V<br>Vnom = 1.8 V<br>Vmax = 1.98 V | It must be provided with sufficient current up to 50 mA. |
| GND | 6, 11, 14, 17, 23, 26, 29, 36, 38, 43, 44, 46, 47, 52, 53, 55, 56, 67, 70, 78, 80–82, 84, 87, 88, 90–100, 103, 104, 107–112 | | | | |
| **Bluetooth Application Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |

| | | | | | |
|---|---|---|---|---|---|
| BT_EN | 69 | DI | Bluetooth enable control | VDD_IO | Active high. |
| PCM_SYNC | 5 | DIO | PCM data frame sync | | In master mode, it is an output signal. In slave mode, it is an input signal. Please ensure that the level logic is low during boot-up. |
| PCM_CLK | 4 | DIO | PCM clock | | In master mode, it is an output signal. In slave mode, it is an input signal. |
| PCM_DIN | 2 | DI | PCM data input | | If unused, keep it open. |
| PCM_DOUT | 3 | DO | PCM data output | | Please ensure that the level logic is high during boot-up. |
| BT_TXD | 74 | DO | Bluetooth UART transmit | | Please ensure that the level logic is high during boot-up. |
| BT_RXD | 75 | DI | Bluetooth UART receive | | |
| BT_RTS | 72 | DO | Request to send signal from the module | | Please ensure that the level logic is high during boot-up. |
| BT_CTS | 73 | DI | Clear to send signal to the module | | |
| **Wi-Fi Application Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |
| WLAN_EN | 68 | DI | WLAN function enable control | VDD_IO | Active high. |
| PCIE_REFCLK_P | 19 | AI | PCIe reference clock (+) | | Require differential impedance of 100 Ω. PCIe Gen 2 compliant. |
| PCIE_REFCLK_M | 18 | AI | PCIe reference clock (-) | | |
| PCIE_TX_M | 16 | AO | PCIe transmit (-) | | |
| PCIE_TX_P | 15 | AO | PCIe transmit (+) | | |
| PCIE_RX_M | 13 | AI | PCIe receive (-) | | |

| | | | | | |
|---|---|---|---|---|---|
| PCIE_RX_P | 12 | AI | PCIe receive (+) | | |
| PCIE_CLKREQ_N | 9 | DO | PCIe clock request | | |
| PCIE_RST_N | 7 | DI | PCIe reset | VDD_IO | |
| PCIE_WAKE_N | 8 | DO | PCIe wake up | | |
| **RF Antenna Interfaces** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |
| ANT_WIFI0 | 45 | AIO | Bluetooth & 2.4 GHz/5 GHz Wi-Fi 0 antenna interface | | 50 Ω characteristic impedance. |
| ANT_WIFI1 | 54 | AIO | 2.4 GHz/5 GHz Wi-Fi 1 antenna interface | | |
| ANT_BT* | 37 | AIO | Reserved dedicated Bluetooth antenna interface | | |
| **Coexistence UART Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |
| COEX_TXD | 76 | DO | WWAN & WLAN/ Bluetooth coexistence transmit | VDD_IO | Please ensure that the level logic is high during boot-up. If unused, keep it open. |
| COEX_RXD | 1 | DI | WWAN & WLAN/ Bluetooth coexistence receive | | If unused, keep it open. |
| **WLAN_SLP_CLK Interface*** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |
| WLAN_SLP_CLK | 22 | DI | WLAN sleep clock | 1.8 V | Internal sleep clock is used by default. Keep it open. |
| **Control Signal Interface*** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristic** | **Comment** |

| | | | | | |
|---|---|---|---|---|---|
| BT_WAKE_HOST | 39 | DO | Bluetooth wake up host | 1.8 V | Please ensure that the level logic is low during boot-up. |
| **Reserved Pins** | | | | | |
| **Pin Name** | **Pin No.** | | | | **Comment** |
| RESERVED | 10, 20, 21, 24, 25, 27, 28, 30–35, 40–42, 48–51, 57–66, 79, 85, 86, 89 | | | | Keep them open. |

## 2.5. EVB Kit

Quectel supplies an evaluation board (V2X&5G EVB) with accessories to develop and test the module. For more details, see ***document [1]***.

# 3 Operating Characteristics

## 3.1. Power Supply

### 3.1.1. Power Supply Interfaces

The following table shows the power supply and ground pins of the module.

**Table 6: Power Supply and GND Pins**

| Pin Name | Pin No. | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD_CORE | 77, 83 | Main power supply for the module | 1.71 | 1.8 | 1.89 | V |
| VDD_PA | 101, 102, 105, 106 | Power supply for RF | 2.09 | 2.2 | 2.31 | V |
| VDD_IO | 71 | Power supply for the module's I/O pins | 1.62 | 1.8 | 1.98 | V |
| GND | 6, 11, 14, 17, 23, 26, 29, 36, 38, 43, 44, 46, 47, 52, 53, 55, 56, 67, 70, 78, 80–82, 84, 87, 88, 90–100, 103, 104, 107–112 | | | | | |

### 3.1.2. Reference Design for Power Supply

The module is powered by VDD_CORE and VDD_PA. It is recommended to use a power supply chip with maximum output current up to 1.3 A for VDD_CORE, and a power supply chip with maximum output current up to 1.5 A for VDD_PA. For better power supply performance, it is recommended to parallel a 100 µF decoupling capacitor and 22 µF, 100 nF, 33 pF and 10 pF filter capacitors near the input terminal of the VDD_CORE and VDD_PA. Meanwhile, it is suggested to add a TVS component near the input terminal of the VDD_CORE and VDD_PA to improve the surge voltage bearing capacity of the module. As per design rules, the longer the traces of the VDD_CORE and VDD_PA are, the wider they should be.

Reference circuit of the input terminal of the VDD_CORE and VDD_PA is shown in the figure below:

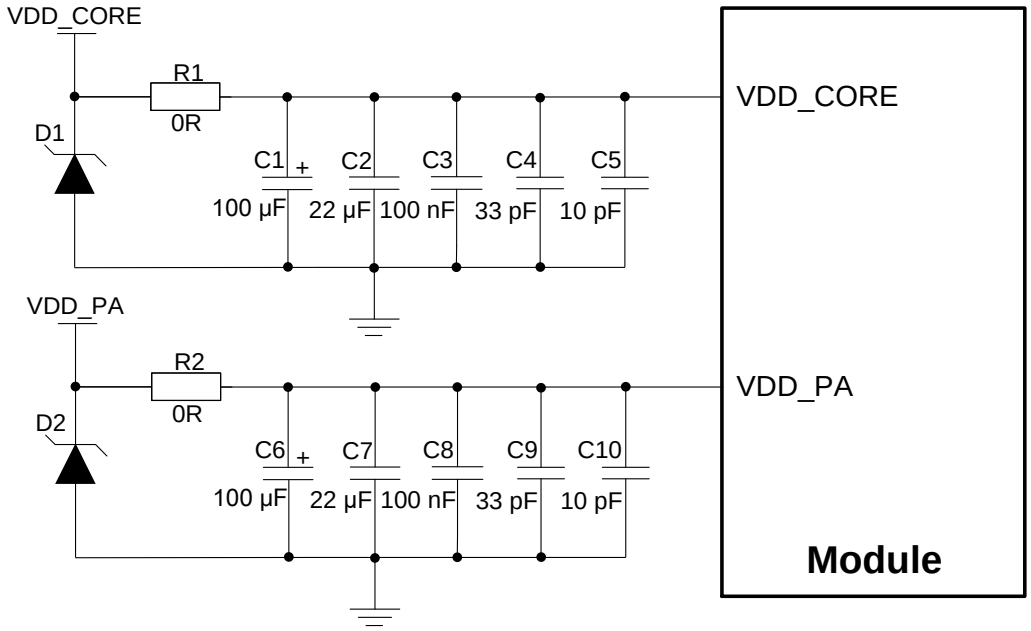



**Figure 3: Reference Design of Power Supply**

### 3.1.3. Power-up/-down Timing

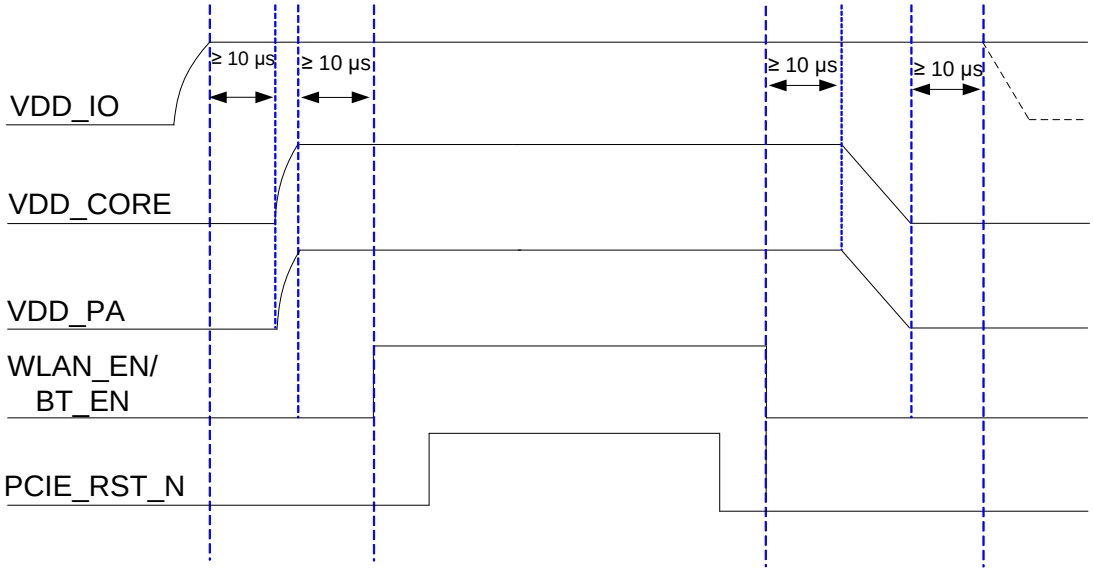



**Figure 4: Power-up and Power-down Timing**

## 3.2. Bootstrap Pins

Bootstrap pins are essential for operational boot-up. If it is designed incorrectly, the module will go into a non-operational mode. Bootstrap pins are sampled within 100 ms after the first enable pin (either WLAN_EN or BT_EN) is pulled high. The bootstrap level will be latched until the module is powered up again.

**Table 7: Bootstrap Pins**

| Pin Name | Pin No. | A 10 kΩ Pull-up Resister Inside the Module | Comment |
|---|---|---|---|
| PCM_DOUT | 3 | √ | Please ensure that the level logic is high during boot-up, so do not add a pull-down resistor or connect it to GND outside the module. |
| PCM_SYNC | 5 | - | Please ensure that the level logic is low during boot-up, so it is recommended to add a 10 kΩ pull-down resistor outside the module. |
| BT_WAKE_HOST | 39 | - | Please ensure that the level logic is low during boot-up, so it is recommended to add a 10 kΩ pull-down resistor outside the module. |
| BT_RTS | 72 | √ | Please ensure that the level logic is high during boot-up, so do not add a pull-down resistor or connect it to GND outside the module. |
| BT_TXD | 74 | √ | Please ensure that the level logic is high during boot-up, so do not add a pull-down resistor or connect it to GND outside the module. |
| COEX_TXD | 76 | √ | Please ensure that the level logic is high during boot-up, so do not add a pull-down resistor or connect it to GND outside the module. |

**NOTE**

Pay attention to the initial state of these pins on the host side.

# 4 Application Interfaces

## 4.1. Wi-Fi Application Interfaces

The following figure shows the Wi-Fi application interface connection between the module and host:

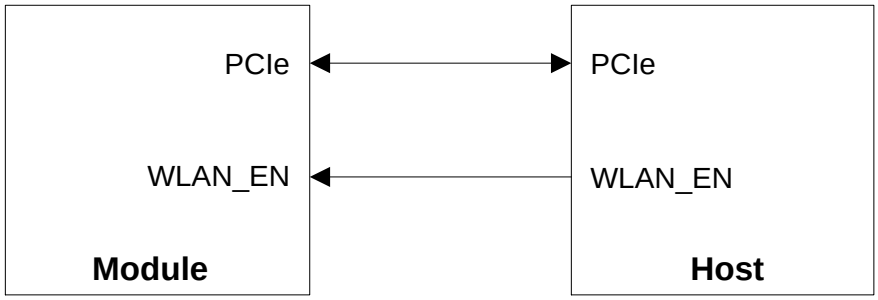



**Figure 5: Block Diagram of Wi-Fi Application Interface Connection**

### 4.1.1. WLAN_EN

WLAN enable function of the module is controlled by WLAN_EN.

**Table 8: Pin Definition of WLAN_EN**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| WLAN_EN | 68 | DI | WLAN function enable control | Active high. |

**NOTE**

WLAN_EN is the sensitive signal. When routing, keep it far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.

### 4.1.2. PCIe Interface

**Table 9: Pin Definition of PCIe Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PCIE_REFCLK_P | 19 | AI | PCIe reference clock (+) | Require differential impedance of 100 Ω. PCIe Gen 2 compliant. |
| PCIE_REFCLK_M | 18 | AI | PCIe reference clock (-) | |
| PCIE_TX_P | 15 | AO | PCIe transmit (+) | |
| PCIE_TX_M | 16 | AO | PCIe transmit (-) | |
| PCIE_RX_P | 12 | AI | PCIe receive (+) | |
| PCIE_RX_M | 13 | AI | PCIe receive (-) | |
| PCIE_CLKREQ_N | 9 | DO | PCIe clock request | VDD_IO power domain. |
| PCIE_RST_N | 7 | DI | PCIe reset | |
| PCIE_WAKE_N | 8 | DO | PCIe wake up | |

The following figure shows the PCIe interface connection between the module and host.

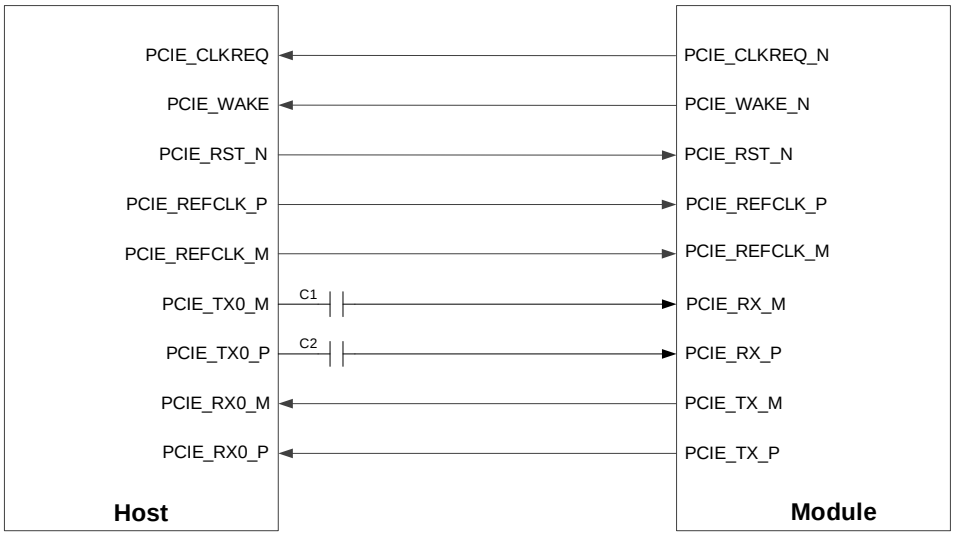



**Figure 6: PCIe Interface Connection**

In order to ensure the signal integrity of PCIe interface, C1 and C2 should be placed close to the host.

The following principles of PCIe interface design should be complied with to meet PCIe Gen 2 specifications.

- It is important to route the PCIe signal traces as differential pairs with total grounding. And the differential impedance is 100 Ω ±10 %.
- For PCIe signal traces, the maximum length of each differential data pair (PCIE_TX/PCIE_RX/PCIE_REFCLK) is recommended to be less than 300 mm, and each differential data pair matching should be less than 0.7 mm (5 ps).
- The spacing between the Tx/Rx signal trace and other signal traces must be greater than 4 times the trace width.
- It is important to route the PCIe differential traces in inner-layer of the PCB and surround the traces on that layer and with ground planes above and below and keep away from the interference sources such as crystals, switching power and RF signal traces.

**NOTE**

1. For PCIE_TX_M and PCIE_TX_P, a 100 nF coupling capacitor has been respectively placed inside the module.
2. For PCIE_CLKREQ_N and PCIE_WAKE_N, a pull-up 10 kΩ resistor has been respectively placed inside the module.

## 4.2. Bluetooth Application Interfaces

The following figure shows the Bluetooth application interface connection between the module and host.

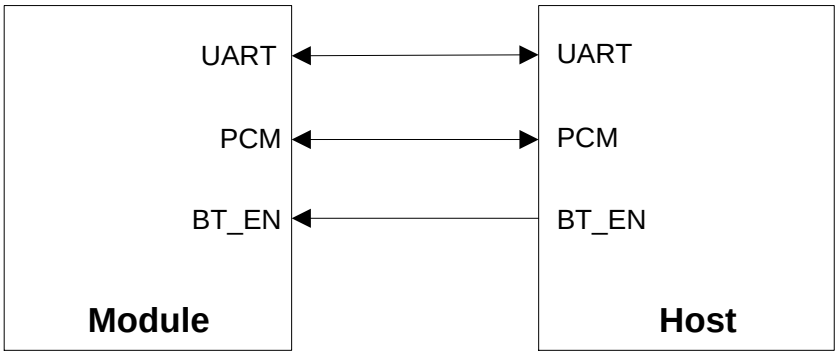



**Figure 7: Block Diagram of Bluetooth Application Interface Connection**

### 4.2.1. BT_EN

Bluetooth function of the module is controlled by BT_EN. When BT_EN is at a high level, Bluetooth function will be enabled.

**Table 10: Pin Definition of BT_EN**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_EN | 69 | DI | Bluetooth enable control | Active high. |

### 4.2.2. PCM Interface

The module provides a PCM interface for audio over Bluetooth.

**Table 11: Pin Definition of PCM Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PCM_SYNC | 5 | DIO | PCM data frame sync | In master mode, it is an output signal.<br>In slave mode, it is an input signal.<br>Please ensure that the level logic is low during boot-up. |
| PCM_CLK | 4 | DIO | PCM clock | In master mode, it is an output signal.<br>In slave mode, it is an input signal. |
| PCM_DIN | 2 | DI | PCM data input | If unused, keep it open. |
| PCM_DOUT | 3 | DO | PCM data output | Please ensure that the level logic is high during boot-up.<br>If unused, keep it open. |

The following figures show reference design for PCM interface connection between the module and host.

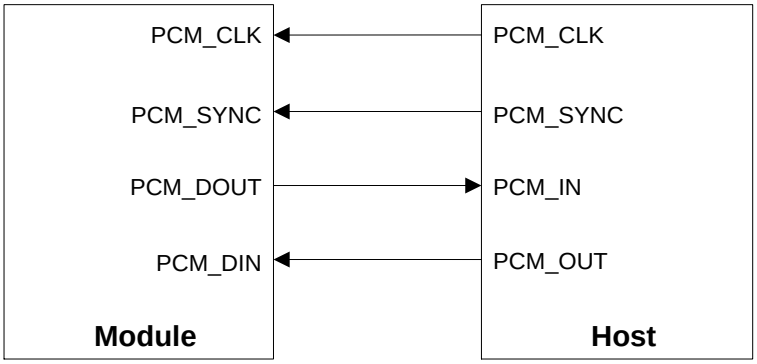



**Figure 8: Block Diagram of PCM Interface (Slave Mode)**

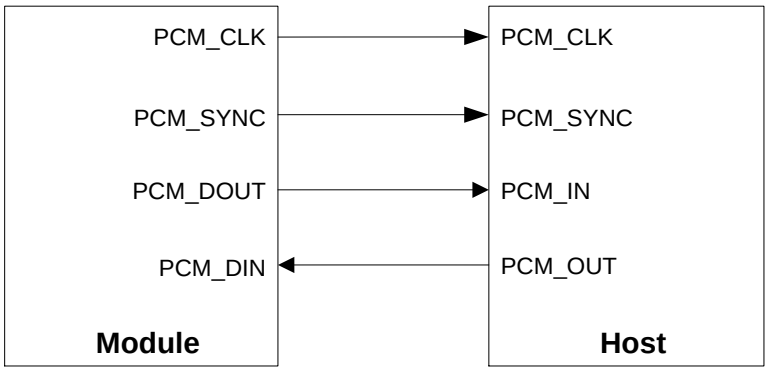



**Figure 9: Block Diagram of PCM Interface (Master Mode)**

When the host PCM voltage level does not match that of the module, it is necessary to add a voltage-level translator. Since PCM_DOUT and PCM_SYNC are bootstrap pins, it is recommended to keep the voltage-level translator disabled during boot-up. The voltage-level translator can be enabled or disabled via OE pin.

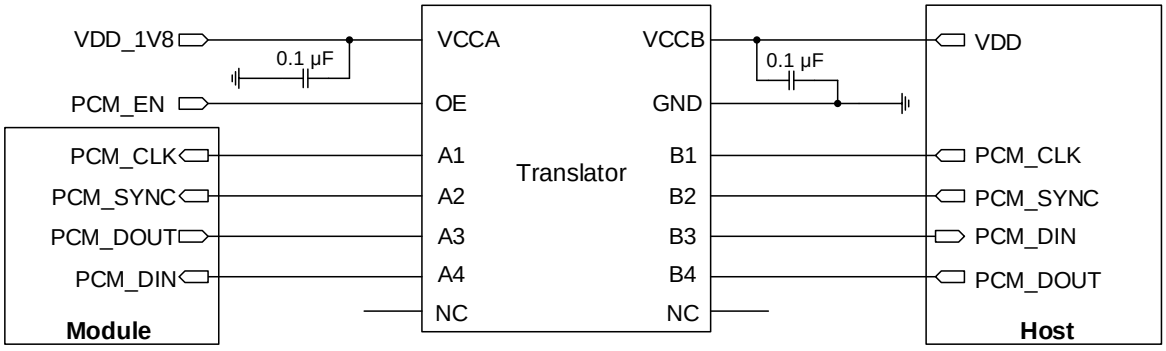



**Figure 10: Voltage-level Translator for PCM Interface**

The PCM interface timing and relevant parameters in both slave and master modes are shown in the following figures and tables:

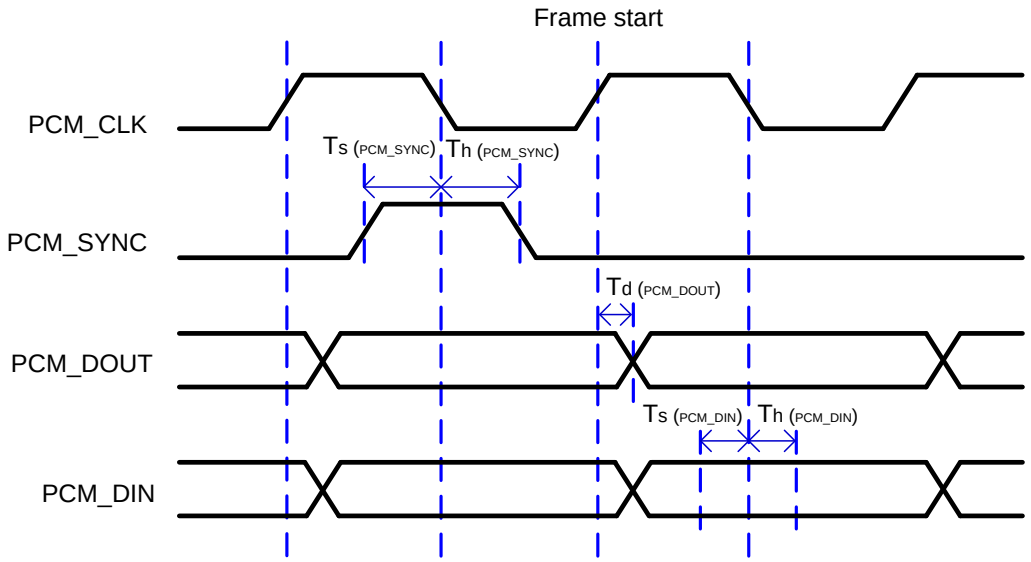



**Figure 11: PCM Timing (Slave Mode)**

**Table 12: PCM Timing Parameter (Slave Mode)**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| - | Frequency of PCM_CLK | 64 | - | 2048 | kHz |
| Ts (PCM_SYNC) | Setup time from PCM_SYNC to PCM_CLK falling edge | 0 | - | - | ns |
| Th (PCM_SYNC) | Holding time from PCM_CLK falling edge to PCM_SYNC falling edge | 150 | - | - | ns |
| Td (PCM_DOUT) | Delay time from PCM_CLK rising edge to PCM_DOUT | 0 | - | 150 | ns |
| Ts (PCM_DIN) | Setup time from PCM_DIN to PCM_CLK falling edge | 0 | - | - | ns |
| Th (PCM_DIN) | Holding time of PCM_DIN after PCM_CLK falls | 150 | - | - | ns |

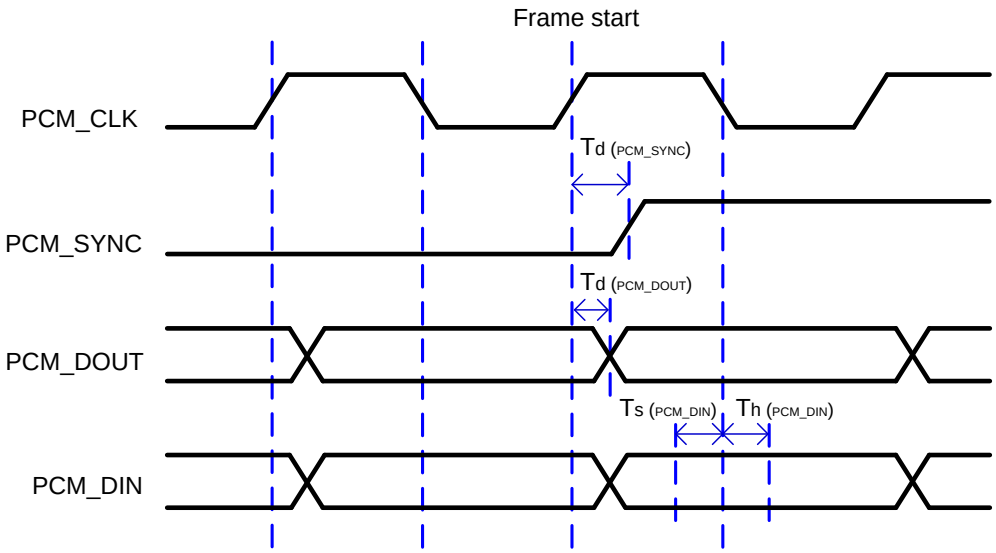



**Figure 12: PCM Timing (Master Mode)**

**Table 13: PCM Timing Parameter (Master Mode)**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| - | Frequency of PCM_CLK | 64 | - | 2048 | kHz |
| Td (PCM_SYNC) | Delay time from PCM_CLK rising edge to PCM_SYNC | -10 | - | 50 | ns |
| Td (PCM_DOUT) | Delay time from PCM_CLK rising edge to PCM_DOUT | -10 | - | 50 | ns |
| Ts (PCM_DIN) | Setup time from PCM_DIN to PCM_CLK falling edge | 50 | - | - | ns |
| Th (PCM_DIN) | Holding time of PCM_DIN after PCM_CLK falls | 150 | - | - | ns |

### 4.2.3. Bluetooth UART

The module supports an HCI UART as defined in *Bluetooth Core Specification Version 5.2*. The UART supports hardware flow control, and it can be used for data transmission with up to 3.2 Mbps baud rates.

**Table 14: Pin Definition of Bluetooth UART**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_TXD | 74 | DO | Bluetooth UART transmit | Please ensure that the level logic is high during |

| | | | | |
|---|---|---|---|---|
| | | | | boot-up. |
| BT_RXD | 75 | DI | Bluetooth UART receive | |
| BT_RTS | 72 | DO | Request to send signal from the module | Please ensure that the level logic is high during boot-up. |
| BT_CTS | 73 | DI | Clear to send signal to the module | |

The following figure shows a reference design for Bluetooth UART connection between the module and host.

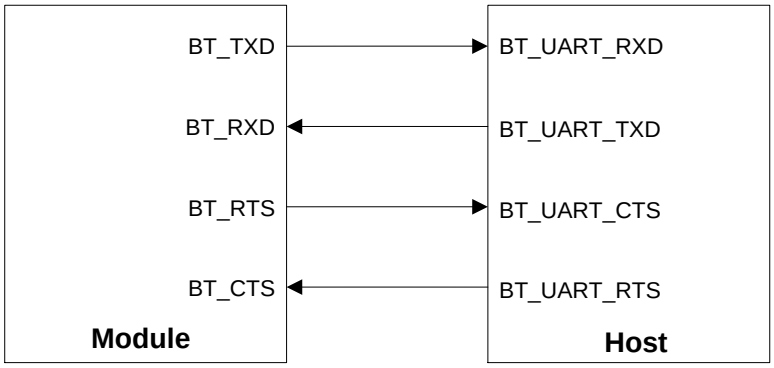



**Figure 13: Block Diagram of Bluetooth UART Connection**

When the host UART voltage level does not match that of the module, it is necessary to add a voltage-level translator.

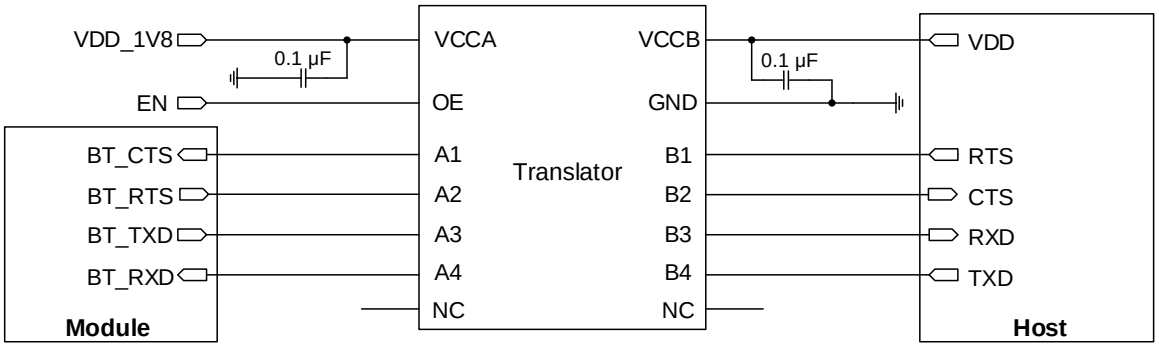



**Figure 14: Voltage-level Translator for UART**

**NOTE**

To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

## 4.3. Coexistence UART Interface

**Table 15: Pin Definition of Coexistence UART Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| COEX_TXD | 76 | DO | WWAN & WLAN/Bluetooth coexistence transmit | Please ensure that the level logic is high during boot-up.<br>If unused, keep it open. |
| COEX_RXD | 1 | DI | WWAN & WLAN/Bluetooth coexistence receive | If unused, keep it open. |

The following figure shows the coexistence UART interface connection between the module and host.

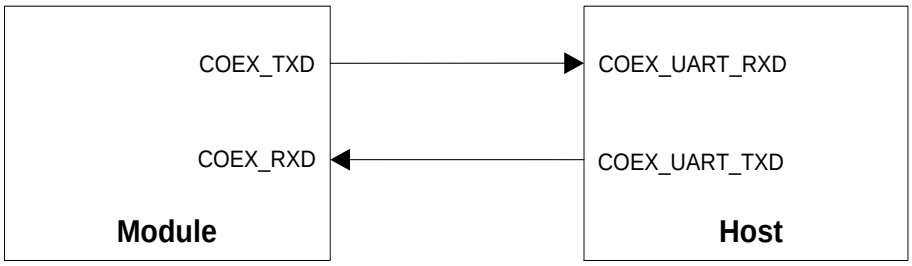



**Figure 15: Block Diagram of Coexistence UART Interface Connection**

## 4.4. Other Interfaces

### 4.4.1. BT_WAKE_HOST*

BT_WAKE_HOST is used to wake up the host and it is active high.

**Table 16: Pin Definition of BT_WAKE_HOST**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| BT_WAKE_HOST | 39 | DO | Bluetooth wake up host | 1.8 V power domain.<br>Please ensure that the level logic is low during boot-up. |

### 4.4.2. WLAN_SLP_CLK*

The 32.768 kHz sleep clock is used in low power consumption modes, such as power saving mode and sleep mode. It can ensure basic logic operations when the module is in sleep mode.

**Table 17: Pin Definition of WLAN_SLP_CLK**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| WLAN_SLP_CLK | 22 | DI | WLAN sleep clock | Internal sleep clock is used by default. Keep it open. |

# 5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

## 5.1. RF Antenna Interfaces

### 5.1.1. Antenna Interfaces & Frequency Bands

**Table 18: Pin Definition of RF Antenna Interfaces**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| ANT_WIFI0 | 45 | AIO | Bluetooth & 2.4 GHz/5 GHz Wi-Fi 0 antenna interface | 50 Ω characteristic impedance. |
| ANT_WIFI1 | 54 | AIO | 2.4 GHz/5 GHz Wi-Fi 1 antenna interface | |
| ANT_BT* | 37 | AIO | Reserved dedicated Bluetooth antenna interface | |

**Table 19: Operating Frequency (Unit: GHz)**

| Parameter | Frequency |
|---|---|
| 2.4 GHz Wi-Fi | 2.400–2.4835 |
| 5 GHz Wi-Fi | 5.150–5.850 |
| Bluetooth | 2.402–2.480 |

### 5.1.2. Reference Design

The module provides three RF antenna pins for Wi-Fi & Bluetooth antenna connection. The RF trace in host PCB connected to the module's RF antenna pins should be microstrip line or other types, with the characteristic impedance close to 50 Ω.

It is recommended to reserve a π-type matching circuit and add an ESD protection component for better RF performance. For ANT_WIFI0, place the matching components C1, R1 and C2 to the antenna as close as possible. Capacitors C1 and C2 are not mounted by default. R1 is mounted with a 0 Ω resistor. C3 is a 33 pF capacitor and D1 is a TVS by default. The reference design of ANT_WIFI1 and ANT_BT is the same.

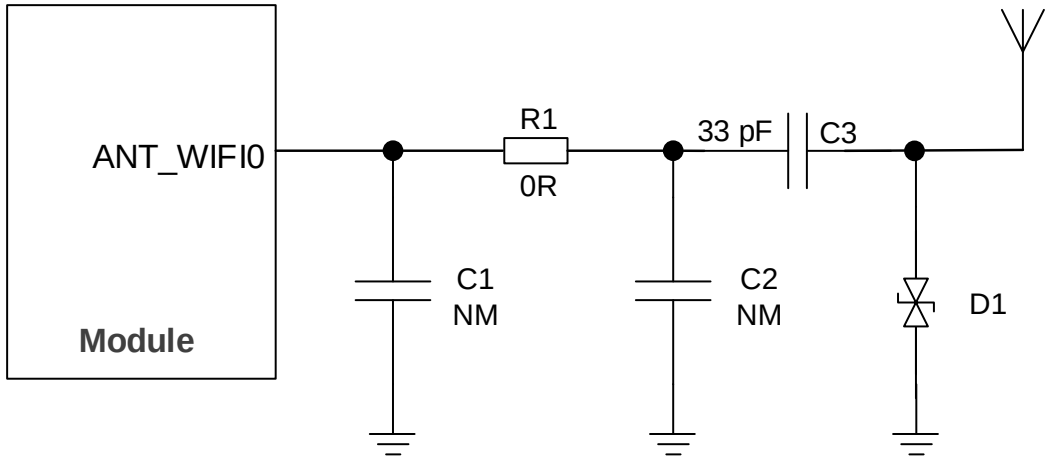



**Figure 16: Reference Design of RF Antenna Interfaces**

Another type of reference circuit for the RF antenna interfaces is shown below. It is designed for vehicle applications. It is recommended to reserve two notch filter circuits and a π-type matching circuit for better RF performance. For ANT_WIFI0, L1, C3, C4 and L3 comprise two notch filter circuits for filtering out interference caused by a particular frequency. When L1, C3, C4 and L3 are not mounted, C1, R1 and C2 comprise a π-type matching circuit. Capacitors (C1, C2, C3 and C4) and inductors (L1 and L3) are not mounted by default, and R1 is only mounted with a 0 Ω resistor by default. The reference design of ANT_WIFI1 and ANT_BT is the same.

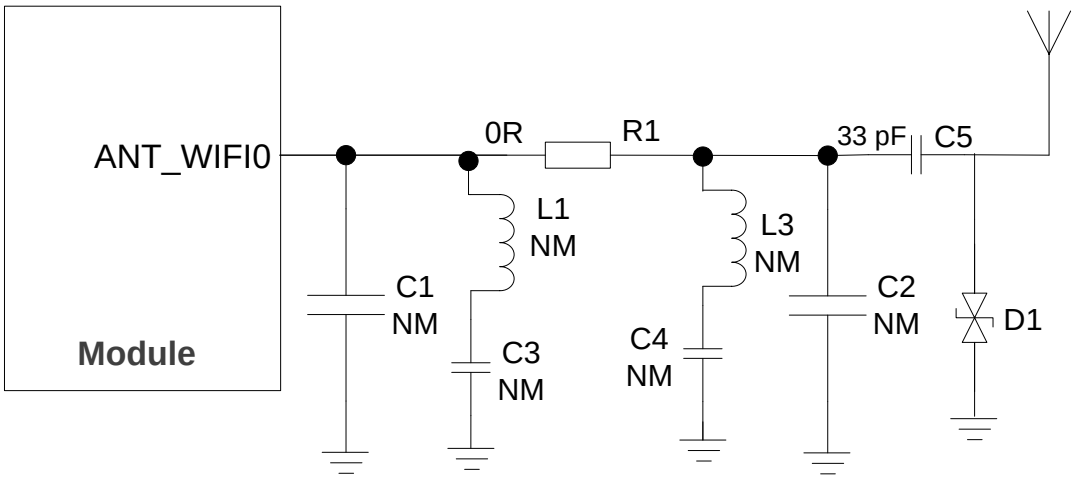



**Figure 17: Reference Design of RF Antenna Interfaces (Vehicle Applications)**

## 5.2. RF Performance

### 5.2.1. Wi-Fi Performance

#### 5.2.1.1. Transmit Power

**Table 20: Conducted RF Transmit Power at 2.4 GHz (Unit: dBm)**

| Standard | Data Rate | Typ. |
|---|---|---|
| 802.11b | 1 Mbps | 17.5 |
| 802.11b | 11 Mbps | 17.5 |
| 802.11g | 6 Mbps | 17 |
| 802.11g | 54 Mbps | 15 |
| 802.11n (HT20) | MCS 0 | 17 |
| 802.11n (HT20) | MCS 7 | 13.5 |
| 802.11n (HT40) | MCS 0 | 16.5 |
| 802.11n (HT40) | MCS 7 | 12 |

**Table 21: Conducted RF Transmit Power at 5 GHz (Unit: dBm)**

| Standard | Data Rate | Typ. |
|---|---|---|
| 802.11a | 6 Mbps | 15.5 |
| 802.11a | 54 Mbps | 13 |
| 802.11n (HT20) | MCS 0 | 15.5 |
| 802.11n (HT20) | MCS 7 | 12.5 |
| 802.11n (HT40) | MCS 0 | 15 |
| 802.11n (HT40) | MCS 7 | 12 |
| 802.11ac (VHT20) | MCS 0 | 15.5 |
| 802.11ac (VHT20) | MCS 8 | 11.5 |
| 802.11ac (VHT40) | MCS 0 | 15 |
| 802.11ac (VHT40) | MCS 9 | 10 |
| 802.11ac (VHT80) | MCS 0 | 14.5 |
| 802.11ac (VHT80) | MCS 9 | 9.5 |

#### 5.2.1.2. Receiver Sensitivity

**Table 22: Conducted RF Receiver Sensitivity at 2.4 GHz (Unit: dBm)**

| Standard | Data Rate | Max. | Typ. |
|---|---|---|---|
| 802.11b | 1 Mbps | -82 | -95 |
| 802.11b | 11 Mbps | -76 | -86.5 |
| 802.11g | 6 Mbps | -82 | -89 |
| 802.11g | 54 Mbps | -65 | -72.5 |
| 802.11n (HT20) | MCS 0 | -82 | -90 |
| 802.11n (HT20) | MCS 7 | -64 | -70 |
| 802.11n (HT40) | MCS 0 | -79 | -87 |

| | | | |
|---|---|---|---|
| 802.11n (HT40) | MCS 7 | -61 | -67.5 |

**Table 23: Conducted RF Receiver Sensitivity at 5 GHz (Unit: dBm)**

| Standard | Data Rate | Max. | Typ. |
|---|---|---|---|
| 802.11a | 6 Mbps | -82 | -90 |
| 802.11a | 54 Mbps | -65 | -71.5 |
| 802.11n (HT20) | MCS 0 | -82 | -89 |
| 802.11n (HT20) | MCS 7 | -64 | -70.5 |
| 802.11n (HT40) | MCS 0 | -79 | -86 |
| 802.11n (HT40) | MCS 7 | -61 | -67.5 |
| 802.11ac (VHT20) | MCS 0 | -82 | -89 |
| 802.11ac (VHT20) | MCS 8 | -59 | -65.5 |
| 802.11ac (VHT40) | MCS 0 | -79 | -86 |
| 802.11ac (VHT40) | MCS 9 | -54 | -63 |
| 802.11ac (VHT80) | MCS 0 | -76 | -82 |
| 802.11ac (VHT80) | MCS 9 | -51 | -57 |

### 5.2.2. Bluetooth Performance

**Table 24: Bluetooth Transmitting and Receiver Performance**

| Mode | Transmit Power | Receiver Sensitivity |
|---|---|---|
| BR | 7 dBm ±2.5 dB | -91 dBm |
| EDR | 2.5 dBm ±2.5 dB | -85 dBm |
| BLE | 7 dBm ±2.5 dB | -94 dBm |

**NOTE**

The data above are tested under Bluetooth power class 1.5.

## 5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

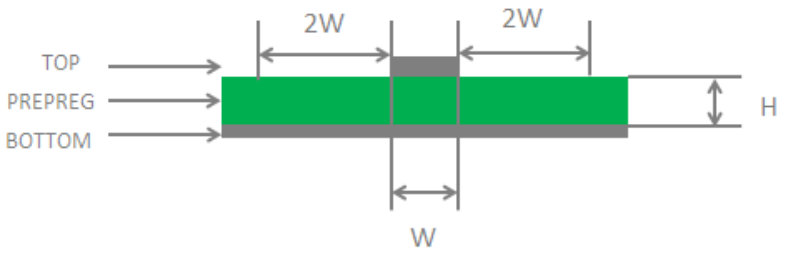



**Figure 18: Microstrip Design on a 2-layer PCB**

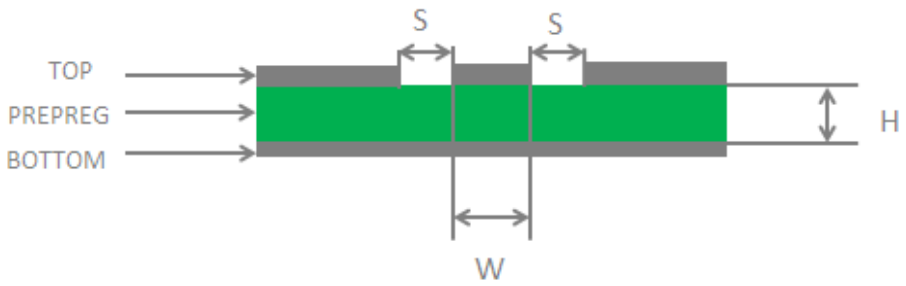



**Figure 19: Coplanar Waveguide Design on a 2-layer PCB**

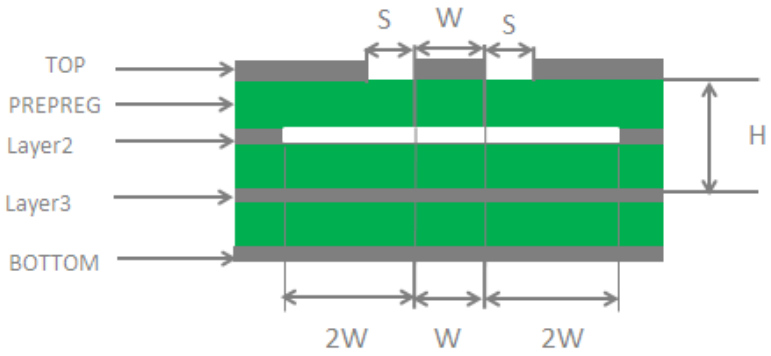



**Figure 20: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**

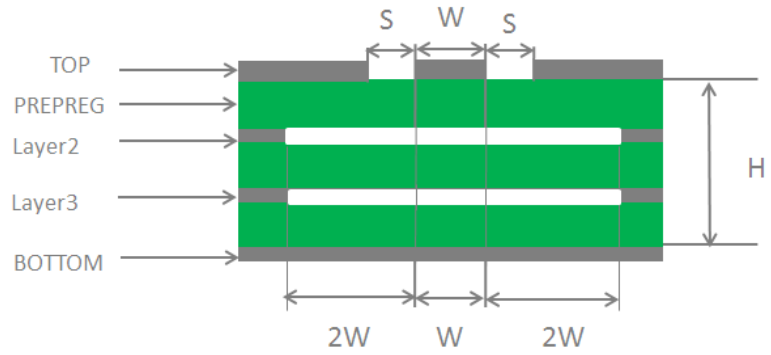



**Figure 21: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

## 5.4. Antenna Design Requirements

**Table 25: Antenna Design Requirements**

| Parameter | Requirement |
|---|---|
| Frequency Range (GHz) | ● 2.4 GHz Wi-Fi: 2.400–2.4835<br>● 5 GHz Wi-Fi: 5.150–5.850<br>● Bluetooth: 2.402–2.480 |
| Cable Insertion Loss (dB) | < 1 |
| VSWR | ≤ 2 (Typ.) |
| Gain (dBi) | 1 (Typ.) |
| Max. Input Power (W) | 50 |
| Input Impedance (Ω) | 50 |
| Polarization Type | Vertical |

## 5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

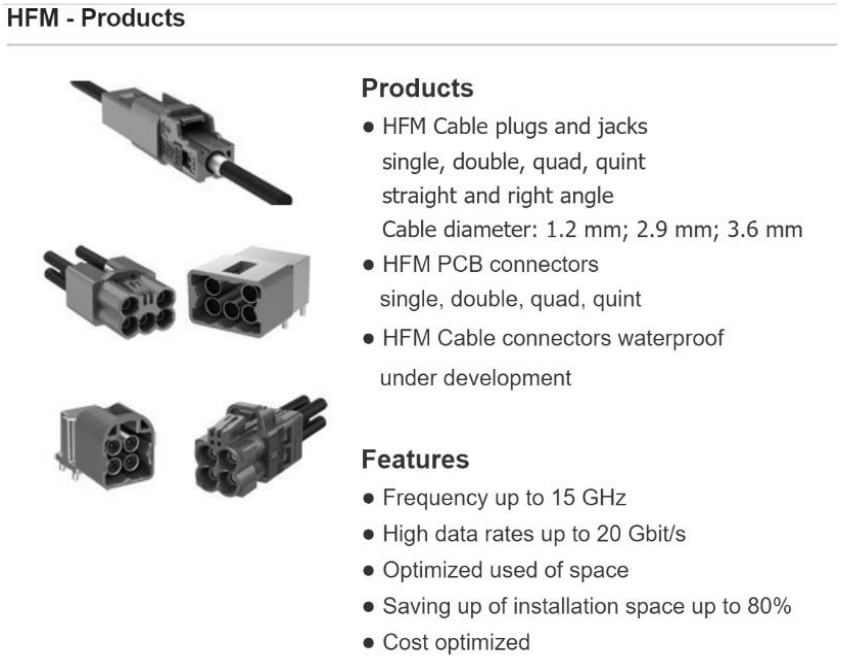



**Figure 22: Feature of the HFM Connector**

For more details, visit http://www.hirose.com.

# 6 Electrical Characteristics and Reliability

## 6.1. Electrical Characteristics

**Table 26: Absolute Maximum Ratings (Unit: V)**

| Parameter | Min. | Max. |
|---|---|---|
| VDD_CORE | -0.5 | 1.98 |
| VDD_PA | -0.5 | 2.42 |
| VDD_IO | -0.5 | 3.6 |
| Voltage at Digital Pins | -0.3 | 2.0 |

**Table 27: Recommended Operating Conditions (Unit: V)**

| Parameter | Min. | Typ. | Max. |
|---|---|---|---|
| VDD_CORE | 1.71 | 1.8 | 1.89 |
| VDD_PA | 2.09 | 2.2 | 2.31 |
| VDD_IO | 1.62 | 1.8 | 1.98 |

## 6.2. Power Consumption

**Table 28: Wi-Fi Power Consumption of the Module (Normal Operation Mode; Unit: mA)**

| Standard | Condition | $I_{VDD\_CORE}$ | $I_{VDD\_IO}$ | $I_{VDD\_PA}$ |
|---|---|---|---|---|
| 802.11b | Tx 1 Mbps @ 17.5 dBm | 280 | 5.6 | 455 |
| | Tx 11 Mbps @ 17.5 dBm | 290 | 5.6 | 460 |
| 802.11g | Tx 6 Mbps @ 17 dBm | 303 | 5.7 | 455 |
| | Tx 54 Mbps @ 15 dBm | 327 | 5.8 | 420 |
| 802.11n (2.4 GHz) | Tx HT20 MCS 0 @ 17 dBm | 305 | 5.8 | 440 |
| | Tx HT20 MCS 7 @ 13.5 dBm | 320 | 5.8 | 390 |
| | Tx HT40 MCS 0 @ 16.5 dBm | 317 | 5.8 | 450 |
| | Tx HT40 MCS 7 @ 12 dBm | 317 | 5.6 | 375 |
| 802.11a | Tx 6 Mbps @ 15.5 dBm | 325 | 5.9 | 515 |
| | Tx 54 Mbps @ 13 dBm | 338 | 5.9 | 456 |
| 802.11n (5 GHz) | Tx HT20 MCS 0 @ 15.5 dBm | 327 | 5.9 | 516 |
| | Tx HT20 MCS 7 @ 12.5 dBm | 343 | 6.0 | 458 |
| | Tx HT40 MCS 0 @ 15 dBm | 358 | 6.0 | 498 |
| | Tx HT40 MCS 7 @ 12 dBm | 348 | 5.8 | 433 |
| 802.11ac | Tx VHT20 MCS 0 @ 15.5 dBm | 326 | 5.9 | 498 |
| | Tx VHT20 MCS 8 @ 11.5 dBm | 345 | 5.9 | 438 |
| | Tx VHT40 MCS 0 @ 15 dBm | 357 | 6.0 | 497 |
| | Tx VHT40 MCS 9 @ 10 dBm | 348 | 5.9 | 408 |
| | Tx VHT80 MCS 0 @ 14.5 dBm | 410 | 6.1 | 462 |
| | Tx VHT80 MCS 9 @ 9.5 dBm | 348 | 5.8 | 400 |

## 6.3. Digital I/O Characteristics

**Table 29: VDD_IO I/O Requirements**

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 1.17 | 1.98 | V |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.63 | V |
| $V_{OH}$ | High-level output voltage | 1.40 | 1.98 | V |
| $V_{OL}$ | Low-level output voltage | -0.3 | 0.3 | V |

## 6.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

**Table 30: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 % ±5 %; Unit: kV)**

| Tested Interfaces | Contact Discharge | Air Discharge |
|---|---|---|
| VDD, GND | ±8 | ±12 |
| Antenna interfaces | ±6 | ±10 |
| Other Interfaces | ±6 | ±10 |

## 6.5. Operating and Storage Temperatures

**Table 31: Operating and Storage Temperatures (Unit: °C)**

| Parameter | Min. | Typ. | Max. |
|---|---|---|---|
| Normal Operating Temperature [2] | -40 | +25 | +85 |
| Storage Temperature | -40 | - | +90 |

## 6.6. Thermal Dissipation

The module exhibits the best performance when all internal chips are working within their designated operating temperature ranges. However, if any chip reaches or exceeds its maximum temperature, the module may still work but its performance and functionalities (such as RF output power and data rate) will be compromised. Therefore, the thermal design should be maximally optimized to ensure that all internal chips consistently remain within their recommended operating temperature ranges.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on the PCB motherboard, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper on the backside of the PCB where the module is mounted.
- Follow the principles below when designing the heatsink:
  - It is recommended to integrate the heatsink with the outer shell of telematic control unit (TCU) according to the module's application scenario. This allows for rapid transfer of the heat generated by the module to the outer shell, thus enhancing heat dissipation efficiency and eliminating the need for fixing the heatsink.
  - The entire shell of the TCU or the shell of the area where the module is located must be made of materials with excellent heat dissipation properties. It is recommended to use die-cast aluminum with higher thermal conductivity.
  - uminum with higher thermal conductivity.
  - Based on the heat dissipation direction of the module, you can choose either of the following optional heatsink installation positions:
    a) The top surface of the module shielding cover;
    b) The bottom surface of the PCBA under the module;
    c) Both the top surface of the module shielding cover and the bottom surface of the PCBA

[2] Within this operating temperature range, the module's related performance meets IEEE and Bluetooth specifications.

under the module.

If the heatsink is located only on one side, option a) is recommended; if the situation allows, option c) is recommended.

- The heatsink must meet the following requirements:
  a) The base plate area of the heatsink should be larger than the module area for full coverage;
  b) Choose a heatsink with adequate fins to ensure effective heat dissipation. The fins should be located within the area where the module is mounted.
- Since the heatsink is in contact with either the top surface of the shielding cover or the bottom surface of the PCBA through the thermal interface material (TIM), it is necessary to choose a TIM with high thermal conductivity, good flexibility, and good wettability.
- Fasten the shell (heatsink) with screws around the TCU to prevent the heatsink from falling off during the drop tests, shock and vibration tests, or transportation.

- Implement other auxiliary cooling methods, such as air cooling or liquid cooling.

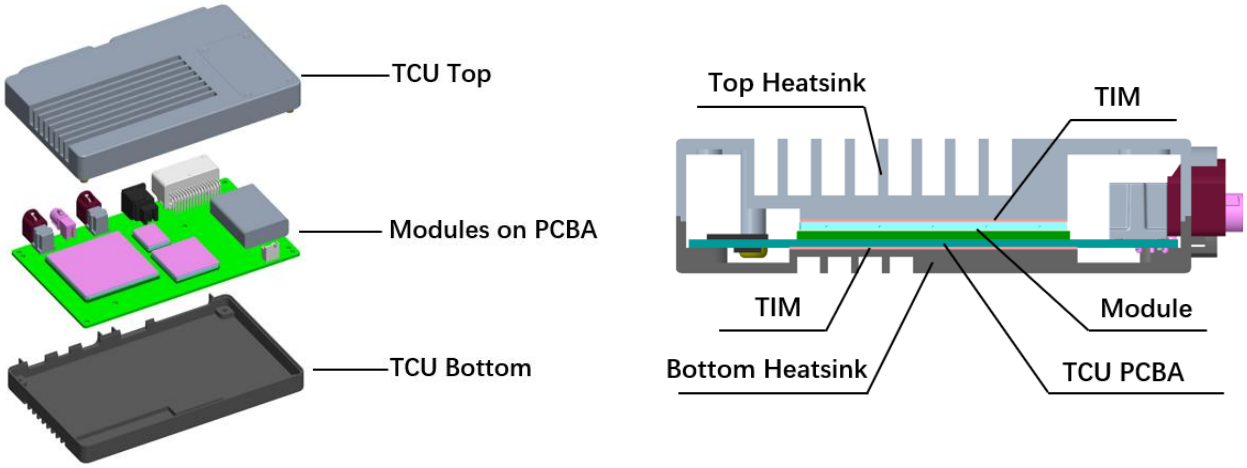



**Figure 23: Heatsink Design Example**

# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

## 7.1. Mechanical Dimensions

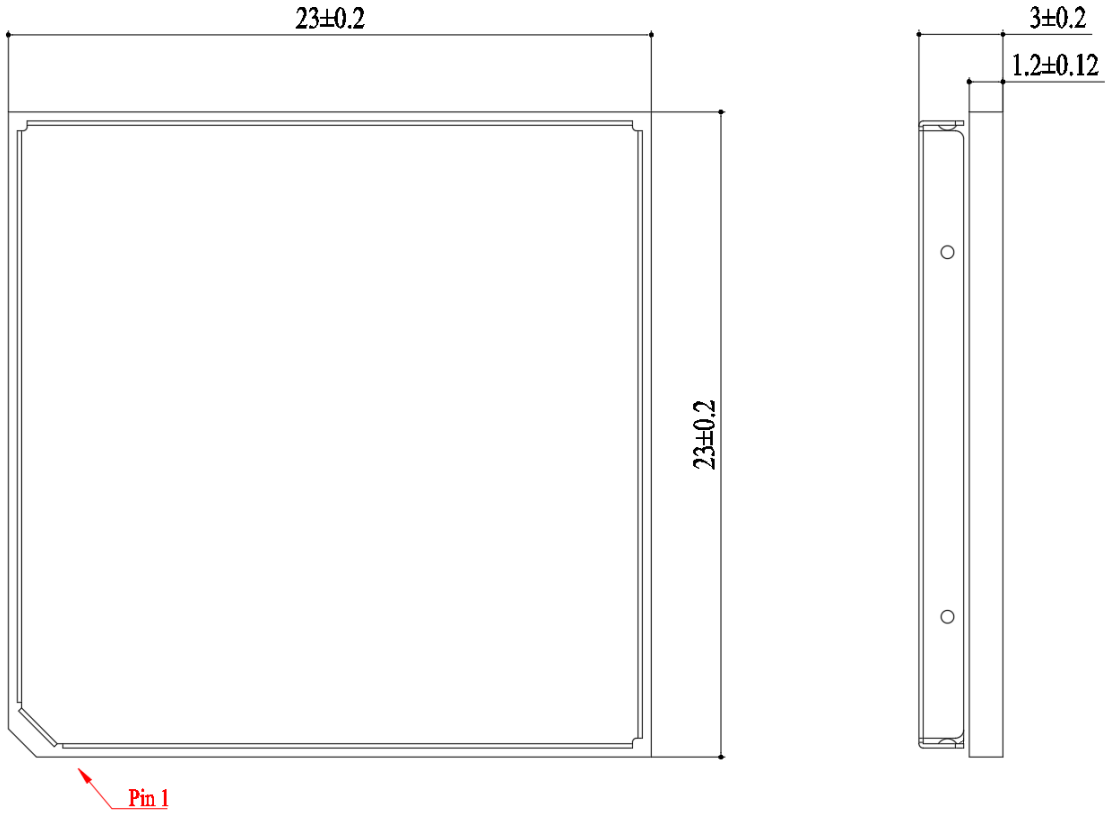



**Figure 24: Top and Side Dimensions**

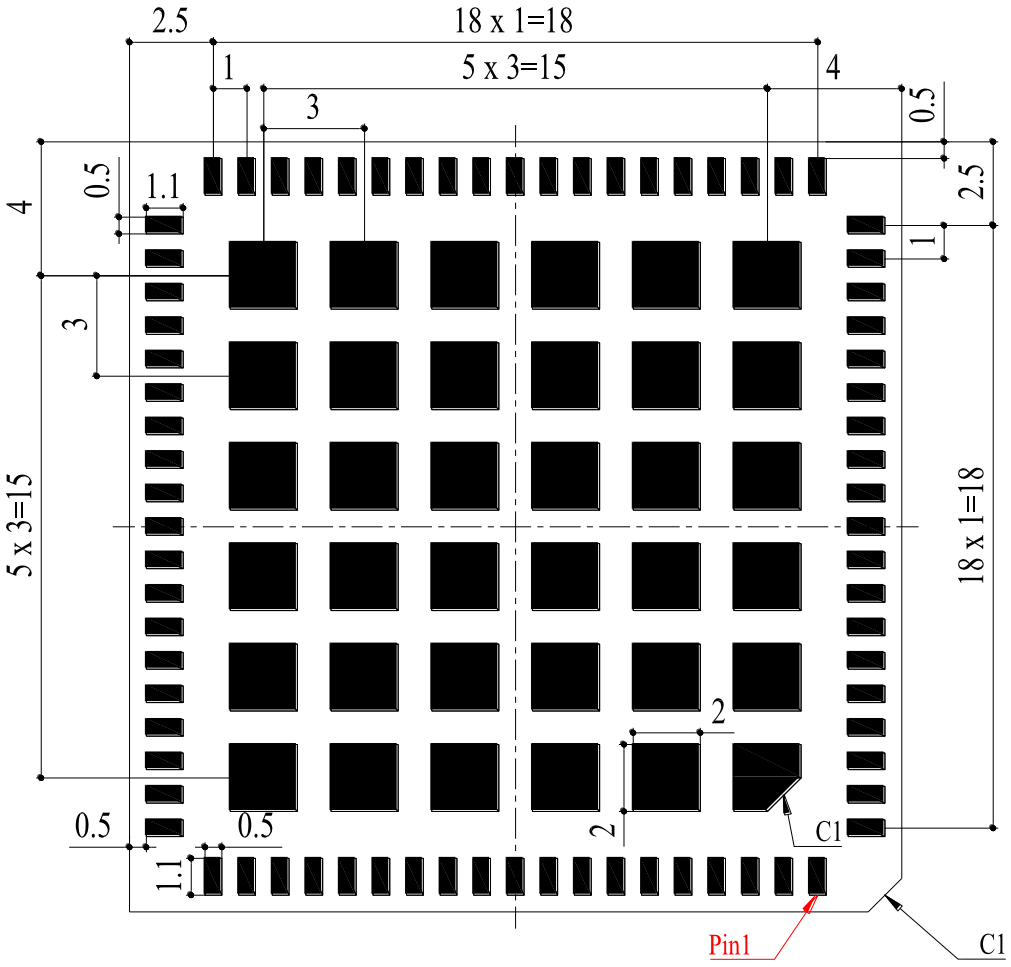



**Figure 25: Bottom Dimensions (Bottom View)**

**NOTE**

The package warpage level of the module refers to the *JEITA ED-7306* standard.

## 7.2. Recommended Footprint

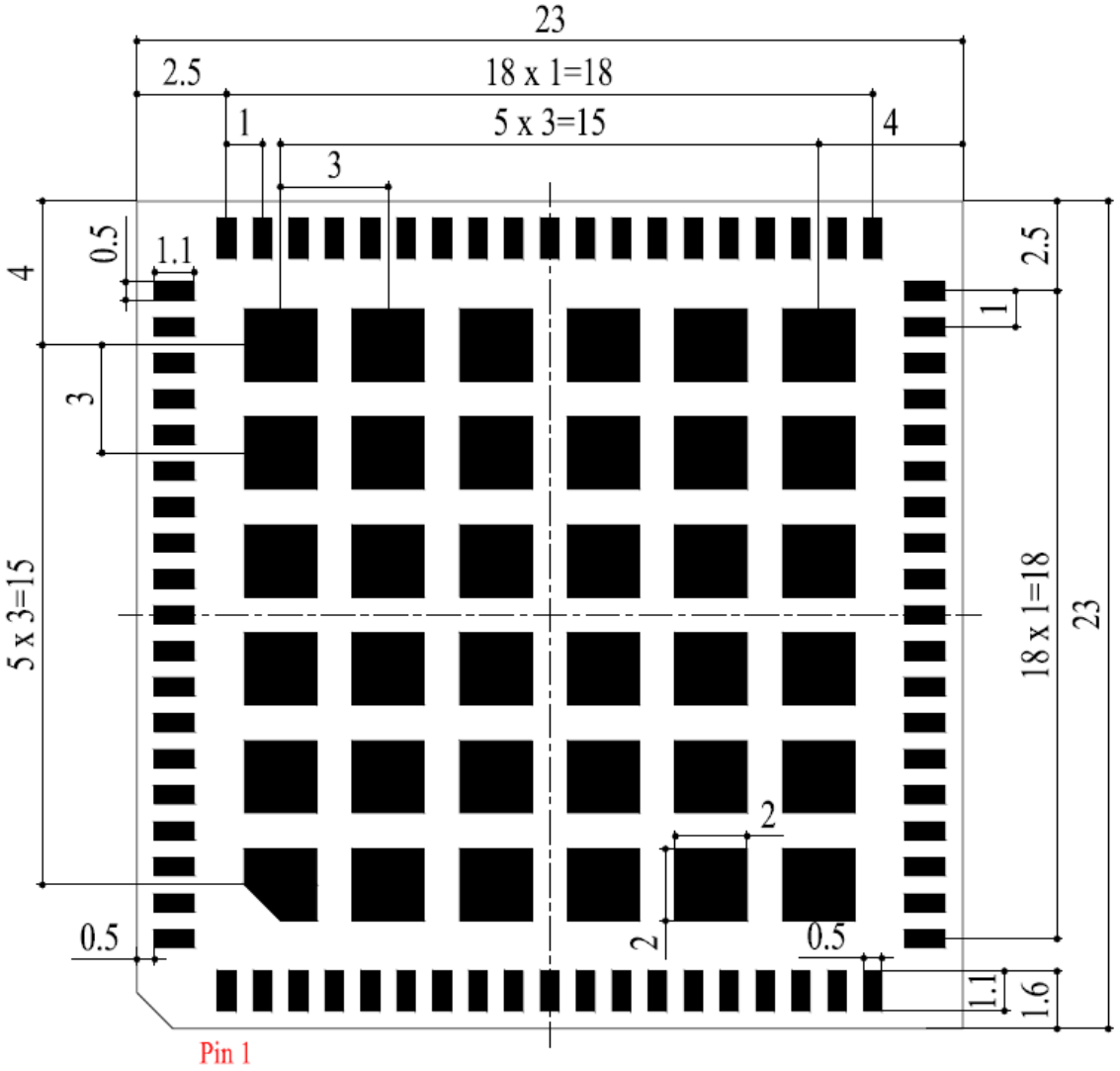



**Figure 26: Recommended Footprint**

**NOTE**

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

## 7.3. Top and Bottom Views

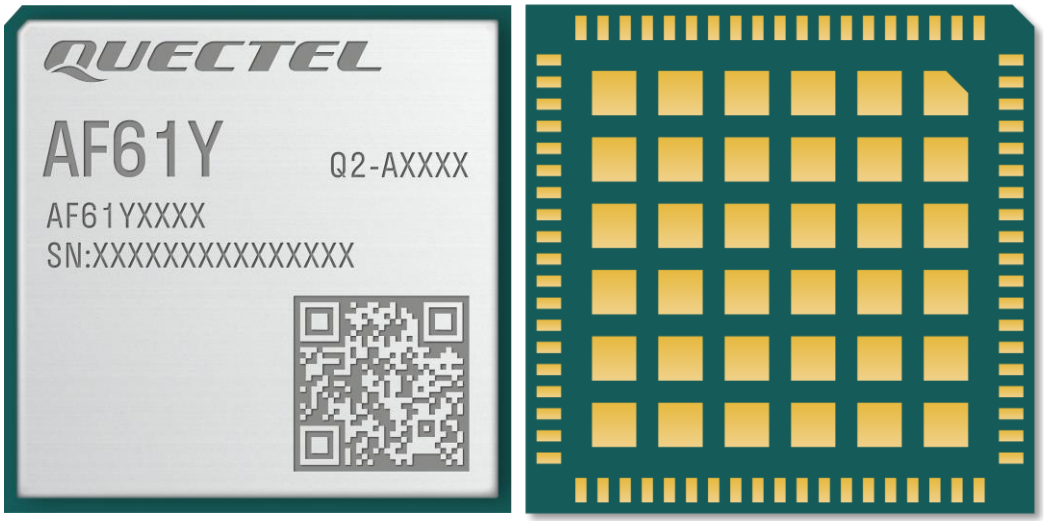



**Figure 27: Top and Bottom Views of the Module**

**NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

# 8 Storage, Manufacturing & Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [3] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[3] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

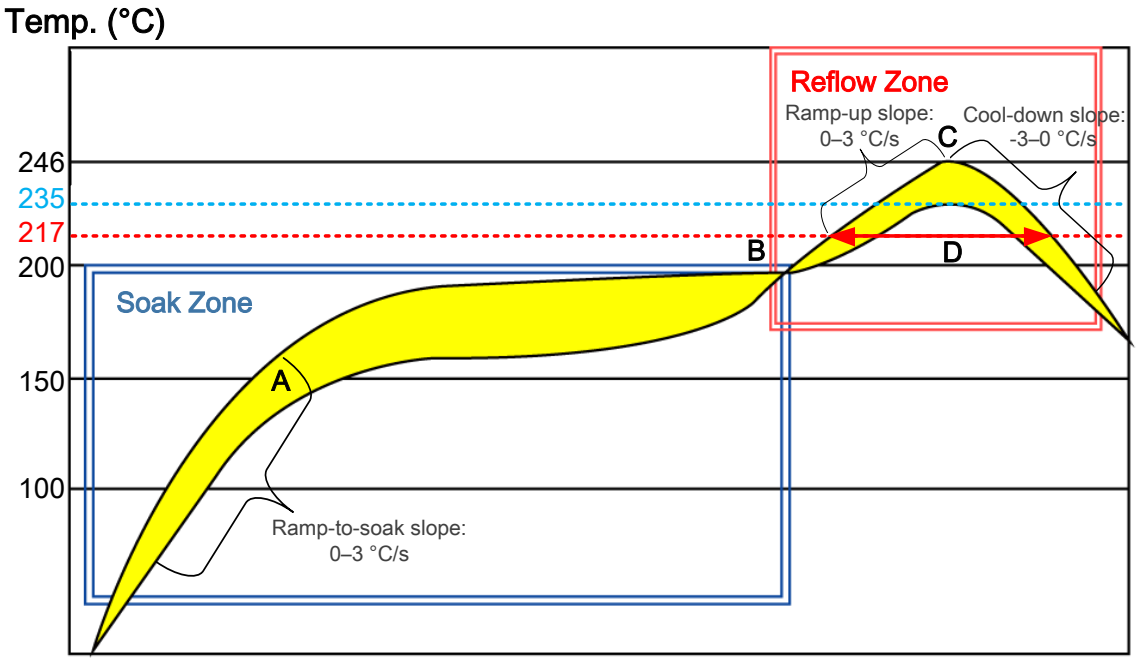



**Figure 28: Recommended Reflow Soldering Thermal Profile**

**Table 32: Recommended Thermal Profile Parameters**

| Factor | Recommended Value |
|---|---|
| **Soak Zone** | |
| Ramp-to-soak slope | 0–3 °C/s |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s |
| **Reflow Zone** | |
| Ramp-up slope | 0–3 °C/s |
| Reflow time (D: over 217 °C) | 40–70 s |
| Max. temperature | 235–246 °C |
| Cool-down slope | -3–0 °C/s |
| **Reflow Cycle** | |
| Max. reflow cycle | 1 |

**NOTE**

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [3]***.

## 8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

### 8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

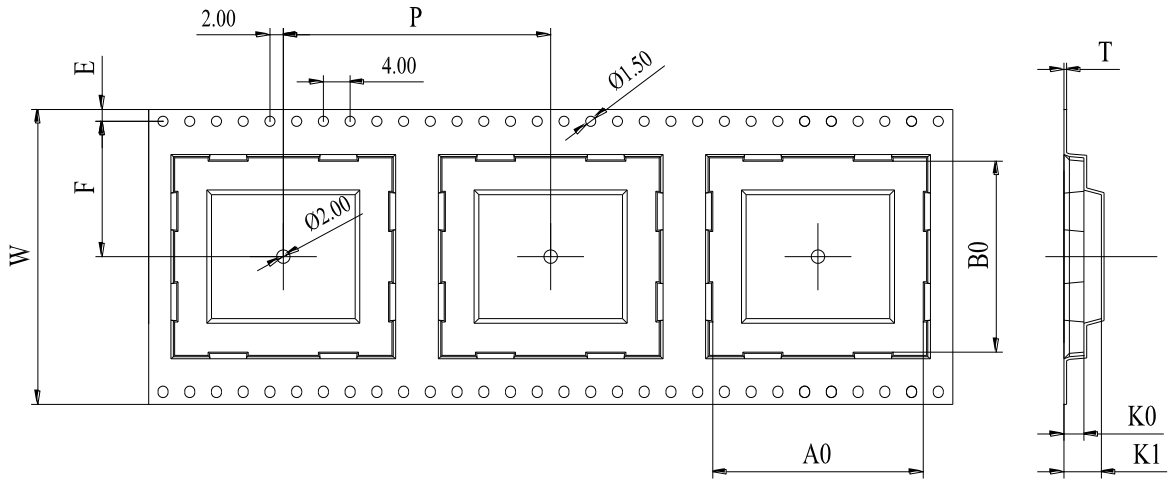



**Figure 29: Carrier Tape Dimension Drawing (Unit: mm)**

**Table 33: Carrier Tape Dimension Table (Unit: mm)**

| W | P | T | A0 | B0 | K0 | K1 | F | E |
|---|---|---|---|---|---|---|---|---|
| 44 | 32 | 0.4 | 23.5 | 23.5 | 3.5 | 6.8 | 20.2 | 1.75 |

### 8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

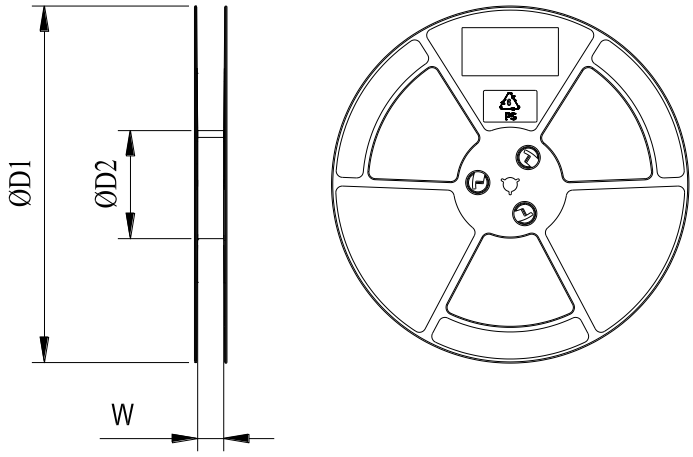



**Figure 30: Plastic Reel Dimension Drawing**

**Table 34: Plastic Reel Dimension Table (Unit: mm)**

| øD1 | øD2 | W |
|---|---|---|
| 330 | 100 | 44.5 |

### 8.3.3. Mounting Direction

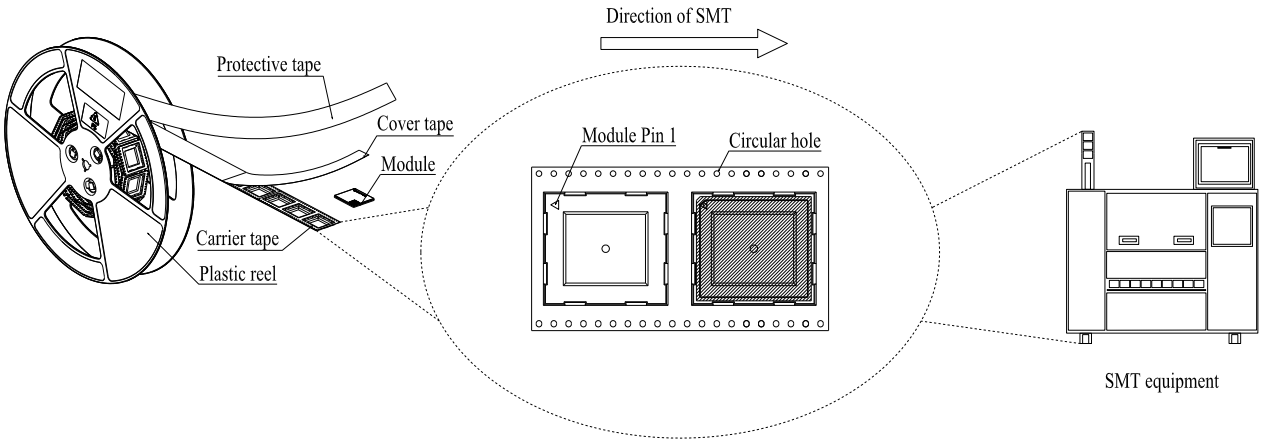
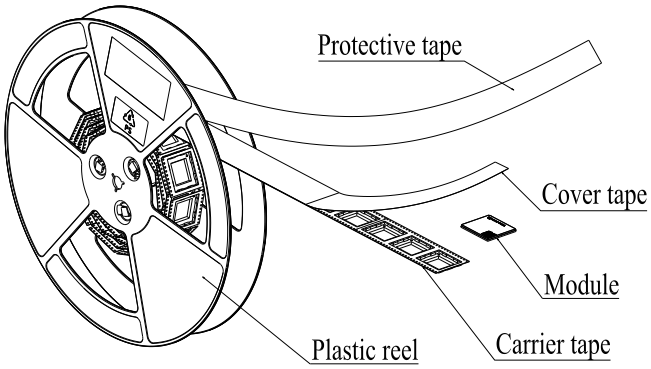


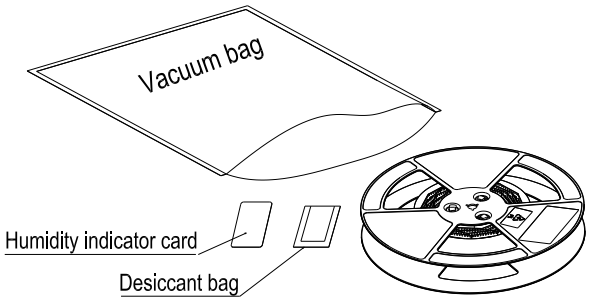

**Figure 31: Mounting Direction**

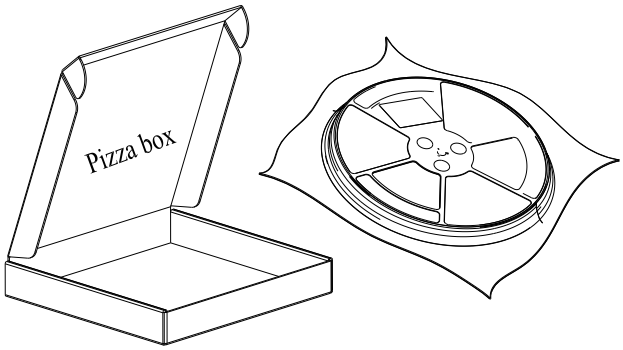
### 8.3.4. Packaging Process




Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.




Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

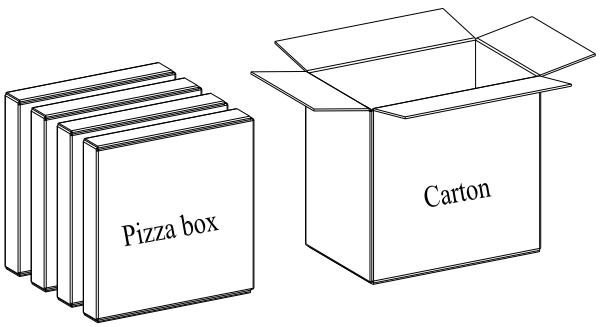



**Figure 32: Packaging Process**

# 9 Appendix References

**Table 35: Related Documents**

| Document Name |
|---|
| [1] Quectel_V2X&5G_EVB_User_Guide |
| [2] Quectel_RF_Layout_Application_Note |
| [3] Quectel_Module_SMT_User_Guide |

**Table 36: Terms and Abbreviations**

| Abbreviation | Description |
|---|---|
| AP | Access Point |
| BLE | Bluetooth Low Energy |
| BPSK | Binary Phase Shift Keying |
| BR | Basic Rate |
| CCK | Complementary Code Keying |
| CTS | Clear To Send |
| DPSK | Differential Phase Shift Keying |
| DQPSK | Differential Quadrature Reference Phase Shift Keying |
| EDR | Enhanced Data Rate |
| ESD | Electrostatic Discharge |
| EVB | Evaluation Board |
| GFSK | Gaussian Frequency Shift Keying |

| | |
|---|---|
| GND | Ground |
| HT | High Throughput |
| IEEE | Institute of Electrical and Electronics Engineers |
| I/O | Input/Output |
| LGA | Land Grid Array |
| Mbps | Megabits per second |
| MCS | Modulation and Coding Scheme |
| MSL | Moisture Sensitivity Levels |
| PA | Power Amplifier |
| PCB | Printed Circuit Board |
| PCBA | Printed Circuit Board Assembly |
| PCIe | Peripheral Component Interconnect Express |
| PCM | Pulse Code Modulation |
| QAM | Quadrature Amplitude Modulation |
| QPSK | Quadrature Phase Shift Keying |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| RTS | Request To Send |
| Rx | Receive |
| RXD | Receive Data (Pin) |
| SDIO | Secure Digital Input/Output |
| SMD | Surface Mount Device |
| SMT | Surface Mount Technology |
| STA | Station |
| TCU | Telematic Control Unit |

| | |
|---|---|
| TIM | Thermal Interface Material |
| Tx | Transmit |
| TXD | Transmit Data (Pin) |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| (U)SIM | (Universal) Subscriber Identity Module |
| VHT | Very High Throughput |
| Vmax | Maximum Voltage |
| Vnom | Nominal Voltage |
| Vmin | Minimum Voltage |
| VSWR | Voltage Standing Wave Ratio |
| WLAN | Wireless Local Area Network |